Low Power, High Output Current Differential Amplifier

AD8390

FEATURES

Voltage feedback amplifier
- **Ideal for ADSL and ADSL2+ central office (CO) and customer premises equipment (CPE) applications**
- **Enables high current differential applications**

Low power operation
- **Single- or dual-power supply operation from 10 V (±5 V) up to 24 V (±12 V)**
- **4 mA total quiescent supply current for full power ADSL and ADSL2+ CO applications**
- **Adjustable supply current to minimize power consumption**

High output voltage and current drive
- **400 mA peak output drive current**
- **44.2 V p-p differential output voltage**

Low distortion
- **–82 dBc @ 1 MHz second harmonic**
- **–91 dBc @ 1 MHz third harmonic**

High speed: 300 V/µs differential slew rate

APPLICATIONS

ADSL/ADSL2+ CO and CPE line drivers

xDSL line driver

High current differential amplifiers

GENERAL DESCRIPTION

The AD8390 is a high output current, low power consumption differential amplifier. It is particularly well suited for the central office (CO) driver interface in digital subscriber line systems such as ADSL and ADSL2+. While in full bias operation, the driver is capable of providing 24.4 dBm output power into low resistance loads. This is enough to power a 20.4 dBm line while compensating for losses due to hybrid insertion, transformer insertion, and back termination resistors.

The AD8390 fully differential amplifier is available in a thermally enhanced lead frame chip scale package (LFCSP-16) and a 16-lead QSOP/EP. Significant control and flexibility in bias current have been designed into the AD8390. The four power modes are controlled by two digital bits, PWDN (1,0) which provide three levels of driver bias and one powered-down state. In addition, the I_{ADJ} pin can be used for fine quiescent current trimming to tailor the performance of the AD8390.

PIN CONFIGURATIONS

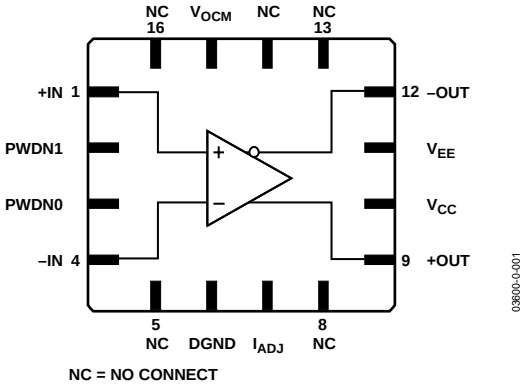


Figure 1. 4 mm × 4 mm 16-Lead LFCSP

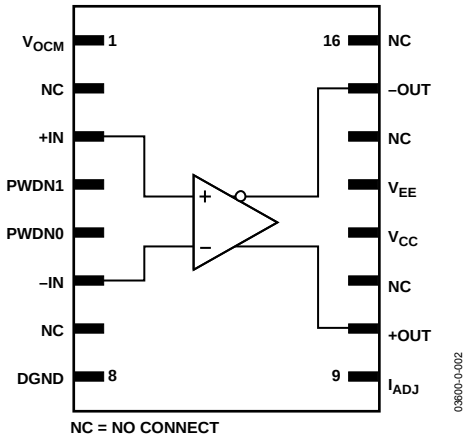


Figure 2. 16-Lead QSOP/EP

The low power consumption, high output current, high output voltage swing, and robust thermal packaging enable the AD8390 to be used as the central office line driver in ADSL, ADSL2+, and proprietary xDSL systems, as well as in other high current applications requiring a differential amplifier.

Rev. C

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REVISION HISTORY

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Change to Ordering Guide 16

2/04–Data Sheet Changed from Rev. A to Rev. B.

Changed pub code 16

1/04–Data sheet changed from Rev. Sp0f to Rev. A.

Added detailed description of product ..... Universal

Updated Outline Dimensions 13

SPECIFICATIONS

V_S = ±12 V or +24 V, R_L = 100 Ω, G = 10, PWDN = (1,1), I_{ADJ} = NC, V_{OCM} = float, T_A = 25°C, unless otherwise noted.[1,2]

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
–3 dB Small Signal Bandwidth	V_{OUT} = 0.2 V p-p, R_F = 10 kΩ	40	60		MHz
Large Signal Bandwidth	V_{OUT} = 4 V p-p	25	40		MHz
Peaking	V_{OUT} = 0.2 V p-p		0.1		dB
Slew Rate	V_{OUT} = 4 V p-p		300		V/µs
NOISE/DISTORTION PERFORMANCE					
Second Harmonic Distortion	f_C = 1 MHz, V_{OUT} = 2 V p-p		–82		dBc
Third Harmonic Distortion	f_C = 1 MHz, V_{OUT} = 2 V p-p		–91		dBc
Multitone Power Ratio (26 kHz to 1.1 MHz)	Z_{LINE} = 100 Ω, P_{LINE} = 19.8 dBm, crest factor (CF) = 5.4		–70		dBc
Multitone Power Ratio (26 kHz to 2.2 MHz)	Z_{LINE} = 100 Ω, P_{LINE} = 19.8 dBm, crest factor (CF) = 5.4		–65		dBc
Voltage Noise (RTI)	f = 10 kHz		8		nV/√Hz
Input Current Noise	f = 10 kHz		1		pA/√Hz
INPUT CHARACTERISTICS					
RTI Offset Voltage ($V_{OS,DM(RTI)}$)	V_{+IN} – $V_{–IN}$, V_{OCM} = midsupply	–3.0	±1.0	+3.0	mV
RTI Offset Voltage ($V_{OS,DM(RTI)}$)	V_{+IN} – $V_{–IN}$, V_{OCM} = float	–3.0	±1.0	+3.0	mV
±Input Bias Current			–4.0	–7.0	µA
Input Offset Current		–0.35	±0.05	+0.35	µA
Input Resistance			400		kΩ
Input Capacitance			2		pF
Common-Mode Rejection Ratio	$(\Delta V_{OS,DM(RTI)})/(\Delta V_{IN,CM})$	58	64		dB
OUTPUT CHARACTERISTICS					
Differential Output Voltage Swing	ΔV_{OUT}	43.8	44.2	44.6	V
Output Balance Error	$(\Delta V_{OS,CM})/\Delta V_{OUT}$		60		dB
Linear Output Current	R_L = 10 Ω, f_C = 100 kHz Worst harmonic = –60 dBc		400		mA
Output Common-Mode Offset	$(V_{+OUT} + V_{–OUT})/2$, V_{OCM} = midsupply	–75	±35	+75	mV
Output Common-Mode Offset	$(V_{+OUT} + V_{–OUT})/2$, V_{OCM} = float	–75	±35	+75	mV
POWER SUPPLY					
Operating Range (Dual Supply)		±5		±12	V
Operating Range (Single Supply)		+10		+24	V
Total Quiescent Current	PWDN1, PWDN0 = (1,1); I_{ADJ} = V_{EE}		5.2	6.5	mA
	(1,0); I_{ADJ} = V_{EE}		3.8	5.0	mA
	(0,1); I_{ADJ} = V_{EE}		2.5	3.5	mA
	(0,0); I_{ADJ} = V_{EE}		0.57	1.0	mA
Total Quiescent Current	PWDN1, PWDN0 = (1,1); I_{ADJ} = NC		10.0	11.0	mA
	(1,0); I_{ADJ} = NC		6.7	8.0	mA
	(0,1); I_{ADJ} = NC		3.8	5.0	mA
	(0,0); I_{ADJ} = NC		0.67	1.0	mA
Power Supply Rejection Ratio (PSRR)	$\Delta V_{OS,DM}/\Delta V_S$, ΔV_S = ±1 V, V_{OCM} = midsupply	70	76		dB
PWDN = 0 (Low Logic State)				1.0	V
PWDN = 1 (High Logic State)		1.6			V
V_{OCM} TO ±V_{OUT} SPECIFICATIONS					
Input Voltage Range			–11.0 to +10.0		V
Input Resistance			28		kΩ
V_{OCM} Accuracy	$\Delta V_{OUT,CM}/\Delta V_{OCM}$	0.996	1.0	1.004	V/V

[1] V_{OCM} bypassed with 0.1 µF capacitor.
[2] See Figure 3.

V_S = ±5 V or +10 V, R_L = 100 Ω, G = 10, PWDN = (1,1), I_{ADJ} = NC, V_{OCM} = float, T_A = 25°C, unless otherwise noted.[1, 2]

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
–3 dB Small Signal Bandwidth	V_{OUT} = 0.2 V p-p, R_F = 10 kΩ, G = 10	40	60		MHz
Large Signal Bandwidth	V_{OUT} = 4 V p-p	25	40		MHz
Peaking	V_{OUT} = 0.2 V p-p		0.1		dB
Slew Rate	V_{OUT} = 4 V p-p		300		V/µs
NOISE/DISTORTION PERFORMANCE					
Second Harmonic Distortion	f_C = 1 MHz, V_{OUT} = 2 V p-p		–82		dBc
Third Harmonic Distortion	f_C = 1 MHz, V_{OUT} = 2 V p-p		–91		dBc
Voltage Noise (RTI)	f = 10 kHz		8		nV/√Hz
Input Current Noise	f = 10 kHz		1		pA/√Hz
INPUT CHARACTERISTICS					
RTI Offset Voltage ($V_{OS,DM(RTI)}$)	$V_{+IN} - V_{-IN}$, V_{OCM} = midsupply	–3.0	±1.0	+3.0	mV
RTI Offset Voltage ($V_{OS,DM(RTI)}$)	$V_{+IN} - V_{-IN}$, V_{OCM} = float	–3.0	±1.0	+3.0	mV
±Input Bias Current			–4.0	–7.0	µA
Input Offset Current		–0.35	±0.05	+0.35	µA
Input Resistance			400		kΩ
Input Capacitance			2		pF
Common-Mode Rejection Ratio	$(\Delta V_{OS,DM(RTI)})/(\Delta V_{IN,CM})$	58	64		dB
OUTPUT CHARACTERISTICS					
Differential Output Voltage Swing	ΔV_{OUT}	16.0	16.4	16.8	V
Output Balance Error	$(\Delta V_{OS,CM})/\Delta V_{OUT}$		60		dB
Linear Output Current	R_L = 10 Ω, f_C = 100 kHz		400		mA
	Worst harmonic = –60 dBc				
Output Common-Mode Offset	$(V_{+OUT} + V_{-OUT})/2$, V_{OCM} = midsupply	–75	±35	+75	mV
Output Common-Mode Offset	$(V_{+OUT} + V_{-OUT})/2$, V_{OCM} = float	–75	±35	+75	mV
POWER SUPPLY					
Operating Range (Dual Supply)		±5		±12	V
Operating Range (Single Supply)		+10		+24	V
Total Quiescent Current	PWDN1, PWDN0 = (1,1); $I_{ADJ} = V_{EE}$		4.5	5.5	mA
	(1,0); $I_{ADJ} = V_{EE}$		3.3	4.0	mA
	(0,1); $I_{ADJ} = V_{EE}$		2.1	3.0	mA
	(0,0); $I_{ADJ} = V_{EE}$		0.43	1.0	mA
Total Quiescent Current	PWDN1, PWDN0 = (1,1); I_{ADJ} = NC		8.7	10.0	mA
	(1,0); I_{ADJ} = NC		5.8	7.0	mA
	(0,1); I_{ADJ} = NC		3.3	4.0	mA
	(0,0); I_{ADJ} = NC		0.55	1.0	mA
Power Supply Rejection Ratio	$\Delta V_{OS,DM}/\Delta V_S$, ΔV_S = ±1 V, V_{OCM} = midsupply	70	76		dB
PWDN = 0 (Low Logic State)				1.0	V
PWDN = 1 (High Logic State)		1.6			V
V_{OCM} TO ±V_{OUT} SPECIFICATIONS					
Input Voltage Range			–4.0 to +3.0		V
Input Resistance			28		kΩ
V_{OCM} Accuracy	$\Delta V_{OUT,CM}/\Delta V_{OCM}$	0.996	1.0	1.004	V/V

[1] V_{OCM} bypassed with 0.1 µF capacitor.
[2] See Figure 3.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	±13.2 V (26.4 V)
V_{OCM}	$V_{EE} < V_{OCM} < V_{CC}$
Package Power Dissipation	$(T_{J\ MAX} - T_A)/\theta_{JA}$
Maximum Junction Temperature ($T_{J\ MAX}$)	150°C
Operating Temperature Range (T_A)	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (Soldering 10 s)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL THERMAL PROPERTIES

Table 4.

Package	Typical Thermal Resistance (θ_{JA})
16-lead LFCSP (CP-16) JEDEC 2S2P – 0 airflow Paddle soldered to board Nine thermal vias in pad	30.4°C/W
16-lead QSOP/EP (RC-16) JEDEC 1S2P – 0 airflow Paddle soldered to board Nine thermal vias in pad	44.3°C/W

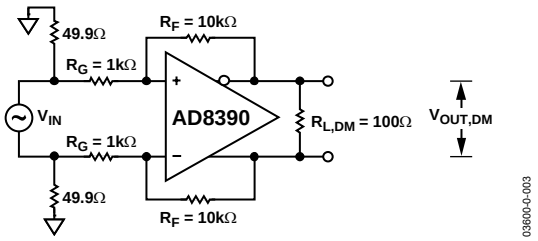


Figure 3. Basic Test Circuit

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



TYPICAL PERFORMANCE CHARACTERISTICS

Default Conditions: V_S = ±12 V or +24 V, R_L = 100 Ω, G = 10, PWDN = (1,1), I_{ADJ} = NC, V_{OCM} = float (bypassed with 0.1 µF capacitor), T_A = 25°C, unless otherwise noted. See Figure 3.

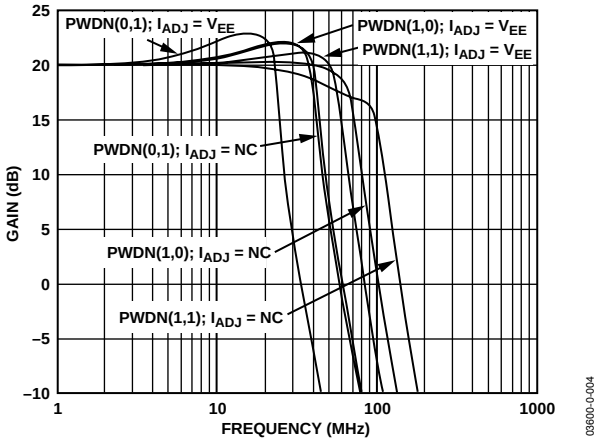


Figure 4. Small Signal Frequency Response; V_S = ±12 V, Gain = 10, V_{OUT} = 200 mV p-p

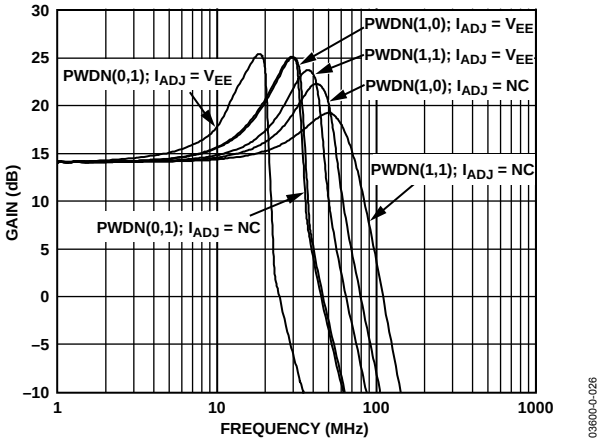


Figure 7. Small Signal Frequency Response; V_S = ±5 V, Gain = 5, V_{OUT} = 200 mV p-p

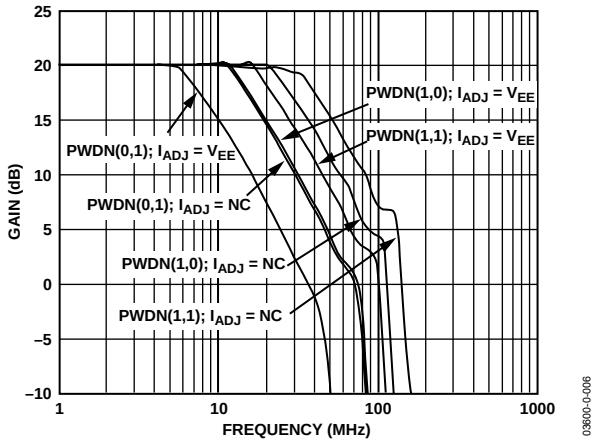


Figure 5. Large Signal Frequency Response; V_S = ±12 V, Gain = 10, V_{OUT} = 4 V p-p

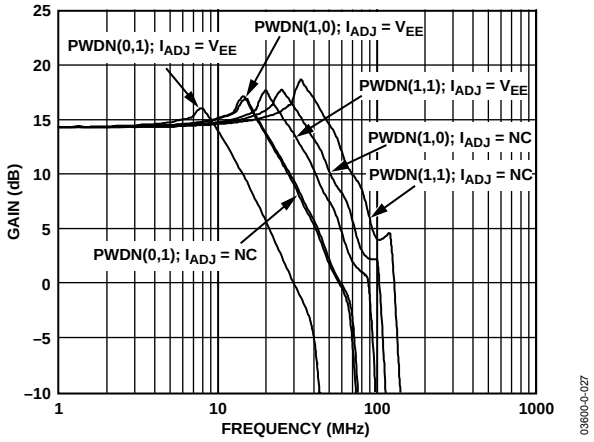


Figure 8. Large Signal Frequency Response; V_S = ±5 V, Gain = 5, V_{OUT} = 2 V p-p

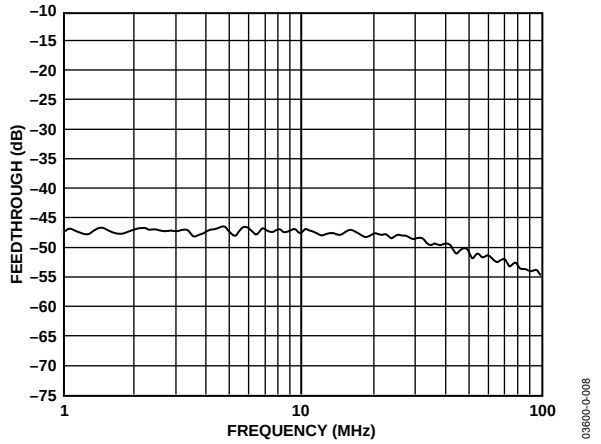


Figure 6. Signal Feedthrough; PWDN = (0,0)

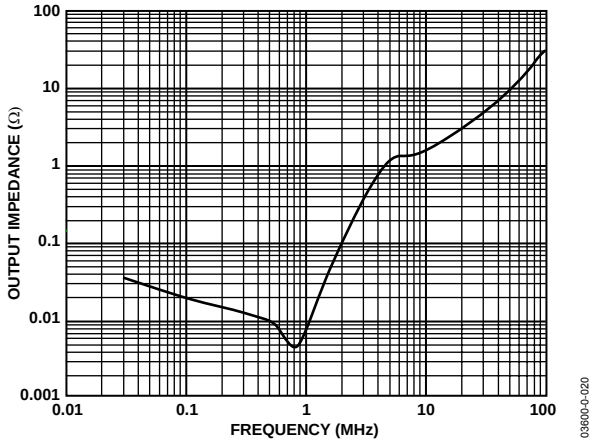


Figure 9. Output Impedance vs. Frequency; PWDN = (1,1)

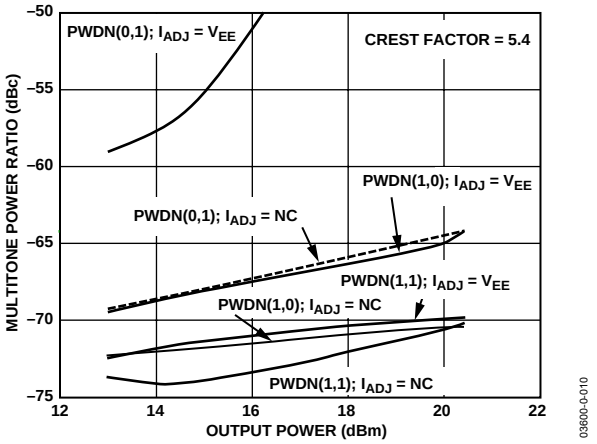


Figure 10. MTPR vs. Output Power; 970 kHz Empty Bin (26 kHz to 1.1 MHz)

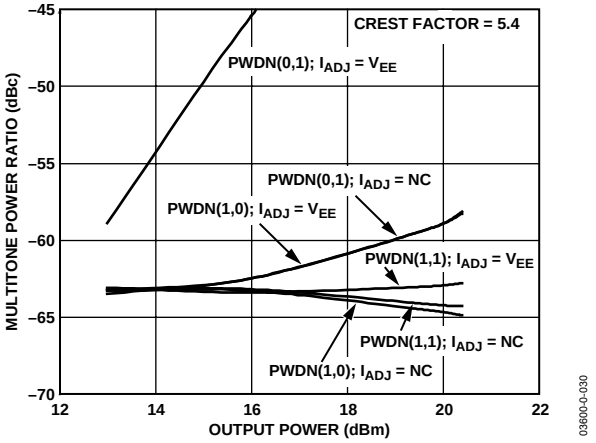


Figure 13. MTPR vs. Output Power; 1.75 MHz Empty Bin (26 kHz to 2.2 MHz)

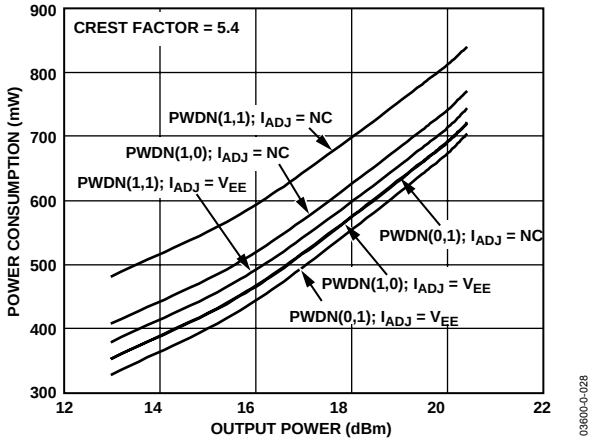


Figure 11. Power Consumption vs. Output Power (Includes Output Power Delivered to Load)

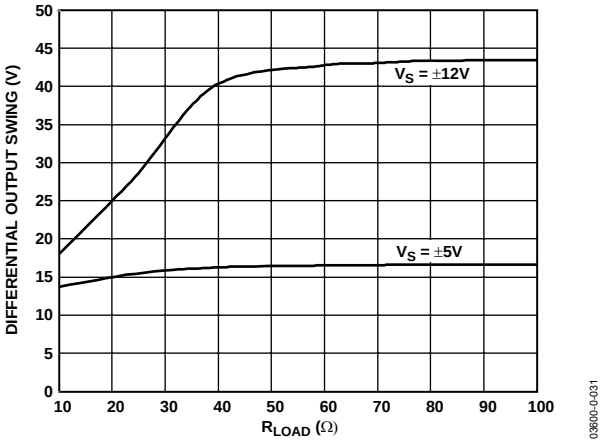


Figure 14. Differential Output Swing vs. R_{LOAD}

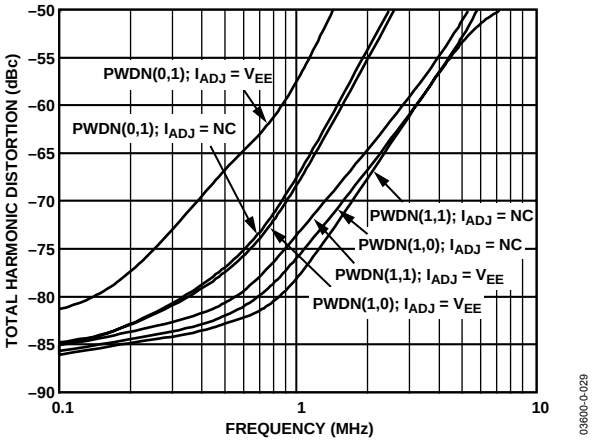


Figure 12. Total Harmonic Distortion vs. Frequency; V_S = ±12 V, V_{OUT} = 2 V p-p

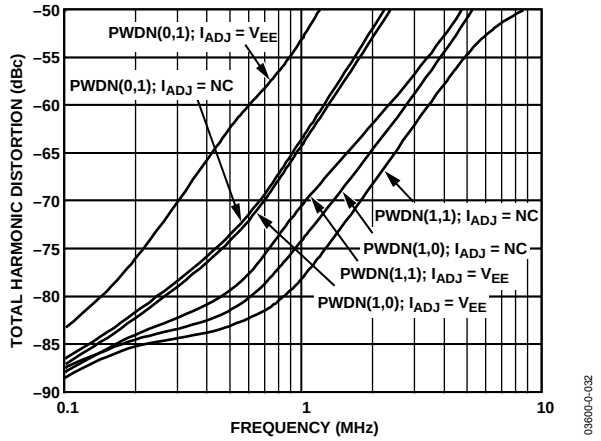


Figure 15. Total Harmonic Distortion vs. Frequency; V_S = ±5 V, V_{OUT} = 2 V p-p

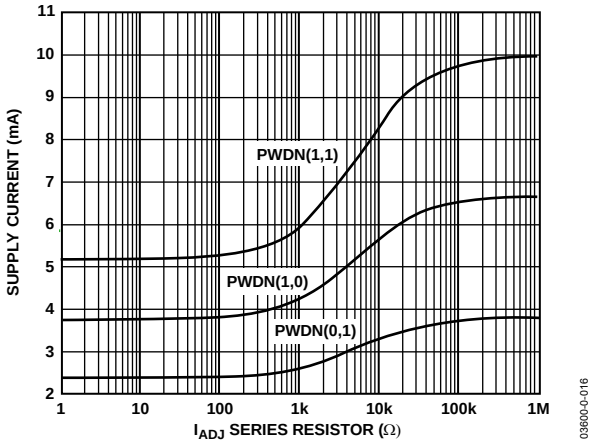


Figure 16. Quiescent Current vs. I_{ADJ} Resistor; $V_S = \pm 12$ V

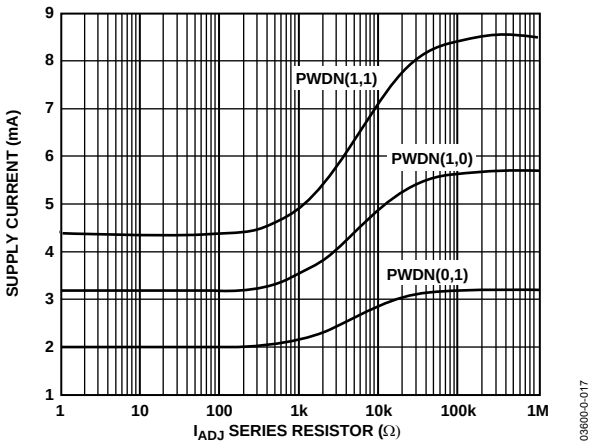


Figure 19. Quiescent Current vs. I_{ADJ} Resistor; $V_S = \pm 5$ V

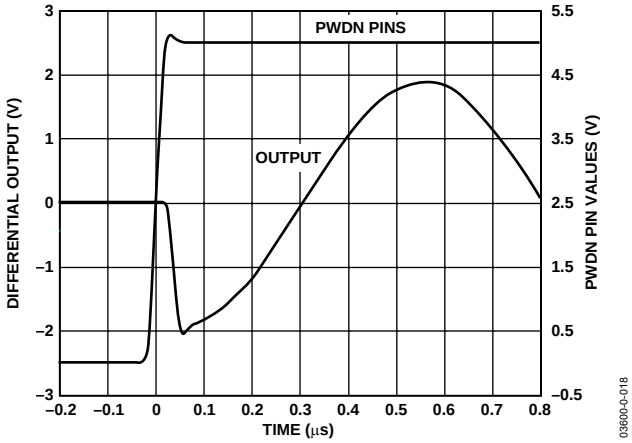


Figure 17. Power-Up Time;
PWDN = (0,0) to PWDN = (1,1)

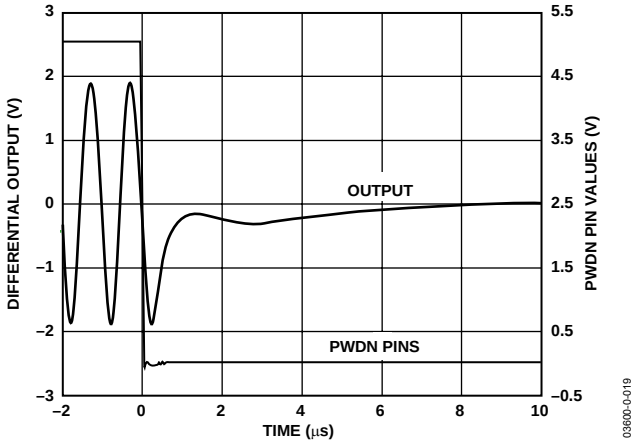


Figure 20. Power-Down Time;
PWDN = (1,1) to PWDN = (0,0)

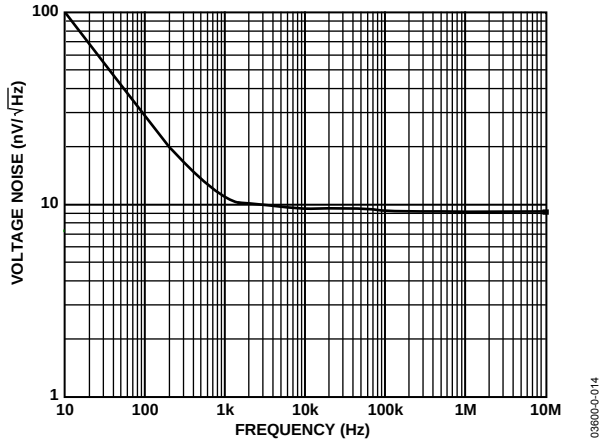


Figure 18. Voltage Noise (RTI)

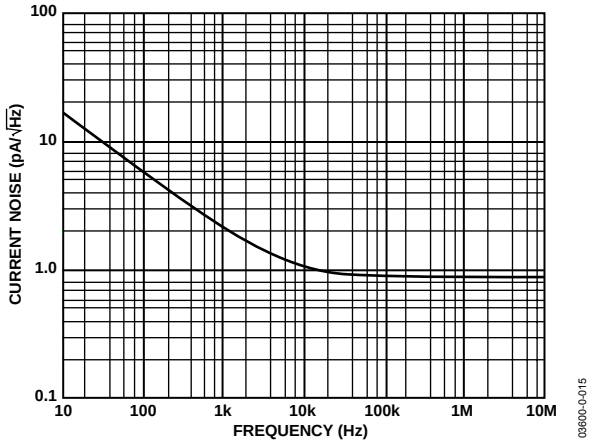


Figure 21. Current Noise (RTI)

THEORY OF OPERATION

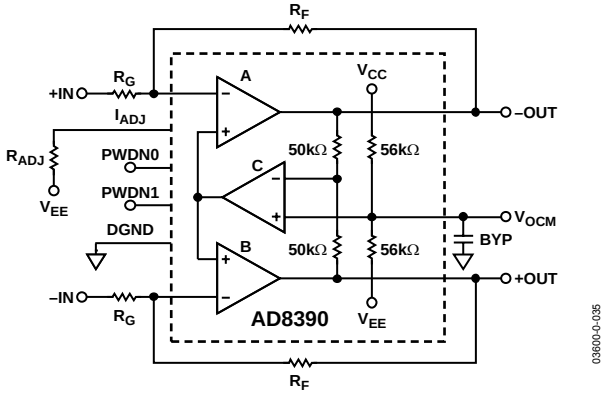


Figure 22. Functional Block Diagram

The AD8390 is a true differential operational amplifier with common-mode feedback. The AD8390 is functionally equivalent to three op amps, as shown in Figure 22. Amplifiers A and B act like a standard dual op amp in an inverting configuration that requires four resistors to set the desired gain.

The third amplifier (C) maintains the common-mode voltage (V_{OCM}) at the output of the AD8390. V_{OCM} is internally generated, as shown in Figure 22. The common-mode feedback amplifier (C) drives the noninverting terminals of A and B such that the difference between the output common-mode voltage and V_{OCM} is always zero. This functionality forces the outputs to sit at midsupply, which results in differential outputs of identical amplitude and 180 degrees out of phase. The user also has the option to externally drive the V_{OCM} pin as an input to set the dc output common-mode voltage. For details, see the Setting the Output Common-Mode Voltage section.

APPLICATIONS

CIRCUIT DEFINITIONS

Differential voltage refers to the difference between two node voltages. For example, the output differential voltage (or output differential-mode voltage) is defined as

$$V_{OUT,DM} = (V_{+OUT} - V_{-OUT}) \quad (1)$$

V_{+OUT} and V_{-OUT} refer to the voltages at the +OUT and –OUT terminals with respect to a common reference.

Common-mode voltage refers to the average of the two node voltages. The output common-mode voltage is defined as

$$V_{OUT,CM} = \frac{(V_{+OUT} + V_{-OUT})}{2} \quad (2)$$

ANALYZING A BASIC APPLICATION CIRCUIT

The AD8390 uses high open-loop gain and negative feedback to force its differential and common-mode output voltages in such a way as to minimize the differential and common-mode error voltages. The differential error voltage is defined as the voltage between the differential inputs +IN and –IN, as shown in Figure 23. For most purposes, this voltage can be assumed to be zero. Similarly, the difference between the actual output common-mode voltage and the voltage applied to V_{OCM} can also be assumed to be zero. Starting from these two assumptions, any application circuit can be analyzed.

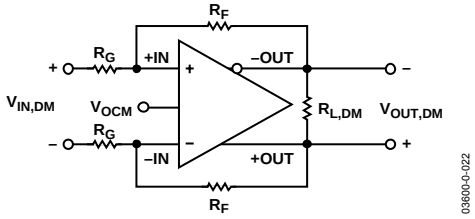


Figure 23. Basic Applications Circuit
(I_{ADJ} Pin Not Connected, and PWDN0 and PWDN1 Held High)

SETTING THE CLOSED-LOOP GAIN

The differential-mode gain of the circuit in Figure 23 can be described by

$$\frac{V_{OUT,DM}}{V_{IN,DM}} = \frac{R_F}{R_G} \quad (3)$$

CALCULATING INPUT IMPEDANCE

The input impedance of the circuit in Figure 23 between the inputs (V_{+IN} and V_{-IN}) is simply

$$R_{IN,DM} = 2 \times R_G \quad (4)$$

SETTING THE OUTPUT COMMON-MODE VOLTAGE

By design, the AD8390's V_{OCM} pin is internally biased at a voltage equal to the midsupply point (average value of the voltages on V_{CC} and V_{EE}), eliminating the need for external resistors. The high impedance nature of the V_{OCM} pin, however, allows the designer to force it to a desired level with an external low impedance source. It should be noted that the V_{OCM} pin is not intended for use as an ac signal input.

The three configurations for the V_{OCM} pin are floating with a single supply, floating with dual supplies, and forcing the pin with an external source. If not externally forcing the V_{OCM} pin, the designer must decouple it to ground with a 0.1 µF capacitor in close proximity to the AD8390.

With dual equal supplies (for example, ±12 V) such that the midpoint of the supplies is nominally 0 V, the user may opt to connect the V_{OCM} pin directly to ground, thus eliminating the need for an external decoupling capacitor.

POWER-DOWN FEATURES AND THE I_{ADJ} PIN

The AD8390 offers significant versatility in setting quiescent bias levels for a particular application from full ON to full OFF. This versatility gives the circuit designer the flexibility to maximize efficiency while maintaining optimal levels of performance.

Optimizing driver efficiency while delivering the required signal level is accomplished with the AD8390 through the use of two on-chip power management features: two PWDN pins used to select one of four bias modes, and an I_{ADJ} pin used for additional power management including fine bias adjustments.

PWDN Pins

Two digitally programmable logic pins, PWDN1 and PWDN0, may be used to select four different bias levels (see Table 5). These levels start with full power if the I_{ADJ} pin is not connected. The top bias level can also start at approximately half of full bias, if the I_{ADJ} pin is connected to V_{EE} or to ground in a single-supply configuration, R_{ADJ} = 0. The bias level can be controlled with CMOS logic levels (high = 1) applied to the PWDN1 and PWDN0 pins alone or in combination with the I_{ADJ} control pin. The digital ground pin (DGND) is the logic ground reference for the PWDN1 and PWDN0 pins. PWDN = (0,0) is the power-down mode of the amplifier.

The AD8390 exhibits a low output impedance for PWDN1,0 = (1,1), (1,0), and (0,1). At PWDN1,0 = (0,0), however, the output impedance is undefined. The lowest power mode (0,0) of the AD8390 alone may not be suitable for systems that rely on a high impedance OFF state, such as multiplexing.

I_{ADJ} Pin

The I_{ADJ} feature offers users significant flexibility in setting the bias level of the AD8390 by allowing for fine tuning of the bias setting. Use of the I_{ADJ} feature is not required for operation of the AD8390.

When I_{ADJ} is not connected, the bias current in the various power modes is set to approximately 10 mA, 6.7 mA, and 3.8 mA for power modes PWDN1,0 = (1,1), (1,0), and (0,1), respectively, as seen in Table 5. Setting $I_{ADJ} = V_{EE}$ for dual-supply operation (or grounding the I_{ADJ} pin for single-supply operation) cuts the bias setting approximately in half for each mode.

A resistor (R_{ADJ}) between I_{ADJ} and ground for single-supply operation, or I_{ADJ} and V_{EE} for dual-supply operation, allows fine bias adjustment between the bias levels preset by the PWDN pins. Figure 16 and Figure 19 depict the effect of different R_{ADJ} values on setting the bias levels.

Table 5. PWDN Code Selection Guide

PWDN1	PWDN0	R_{ADJ} (Ω)	I_Q (mA)
1	1	∞	10.0
1	0	∞	6.7
0	1	∞	3.8
0	0	∞	0.67
1	1	0	5.2
1	0	0	3.8
0	1	0	2.5
0	0	0	0.57

ADSL and ADSL2+ Applications

The AD8390 line driver amplifier is an efficient class AB amplifier that is ideal for driving xDSL signals. The AD8390 may be used for driving ADSL or ADSL2+ modulated signals in either direction: upstream from CPE to the CO or downstream from the CO to CPE.

ADSL and ADSL2+ Applications Circuit

Increased CO port density has made driver power efficiency an important requirement in ADSL and ADSL2+ systems. The largest impact on efficiency is due to the need for back termination of the driver. In the simplest case, this is accomplished with a pair of resistors, each equal to half the reflected line impedance, in series with the outputs of the differential driver. In this scenario, half the transmitted power is consumed by the back termination resistors. This results in the need for higher turns ratio transformers, which attenuate the receive signal and tend to be more lossy. They also increase current requirements of the driver, effectively reducing headroom because the output devices can no longer swing as close to the rail.

To solve this problem, it is common practice to use a combination of negative and positive feedback to synthesize the output impedance, thus decreasing the required ohmic value of the back termination. Overall efficiency is improved because less power is wasted in the back termination and a lower turns ratio transformer can be used without the need for increased supply rails. The application circuit in Figure 24 depicts such an approach, where the positive feedback, negative feedback, and back termination are provided by R2, R3, and R_M, respectively.

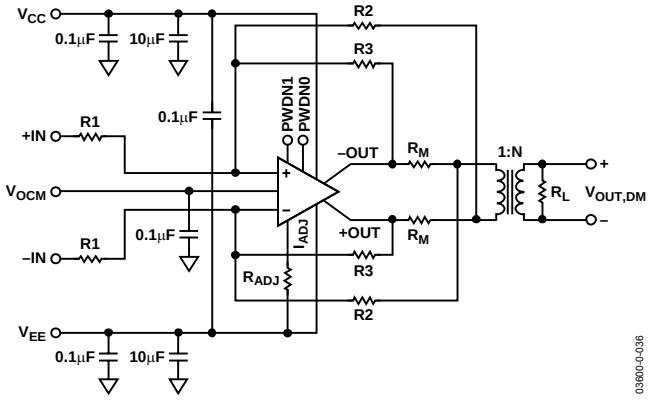


Figure 24. ADSL/ADSL2+ Application Circuit

Referring to Figure 24, the following describes how to calculate the resistor values necessary to obtain the desired input impedance, gain, and output impedance.

The differential input impedance to the circuit is simply 2*R1*. As such, *R1* is chosen by the designer to yield the desired input impedance.

When synthesizing the output impedance, a factor *k* is introduced, which is used to express the ratio of the negative feedback resistor to the positive feedback resistor by

$$1-k=\frac{R3}{R2} \tag{5}$$

Along with the turns ratio *N*, *k* is also used to define the value of the back termination resistors R_M. Commonly used values for *k* are 0.1 to 0.25. A *k* value of 0.1 would result in back termination resistors that are only 1/10 as large as those in the simplest case described above. Lower values of *k* result in greater amounts of positive feedback. Therefore, values much lower than 0.1 can lead to instability and are generally not recommended.

$$R_M=k\times\frac{R_L}{2\times N^2} \tag{6}$$

This factor (*k*), along with *R1*, R_M, and the desired gain (A_V), is then used to calculate the necessary values for *R3* and *R2*.

$$R3=A_V\times R1\times k+\sqrt{A_V\times R1\times\left(A_V\times R1\times k^2+R_M-k\times R_M\right)} \tag{7}$$

The usually small value for R_M allows a simplified approximation for *R3*.

$$R3\cong R1\times 2\times k\times A_V \tag{8}$$

$$R2=\frac{R3}{1-k} \tag{9}$$

Once R_M, *R3*, and *R2* are computed, the closest 1% resistors can be chosen and the gain rechecked with the following equation:

$$A_V=\frac{R2\times R3}{\left(R_M+k\times R2+R2-R3\right)\times R1} \tag{10}$$

Table 6 shows a comparison of the results using the exact values, the simplified approximation, and the closest 1% resistor values. In this example, *R1*, A_V, and *k* were chosen to be 1.0 kΩ, 10 kΩ, and 0.1 kΩ, respectively.

It should be noted that decreasing the value of the back termination resistors attenuates the receive signal by approximately 1/k. However, advances in low noise receive amplifiers permit k values as small as 0.1 to be commonly used.

The line impedance, turns ratio, and k factor specify the output voltage and current requirements from the AD8390. To accommodate higher crest factors or lower supply rails, the turns ratio, N, may have to be increased. Since higher turns ratios and smaller k factors both attenuate the receive signal, a large increase in N may require an increase in k to maintain the desired noise performance. Any particular design process requires that these trade-offs be visited.

Table 6. Resistor Selection

Component	Exact Values	Approximate Calculation	Standard 1% Resistor Values
R1 (Ω)	1000	1000	1000
R2 (Ω)	2246.95	2222.22	2210
R3 (Ω)	2022.25	2000	2000
R_M (Ω)	5	5	4.99
Actual A_V	10.000	9.889	10.138
Actual k (Eq. 5)	0.1	0.1	0.095

MULTITONE POWER RATIO (MTPR)

Multitone power ratio is a commonly used figure of merit that xDSL designers use to help describe system performance. MTPR is the measured delta between the peak of a filled frequency bin and the harmonic products that appear in an intentionally empty frequency bin. Figure 25 illustrates this principle. The plots in Figure 10 and Figure 13 show MTPR performance in various power modes. All data were taken with a circuit with a k factor of 0.1, a 1:1 turns ratio transformer, and a waveform with a 5.4 peak-to-average ratio, also known as the crest factor (CF).

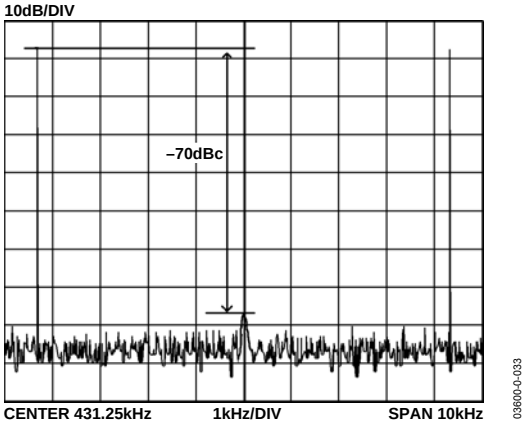


Figure 25. MTPR Measurement

LAYOUT, GROUNDING, AND BYPASSING

The first layout requirement is for a good solid ground plane that covers as much of the board area around the AD8390 as possible. The only exception to this is that the two input pins should be kept a few millimeters from the ground plane, and ground should be removed from inner layers and the opposite side of the board under the input traces. This minimizes the stray capacitance on these nodes and helps preserve the gain flatness versus frequency.

The power supply pins should be bypassed as close as possible to the device on a ground plane common with signal ground. Good high frequency, ceramic chip capacitors should be used. This bypassing should be done with a capacitance value of 0.01 µF to 0.1 µF for each supply. Low frequency bypassing should be provided with 10 µF tantalum capacitors from each supply to signal ground. The signal routing should be short and direct to avoid parasitic effects, particularly on traces connected to the amplifier inputs. Wherever there are complementary signals, a symmetrical layout should be provided to the extent possible to maximize the balance performance. When running differential signals over a long distance, the traces on the PCB should be close together.

POWER DISSIPATION AND THERMAL MANAGEMENT

The AD8390 was designed to be the most efficient class AB ADSL/ADSL2+ line driver available. Figure 11 shows the total power consumption (delivered line power and power consumed) of the AD8390 driving ADSL signals at varying output powers and power modes. To accurately determine the amount of power dissipated by the AD8390, it is necessary to subtract the power delivered to the load, matching losses, and transformer losses as follows:

$$P_{AD8390} = P_{supply,mW} - P_{load,mW} - P_{losses,mW} \quad (11)$$

where:

$P_{supply,mW}$ is the total supply power in mW drawn by the AD8390.
$P_{load,mW}$ is the power delivered into a 100 Ω twisted-pair line in mW.
$P_{losses,mW}$ is the power dissipated by the matching resistors and the transformer in mW.

While this discussion focuses mainly on ADSL applications, the same premise can be applied to determining the power dissipation of the AD8390 in any application.

To obtain optimum thermal performance from the AD8390 in either package, it is essential that the thermal pad be soldered to a ground plane with minimal thermal resistance. This is particularly true for dense circuit designs with multiple integrated circuits. Furthermore, the PCB should be designed in such a manner as to draw the heat away from the ICs. Figure 26 illustrates the relationship between thermal resistance (°C/W) and the copper area (mm^2) for the AD8390ACP soldered down to a 4-layer board with a given copper area.

Figure 26 can be used to help determine the copper board area required for proper thermal management of the AD8390. The power dissipation of the AD8390 can be computed using Equation 11. This number can then be inserted into the following equation to yield the required θ_{JA}:

$$\theta_{JA} = \frac{T_{RISE}}{P_{AD8390}} = \frac{°C}{W} \quad (12)$$

where T_{RISE} is the delta from the maximum expected ambient temperature to the highest allowable die temperature. It is generally recommended that the maximum die temperature be limited to 125°C, and in no case should it be allowed to exceed 150°C.

Using the θ_{JA} computed in Equation 12, Figure 26 can be used to determine the minimum copper area required for proper thermal dissipation of the AD8390.

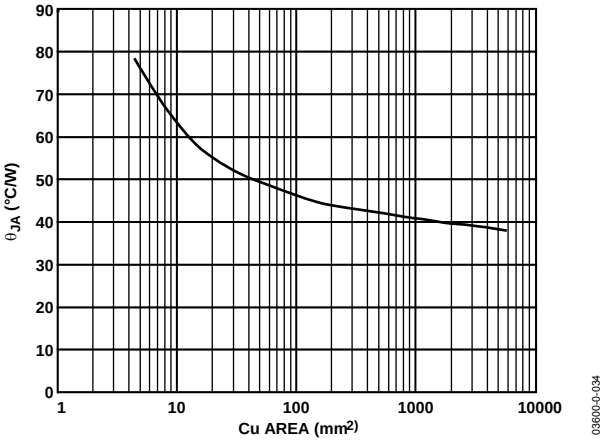
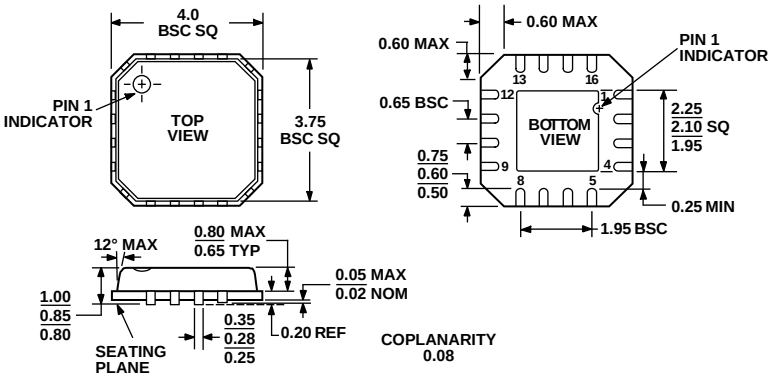


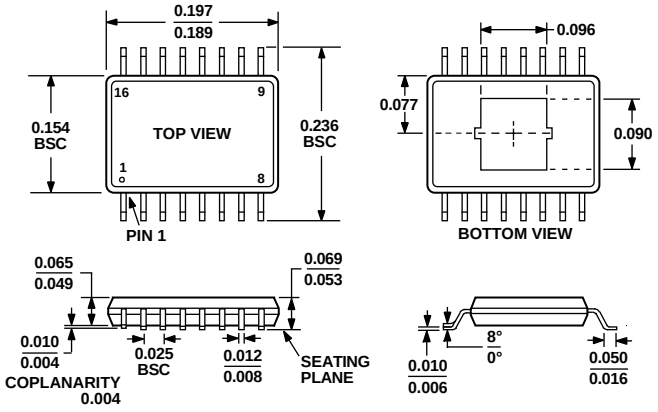
Figure 26. Thermal Resistance vs. Copper Area

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VGGC

Figure 27. 4 × 4 mm 16-Lead Lead Frame Chip Scale Package [LFCSP]
(CP-16)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-137

Figure 28. 16-Lead Shrink Small Outline Package, Exposed Pad [QSOP/EP]
(RC-16)
Dimensions shown in inches

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8390ACP-R2	–40°C to +85°C	16-Lead LFCSP	CP-16, 250 Piece Reel
AD8390ACP-REEL	–40°C to +85°C	16-Lead LFCSP	CP-16, 13" Tape and Reel
AD8390ACP-REEL7	–40°C to +85°C	16-Lead LFCSP	CP-16, 7" Tape and Reel
AD8390ACP-EVAL		Evaluation Board	LFCSP
AD8390ARC	–40°C to +85°C	16-Lead QSOP/EP	RC-16
AD8390ARC-REEL	–40°C to +85°C	16-Lead QSOP/EP	RC-16, 13" Tape and Reel
AD8390ARC-REEL7	–40°C to +85°C	16-Lead QSOP/EP	RC-16, 7" Tape and Reel
AD8390ARC-EVAL		Evaluation Board	QSOP/EP

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