

MNCLC501A-X REV 0A0

 Original Creation Date: 08/06/98
 Last Update Date: 03/09/99
 Last Major Revision Date: 02/26/99

HIGH-SPEED OUTPUT CLAMPING OP AMP
General Description

The CLC501 is a high-speed current-feedback op amp with the unique feature of output voltage clamping. This feature allows both the maximum positive (Vhigh) and negative (Vlow) output voltage levels to be established. This is useful in a number of applications in which "downstream" circuitry must be protected from overdriving input signals. Not only can this prevent damage to downstream circuitry, but can also reduce time delays since saturation is avoided. The CLC501's very fast lns overload/clamping recovery time is useful in applications in which information-containing signals follow overdriving signals.

Engineers designing high-resolution, subranging A/D systems have long sought an amplifier capable of meeting the demanding requirements of the residue amplifier function. Amplifiers providing the residue function must not only settle quickly, but recover from overdrive quickly, protect the second stage A/D, and provide high fidelity at relatively high gain settings. The CLC501, which excels in these areas, is the ideal design solution in this onerous application. To further support this application, the CLC501 is both characterized and tested at a gain setting of +32, the most common gain setting for residue amplifier applications.

The CLC501's other features provide a quick, high-performance design solution. Since the CLC501's current feedback design requires no external compensation, designers need not spend their time designing compensation networks. The small 8-pin package and low, 180mW power consumption make the CLC501 ideal in numerous applications having small power and size budgets.

Industry Part Number

CLC501A

Prime Die

UB1148C

NS Part Numbers

 CLC501AJ-MLS
 CLC501AJ-QML*
 CLC501AWG-MLS
 CLC501AWG-QML**

Controlling Document

5962-8997401PA*,MXA**

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- Output clamping (Vhigh and Vlow)
- 1ns recovery from clamping/overdrive
- 0.05% settling in 12ns
- Characterized and guaranteed at Av = +32
- Low power, 180mW

Applications

- Residue amplifier in high-accuracy, subranging A/D systems
- High-speed communications
- Output clamping applications
- Pulse amplitude modulation systems

(Absolute Maximum Ratings)

(Note 1)

Supply Voltage (Vs)	±7V dc
Output Current (Iout)	70mA
Junction Temperature (Tj)	+175 C
Storage Temperature	-65 C to +150 C
Lead Temperature (soldering, 10 seconds)	+300 C
Power Dissipation (Pd) (Note 2)	TBD
Common Mode Input Voltage (Vcm)	Vs
Thermal Resistance	
ThetaJA (Junction to Ambient)	
CERAMIC DIP (Still Air) (500LFPM)	TBD TBD
SOIC (Still Air) (500LFPM)	TBD TBD
ThetaJC (Junction to Case)	
CERAMIC DIP	TBD
SOIC	TBD
Package Weight (Typical)	
CERAMIC DIP	TBD
SOIC	TBD
ESD Tolerance (Note 3)	
ESD Rating	<1000V

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperature). The maximum allowable power dissipation at any temperature is Pdmax = (Tjmax - TA)/ThetaJA or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: Human body model, 100pF discharged through 1.5K Ohms.

Recommended Operating Conditions

Supply Voltage (Vs)	±5V dc
Gain Range (Av)	+7 to +50 and -1 to -50
Ambient Operating Temperature Range (Ta)	-55 C to +125 C

Electrical Characteristics

DC PARAMETERS: Open Loop Characteristics

(The following conditions apply to all the following parameters, unless otherwise specified.)
 DC: $R_l = 100\Omega$, $V_s = \pm 5V$ dc, $V_{high} = +3V$, $V_{low} = -3V$, $A_v = +32$, feedback resistance (R_f) = $1.5k\Omega$, and gain setting resistance (R_g) = 48.3Ω . $-55\text{ C} \leq T_a \leq +125\text{ C}$ (note 3)

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
+I _{in}	Input Bias Current (noninverting)	R _s = 50Ω				±25	μA	1
						±35	μA	2
						±37	μA	3
-I _{in}	Input Bias Current (inverting)	R _s = 50Ω				±30	μA	1
						±40	μA	2
						±46	μA	3
V _{io}	Input Offset Voltage	R _s = 50Ω				±3.0	mV	1
						±5.0	mV	2
						±4.6	mV	3
T _c (+I _{in})	Average +Input Bias Current Drift	R _s = 50Ω	1			±100	nA/C	2
			1			±150	nA/C	3
T _c (-I _{in})	Average -Input Bias Current Drift	R _s = 50Ω	1			±100	nA/C	2
			1			±200	nA/C	3
T _c (V _{io})	Average Offset Voltage Drift	R _s = 50Ω	1			±20	μV/C	1, 2, 3
I _s	Supply Current	No Load				24	mA	1, 2
						25	mA	3
PSRR	Power Supply Rejection Ratio	+V _s = +4.5V to +5.0V, -V _s = -4.5V to -5.0V			60		dB	1, 2
					55		dB	3
CMRR	Common Mode Rejection Ratio	V _{cm} = ±1V	1		60		dB	1, 2
		V _{cm} = ±1V	1		55		dB	3
±I _{out}	Output Current	R _l = 100Ω	1		±50		mA	1, 2
±I _{out}	Output Current	R _l = 100Ω	1		±30		mA	3
R _{out}	Output Impedance at dc	R _l = 100Ω	1			0.3	Ω	1, 2, 3
+R _{in}	Input Resistance		1		100		kΩ	1, 2
			1		50		kΩ	3
C _{in}	Input Capacitance	T _a = +25 C	1			7	pF	4
±V _{out}	Output Voltage Swing	R _l = 100Ω			±2.4		V	4, 5, 6

Electrical Characteristics

DC PARAMETERS: CLAMPING CHARACTERISTICS

(The following conditions apply to all the following parameters, unless otherwise specified.)
 DC: $R_l = 100\Omega$, $V_s = \pm 5V$ dc, $V_{high} = +3V$, $V_{low} = -3V$, $A_v = +32$, feedback resistance (R_f) = 1.5k Ω , and gain setting resistance (R_g) = 48.3k Ω . $-55\text{ C} \leq T_a \leq +125\text{ C}$ (note 3)

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Voc	Clamp Accuracy					± 0.2	V	1, 2, 3
ICL	Input Bias Current on Vhigh and Vlow		1			± 50	μA	1, 2
			1			± 100	μA	3
CDR	Input Offset Voltage Drift After Recovery		1			200	μV	1, 2, 3
OVC	Overshoot in Clamp		1			15	%	4
CMC	Clamping Range	At Vhigh or Vlow	1		± 3.3		V	4, 5
			1		± 3.0		V	6
TSO	Overload Recovery from Clamp		1			3	ns	9, 10, 11

AC PARAMETERS: FREQUENCY DOMAIN CHARACTERISTICS

(The following conditions apply to all the following parameters, unless otherwise specified.)
 AC: $R_l = 100\Omega$, $V_s = \pm 5V$ dc, $V_{high} = +3V$, $V_{low} = -3V$, $A_v = +32$, feedback resistance (R_f) = 1.5k Ω , and gain setting resistance (R_g) = 48.3k Ω . $-55\text{ C} \leq T_a \leq +125\text{ C}$ (note 3)

SSBW	Small Signal Bandwidth	-3dB bandwidth, $V_{out} < 5V_{pp}$			60		MHz	4
			2		45		MHz	5
			2		60		MHz	6
		-3dB bandwidth, $A_v = +20$, $V_{out} < 2V_{pp}$	1		85		MHz	4
			1		55		MHz	5
			1		85		MHz	6
GFPL	Gain Flatness, Peaking Low	0.1MHz to 15MHz, $V_{out} < 5V_{pp}$				0.1	dB	4
			2			0.1	dB	5, 6
GFPH	Gain Flatness, Peaking High	> 15MHz, $V_{out} < 5V_{pp}$				0.2	dB	4
			2			0.2	dB	5, 6
GFR	Gain Flatness, Rolloff	0.1MHz to 30MHz, $V_{out} < 5V_{pp}$				1.0	dB	4
			2			1.3	dB	5
			2			1.0	dB	6
LPD	Linear Phase Deviation	0.1MHz to 30MHz, $V_{out} < 5V_{pp}$	1			1.0	Deg	4, 5, 6

Electrical Characteristics

AC PARAMETERS: Distortion and Noise Characteristics

(The following conditions apply to all the following parameters, unless otherwise specified.)
 AC: $R_l = 100\Omega$, $V_s = \pm 5V$ dc, $V_{high} = +3V$, $V_{low} = -3V$, $A_v = +32$, feedback resistance (R_f) = 1.5k Ω , and gain setting resistance (R_g) = 48.3k Ω . $-55\text{ C} \leq T_a \leq +125\text{ C}$ (note 3)

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
HD2	2nd Harmonic Distortion	2Vpp at 20MHz			-33		dBc	4
			2		-30		dBc	5, 6
HD3	3rd Harmonic Distortion	2Vpp at 20MHz			-50		dBc	4
			2		-50		dBc	5
			2		-45		dBc	6
SNF	Noise Floor	> 1MHz	1			-156	dBm 1Hz	4, 6
			1			-155	dBm 1Hz	5
INV	Integrated Noise	1MHz to 100MHz	1			35	μ V	4, 6
			1			40	μ V	5

AC PARAMETERS: Timing Domain Characteristics

(The following conditions apply to all the following parameters, unless otherwise specified.)
 AC: $R_l = 100\Omega$, $V_s = \pm 5V$ dc, $V_{high} = +3V$, $V_{low} = -3V$, $A_v = +32$, feedback resistance (R_f) = 1.5k Ω , and gain setting resistance (R_g) = 48.3k Ω . $-55\text{ C} \leq T_a \leq +125\text{ C}$ (note 3)

SR	Slew Rate	$C_l < 10\text{pF}$, measured at $\pm 1V$ with 3V step	1		800		V/ μ S	4, 6
		$C_l < 10\text{pF}$, measured at $\pm 1V$ with 3V step	1		700		V/ μ S	5
Tr	Rise and Fall Time	2V step, $C_l < 10\text{pF}$	1		5.8		nS	9, 11
			1		7.8		nS	10
Tf	Rise and Fall Time	5V step, $C_l < 10\text{pF}$	1		6.5		nS	9, 11
			1		8		nS	10
Ts	Settling Time	2V step at $\pm 0.05\%$ of the fixed value, $C_l < 10\text{pF}$	1		18		nS	9, 11
		2V step at $\pm 0.05\%$ of the fixed value, $C_l < 10\text{pF}$	1		24		nS	10
OS	Overshoot	2V step, $C_l < 10\text{pF}$	1		5		%	9, 10, 11

Electrical Characteristics

DC PARAMETERS: DRIFT LIMITS

(The following conditions apply to all the following parameters, unless otherwise specified.)
 DC: $R_l = 100\Omega$, $V_s = \pm 5V$ dc, $V_{high} = +3V$, $V_{low} = -3V$, $A_v = +32$, $(R_f) = 1.5k\Omega$, $(R_g) = 48.3\Omega$.
 "Deltas not required on B-level product. Deltas required for S-level (-MLS) product as specified on Internal Processing Instructions (IPI)." (note 3)

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
+Iin	Input Bias Current (noninverting)	$R_s = 50\ \Omega$				± 2.5	μA	1
-Iin	Input Bias Current (inverting)	$R_s = 50\ \Omega$				± 3.0	μA	1
Vio	Input Offset Voltage	$R_s = 50\ \Omega$				± 0.3	mV	1
Is	Supply Current	No Load				± 2.4	mA	1

Note 1: If not tested, shall be guaranteed to the limits specified in table I herein.

Note 2: Group A testing only.

Note 3: The limiting terms, "Min" (minimum) and "Max" (maximum) shall be considered to apply to magnitudes only. Negative current shall be defined as conventional current flow out of a device terminal.

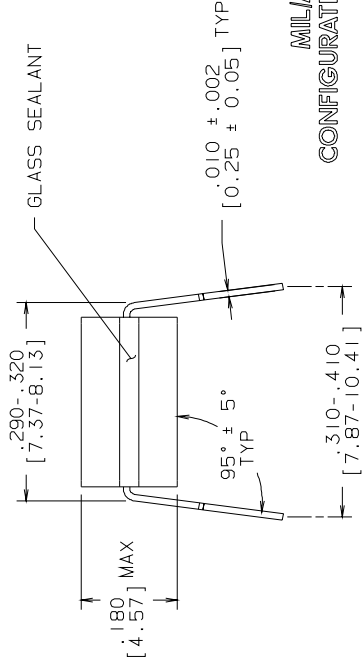
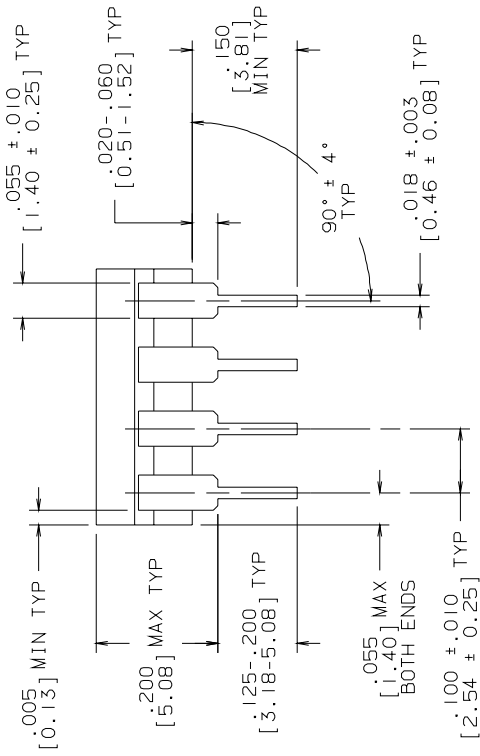
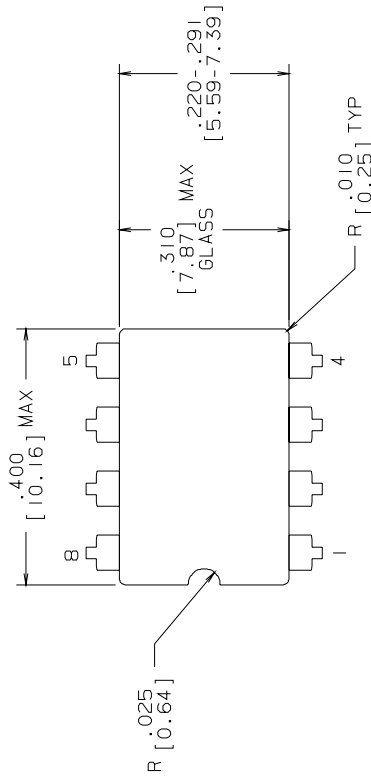
Graphics and Diagrams

GRAPHICS#	DESCRIPTION
07070HRA2	CERAMIC SOIC (WG), 10 LEAD (B/I CKT)
07081HRA3	CERDIP (J), 8 LEAD (B/I CKT)
J08ARL	CERDIP (J), 8 LEAD (P/P DWG)
P000409A	CERDIP (J), 8 LEAD (PINOUT)
P000448A	CERAMIC SOIC (WG), 10 LEAD (PINOUT)
WG10ARB	CERAMIC SOIC (WG), 10 LEAD (P/P DWG)

See attached graphics following this page.

REV I S I O N S

LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
L	REVISE PER CURRENT STD; REDRAW	10002	09/21/93	TL/



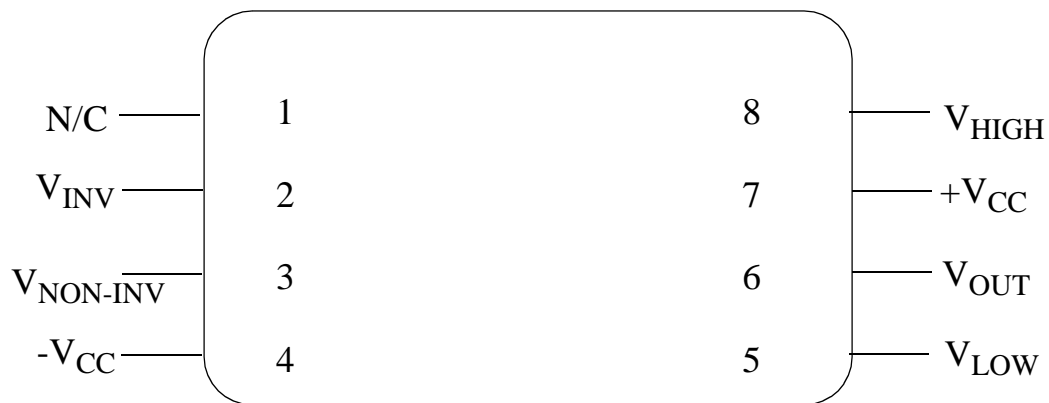
MILAERO
CONFIGURATION CONTROL
MIL-M-38510
CONFIGURATION CONTROL

CONTROLLING DIMENSION: INCH

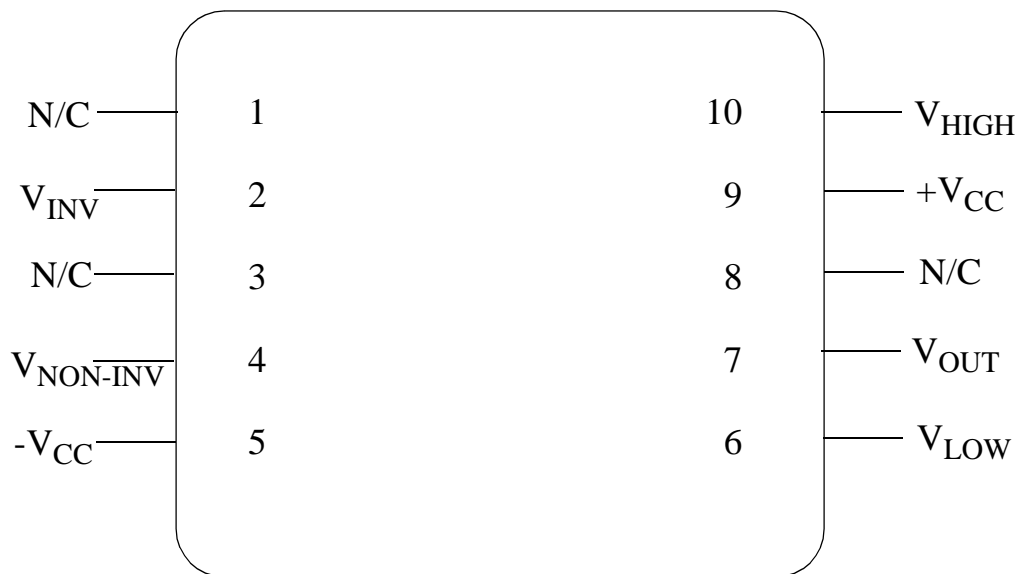
APPROVALS	DATE	NATIONAL SEMICONDUCTOR CORPORATION 2900 Semiconductor Drive, Santa Clara, CA 95052-8090	
DRAWN T. LEQUANG	09/21/93	SCALE	DRAWING NUMBER
DFTG. CHK.		N/A	B
ENGR. CHK.		DO NOT SCALE DRAWING	SHEET
APPROVAL			1 OF 1
 INCH [MM]		SIZE	REV
		MKT-J08A	L
		CERDIP (J), 8 LEAD	

NOTES: UNLESS OTHERWISE SPECIFIED

- LEAD FINISH TO BE 200 MICROMETERS / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
- JEDEC REGISTRATION MO-036, VARIATION AA, DATED 04/1981.



CLC501J
8 - LEAD DIP
CONNECTION DIAGRAM
TOP VIEW
P000409A



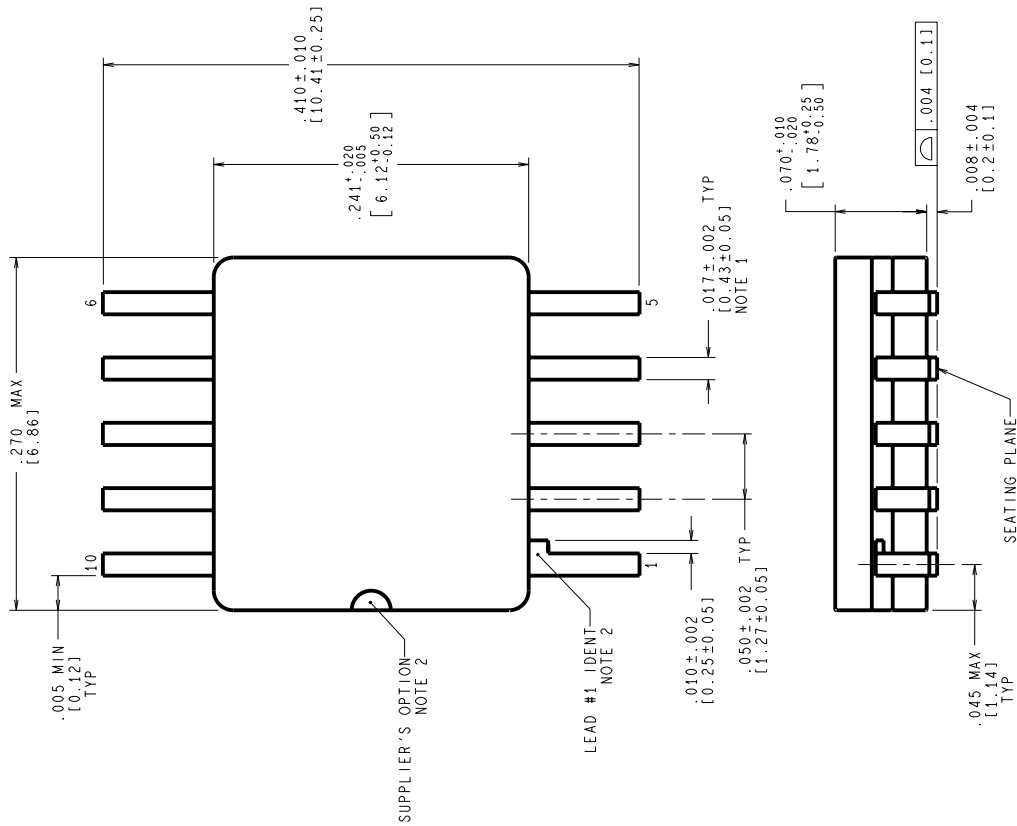
CLC501AWG
10 - LEAD CERAMIC SOIC
CONNECTION DIAGRAM
TOP VIEW
P000448A



National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

REVISIONS

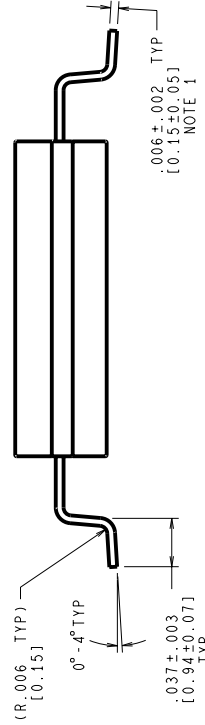
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL LD PITCH TOL WAS ±.005; CHANGE LD RADIUS TO REF DIM; REMOVE THE OTHER R.006 ±.002	11374	02/29/96	MS/MH
B		11441	04/15/96	MS/



CONTROLLING DIMENSION IS INCH
VALUES IN [] ARE MILLIMETERS

NOTES: UNLESS OTHERWISE SPECIFIED

- LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-PRF-38535 TO A MINIMUM THICKNESS OF 200 MICRONS/ 5.08 MICROMETERS. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE. MAXIMUM LIMIT MAY BE INCREASED BY .003 IN/ 0.08mm AFTER LEAD FINISH APPLIED.
- LEAD 1 IDENTIFICATION SHALL BE:
 - A NOTCH OR OTHER MARK WITHIN THIS AREA
 - A TAB ON LEAD 1, EITHER SIDE
- NO JEDEC REGISTRATION AS OF FEBRUARY 1996.



MIL-PRF-38535
CONFIGURATION CONTROL

APPROVALS	DATE	SCALE	SIZE	DRAWING NUMBER	REV
DRN: MARTA SUCHY	02/29/96	N/A	C	MKT-WG10A	B
DATE: CHK.					
ENGR: CHK.					
National Semiconductor 2800 Semiconductor Dr., Santa Clara, CA 95052-8090					
CERPACK, 10 LEAD, GULL WING					
DO NOT SCALE DRAWING SHEET 1 of 1					

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0A0	M0003288	03/09/99	Shaw Mead	Initial MDS Release