

VT82C596B
South Bridge

PIPC
PCI Integrated Peripheral Controller

PC98 Compliant PCI-to-ISA Bridge with ACPI, Enhanced Power Management, SMBus, APIC, Distributed DMA, Serial IRQ, Plug and Play, UltraDMA-33/66 Master Mode PCI-EIDE Controller USB Controller, Keyboard Controller, and RTC

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REVISION HISTORY

Document Release	Date	Revision	Initials
Revision 0.1	2/23/99	Initial release based on 82C596A Data Sheet revision 1.1 - Added UltraDMA-66 to feature bullets and overview - Added integrated APIC (changed H18, K18, J17 pin descriptions) - Added note to RTC CMOS Register Summary - Added / changed function 0 Rx42[6], Rx48[7-4], Rx5B[3], Rx5C[7-4, 2], Rx74[29-24, 8, 1], Rx87-89 - Added / changed function 3 Rx8, Rx4D[2-0], Rx54-55, Rx58-5B, Rx90-91, RxD2-D6 (80-88 renumbered), PMU I/O Offset 0[11], 20[14, 7-1], 22[14, 7-1], 24[14, 7-1], 28[15-11], 2A[15-11], 2C[11-10], 38[2-1], 44[10-1], 4C[30-0]	DH
Revision 0.2	3/9/99	Updated feature bullets, overview, and pin descriptions Replaced IDE function 1 with registers from 686B to reflect UltraDMA-66 Added / changed PMU function 3 registers Rx42[7-6, 4], Rx58-5B, PMU I/O Offset 0[8], 2C[2], 30[10-0], 34[10-0], 38[6, 4-3], 40 (removed)	DH
Revision 0.3	6/17/99	Changed Function 0 Rx42[2-0], 43[5-4], 50 default, 55[3-0], 57[3-0], 58[3-0], 88[5], Function 1 RxD, 42-43, 45[3-2], 54[4-3], 70, 74-75, 78, 7C-7D, Function 2 Rx41[7-3], Function 3 Rx4C-4F default value	DH

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VT82C596B PIPC
PCI INTEGRATED PERIPHERAL CONTROLLER

PC98 COMPLIANT PCI-TO-ISA BRIDGE WITH ACPI, ENHANCED POWER MANAGEMENT, SMBUS, APIC, DISTRIBUTED DMA, SERIAL IRQ, PLUG AND PLAY, ULTRADMA-33/66 MASTER MODE PCI-EIDE CONTROLLER, USB CONTROLLER, KEYBOARD CONTROLLER, AND RTC

- **Inter-operable with VIA and other Host-to-PCI Bridges**
  - Combine with VT82C598 (Apollo MVP3) for a complete 66 / 75 / 83 / 100MHz Socket-7 PCI / AGP / ISA system
  - Combine with VT82C693 (Apollo ProPlus) for a complete 66 / 100 MHz Socket-370 or Slot-1 PCI / ISA system
  - Combine with VT82C693A (Apollo Pro133) for a complete 66 / 100 / 133 MHz Skt-370 or Slot-1 PCI / ISA system
- **PC98 Compliant PCI to ISA Bridge**
  - Integrated ISA Bus Controller with integrated DMA, timer, and interrupt controller
  - Integrated Keyboard Controller with PS2 mouse support
  - Integrated DS12885-style Real Time Clock with extended 256 byte CMOS RAM and Day/Month Alarm for ACPI
  - Integrated USB Controller with root hub and two function ports
  - Integrated UltraDMA-33/66 master mode EIDE controller with enhanced PCI bus commands
  - PCI-2.1 compliant with delay transaction
  - Eight double-word line buffer between PCI and ISA bus
  - One-level PCI to ISA post-write buffer
  - Supports type F DMA transfers
  - Distributed DMA support for ISA legacy DMA across the PCI bus
  - Sideband signal support for PC/PCI and serial interrupt for docking and non-docking applications
  - Serial Interrupt input
  - Fast reset and Gate A20 operation
  - Edge trigger or level-sensitive interrupts
  - Flash EPROM, 2Mb EPROM and combined BIOS support
  - Supports positive and subtractive decoding
- **Universal Serial Bus Controller**
  - USB v.1.1 and Intel Universal HCI v.1.1 compatible
  - Eighteen level (doublewords) data FIFO with full scatter / gather capabilities
  - Root hub and two function ports
  - Integrated physical layer transceivers with over-current detection status on USB inputs
  - Legacy keyboard and PS/2 mouse support
- **Advanced Programmable Interrupt Controller (APIC)**
  - Integrated on-chip
  - Control pins provided for support of optional external APIC
  - Used to extend system interrupt capability
  - PC98 compliant

- **UltraDMA-33/66 Master Mode PCI EIDE Controller**
  - Dual channel master mode PCI supporting four Enhanced IDE devices
  - Transfer rate up to 22MB/sec to cover PIO mode 4, multi-word DMA mode 2 drives, and beyond
  - Extension to UltraDMA-33 interface for transfer rates to 33MB/sec
  - Extension to UltraDMA-66 interface for transfer rates to 66MB/sec
  - Thirty-two levels (doublewords) of prefetch and write buffers
  - Dual DMA engine for concurrent dual channel operation
  - Bus master programming interface for SFF-8038i rev.1.0 and Windows-95 compliant
  - Full scatter gather capability
  - Support ATAPI compliant devices including DVD devices
  - Support PCI native and ATA compatibility modes
  - Complete software driver support
  - Supports glue-less “Swap-Bay” option with full electrical isolation
- **System Management Bus Interface**
  - Host interface for processor communications
  - Slave interface for external SMBus masters
- **Sophisticated PC98-Compatible Mobile Power Management**
  - Supports both ACPI (Advanced Configuration and Power Interface) and legacy (APM) power management
  - ACPI v1.0 Compliant
  - APM v1.2 Compliant
  - CPU clock throttling and clock stop control for complete ACPI C0 to C3 state support
  - PCI bus clock run and PCI/CPU clock generator stop control
  - Supports multiple system suspend types: power-on suspends with flexible CPU/PCI bus reset options, suspend to DRAM, and suspend to disk (soft-off), all with hardware automatic wake-up
  - Multiple suspend power plane controls and suspend status indicators
  - One idle timer, one peripheral timer and one general purpose timer, plus 24/32-bit ACPI compliant timer
  - Normal, doze, sleep, suspend and conserve modes
  - Global and local device power control
  - System event monitoring with two event classes
  - Primary and secondary interrupt differentiation for individual channels
  - Dedicated input pins for power and sleep buttons, external modem ring indicator, and notebook lid open/close for system wake-up
  - Up to 22 general purpose input ports and 31 output ports
  - Multiple internal and external SMI sources for flexible power management models
  - Two programmable chip selects and one microcontroller chip select
  - Enhanced integrated real time clock (RTC) with date alarm, month alarm, and century field
  - Thermal alarm support
  - Cache SRAM power-down control
  - Hot docking support
  - I/O pad leakage control
- **Plug and Play Controller**
  - PCI interrupts steerable to any interrupt channel
  - Dual interrupt and DMA signal steering for on-board plug and play devices
  - Microsoft Windows 95™ and plug and play BIOS compliant
- **Built-in NAND-tree pin scan test capability**
- **0.5u, 3.3V, low power CMOS process**
- **Single chip 324 pin BGA**

OVERVIEW

The VT82C596B south bridge is a high integration, high performance, power-efficient, and high compatibility device that supports PCI / ISA bus bridge functionality to make a complete Microsoft PC98-compliant system. In addition to complete ISA extension bus functionality, the VT82C596B includes standard intelligent peripheral controllers:

a) Master mode enhanced IDE controller with dual channel DMA engine and interlaced dual channel commands. Dedicated FIFO coupled with scatter and gather master mode operation allows high performance transfers between PCI and IDE devices. In addition to standard PIO and DMA mode operation, the VT82C596B also supports the UltraDMA-33 standard to allow reliable data transfer rates up to 33MB/sec throughput and the UltraDMA-66 standard for 66MB/sec data transfer. The IDE controller is SFF-8038i v1.0 and Microsoft Windows-95 / 98 / NT compliant.

b) Universal Serial Bus controller that is USB v1.1 and Universal HCI v1.1 compliant. The VT82C596B includes the root hub with two function ports with integrated physical layer transceivers. The USB controller allows hot plug and play and isochronous peripherals to be inserted into the system with universal driver support. The controller also implements legacy keyboard and mouse support so that legacy software can run transparently in a non-USB-aware operating system environment.

c) Keyboard controller with PS2 mouse support.

d) Real Time Clock with 256 byte extended CMOS. In addition to the standard ISA RTC functionality, the integrated RTC also includes the date alarm, century field, and other enhancements for compatibility with the ACPI standard.

e) Notebook-class power management functionality compliant with ACPI and legacy APM requirements. Multiple sleep states (power-on suspend, suspend-to-DRAM, and suspend-to-Disk) are supported with hardware automatic wake-up. Additional functionality includes event monitoring, CPU clock throttling and stop (Intel processor protocol), PCI bus clock stop control, modular power, clock and leakage control, hardware-based and software-based event handling, general purpose I/O, chip select and external SMI.

f) Full System Management Bus (SMBus) interface.

g) Distributed DMA capability for support of ISA legacy DMA over the PCI bus. PC/PCI and Serial IRQ mechanisms are also supported for docking and non-docking applications.

h) Plug and Play controller that allows complete steerability of all PCI interrupts to any interrupt channel. Three additional steerable interrupt channels are provided to allow plug and play and reconfigurability of on-board peripherals for Windows 95 compliance.

i) Integrated APIC (see the Win98 Hardware Design Guide)

The VT82C596B also enhances the functionality of the standard ISA peripherals. The integrated interrupt controller supports both edge and level triggered interrupts channel by channel. The integrated DMA controller supports type F DMA in addition to standard ISA DMA modes. Compliant with the PCI-2.1 specification, the VT82C596B supports delayed transactions so that slower ISA peripherals do not block the traffic of the PCI bus. Special circuitry is built in to allow concurrent operation without causing dead lock even in a PCI-to-PCI bridge environment. The chip also includes eight levels (doublewords) of line buffers from the PCI bus to the ISA bus to further enhance overall system performance.

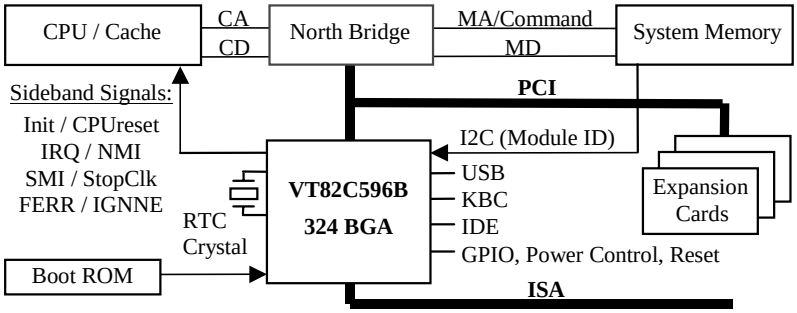


Figure 1. PC System Configuration Using the VT82C596B

PINOUTS

Figure 2. VT82C596B Ball Diagram (Top View)

Key	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	PCI RST#	AD 27	ID SEL	AD 19	FRA ME#	SERR#	AD 13	AD 9	AD 5	AD 1	PCI RQB#	P GNT#	SD D6	SD D4	SD D13	SD DRQ	SD DACK#	SD A2	PD D8	PD D7
B	AD 31	AD 26	AD 23	AD 18	I RDY#	PAR	AD 12	AD 8	AD 4	AD 0	PCI RQC#	P REQ#	SD D9	SD D11	SD D1	SD IOW#	SD A1	SD CS1#	PD D9	PD D6
C	AD 30	AD 25	AD 22	AD 17	T RDY#	CBE 1#	AD 11	CBE 0#	AD 3	PCK RUN#	PCI RQD#	SD D7	SD D5	SD D3	SD D14	SD IOR#	SD A0	SD CS3#	PD D10	PD D5
D	AD 28	CBE 3#	AD 20	CBE 2#	STOP#	AD 14	AD 10	AD 6	AD 2	**GND**	P CLK	SD D8	SD D10	SD D2	SD D15	SD RDY	PD D12	PD D3	PD D11	PD D4
E	AD 29	AD 24	AD 21	AD 16	DEV SEL#	AD 15	**GND**	AD 7	**VCC**	PCI RQA#	**VCC**	**VCC**	**GND**	SD D12	SD D0	**VCC**	PD D14	PD D1	PD D13	PD D2
F	USB-P1+	GPO 28	GPO29 SCI#	GPO 30	**VCC**	**VCC**								**VCC**	**VCC**	PD IOW#	PD IOR#	PD DRQ	PD D15	PD D0
G	PIRQ D#	USB-P0+	GPI 21	GPO 0	GPO 27	**VCC**										PD A0	PD A2	PD A1	PD DACK#	PD RDY
H	GPI 18	USB P1-	USB P0-	GPI 19	GPI 20											PD CS3#	PD CS1#	ACS#/ APD0	TH RM#	IRQ0 OUT
J	USB OC0#	USB OC1#	GPI 14	NC / KEYL	**GND USB**											**VREF**	AAK#/ APD1	STP CLK#	SER IRQ	IRQ 1
K	KBCS# /MSDT	ROM CS#	GPI 16	GPI 17	**VCC USB**											ZZ	SPKR	ARQ#/ WSC#	FERR#	SLP#
L	RTC-ALE	GPI 13	USB CLK	PCS 0#	GPI 15											**V BAT**	IGN NE#	INIT	INTR	NMI
M	REQ A#	RTC CS#	X DIR#	X OE#	NC / KBDT											NC	RSM RST#	PWR GD	CPU RST	A20 M#
N	GNT A#	REQ B#	NC / KBCK	MC CS#	PCS 1#											**VCC SUS**	SMB ALRT#	NC	RTC X1	RC IN#
P	A20G/ MSCK	GNT B#	REQ C#	GNT C#	PIRQ C#										**VCC**	LID	SUS CLK	RI#	GPI 1	SMI#
R	CPU STP#	PCI STP#	PIRQ A#	PIRQ B#	**NC**	**VCC**	**VCC**								**VCC**	**VCC SUS**	CFG 1	CFG 2	SMB CLK	RTC X2
T	**SD 6**	**SD 3**	IOCH RDY	IOW#	SA 16	**VCC**	B CLK	SA 9	IRQ 3	SA 4	SA 1	LA 23	IRQ 12	LA 18	DACK 5#	**SD9**	SUS ST1#	SUS ST2#	GPO 8	SMB DATA
U	IRQ 9	**SD 2**	SMEM W#	SA 18	DRQ 3	DRQ 1	SA 11	IRQ 5	SA 6	BALE	SA 0	IRQ 10	LA 20	DACK 0#	MEM W#	DRQ 6	DRQ 7	SUS C#	BAT LOW#	PWR BTN#
V	**SD 7**	DRQ 2	**SD 0**	SA 19	DACK 3#	SA 14	SA 12	IRQ 6	SA 7	TC	OSC	IOCS 16#	LA 21	IRQ 14	MEM R#	DACK 6#	**SD 11**	TEST#	SUS B#	EXT SMI#
W	RST DRV	**SD 4**	**SD 1**	SMEM R#	SA 17	DACK 1#	RFSH#	SA 10	IRQ 4	SA 5	SA 2	S BHE#	IRQ 11	LA 19	DRQ 0	**SD 8**	DACK 7#	**SD 13**	**SD 15**	SUS A#
Y	IO CHK#	**SD 5**	ZWS#	AEN	IOR#	SA 15	SA 13	IRQ 7	SA 8	DACK 2#	SA 3	MCS 16#	LA 22	IRQ 15	LA 17	DRQ 5	**SD 10**	**SD 12**	**SD 14**	IRQ 8#

GND GND GND GND
GND GND GND GND
GND GND GND GND
GND GND GND GND

Note: Some of the pins above have alternate functions and alternate names. The table above contains only one name, but the pin lists and pin descriptions contain all names.

Figure 3. VT82C596B Pin List (Numerical Order)

Pin		Pin Name	Pin		Pin Name	Pin		Pin Name	Pin		Pin Name	Pin		Pin Name
A01	O	PCIRST#	D06	IO	AD14	H17	O	PDCS1#	**N16**	**P**	**VCCSUS**	U17	I	DRQ7
A02	IO	AD27	D07	IO	AD10	H18	O	APICCS#/D0/GPO13	N17	I	SMBALRT# / GPI11	U18	O	SUSC# / GPO16
A03	I	IDSEL	D08	IO	AD6	H19	I	THRM# / GPI8	N18	-	NC	U19	I	BATLOW# / GPI9
A04	IO	AD19	D09	IO	AD2	H20	O	IRQ0OUT / GPO14	N19	I	RTCX1	U20	I	PWRBTN#
A05	IO	FRAME#	**D10**	**P**	**GND**	J01	I	USBOC0#	N20	I	RCIN#	V01	IO	SD7
A06	I	SERR#	D11	I	PCLK	J02	I	USBOC1#	P01	IO	A20GATE / MSCK	V02	I	DRQ2
A07	IO	AD13	D12	IO	SDD8	J03	I	GPI14	P02	O	GNTB# / GPO10	V03	IO	SD0
A08	IO	AD9	D13	IO	SDD10	J04	I	NC / KEYLOCK	P03	I	REQC# / GPI4	V04	IO	SA19
A09	IO	AD5	D14	IO	SDD2	**J05**	**P**	**GNDUSB**	P04	O	GNTC# / GPO11	V05	O	DACK3#
A10	IO	AD1	D15	IO	SDD15	**J09**	**P**	**GND**	P05	IOD	PIRQC#	V06	IO	SA14
A11	I	PCIREQB#	D16	I	SDRDY	**J10**	**P**	**GND**	**P15**	**P**	**VCC**	V07	IO	SA12
A12	I	PGNT#	D17	IO	PDD12	**J11**	**P**	**GND**	P16	I	LID / GPI10	V08	I	IRQ6
A13	IO	SDD6	D18	IO	PDD3	**J12**	**P**	**GND**	P17	O	SUSCLK	V09	IO	SA7
A14	IO	SDD4	D19	IO	PDD11	**J16**	**P**	**VREF**	P18	I	RI# / GPI12	V10	O	TC
A15	IO	SDD13	D20	IO	PDD4	J17	O	APICACK#/D1/GPO12	P19	I	GPI1 / PME#	V11	I	OSC
A16	I	SDDRQ	E01	IO	AD29	J18	OD	STPCLK#	P20	OD	SMI#	V12	IO	IOCS16#
A17	O	SDDACK#	E02	IO	AD24	J19	I	SERIRQ / GPI7	R01	O	CPUSTP# / GPO17	V13	IO	LA21
A18	O	SDA2	E03	IO	AD21	J20	I	IRQ1	R02	O	PCISTP# / GPO18	V14	I	IRQ14
A19	IO	PDD8	E04	IO	AD16	K01	IO	KBCS#/GPO26/MSDT	R03	IOD	PIRQA#	V15	IO	MEMR#
A20	IO	PDD7	E05	IO	DEVSEL#	K02	O	ROMCS#	R04	IOD	PIRQB#	V16	O	DACK6#
B01	IO	AD31	E06	IO	AD15	K03	I	GPI16	R05	-	NC	V17	IO	SD11
B02	IO	AD26	**E07**	**P**	**GND**	K04	I	GPI17	**R06**	**P**	**VCC**	V18	I	TEST#
B03	IO	AD23	E08	IO	AD7	**K05**	**P**	**VCCUSB**	**R07**	**P**	**VCC**	V19	O	SUSB# / GPO15
B04	IO	AD18	**E09**	**P**	**VCC**	**K09**	**P**	**GND**	**R15**	**P**	**VCC**	V20	IOD	EXTSMI#
B05	IO	IRDY#	E10	I	PCIREQA#	**K10**	**P**	**GND**	**R16**	**P**	**VCCSUS**	W01	O	RSTDRV
B06	O	PAR	**E11**	**P**	**VCC**	**K11**	**P**	**GND**	R17	I	CFG1	W02	IO	SD4
B07	IO	AD12	**E12**	**P**	**VCC**	**K12**	**P**	**GND**	R18	I	CFG2	W03	IO	SD1
B08	IO	AD8	**E13**	**P**	**GND**	K16	O	ZZ / GPO19	R19	IO	SMBCLK	W04	O	SMEMR#
B09	IO	AD4	E14	IO	SDD12	K17	O	SPKR	R20	O	RTCX2	W05	IO	SA17
B10	IO	AD0	E15	IO	SDD0	K18	I	APICRQ#/WSC#/GPI5	T01	IO	SD6	W06	O	DACK1#
B11	I	PCIREQC#	**E16**	**P**	**VCC**	K19	I	FERR#	T02	IO	SD3	W07	IO	RFSH#
B12	O	PREQ#	E17	IO	PDD14	K20	OD	SLP#	T03	IOD	IOCHRDY	W08	IO	SA10
B13	IO	SDD9	E18	IO	PDD1	L01	O	RTCAS / GPO25	T04	IO	IOW#	W09	I	IRQ4
B14	IO	SDD11	E19	IO	PDD13	L02	I	GPI13 / SLPBTN#	T05	IO	SA16	W10	IO	SA5
B15	IO	SDD1	E20	IO	PDD2	L03	I	USBCLK	**T06**	**P**	**VCC**	W11	IO	SA2
B16	O	SDIOW#	F01	IO	USBP1+	L04	O	PCS0#	T07	O	BCLK	W12	IO	SBHE#
B17	O	SDA1	F02	O	GPO28	L05	I	GPI15	T08	IO	SA9	W13	I	IRQ11
B18	O	SDCS1#	F03	O	GPO29/SCI#	**L09**	**P**	**GND**	T09	I	IRQ3	W14	IO	LA19 / GPO3
B19	IO	PDD9	F04	O	GPO30	**L10**	**P**	**GND**	T10	IO	SA4	W15	I	DRQ0
B20	IO	PDD6	**F05**	**P**	**VCC**	**L11**	**P**	**GND**	T11	IO	SA1	W16	IO	SD8
C01	IO	AD30	**F06**	**P**	**VCC**	**L12**	**P**	**GND**	T12	IO	LA23 / GPO7	W17	O	DACK7#
C02	IO	AD25	**F14**	**P**	**VCC**	**L16**	**P**	**VBAT**	T13	I	IRQ12	W18	IO	SD13
C03	IO	AD22	**F15**	**P**	**VCC**	L17	OD	IGNNE#	T14	IO	LA18 / GPO2	W19	IO	SD15
C04	IO	AD17	F16	O	PDIOW#	L18	OD	INIT	T15	O	DACK5#	W20	O	SUSA#
C05	IO	TRDY#	F17	O	PDIOR#	L19	OD	INTR	T16	IO	SD9	Y01	I	IOCHCK# / GPI0
C06	IO	CBE1#	F18	I	PDDRQ	L20	OD	NMI	T17	O	SUSST1# / GPO20	Y02	IO	SD5
C07	IO	AD11	F19	IO	PDD15	M01	I	REQA# / GPI2	T18	O	SUSST2# / GPO21	Y03	I	ZWS#
C08	IO	CBE0#	F20	IO	PDD0	M02	O	RTCCS# / GPO24	T19	O	GPO8	Y04	O	AEN
C09	IO	AD3	G01	IOD	PIRQD#	M03	O	XDIR# / GPO22	T20	IO	SMBDATA	Y05	IO	IOR#
C10	IO	PCKRUN#	G02	IO	USBP0+	M04	O	XOE# / GPO23	U01	I	IRQ9	Y06	IO	SA15
C11	I	PCIREQD#	G03	I	GPI21	M05	IO	NC / KBDT	U02	IO	SD2	Y07	IO	SA13
C12	IO	SDD7	G04	O	GPO0	**M09**	**P**	**GND**	U03	O	SMEMW#	Y08	I	IRQ7
C13	IO	SDD5	G05	O	GPO27	**M10**	**P**	**GND**	U04	IO	SA18	Y09	IO	SA8
C14	IO	SDD3	**G06**	**P**	**VCC**	**M11**	**P**	**GND**	U05	I	DRQ3	Y10	O	DACK2#
C15	IO	SDD14	G16	O	PDA0	**M12**	**P**	**GND**	U06	I	DRQ1	Y11	IO	SA3
C16	O	SDIOR#	G17	O	PDA2	M16	-	NC	U07	IO	SA11	Y12	IO	MCS16#
C17	O	SDA0	G18	O	PDA1	M17	I	RSMRST#	U08	I	IRQ5	Y13	IO	LA22 / GPO6
C18	O	SDCS3#	G19	O	PDDACK#	M18	I	PWRGD	U09	IO	SA6	Y14	I	IRQ15
C19	IO	PDD10	G20	I	PDRDY	M19	OD	CPURST	U10	O	BALE	Y15	IO	LA17 / GPO1
C20	IO	PDD5	H01	I	GPI18	M20	OD	A20M#	U11	IO	SA0	Y16	I	DRQ5
D01	IO	AD28	H02	IO	USBP1-	N01	O	GNTA# / GPO9	U12	I	IRQ10	Y17	IO	SD10
D02	IO	CBE3#	H03	IO	USBP0-	N02	I	REQB# / GPI3	U13	IO	LA20 / GPO4	Y18	IO	SD12
D03	IO	AD20	H04	I	GPI19	N03	IO	NC / KBCK	U14	O	DACK0#	Y19	IO	SD14
D04	IO	CBE2#	H05	I	GPI20	N04	O	MCCS#	U15	IO	MEMW#	Y20	I	IRQ8# / GPI6
D05	IO	STOP#	H16	O	PDCS3#	N05	O	PCS1#	U16	I	DRQ6			

Figure 4. VT82C596B Pin List (Alphabetical Order)

Pin		Pin Name	Pin		Pin Name	Pin		Pin Name	Pin		Pin Name	Pin		Pin Name
P01	IO	A20GATE / MSCK	K19	I	FERR#	K01	IO	KBCS#/GPO26/MSDT	M18	I	PWRGD	B13	IO	SDD09
M20	OD	A20M#	A05	IO	FRAME#	Y15	IO	LA17 / GPO1	N20	I	RCIN#	D13	IO	SDD10
B10	IO	AD00	**D10**	**P**	**GND**	T14	IO	LA18 / GPO2	M01	I	REQA# / GPI2	B14	IO	SDD11
A10	IO	AD01	**E07**	**P**	**GND**	W14	IO	LA19 / GPO3	N02	I	REQB# / GPI3	E14	IO	SDD12
D09	IO	AD02	**E13**	**P**	**GND**	U13	IO	LA20 / GPO4	P03	I	REQC# / GPI4	A15	IO	SDD13
C09	IO	AD03	**J09**	**P**	**GND**	V13	IO	LA21 / GPO5	W07	IO	RFSH#	C15	IO	SDD14
B09	IO	AD04	**J10**	**P**	**GND**	Y13	IO	LA22 / GPO6	P18	I	RI# / GPI12	D15	IO	SDD15
A09	IO	AD05	**J11**	**P**	**GND**	T12	IO	LA23 / GPO7	K02	O	ROMCS#	A17	O	SDDACK#
D08	IO	AD06	**J12**	**P**	**GND**	P16	I	LID / GPI10	M17	I	RSMRST#	A16	I	SDDRQ
E08	IO	AD07	**K09**	**P**	**GND**	N04	O	MCCS#	W01	O	RSTDRV	C16	O	SDIOR#
B08	IO	AD08	**K10**	**P**	**GND**	Y12	IO	MCS16#	L01	O	RTCAS/GPO25	B16	O	SDIOW#
A08	IO	AD09	**K11**	**P**	**GND**	V15	IO	MEMR#	M02	O	RTCCS#/GPO24	J19	I	SERIRQ / GPI7
D07	IO	AD10	**K12**	**P**	**GND**	U15	IO	MEMW#	N19	I	RTCX1	A06	I	SERR#
C07	IO	AD11	**L09**	**P**	**GND**	J04	I	NC / KEYLOCK	R20	O	RTCX2	D16	I	SDRDY
B07	IO	AD12	**L10**	**P**	**GND**	M05	IO	NC / KBDT	U11	IO	SA00	K20	OD	SLP#
A07	IO	AD13	**L11**	**P**	**GND**	N03	IO	NC / KBCK	T11	IO	SA01	N17	I	SMBALRT#/GPI11
D06	IO	AD14	**L12**	**P**	**GND**	M16	-	NC	W11	IO	SA02	R19	IO	SMBCLK
E06	IO	AD15	**M09**	**P**	**GND**	N18	-	NC	Y11	IO	SA03	T20	IO	SMBDATA
E04	IO	AD16	**M10**	**P**	**GND**	R05	-	NC	T10	IO	SA04	W04	O	SMEMR#
C04	IO	AD17	**M11**	**P**	**GND**	L20	OD	NMI	W10	IO	SA05	U03	O	SMEMW#
B04	IO	AD18	**M12**	**P**	**GND**	V11	I	OSC	U09	IO	SA06	P20	OD	SMI#
A04	IO	AD19	**J05**	**P**	**GNDUSB**	B06	O	PAR	V09	IO	SA07	K17	O	SPKR
D03	IO	AD20	N01	O	GNTA# / GPO9	C10	IO	PCKRUN#	Y09	IO	SA08	D05	IO	STOP#
E03	IO	AD21	P02	O	GNTB# / GPO10	D11	I	PCLK	T08	IO	SA09	J18	OD	STPCLK#
C03	IO	AD22	P04	O	GNTC# / GPO11	E10	I	PCIREQA#	W08	IO	SA10	W20	O	SUSA#
B03	IO	AD23	P19	I	GPI1 / PME#	A11	I	PCIREQB#	U07	IO	SA11	V19	O	SUSB# / GPO15
E02	IO	AD24	L02	I	GPI13 / SLPBTN#	B11	I	PCIREQC#	V07	IO	SA12	U18	O	SUSC# / GPO16
C02	IO	AD25	J03	I	GPI14	C11	I	PCIREQD#	Y07	IO	SA13	P17	O	SUSCLK
B02	IO	AD26	L05	I	GPI15	A01	O	PCIRST#	V06	IO	SA14	T17	O	SUSST1# / GPO20
A02	IO	AD27	K03	I	GPI16	R02	O	PCISTP#/GPO18	Y06	IO	SA15	T18	O	SUSST2# / GPO21
D01	IO	AD28	K04	I	GPI17	L04	O	PCS0#	T05	IO	SA16	V10	O	TC
E01	IO	AD29	H01	I	GPI18	N05	O	PCS1#	W05	IO	SA17	V18	I	TEST#
C01	IO	AD30	H04	I	GPI19	G16	O	PDA0	U04	IO	SA18	H19	I	THRM# / GPI8
B01	IO	AD31	H05	I	GPI20	G18	O	PDA1	V04	IO	SA19	C05	IO	TRDY#
Y04	O	AEN	G03	I	GPI21	G17	O	PDA2	W12	IO	SBHE#	L03	I	USBCLK
J17	O	APICAK#//D1/O12	G04	O	GPO00	H17	O	PDCS1#	V03	IO	SD00	J01	I	USBOC0#
H18	O	APICCS#/D0/O13	T19	O	GPO08	H16	O	PDCS3#	W03	IO	SD01	J02	I	USBOC1#
K18	I	APICRQ#/WSC#/I5	G05	O	GPO27	F20	IO	PDD00	U02	IO	SD02	H03	IO	USBP0-
U10	O	BALE	F02	O	GPO28	E18	IO	PDD01	T02	IO	SD03	G02	IO	USBP0+
U19	I	BATLOW# / GPI9	F03	O	GPO29 / SCIOUT#	E20	IO	PDD02	W02	IO	SD04	H02	IO	USBP1-
T07	O	BCLK	F04	O	GPO30	D18	IO	PDD03	Y02	IO	SD05	F01	IO	USBP1+
C08	IO	CBE0#	A03	I	IDSEL	D20	IO	PDD04	T01	IO	SD06	**L16**	**P**	**VBAT**
C06	IO	CBE1#	L17	OD	IGNNE#	C20	IO	PDD05	V01	IO	SD07	**E09**	**P**	**VCC**
D04	IO	CBE2#	L18	OD	INIT	B20	IO	PDD06	W16	IO	SD08	**E11**	**P**	**VCC**
D02	IO	CBE3#	L19	OD	INTR	A20	IO	PDD07	T16	IO	SD09	**E12**	**P**	**VCC**
R17	I	CFG1	Y01	I	IOCHCK# / GPI0	A19	IO	PDD08	Y17	IO	SD10	**E16**	**P**	**VCC**
R18	I	CFG2	T03	IOD	IOCHRDY	B19	IO	PDD09	V17	IO	SD11	**F05**	**P**	**VCC**
M19	OD	CPURST	V12	IO	IOCS16#	C19	IO	PDD10	Y18	IO	SD12	**F06**	**P**	**VCC**
R01	O	CPUSTP# / GPO17	Y05	IO	IOR#	D19	IO	PDD11	W18	IO	SD13	**F14**	**P**	**VCC**
U14	O	DACK0#	T04	IO	IOW#	D17	IO	PDD12	Y19	IO	SD14	**F15**	**P**	**VCC**
W06	O	DACK1#	B05	IO	IRDY#	E19	IO	PDD13	W19	IO	SD15	**G06**	**P**	**VCC**
Y10	O	DACK2#	H20	**O**	IRQ0OUT / GPO14	E17	IO	PDD14	C17	O	SDA0	**P15**	**P**	**VCC**
V05	O	DACK3#	J20	I	IRQ1	F19	IO	PDD15	B17	O	SDA1	**R06**	**P**	**VCC**
T15	O	DACK5#	T09	I	IRQ3	G19	O	PDDACK#	A18	O	SDA2	**R07**	**P**	**VCC**
V16	O	DACK6#	W09	I	IRQ4	F18	I	PDDRQ	B18	O	SDCS1#	**R15**	**P**	**VCC**
W17	O	DACK7#	U08	I	IRQ5	F17	O	PDIOR#	C18	O	SDCS3#	**T06**	**P**	**VCC**
E05	IO	DEVSEL#	V08	I	IRQ6	F16	O	PDIOW#	E15	IO	SDD00	**N16**	**P**	**VCCSUS**
W15	I	DRQ0	Y08	I	IRQ7	A12	I	PGNT#	B15	IO	SDD01	**R16**	**P**	**VCCSUS**
U06	I	DRQ1	Y20	I	IRQ8# / GPI6	B12	O	PREQ#	D14	IO	SDD02	**K05**	**P**	**VCCUSB**
V02	I	DRQ2	U01	I	IRQ9	G20	I	PDRDY	C14	IO	SDD03	**J16**	**P**	**VREF**
U05	I	DRQ3	U12	I	IRQ10	R03	IOD	PIRQA#	A14	IO	SDD04	M03	O	XDIR# / GPO22
Y16	I	DRQ5	W13	I	IRQ11	R04	IOD	PIRQB#	C13	IO	SDD05	M04	O	XOE# / GPO23
U16	I	DRQ6	T13	I	IRQ12	P05	IOD	PIRQC#	A13	IO	SDD06	Y03	I	ZWS#
U17	I	DRQ7	V14	I	IRQ14	G01	IOD	PIRQD#	C12	IO	SDD07	K16	O	ZZ / GPO19
V20	IOD	EXTSMI#	Y14	I	IRQ15	U20	I	PWRBTN#	D12	IO	SDD08			

Referenced to VCCSUS: BATLOW#, CFG1-2, EXTSMI#, GPI1, GPO8, IRQ8#, LID, PWRBTN#, PWRGD, RI#, RSMRST#, SUSA-C#, SUSST1-2#, TEST#

Table 1. Pin Descriptions

PCI Bus Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
PCLK	D11	I	**PCI Clock.** PCLK provides timing for all transactions on the PCI Bus.
FRAME#	A5	IO	**Frame.** Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer is desired by the cycle initiator.
AD[31:0]	B1, C1, E1, D1, A2, B2, C2, E2, B3, C3, E3, D3, A4, B4, C4, E4, E6, D6, A7, B7, C7, D7, A8, B8, E8, D8, A9, B9, C9, D9, A10, B10	IO	**Address/Data Bus.** The standard PCI address and data lines. The address is driven with FRAME# assertion and data is driven or received in following cycles.
C/BE[3:0]#	D2, D4, C6, C8	IO	**Command/Byte Enable.** The command is driven with FRAME# assertion. Byte enables corresponding to supplied or requested data are driven on following clocks.
IRDY#	B5	IO	**Initiator Ready.** Asserted when the initiator is ready for data transfer.
TRDY#	C5	IO	**Target Ready.** Asserted when the target is ready for data transfer.
STOP#	D5	IO	**Stop.** Asserted by the target to request the master to stop the current transaction.
DEVSEL#	E5	IO	**Device Select.** The VT82C596B asserts this signal to claim PCI transactions through positive or subtractive decoding.
PAR	B6	IO	**Parity.** A single parity bit is provided over AD[31:0] and C/BE[3:0]#.
SERR#	A6	I	**System Error.** SERR# can be pulsed active by any PCI device that detects a system error condition. Upon sampling SERR# active, the VT82C596B can be programmed to generate an NMI to the CPU.
IDSEL	A3	I	**Initialization Device Select.** IDSEL is used as a chip select during PCI configuration read and write cycles.
PIRQA-D#	R3, R4, P5, G1	I	**PCI Interrupt Request**. These pins are typically connected to the PCI bus INTA#-INTD# pins as follows: PIRQA# / PIRQB# / PIRQC# / PIRQD# PCI Slot 1: INTA# / INTB# / INTC# / INTD# PCI Slot 2: INTB# / INTC# / INTD# / INTA# PCI Slot 3: INTC# / INTD# / INTA# / INTB# PCI Slot 4: INTD# / INTA# / INTB# / INTC#
PREQ#	B12	O	**PCI Request.** This signal goes to the North Bridge to request the PCI bus.
PGNT#	A12	I	**PCI Grant.** This signal is driven by the North Bridge to grant PCI access to the VT82C596B.
PCKRUN#	C10	IO	**PCI Bus Clock Run.** This signal indicates whether the PCI clock is or will be stopped (high) or running (low). The VT82C596B drives this signal low when the PCI clock is running (default on reset) and releases it when it stops the PCI clock. External devices may assert this signal low to request that the PCI clock be restarted or prevent it from stopping. Refer to the PCI Mobile Design Guide for more details.

CPU Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
CPURST	M19	OD	**CPU Reset.** The VT82C596B asserts CPURST to reset the CPU during power-up.
INTR	L19	OD	**CPU Interrupt.** INTR is driven by the VT82C596B to signal the CPU that an interrupt request is pending and needs service.
NMI	L20	OD	**Non-Maskable Interrupt.** NMI is used to force a non-maskable interrupt to the CPU. The VT82C596B generates an NMI when either SERR# or IOCHK# is asserted.
INIT	L18	OD	**Initialization.** The VT82C596B asserts INIT if it detects a shut-down special cycle on the PCI bus or if a soft reset is initiated by the register
STPCLK#	J18	OD	**Stop Clock.** STPCLK# is asserted by the VT82C596B to the CPU in response to different Power-Management events.
SMI#	P20	OD	**System Management Interrupt.** SMI# is asserted by the VT82C596B to the CPU in response to different Power-Management events.
FERR#	K19	I	**Numerical Coprocessor Error.** This signal is tied to the coprocessor error signal on the CPU. Internally generates interrupt 13 if active.
IGNNE#	L17	OD	**Ignore Numeric Error.** This pin is connected to the "ignore error" pin on the CPU.
SLP#	K20	OD	**Sleep.** Used to put the CPU to sleep. Used with slot-1 CPUs only. Not currently used with socket-7 CPUs.

Universal Serial Bus Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
USBP0+	G2	IO	**USB Port 0 Data +**
USBP0-	H3	IO	**USB Port 0 Data -**
USBOC0#	J1	I	**USB Port 0 Over Current Detect.** Port 0 is disabled if this input is low.
USBP1+	F1	IO	**USB Port 1 Data +**
USBP1-	H2	IO	**USB Port 1 Data -**
USBOC1#	J2	I	**USB Port 1 Over Current Detect.** Port 1 is disabled if this input is low.
USBCLK	L3	I	**USB Clock.** 48MHz clock input for Universal Serial Bus interface

System Management Bus (SMB) Interface (I^2C Bus)			
Signal Name	**Pin #**	**I/O**	**Signal Description**
SMBCLK	R19	IO	**SMB / I^2C Clock.**
SMBDATA	T20	IO	**SMB / I^2C Data.**
SMBALRT# / GPI11	N17	I	**MultiFunction Pin** **SMB Alert.** (Rx74[5] = 0) When the chip is enabled to allow it, assertion generates an IRQ or SMI interrupt or a power management resume event. **General Purpose Input 11.** (Rx74[5] = 1) General purpose input.

UltraDMA-33 / 66 Enhanced IDE Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
PDRDY / PDDMARDY# / PDSTROBE	G20	I	EIDE Mode: **Primary I/O Channel Ready.** Device ready indicator UltraDMA Mode: **Primary Device DMA Ready**. Output flow control. The device may assert PDDMARDY# to pause output transfers **Primary Device Strobe**. Input data strobe (both edges). The device may stop PDSTROBE to pause input data transfers
SDRDY / SDDMARDY# / SDSTROBE	D16	I	EIDE Mode: **Secondary I/O Channel Ready.** Device ready indicator UltraDMA Mode: **Secondary Device DMA Ready**. Output flow control. The device may assert SDDMARDY# to pause output transfers **Secondary Device Strobe**. Input data strobe (both edges). The device may stop SDSTROBE to pause input data transfers
PDIOR# / PHDMARDY# / PHSTROBE	F17	O	EIDE Mode: **Primary Device I/O Read.** Device read strobe UltraDMA Mode: **Primary Host DMA Ready**. Primary channel input flow control**.** The host may assert PHDMARDY# to pause input transfers **Primary Host Strobe**. Output data strobe (both edges). The host may stop PHSTROBE to pause output data transfers
SDIOR# / SHDMARDY# / SHSTROBE	C16	O	EIDE Mode: **Secondary Device I/O Read.** Device read strobe UltraDMA Mode: **Secondary Host DMA Ready**. Input flow control. The host may assert SHDMARDY# to pause input transfers **Host Strobe B**. Output strobe (both edges). The host may stop SHSTROBE to pause output data transfers
PDIOW# / PSTOP	F16	O	EIDE Mode: **Primary Device I/O Write.** Device write strobe UltraDMA Mode: **Primary Stop**. Stop transfer: Asserted by the host prior to initiation of an UltraDMA burst; negated by the host before data is transferred in an UltraDMA burst. Assertion of STOP by the host during or after data transfer in UltraDMA mode signals the termination of the burst.
SDIOW# / SSTOP	B16	O	EIDE Mode: **Secondary Device I/O Write.** Device write strobe UltraDMA Mode: **Secondary Stop**. Stop transfer: Asserted by the host prior to initiation of an UltraDMA burst; negated by the host before data is transferred in an UltraDMA burst. Assertion of STOP by the host during or after data transfer in UltraDMA mode signals the termination of the burst.
PDDRQ	F18	I	**Primary Device DMA Request.** Primary channel DMA request
SDDRQ	A16	I	**Secondary Device DMA Request.** Secondary channel DMA request
PDDACK#	G19	O	**Primary Device DMA Acknowledge.** Primary channel DMA acknowledge
SDDACK#	A17	O	**Secondary Device DMA Acknowledge.** Secondary channel DMA acknowledge

UltraDMA-33 / 66 Enhanced IDE Interface (continued)			
Signal Name	**Pin #**	**I/O**	**Signal Description**
PDCS1#	H17	O	**Primary Master Chip Select.** This signal corresponds to CS1FX# on the primary IDE connector.
PDCS3#	H16	O	**Primary Slave Chip Select.** This signal corresponds to CS3FX# on the primary IDE connector.
SDCS1#	B18	O	**Secondary Master Chip Select.** This signal corresponds to CS17X# on the secondary IDE connector.
SDCS3#	C18	O	**Secondary Slave Chip Select.** This signal corresponds to CS37X# on the secondary IDE connector.
PDA[2-0]	G17, G18, G16	O	**Primary Disk Address.** PDA[2:0] are used to indicate which byte in either the ATA command block or control block is being accessed.
SDA[2-0]	A18, B17, C17	O	**Secondary Disk Address.** SDA[2:0] are used to indicate which byte in either the ATA command block or control block is being accessed.
PDD[15-0]	F19, E17, E19, D17, D19, C19, B19, A19, A20, B20, C20, D20, D18, E20, E18, F20	IO	**Primary Disk Data**
SDD[15-0]	D15, C15, A15, E14, B14, D13, B13, D12, C12, A13, C13, A14, C14, D14, B15, E15	IO	**Secondary Disk Data**

ISA Bus Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
SA[19:0]	V4, U4, W5, T5, Y6, V6, Y7, V7, U7, W8, T8, Y9, V9, U9, W10, T10, Y11, W11, T11, U11	IO	**ISA Address Bus**
LA[23:17]	T12, Y13, V13, U13, W14, T14, Y15	IO	**ISA "Latched" Address Bus**: The LA[23:17] address lines are bi-directional. These address lines allow accesses to physical memory on the ISA bus up to 16Mbytes.
SD[15:0]	W19, Y19, W18, Y18, V17, Y17, T16, W16, V1, T1, Y2, W2, T2, U2, W3, V3	IO	**ISA Bus Data.** SD[15:0] provide the data path for devices residing on the ISA bus. SD7:4 are strap options for keyboard inputs 6:3 (see Function 0 Rx5A)
SBHE#	W12	IO	**ISA Byte High Enable.** SBHE# indicates, when asserted, that a byte is being transferred on the upper byte (SD[15:8]) of the data bus. SBHE# is negated during refresh cycles.
IOR#	Y5	IO	**ISA I/O Read.** IOR# is the command to an ISA I/O slave device which indicates that the slave may drive data on to the ISA data bus.
IOW#	T4	IO	**ISA I/O Write.** IOW# is the command to an ISA I/O slave device which indicates that the slave may latch data from the ISA data bus.
MEMR#	V15	IO	**ISA Memory Read.** MEMR# is the command to a memory slave which indicates that it may drive data onto the ISA data bus.
MEMW#	U15	IO	**ISA Memory Write.** MEMW# is the command to a memory slave which indicates that it may latch data from the ISA data bus.
SMEMR#	W4	O	**ISA Standard Memory Read.** SMEMR# is the command to a memory slave, under 1MB, which indicates that it may drive data onto the ISA data bus
SMEMW#	U3	O	**ISA Standard Memory Write.** SMEMW# is the command to a memory slave, under 1MB, which indicates that it may latch data from the ISA data bus.
BALE	U10	O	**ISA Bus Address Latch Enable.** BALE is an active high signal asserted by the VT82C596B to indicate that the address (SA[19:0], LA[23:17] and the SBHE# signal) is valid
IOCS16#	V12	IO	**ISA 16-Bit I/O Chip Select.** This signal is driven by I/O devices on the ISA Bus to indicate that they support 16-bit I/O bus cycles.
MCS16#	Y12	IO	**ISA Memory Chip Select 16.** ISA slaves that are 16-bit memory devices drive this line low to indicate they support 16-bit memory bus cycles.
IOCHCK#	Y1	I	**ISA I/O Channel Check.** When this signal is asserted, it indicates that a parity or an uncorrectable error has occurred for a device or memory on the ISA Bus.
IOCHRDY	T3	IOD	**ISA I/O Channel Ready.** This signal is normally high. Devices on the ISA Bus assert IOCHRDY low to indicate that additional time (wait states) is required to complete the cycle.
ZWS#	Y3	I	**ISA Zero Wait State.** Devices on the ISA Bus assert ZWS# to indicate that no wait states are required.

ISA Bus Interface (continued)			
Signal Name	**Pin #**	**I/O**	**Signal Description**
RFSH#	W7	IO	**Refresh.** As an output RFSH# indicates when a refresh cycle is in progress. As an input RFSH# is driven by 16-bit ISA Bus masters to indicate refresh cycle.
AEN	Y4	O	**Address Enable.** AEN is asserted during DMA cycles to prevent I/O slaves from misinterpreting DMA cycles as valid I/O cycles.
IRQ0OUT / GPO14	H20	O	**Multifunction Pin** Rx74[7] = 1 **Interrupt Request 0 Output.** Reflects the state of the internal system timer IRQ0 signal. Rx74[7] = 0 **General Purpose Output 14**.
IRQ1	J20	I	**Interrupt Request 1.**
IRQ3	T9	I	**Interrupt Request 3.**
IRQ4	W9	I	**Interrupt Request 4.**
IRQ5	U8	I	**Interrupt Request 5.**
IRQ6	V8	I	**Interrupt Request 6.**
IRQ7	Y8	I	**Interrupt Request 7.**
IRQ8# / GPI6	Y20	I	**Multifunction Pin** Rx5A[2] = 0 Internal RTC disabled. **Interrupt Request 8** from external RTC Rx5A[2] = 1 Internal RTC enabled. **General Purpose Input 6**.
IRQ9	U1	I	**Interrupt Request 9.**
IRQ10	U12	I	**Interrupt Request 10.**
IRQ11	W13	I	**Interrupt Request 11.**
IRQ12	T13	I	**Interrupt Request 12.**
IRQ14	V14	I	**Interrupt Request 14.**
IRQ15	Y14	I	**Interrupt Request 15.**
DRQ7-5, 3-0	U17, U16, Y16, U5, V2, U6, W15	I	**DMA Request.** Used to request DMA services from the internal DMA controller.
DACK7-5, 3-0#	W17, V16, T15, V5, Y10, W6, U14	O	**Acknowledge.** Used by the internal DMA controller to indicate that a request for DMA service has been granted.
TC	V10	O	**Terminal Count.** Asserted to DMA slaves as a terminal count indicator.
SPKR	K17	O	**Speaker Drive.** The output of internal timer/counter 2.

XD Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
XDIR# / GPO22	M3	O	**MultiFunction Pin** **X-Bus Data Direction.** (Rx75[6]=0) Asserted low for all I/O read cycles and for memory read cycles to the programmed BIOS or APIC address space. XDIR# is tied directly to the direction control of a 74F245 transceiver that buffers the X-Bus data and ISA-Bus data. SD0-7 connect to the "A" side of the transceiver and XD0-7 connect to the "B" side. XDIR# high indicates that SD0-7 drives XD0-7. **General Purpose Output 22.** (Rx75[6]=1) General purpose output.
XOE# / GPO23	M4	O	**MultiFunction Pin** **X-Bus Output Enable.** (Rx75[6]=0) Asserted low for all decoded X-Bus cycles. XOE# is tied directly to the output enable of a 74F245 transceiver that buffers the X-Bus data and ISA-Bus data (see XDIR# above). **General Purpose Output 23.** (Rx75[6]=1) General purpose output.
KBCS# / GPO26	K1	O	**MultiFunction Pin** **External Keyboard Controller Chip Select.** (Rx76[2] = 0) Asserted during read or write accesses to I/O ports 60h and 64h. **General Purpose Output 26.** (Rx76[2]=1) General purpose output.
ROMCS#	K2	O	**ROM Chip Select.** Chip Select to the BIOS ROM.
MCCS#	N4	O	**Microcontroller Chip Select.** Asserted during read or write accesses to I/O ports 62h or 66h.
PCS[1-0]#	N5, L4	O	**Programmable Chip Selects.** Asserted during I/O cycles to programmable read or write ISA address ranges. Devices selected by these pins are assumed to be on the X-Bus (XDIR# and XOE# are enabled).

Internal Real Time Clock			
Signal Name	**Pin #**	**I/O**	**Signal Description**
RTCX1	N19	I	**RTC Crystal Input**: 32.768 KHz crystal or oscillator input.
RTCX2	R20	O	**RTC Crystal Output**: 32.768 KHz crystal output
RTCCS# / GPO24	M2	O	**MultiFunction Pin** **External RTC Chip Select.** (Rx76[0] = 0) Asserted for read or write accesses to RTC port 71h. Externally connected to a pair of OR gates (to logically AND the chip select with IOR# and IOW#) to generate the active-low RTC read and write commands. **General Purpose Output 24.** (Rx76[0] = 1) General purpose output.
RTCAS / GPO25	L1	O	**MultiFunction Pin** **External RTC Address Strobe.** (Rx76[1] = 0) Asserted for writes to RTC I/O Port 70h. **General Purpose Output 25.** (Rx76[1] = 1) General purpose output.

Internal Keyboard Controller			
Signal Name	**Pin #**	**I/O**	**Signal Description**
KEYLOCK / PIRQ1	J4	I	**Extended Function** (PIIX4 PIRQ1) Rx59[1]=1 **Key Lock.** Input to internal keyboard controller
KBCK / NC	N3	IO	**Extended Function** (PIIX4 No Connect) Rx5A[0]=1 (Internal keyboard controller enabled –strapped from XD0) **Keyboard Clock**
KBDT / NC	M5	IO	**Extended Function** (PIIX4 No Connect) Rx5A[0]=1 (Internal keyboard controller enabled –strapped from XD0) **Keyboard Data**
MSCK / A20GATE	P1	IO	**MultiFunction Pin** Rx5A[1]=0 (internal keyboard controller disabled – strapped from XD1) **Gate A20.** From optional external keyboard controller Rx5A[1]=1 (internal keyboard controller enabled –strapped from XD1) **Mouse Clock.** Mouse clock (extended function not available on PIIX4)
MSDT / KBCS# / GPO26	K1	IO	**MultiFunction Pin** Rx5A[1]=0 (Internal keyboard controller disabled –strapped from XD1) **Keyboard Controller Chip Select.** (Rx76[2]=0 external keyboard controller enabled) Chip select for external keyboard controller. **General Purpose Output 26** (Rx76[2]=1 external keyboard controller disabled) General purpose output Rx5A[1]=1 (Internal keyboard controller enabled –strapped from XD1) **Mouse Data.** Mouse data (extended function not available on PIIX4)

PC/PCI and Serial IRQ Control			
Signal Name	**Pin #**	**I/O**	**Signal Description**
REQ[A-C]# / GPI[2-4]	M1, N2, P3	I	**PC/PCI DMA Requests.** Used by PCI agent to request DMA services per the PC/PCI protocol. For GPI functions refer to Rx7D[2-0].
GNT[A-C]# / GPO[9-11]	N1, P2, P4	O	**PC/PCI DMA Grants.** Used to acknowledge DMA services per the PC/PCI protocol. For GPO functions refer to Rx7D[2-0].
SERIRQ / GPI7	J19	I	**Serial Interrupt Request.** Used with Distributed DMA. For GPI see Rx68[3].

A20 Control			
Signal Name	**Pin #**	**I/O**	**Signal Description**
A20GATE / MSCK	P1	I	**Gate A20:** Gate A20 output from optional external keyboard controller if used. Logically combined with Port 92 bit-1 (Fast_A20) and output on the A20M# signal. If the internal keyboard / PS2 mouse controller is used, this pin becomes the mouse clock input (the A20GATE signal comes directly from the internal keyboard controller).
A20M#	M20	OD	**A20 Mask.** Connect to A20 mask input of the CPU.

APIC Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
APICREQ# / WSC# / GPI5	K18	I / I / I	**MultiFunction Pin** **Internal APIC Write Snoop Complete.** (Rx74[7]=1 & Rx74[1]=1) Asserted by the north bridge to indicate that all snoop activity on the CPU bus initiated by the last PCI-to-DRAM write is complete and that it is safe to perform an APIC interrupt. **External APIC Request.** (Rx74[7]=1 & Rx74[1]=0) Asserted by external APIC synchronous to PCICLK prior to sending an interrupt over the APIC serial bus. This signals the VT82C596B to flush its internal buffers. **General Purpose Input 5.** (Rx74[7] = 0)
APICCS# / APICD0 / GPO13	H18	O / O / O	**MultiFunction Pin** **Internal APIC Data 0.** (Rx74[7]=1 & Rx74[1]=1) **External APIC Chip Select.** (Rx74[7]=1 & Rx74[1]=0) The VT82C596B drives this signal active to select an external APIC (if used). This occurs if the external APIC is enabled and a PCI cycle is detected within the programmed APIC address range. **General Purpose Output 13.** (Rx74[7] = 0)
APICACK# / APICD1 / GPO12	J17	O / O / O	**MultiFunction Pin** **Internal APIC Data 1.** (Rx74[7]=1 & Rx74[1]=1) **External APIC Acknowledge.** (Rx74[7]=1 & Rx74[1]=0) Asserted by the VT82C596B to indicate that it internal buffers have been flushed (in response to APICREQ#). This indicates to the external APIC that the VT82C596B's internal buffers have been flushed and that it is OK for the APIC to send its interrupt. **General Purpose Output 12.** (Rx74[7] = 0)

General Purpose Inputs			
Signal Name	**Pin #**	**I/O**	**Signal Description**
GPI0 / IOCHCK#	Y1	I	**General Purpose Input 0.** (Rx74[0] = 0)
GPI1 / PME#	P19	I	**General Purpose Input 1.**
GPI2 / REQA#	M1	I	**General Purpose Input 2.** (Rx7D[0] = 0)
GPI3 / REQB#	N2	I	**General Purpose Input 3.** (Rx7D[1] = 0)
GPI4 / REQC#	P3	I	**General Purpose Input 4.** (Rx7D[2] = 0)
GPI5 / APICREQ#	K18	I	**General Purpose Input 5.** (Rx74[7] = 0)
GPI6 / IRQ8#	Y20	I	**General Purpose Input 6.** (Rx5A[2] = 1)
GPI7 / SERIRQ	J19	I	**General Purpose Input 7.** (Rx68[3] = 0)
GPI8 / THRM#	H19	I	**General Purpose Input 8.** (Rx74[2] = 1)
GPI9 / BATLOW#	U19	I	**General Purpose Input 9.** (Rx74[3] = 1)
GPI10 / LID	P16	I	**General Purpose Input 10.** (Rx74[4] = 1)
GPI11 / SMBALRT#	N17	I	**General Purpose Input 11.** (Rx74[5] = 1)
GPI12 / RI#	P18	I	**General Purpose Input 12.** (Rx74[6] = 1)
GPI13 / SLPBTN#	L2	I	**General Purpose Input 13.** Also functions as the ACPI sleep button if bit-9 of register 0 of ACPI I/O Space (Function 3) is enabled
GPI14	J3	I	**General Purpose Input 14.**
GPI15	L5	I	**General Purpose Input 15.**
GPI16	K3	I	**General Purpose Input 16.**
GPI17	K4	I	**General Purpose Input 17.**
GPI18	H1	I	**General Purpose Input 18.**
GPI19	H4	I	**General Purpose Input 19.**
GPI20 / PIRQ0	H5	I	**General Purpose Input 20.** (Rx59[0] = 1) See also Rx55[3:0]
GPI21 / PIRQ2	G3	I	**General Purpose Input 21.** (Rx59[2] = 1) See also Rx58[3:0]

The underlined name above indicates the default function on power up.

General Purpose Outputs			
Signal Name	**Pin #**	**I/O**	**Signal Description**
GPO0	G4	O	**General Purpose Output 0.**
GPO1 / LA17	Y15	**IO**	**General Purpose Output 1.** Rx74[0] = 0.
GPO2 / LA18	T14	**IO**	**General Purpose Output 2.** Rx74[0] = 0.
GPO3 / LA19	W14	**IO**	**General Purpose Output 3.** Rx74[0] = 0.
GPO4 / LA20	U13	**IO**	**General Purpose Output 4.** Rx74[0] = 0.
GPO5 / LA21	V13	**IO**	**General Purpose Output 5.** Rx74[0] = 0.
GPO6 / LA22	Y13	**IO**	**General Purpose Output 6.** Rx74[0] = 0.
GPO7 / LA23	T12	**IO**	**General Purpose Output 7.** Rx74[0] = 0.
GPO8	T19	O	**General Purpose Output 8.** F3Rx54[1-0]. Optional 1Hz / 2Hz / 4Hz clock output
GPO9 / GNTA#	N1	O	**General Purpose Output 9.** Rx7D[0] = 0.
GPO10 / GNTB#	P2	O	**General Purpose Output 10.** Rx7D[1] = 0.
GPO11 / GNTC#	P4	O	**General Purpose Output 11.** Rx7D[2] = 0.
GPO12 / APICACK#	J17	O	**General Purpose Output 12.** Rx74[7] = 0.
GPO13 / APICCS#	H18	O	**General Purpose Output 13.** Rx74[7] = 0.
GPO14 / IRQ0OUT	H20	O	**General Purpose Output 14.** Rx74[7] = 0.
GPO15 / SUSB#	V19	O	**General Purpose Output 15.** Rx75[0] = 1. See also F3Rx54[3].
GPO16 / SUSC#	U18	O	**General Purpose Output 16.** Rx75[0] = 1. See also F3Rx54[2].
GPO17 / CPUSTP#	R1	O	**General Purpose Output 17.** Rx75[1] = 1.
GPO18 / PCISTP#	R2	O	**General Purpose Output 18.** Rx75[2] = 1.
GPO19 / ZZ	K16	O	**General Purpose Output 19.** Rx75[3] = 1.
GPO20 / SUSST1#	T17	O	**General Purpose Output 20.** Rx75[4] = 1. See also F3Rx54[4].
GPO21 / SUSST2#	T18	O	**General Purpose Output 21.** Rx75[5] = 1. See also F3Rx54[7].
GPO22 / XDIR#	M3	O	**General Purpose Output 22.** Rx75[6] = 1.
GPO23 / XOE#	M4	O	**General Purpose Output 23.** Rx75[6] = 1.
GPO24 / RTCCS#	M2	O	**General Purpose Output 24.** Rx76[0] = 1.
GPO25 / RTCAS	L1	O	**General Purpose Output 25.** Rx76[1] = 1.
GPO26 / KBCS#	K1	O	**General Purpose Output 26.** Rx76[2] = 1.
GPO27	G5	O	**General Purpose Output 27.**
GPO28	F2	O	**General Purpose Output 28.**
GPO29 / SCIOUT#	F3	O	**General Purpose Output 29.** Rx74[7] = 0.
GPO30	F4	O	**General Purpose Output 30.**

The underlined name above indicates the default function on power up.

Power Management			
Signal Name	**Pin #**	**I/O**	**Signal Description**
PWRBTN#	U20	I	**Power Button.** Used by the Power Management subsystem to monitor an external system on/off button or switch. The VT82C596B performs a 200us debounce of this input if Rx40[5] is set to 1. This input is referenced to VCCSUS.
SLPBTN# / GPI13	L2	I	**ACPI Sleep Button.** General purpose input 13, but also functions as the ACPI sleep button if bit-9 of register 0 of ACPI I/O Space (Function 3) is enabled.
RCIN#	N20	I	**Reset CPU.** This signal from an optional external keyboard controller (if used) causes an INIT signal to be generated to the CPU.
RSMRST#	M17	I	**Resume Reset.** Resets the internal logic connected to the VCCSUS power plane and also resets portions of the internal RTC logic.
EXTSMI#	V20	IOD	**External System Management Interrupt.** When enabled to allow it, a falling edge on this input causes an SMI# to be generated to the CPU to enter SMI mode. Once asserted, this pin should be held low for at least four PCICLKs. The VT82C596B also asserts EXTSMI# in response to SMI# being activated within the Serial IRQ function. This pin should be connected to an external pullup.
PCIREQ[A-D]#	E10, A11, B11, C11	I	**Power Management PCI Requests.** Used by internal power management to monitor PCI requests for use of the PCI bus.

Power Management (continued)			
Signal Name	**Pin #**	**I/O**	**Signal Description**
LID / GPI10	P16	I	**Notebook Computer Display Lid Open / Closed Monitor.** Used by the Power Management subsystem to monitor the opening and closing of the display lid of notebook computers. Can be used to detect either low-to-high and/or high-to-low transitions to generate an SMI#. The VT82C596B performs a 200 usec debounce of this input if Rx40[5] is set to 1. May optionally be programmed as a general purpose input (Rx74[4]=1).
RI# / GPI12	P18	I	**Ring Indicator.** May be connected to external modem circuitry to allow the system to be re-activated by a received phone call. This input is referenced to VCCSUS. May optionally be programmed as a general purpose input (Rx74[6]=1).
THRM# / GPI8	H19	I	**Thermal Detect.** If the VT82C596B is enabled to allow it, asserting this signal initiates hardware Clock Throttling mode. This causes STPCLK# to be cycled at a preset programmable rate (see Function 3 configuration space Rx4C). May optionally be programmed as a general purpose input (Rx74[2]=1).
SCIOUT# / GPO29	F3	O	**ACPI System Control Interrupt.** Connected to the external APIC if used. May optionally be programmed as a general purpose output (Rx74[7]=0).
CPUSTP# / GPO17	R1	O	**CPU Clock Stop.** Signals the system clock generator to disable the CPU clock outputs. May optionally be programmed as a general purpose output (Rx75[1]=1).
PCISTP# / GPO18	R2	O	**PCI Clock Stop.** Signals the system clock generator to disable the PCI clock outputs. May optionally be programmed as a general purpose output (Rx75[2]=1).
ZZ / GPO19	K16	O	**L2 Cache SRAM Low Power Mode.** Used to power down the L2 Cache SRAMs during CPU Stop Clock state. May optionally be programmed as a general purpose output (Rx75[3]=1).
SUSA#	W20	O	**Suspend Plane A Control.** Asserted during power management POS, STR, and STD suspend states. Used to control the primary power plane.
SUSB# / GPO15	V19	O	**Suspend Plane B Control.** Asserted during power management STR and STD suspend states. Used to control the secondary power plane. May optionally be programmed as a general purpose output (Rx75[0]=1).
SUSC# / GPO16	U18	O	**Suspend Plane C Control.** Asserted during power management STD suspend state. Used to control the tertiary power plane. May optionally be programmed as a general purpose output (Rx75[0]=1).
SUSST1# / GPO20	T17	O	**Suspend Status 1.** Typically connected to the North Bridge (e.g., VT82C598 Apollo MVP3) to provide information on host clock status. Asserted when the system may stop the host clock, such as Stop Clock or during POS, STR, or STD suspend states. May optionally be programmed as a general purpose output (Rx75[4]=1).
SUSST2# / GPO21	T18	O	**Suspend Status 2.** Typically connected to other system devices to provide information on system suspend state. Asserted during POS, STR, or STD suspend states. May optionally be programmed as a general purpose output (Rx75[5]=1).

Resets and Clocks			
Signal Name	**Pin #**	**I/O**	**Signal Description**
PWRGD	M18	I	**Power Good.** Connected to the PWRGOOD signal on the Power Supply.
PCIRST#	A1	O	**PCI Reset.** Active low reset signal for the PCI bus. The VT82C596B will assert this pin during power-up or from the control register.
RSTDRV	W1	O	**Reset Drive.** Reset signal to the ISA bus.
BCLK	T7	O	**Bus Clock.** ISA bus clock.
OSC	V11	I	**Oscillator.** 14.31818 MHz clock signal used by the internal Timer.
SUSCLK	P17	O	**Suspend Clock.** 32.768 KHz output clock for use by the North Bridge (e.g., VT82C598 Apollo MVP3) for DRAM refresh purposes. Stopped during Suspend-to-Disk and Soft-Off modes.

Configuration and Test			
Signal Name	**Pin #**	**I/O**	**Signal Description**
CFG1	R17	I	**Configuration 1.** Used to select the CPU type (0=Socket-7, 1=Slot-1). Determines the polarity of the INIT and CPURST signals.
CFG2	R18	I	**Configuration 2.** Used to select the type of decoding for the top 64 Kbytes of memory (FFFF0000h-FFFFFFFFh): 0 = Positive decode, 1 = Subtractive decode.
TEST#	V18	I	**Test.** Used to select chip test modes. Pulled up externally to VCCSUS for normal operation.

Power and Ground			
Signal Name	**Pin #**	**I/O**	**Signal Description**
VCC	E9, E11, E12, E16, F5, F6, F14, F15, G6, P15, R6, R7, R15, T6	P	**Core Power.** 3.3V nominal (3.15V to 3.45V). This supply is turned on only when the mechanical switch on the power supply is turned on and the PWRON signal is conditioned high. This pin should be connected to the same voltage as the CPU I/O circuitry.
VREF	J16	P	**Voltage Reference.** 5V nominal (4.75 to 5.25) to provide 5V input tolerance. This voltage should be on only when the mechanical switch on the power supply is turned on and the PWRON signal is conditioned high.
VCCSUS	N16, R16	P	**Suspend Power.** Always available unless the mechanical switch of the power supply is turned off. If the "soft-off" state is not implemented, then this pin can be connected to VCC. Signals powered by or referenced to this plane are: BATLOW#, CFG1-2, EXTSMI#, GPI1, GPO8, IRQ8#, LID, RI#, SMBALRT#, SMBCLK, SMBDATA, PWRBTN#, SUS[A-C]#, SUSCLK, SUSST[1-2]#, TEST#, PWROK, RSMRST#.
VBAT	L16	P	**RTC Battery.** Battery input for internal RTC (RTCX1, RTCX2)
VCCUSB	K5	P	**USB Differential Output Power Source** (USBP0+, P0-, P1+, P1-)
GNDUSB	J5	P	**USB Differential Output Ground**
GND	D10, E7, E13, J9-12, K9-12, L9-12, M9-12	P	**Ground**
NC	J4, M5, M16, N3, N18, R5	-	**No Connect**

REGISTERS

Register Overview

The following tables summarize the configuration and I/O registers of the VT82C596B. These tables also document the power-on default value ("Default") and access type ("Acc") for each register. Access type definitions used are RW (Read/Write), RO (Read/Only), "—" for reserved / used (essentially the same as RO), and RWC (or just WC) (Read / Write 1's to Clear individual bits). Registers indicated as RW may have some read/only bits that always read back a fixed value (usually 0 if unused); registers designated as RWC or WC may have some read-only or read write bits (see individual register descriptions for details).

Detailed register descriptions are provided in the following section of this document. All offset and default values are shown in hexadecimal unless otherwise indicated

Table 2. System I/O Map

Port	Function	Actual Port Decoding
00-1F	Master DMA Controller	0000 0000 000x nnnn
20-3F	Master Interrupt Controller	0000 0000 001x xxxn
40-5F	Timer / Counter	0000 0000 010x xxnn
60-6F	Keyboard Controller	0000 0000 0110 xnxn
(60h)	KBC Data	0000 0000 0110 x0x0
(61h)	Misc Functions & Spkr Ctrl	0000 0000 0110 xxx1
(64h)	KBC Command / Status	0000 0000 0110 x1x0
70-77	RTC/CMOS/NMI-Disable	0000 0000 0111 0nnn
78-7F	-available for system use-	0000 0000 0111 1xxx
80	-reserved- (debug port)	0000 0000 1000 0000
81-8F	DMA Page Registers	0000 0000 1000 nnnn
90-91	-available for system use-	0000 0000 1001 000x
92	System Control	0000 0000 1001 0010
93-9F	-available for system use-	0000 0000 1001 nnnn
A0-BF	Slave Interrupt Controller	0000 0000 101x xxxn
C0-DF	Slave DMA Controller	0000 0000 110n nnnx
E0-FF	-available for system use-	0000 0000 111x xxxx
100-CF7	-available for system use-	
CF8-CFB	PCI Configuration Address	0000 1100 1111 10xx
CFC-CFF	PCI Configuration Data	0000 1100 1111 11xx
D00-FFFF	-available for system use-	

Table 3. Registers

Legacy I/O Registers

Port	Master DMA Controller Registers	Default	Acc
00	Channel 0 Base & Current Address		RW
01	Channel 0 Base & Current Count		RW
02	Channel 1 Base & Current Address		RW
03	Channel 1 Base & Current Count		RW
04	Channel 2 Base & Current Address		RW
05	Channel 2 Base & Current Count		RW
06	Channel 3 Base & Current Address		RW
07	Channel 3 Base & Current Count		RW
08	Status / Command		RW
09	Write Request		**WO**
0A	Write Single Mask		**WO**
0B	Write Mode		**WO**
0C	Clear Byte Pointer FF		**WO**
0D	Master Clear		**WO**
0E	Clear Mask		**WO**
0F	Read / Write Mask		RW

Port	Master Interrupt Controller Regs	Default	Acc
20	Master Interrupt Control	—	*
21	Master Interrupt Mask	—	*
20	Master Interrupt Control Shadow	—	**RW**
21	Master Interrupt Mask Shadow	—	**RW**

* RW if shadow registers are disabled

Port	Timer/Counter Registers	Default	Acc
40	Timer / Counter 0 Count		RW
41	Timer / Counter 1 Count		RW
42	Timer / Counter 2 Count		RW
43	Timer / Counter Control		**WO**

Port	Keyboard Controller Registers	Default	Acc
60	Keyboard Controller Data		RW
61	Misc Functions & Speaker Control		RW
64	Keyboard Ctrlr Command / Status		RW

Port	CMOS / RTC / NMI Registers	Default	Acc
70	CMOS Memory Address & NMI Disa		**WO**
71	CMOS Memory Data (128 bytes)		RW
72	CMOS Memory Address		RW
73	CMOS Memory Data (256 bytes)		RW
74	CMOS Memory Address		RW
75	CMOS Memory Data (256 bytes)		RW

NMI Disable is port 70h (CMOS Memory Address) bit-7.
RTC control occurs via specific CMOS data locations (0-0Dh).
Ports 72-73 may be used to access all 256 locations of CMOS.
Ports 74-75 may be used to access CMOS if the internal RTC is disabled.

Port	DMA Page Registers	Default	Acc
87	DMA Page - DMA Channel 0		RW
83	DMA Page - DMA Channel 1		RW
81	DMA Page - DMA Channel 2		RW
82	DMA Page - DMA Channel 3		RW
8F	DMA Page - DMA Channel 4		RW
8B	DMA Page - DMA Channel 5		RW
89	DMA Page - DMA Channel 6		RW
8A	DMA Page - DMA Channel 7		RW

Port	System Control Registers	Default	Acc
92	System Control		RW

Port	Slave Interrupt Controller Regs	Default	Acc
A0	Slave Interrupt Control	—	*
A1	Slave Interrupt Mask	—	*
A0	Slave Interrupt Control Shadow	—	**RW**
A1	Slave Interrupt Mask Shadow	—	**RW**

* RW accessible if shadow registers are disabled

Port	Slave DMA Controller Registers	Default	Acc
C0	Channel 0 Base & Current Address		RW
C2	Channel 0 Base & Current Count		RW
C4	Channel 1 Base & Current Address		RW
C6	Channel 1 Base & Current Count		RW
C8	Channel 2 Base & Current Address		RW
CA	Channel 2 Base & Current Count		RW
CC	Channel 3 Base & Current Address		RW
CE	Channel 3 Base & Current Count		RW
D0	Status / Command		RW
D2	Write Request		**WO**
D4	Write Single Mask		**WO**
D6	Write Mode		**WO**
D8	Clear Byte Pointer FF		**WO**
DA	Master Clear		**WO**
DC	Clear Mask		**WO**
DE	Read / Write Mask		RW

PCI Function 0 Registers - PCI-to-ISA Bridge

Configuration Space PCI-to-ISA Bridge Header Registers

Offset	PCI Configuration Space Header	Default	Acc
1-0	Vendor ID	1106	RO
3-2	Device ID	0596	RO
5-4	Command	0087	**RW**
7-6	Status	0200	**WC**
8	Revision ID	nn	RO
9	Programming Interface	00	RO
A	Sub Class Code	01	RO
B	Base Class Code	06	RO
C	-reserved- (cache line size)	00	—
D	-reserved- (latency timer)	00	—
E	Header Type	80	RO
F	Built In Self Test (BIST)	00	RO
10-27	-reserved- (base address registers)	00	—
28-2B	-reserved- (unassigned)	00	—
2F-2C	Subsystem ID Read	00	RO
30-33	-reserved- (expan. ROM base addr)	00	—
34-3B	-reserved- (unassigned)	00	—
3C	-reserved- (interrupt line)	00	—
3D	-reserved- (interrupt pin)	00	—
3E	-reserved- (min gnt)	00	—
3F	-reserved- (max lat)	00	—

Configuration Space PCI-to-ISA Bridge-Specific Registers

Offset	ISA Bus Control	Default	Acc
40	ISA Bus Control	00	RW
41	ISA Test Mode	00	RW
42	ISA Clock Control	00	RW
43	ROM Decode Control	00	RW
44	Keyboard Controller Control	00	RW
45	Type F DMA Control	00	RW
46	Miscellaneous Control 1	00	RW
47	Miscellaneous Control 2	00	RW
48	Miscellaneous Control 3	01	RW
49	-reserved-	00	—
4A	IDE Interrupt Routing	04	RW
4B	-reserved-	00	—
4C	DMA / Master Mem Access Control 1	00	RW
4D	DMA / Master Mem Access Control 2	00	RW
4F-4E	DMA / Master Mem Access Control 3	0300	RW

Configuration Space PCI-to-ISA Bridge-Specific Registers

Offset	Plug and Play Control	Default	Acc
50	-reserved- (do not program)	24	RW
51-53	-reserved-	00	—
54	PCI IRQ Edge / Level Selection	00	RW
55	PnP Routing for External MIRQ0-1	00	RW
56	PnP Routing for PCI INTB-A	00	RW
57	PnP Routing for PCI INTD-C	00	RW
58	PnP Routing for External MIRQ2	00	RW
59	PIRQ Pin Configuration	04	RW
5A	KBC / RTC Control	x4†	RW
5B	Internal RTC Test Mode	00	RW
5C	DMA Control	00	RW
5F-5D	-reserved-	00	—

† Bit 7-4 power-up default value depends on external strapping

Offset	Distributed DMA	Default	Acc
61-60	Channel 0 Base Address / Enable	0000	RW
63-62	Channel 1 Base Address / Enable	0000	RW
65-64	Channel 2 Base Address / Enable	0000	RW
67-66	Channel 3 Base Address / Enable	0000	RW
69-68	Serial IRQ Control	0000	RW
6B-6A	Channel 5 Base Address / Enable	0000	RW
6D-6C	Channel 6 Base Address / Enable	0000	RW
6F-6E	Channel 7 Base Address / Enable	0000	RW

Offset	Miscellaneous	Default	Acc
70	Subsystem ID Write	00	WO
71-73	-reserved-	00	—
77-74	GPIO / Chip Select Control	0000 0000	RW
7B-78	Programmable Chip Select Control	0000 0000	RW
7F-7C	PC/PCI Control	0000 0000	RW
80	Programmable Chip Select Mask	00	RW
81	ISA Positive Decoding Control 1	00	RW
82	ISA Positive Decoding Control 2	00	RW
83	ISA Positive Decoding Control 3	00	RW
84	ISA Positive Decoding Control 4	00	RW
85-86	-reserved-	00	—
87	Test 1	00	RW
88	Test 2	00	RW
89	PLL Control	00	RW
8A-FF	-reserved-	00	—

PCI Function 1 Registers – IDE Controller

Configuration Space IDE Header Registers

Offset	PCI Configuration Space Header	Default	Acc
1-0	Vendor ID	1106	RO
3-2	Device ID	0571	RO
5-4	Command	0080	RO
7-6	Status	0280	**RW**
8	Revision ID	nn	RO
9	Programming Interface	85	**RW**
A	Sub Class Code	01	RO
B	Base Class Code	01	RO
C	-reserved- (cache line size)	00	—
D	Latency Timer	00	RW
E	Header Type	00	RO
F	Built In Self Test (BIST)	00	RO
13-10	Base Address – Pri Data / Command	000001F0	RO
17-14	Base Address – Pri Control / Status	000003F4	RO
1B-18	Base Address – Sec Data / Command	00000170	RO
1F-1C	Base Address – Sec Control / Status	00000374	RO
23-20	Base Address – Bus Master Control	0000CC01	**RW**
24-2F	-reserved- (unassigned)	00	—
30-33	-reserved- (expan ROM base addr)	00	—
34-3B	-reserved- (unassigned)	00	—
3C	Interrupt Line	0E	RW
3D	Interrupt Pin	00	RO
3E	Minimum Grant	00	RO
3F	Maximum Latency	00	RO

Configuration Space IDE-Specific Registers

Offset	Configuration Space IDE Registers	Default	Acc
40	Chip Enable	08	RW
41	IDE Configuration	02	RW
42	-reserved- (do not program)	09	**RW**
43	FIFO Configuration	3A	RW
44	Miscellaneous Control 1	68	RW
45	Miscellaneous Control 2	00	RW
46	Miscellaneous Control 3	C0	RW
4B-48	Drive Timing Control	A8A8A8A8	RW
4C	Address Setup Time	FF	RW
4D	-reserved- (do not program)	00	**RW**
4E	Sec Non-1F0 Port Access Timing	FF	RW
4F	Pri Non-1F0 Port Access Timing	FF	RW
53-50	UltraDMA33 Extd Timing Control	03030303	RW
54	UltraDMA FIFO Control	06	RW
55-5F	-reserved-	00	—
61-60	IDE Primary Sector Size	0200	RW
62-67	-reserved-	00	—
69-68	IDE Secondary Sector Size	0200	RW
69-6F	-reserved-	00	—
70	IDE Primary Status	00	RW
71	IDE Primary Interrupt Control	00	RW
72-73	-reserved-	00	—
74	IDE Primary Command 1	00	RW
75	IDE Primary Command 2	00	RW
76-77	-reserved-	00	—
78	IDE Secondary Status	00	RW
79	IDE Secondary Interrupt Control	00	RW
7A-7B	-reserved-	00	—
7C	IDE Secondary Command 1	00	RW
7D	IDE Secondary Command 2	00	RW
7E-7F	-reserved-	00	—
83-80	IDE Primary S/G Descriptor Address	0000 0000	RW
84-87	-reserved-	00	—
8B-88	IDE Secondary S/G Descriptor Addr	0000 0000	RW
8C-FF	-reserved-	00	—

I/O Registers – IDE Controller (SFF 8038 v1.0 Compliant

Offset	IDE I/O Registers	Default	Acc
0	Primary Channel Command	00	RW
1	-reserved-	00	—
2	Primary Channel Status	00	WC
3	-reserved-	00	—
4-7	Primary Channel PRD Table Addr	00	RW
8	Secondary Channel Command	00	RW
9	-reserved-	00	—
A	Secondary Channel Status	00	WC
B	-reserved-	00	—
C-F	Secondary Channel PRD Table Addr	00	RW

PCI Function 2 Registers – USB Controller

Configuration Space USB Header Registers

Offset	PCI Configuration Space Header	Default	Acc
1-0	Vendor ID	1106	RO
3-2	Device ID	3038	RO
5-4	Command	0000	**RW**
7-6	Status	0200	**WC**
8	Revision ID	nn	RO
9	Programming Interface	00	RO
A	Sub Class Code	03	RO
B	Base Class Code	0C	RO
C	Cache Line Size	00	RO
D	Latency Timer	16	**RW**
E	Header Type	00	RO
F	BIST	00	RO
10-1F	-reserved-	00	—
23-20	Base Address	00000301	**RW**
24-3B	-reserved-	00	—
3C	Interrupt Line	00	**RW**
3D	Interrupt Pin	04	**RO**
3E-3F	-reserved-	00	—

Configuration Space USB-Specific Registers

Offset	USB Control	Default	Acc
40	Miscellaneous Control 1	00	**RW**
41	Miscellaneous Control 2	00	**RW**
42-43	-reserved-	00	RO
44-45	-reserved- (test only, do not program)		**RW**
46-47	-reserved- (test)		RO
48-5F	-reserved-	00	—
60	Serial Bus Release Number	10	RO
61-BF	-reserved-	00	—
C1-C0	Legacy Support	2000	**RW**
C2-FF	-reserved-	00	—

I/O Registers – USB Controller

Offset	USB I/O Registers	Default	Acc
1-0	USB Command	0000	RW
3-2	USB Status	0000	**WC**
5-4	USB Interrupt Enable	0000	RW
7-6	Frame Number	0000	RW
B-8	Frame List Base Address	00000000	RW
C	Start Of Frame Modify	40	RW
11-10	Port 1 Status / Control	0080	**WC**
13-12	Port 2 Status / Control	0080	**WC**

PCI Function 3 Registers – Power Management

Configuration Space Power Management Header Registers

Offset	PCI Configuration Space Header	Default	Acc
1-0	Vendor ID	1106	RO
3-2	Device ID	3050	RO
5-4	Command	0000	RO
7-6	Status	0280	**WC**
8	Revision ID	nn	RO
9	Programming Interface	00†	RO
A	Sub Class Code	00†	RO
B	Base Class Code	00†	RO
C	Cache Line Size	00	RO
D	Latency Timer	00	RO
E	Header Type	00	RO
F	BIST	00	RO
10-3F	-reserved-	00	—

† Default values may be changed by writing to offsets 61-63h.

Configuration Space Power Management-Specific Registers

Offset	Power Management	Default	Acc
40	Debounce Control	00	RW
41	General Configuration	00	RW
42	SCI Interrupt Configuration	00	RW
43	-reserved-	00	—
45-44	Primary Interrupt Channel	0000	RW
47-46	Secondary Interrupt Channel	0000	RW
4B-48	Power Mgmt I/O Base (256 Bytes)	0000 0001	RW
4C	Host Bus Power Management Control	00	RW
4D	Clock Stop Control	00	RW
4E-4F	-reserved-	00	—
53-50	GP0/1 Timer Control	0000 0000	RW
54	GPIO Select	00	RW
55	Wakeup Control	00	RW
56-57	-reserved-	00	—
5B-58	GP2/3 Timer Control	0000 0000	RW
5C-60	-reserved-	00	—
61	Write value for Offset 9 (Prog Intfc)	00	**WO**
62	Write value for Offset A (Sub Class)	00	**WO**
63	Write value for Offset B (Base Class)	00	**WO**
64-8F	-reserved-	00	—
Offset	**System Management Bus**	**Default**	**Acc**
93-90	SMBus I/O Base	0000 0001	RW
94-D1	-reserved-	00	—
D2	SMBus Control	00	RW
D3	SMBus Host Slave Command	00	RW
D4	SMBus Slave Address for Port 1	00	RW
D5	SMBus Slave Address for Port 2	00	RW
D6	SMBus Revision ID	nn	**RO**
D7-FF	-reserved-	00	—

I/O Space System Management Bus Registers

Offset	System Management Bus	Default	Acc
0	SMBus Host Status	00	**WC**
1	SMBus Slave Status	00	RW
2	SMBus Host Control	00	RW
3	SMBus Host Command	00	RW
4	SMBus Host Address	00	RW
5	SMBus Host Data 0	00	RW
6	SMBus Host Data 1	00	RW
7	SMBus Block Data	00	RW
8	SMBus Slave Control	00	RW
9	SMBus Shadow Command	00	**RO**
A-B	SMBus Slave Event	0000	RW
C-D	SMBus Slave Data	0000	**RO**
E-F	-reserved-	00	—

I/O Space Power Management- Registers

Offset	Basic Control / Status Registers	Default	Acc
1-0	Power Management Status	0000	**WC**
3-2	Power Management Enable	0000	RW
5-4	Power Management Control	0000	RW
6-7	-reserved-	00	—
B-8	Power Management Timer	0000 0000	RW
C-F	-reserved-	00	—
Offset	**Processor Registers**	**Default**	**Acc**
13-10	Processor and PCI Bus Control	0000 0000	RW
14	Processor LVL2	00	**RO**
15	Processor LVL3	00	**RO**
16-1F	-reserved-	00	—
Offset	**General Purpose Registers**	**Default**	**Acc**
21-20	General Purpose Status	0000	**WC**
23-22	General Purpose SCI Enable	0000	RW
25-24	General Purpose SMI Enable	0000	RW
26-27	-reserved-	00	—
Offset	**Generic Registers**	**Default**	**Acc**
29-28	Global Status	0000	**WC**
2B-2A	Global Enable	0000	RW
2D-2C	Global Control	0010	RW
2E	-reserved-	00	—
2F	SMI Command	00	RW
33-30	Primary Activity Detect Status	0000 0000	**WC**
37-34	Primary Activity Detect Enable	0000 0000	RW
3B-38	GP Timer Reload Enable	0000 0000	RW
3C-3F	-reserved-	00	—
Offset	**General Purpose I/O Registers**	**Default**	**Acc**
40	General Purpose Control	00	RW
41-43	-reserved-	00	—
45-44	External SMI Input Value	input	**RO**
46-47	-reserved-	00	—
4B-48	GPI Port Input Value	input	**RO**
4F-4C	GPO Port Output Value	7FFFFFFF	RW
50-FF	-reserved-	00	—

Configuration Space I/O

Mechanism #1

These ports respond only to double-word accesses. Byte or word accesses will be passed on unchanged.

Port CFB-CF8 - Configuration Address .....RW

31 Configuration Space Enable
- 0 Disabled .....default
- 1 Convert configuration data port writes to configuration cycles on the PCI bus

30-24 Reserved ..... always reads 0

23-16 PCI Bus Number
Used to choose a specific PCI bus in the system

15-11 Device Number
Used to choose a specific device in the system

10-8 Function Number
Used to choose a specific function if the selected device supports multiple functions

7-2 Register Number
Used to select a specific DWORD in the device's configuration space

1-0 Fixed ..... always reads 0

Port CFF-CFC - Configuration Data .....RW

Refer to PCI Bus Specification Version 2.1 for further details on operation of the above configuration registers.

Register Descriptions

Legacy I/O Ports

This group of registers includes the DMA Controllers, Interrupt Controllers, and Timer/Counters as well as a number of miscellaneous ports originally implemented using discrete logic on original PC/AT motherboards. All of the registers listed are integrated on-chip. These registers are implemented in a precise manner for backwards compatibility with previous generations of PC hardware. These registers are listed for information purposes only. Detailed descriptions of the actions and programming of these registers are included in numerous industry publications (duplication of that information here is beyond the scope of this document). All of these registers reside in I/O space.

Port 61 - Misc Functions & Speaker Control .....RW

7 Reserved ..... always reads 0

6 IOCHCK# Active ..... RO

This bit is set when the ISA bus IOCHCK# signal is asserted. Once set, this bit may be cleared by setting bit-3 of this register. Bit-3 should be cleared to enable recording of the next IOCHCK#. IOCHCK# generates NMI to the CPU if NMI is enabled.

5 Timer/Counter 2 Output ..... RO

This bit reflects the output of Timer/Counter 2 without any synchronization.

4 Refresh Detected ..... RO

This bit toggles on every rising edge of the ISA bus REFRESH# signal.

3 IOCHCK# Disable ..... RW

0 Enable IOCHCK# assertions.....default

1 Force IOCHCK# inactive and clear any "IOCHCK# Active" condition in bit-6

2 Reserved ..... RW, default=0

1 Speaker Enable..... RW

0 Disable .....default

1 Enable Timer/Ctr 2 output to drive SPKR pin

0 Timer/Counter 2 Enable..... RW

0 Disable .....default

1 Enable Timer/Counter 2

Port 92h - System Control..... RW

7-6 Hard Disk Activity LED Status

0 Off ..... default

1-3 On

5-4 Reserved ..... always reads 0

3 Power-On Password Bytes Inaccessable .. default=0

2 Reserved ..... always reads 0

1 A20 Address Line Enable

0 A20 disabled / forced 0 (real mode) ..... default

1 A20 address line enabled

0 High Speed Reset

0 Normal

1 Briefly pulse system reset to switch from protected mode to real mode

Keyboard Controller Registers

The keyboard controller handles the keyboard and mouse interfaces. Two ports are used: port 60 and port 64. Reads from port 64 return a status byte. Writes to port 64h are command codes (see command code list following the register descriptions). Input and output data is transferred via port 60.

A "Control" register is also available. It is accessable by writing commands 20h / 60h to the command port (port 64h); The control byte is written by first sending 60h to the command port, then sending the control byte value. The control register may be read by sending a command of 20h to port 64h, waiting for "Output Buffer Full" status = 1, then reading the control byte value from port 60h.

Traditional (non-integrated) keyboard controllers have an "Input Port" and an "Output Port" with specific pins dedicated to certain functions and other pins available for general purpose I/O. Specific commands are provided to set these pins high and low. All outputs are "open-collector" so to allow input on one of these pins, the output value for that pin would be set high (non-driving) and the desired input value read on the input port. These ports are defined as follows:

Bit	Input Port	Lo Code	Hi Code
0	P10 - Keyboard Data In	B0	B8
1	P11 - Mouse Data In	B1	B9
2	P12 - Turbo Pin (PS/2 mode only)	B2	BA
3	P13 - user-defined	B3	BB
4	P14 - user-defined	B6	BE
5	P15 - user-defined	B7	BF
6	P16 - user-defined	–	–
7	P17 - undefined	–	–

Bit	Output Port	Lo Code	Hi Code
0	P20 - SYSRST (1=execute reset)	–	–
1	P21 - GATEA20 (1=A20 enabled)	–	–
2	P22 - Mouse Data Out	B4	BC
3	P23 - Mouse Clock Out	B5	BD
4	P24 - Keyboard OBF Interrupt (IRQ1)	–	–
5	P25 - Mouse OBF Interrupt (IRQ 12)	–	–
6	P26 - Keyboard Clock Out	–	–
7	P27 - Keyboard Data Out	–	–

Bit	Test Port	Lo Code	Hi Code
0	T0 - Keyboard Clock In	–	–
1	T1 - Mouse Clock In	–	–

Note: Command code C0h transfers input port data to the output buffer. Command code D0h copies output port values to the output buffer. Command code E0h transfers test input port data to the output buffer.

Port 60 - Keyboard Controller Input Buffer ..... WO

Only write to port 60h if port 64h bit-1 = 0 (1=full).

Port 60 - Keyboard Controller Output Buffer .....RO

Only read from port 60h if port 64h bit-0 = 1 (0=empty).

Port 64 - Keyboard / Mouse Status ..... RO

0 Keyboard Output Buffer Full
- 0 Keyboard Output Buffer Empty..... default
- 1 Keyboard Output Buffer Full

1 Input Buffer Full
- 0 Input Buffer Empty..... default
- 1 Input Buffer Full

2 System Flag
- 0 Power-On Default..... default
- 1 Self Test Successful

3 Command / Data
- 0 Last write was data write ..... default
- 1 Last write was command write

4 Keylock Status
- 0 Locked
- 1 Free

5 Mouse Output Buffer Full
- 0 Mouse output buffer empty..... default
- 1 Mouse output buffer holds mouse data

6 General Receive / Transmit Timeout
- 0 No error ..... default
- 1 Error

7 Parity Error
- 0 No parity error (odd parity received)..... default
- 1 Even parity occurred on last byte received from keyboard / mouse

KBC Control Register .....(R/W via Commands 20h/60h)

7 Reserved .....always reads 0

6 PC Compatibility
- 0 Disable scan conversion
- 1 Convert scan codes to PC format; convert 2-byte break sequences to 1-byte PC-compatible break codes ..... default

5 Mouse Disable
- 0 Enable Mouse Interface ..... default
- 1 Disable Mouse Interface

4 Keyboard Disable
- 0 Enable Keyboard Interface ..... default
- 1 Disable Keyboard Interface

3 Keyboard Lock Disable
- 0 Enable Keyboard Inhibit Function..... default
- 1 Disable Keyboard Inhibit Function

2 System Flag .....default=0

This bit may be read back as status register bit-2

1 Mouse Interrupt Enable
- 0 Disable mouse interrupts ..... default
- 1 Generate interrupt on IRQ12 when mouse data comes in output bufer

0 Keyboard Interrupt Enable
- 0 Disable Keyboard Interrupts..... default
- 1 Generate interrupt on IRQ1 when output buffer has been written.

Port 64 - Keyboard / Mouse Command..... WO

This port is used to send commands to the keyboard / mouse controller. The command codes recognized by the VT82C596B are listed n the table below.

Note: The VT82C596B Keyboard Controller is compatible with the VIA VT82C42 Industry-Standard Keyboard Controller except that due to its integrated nature, many of the input and output port pins are not available externally for use as general purpose I/O pins (even though P13-P16 are set on power-up as strapping options). In other words, many of the commands below are provided and "work", but otherwise perform no useful function (e.g., commands that set P12-P17 high or low). Also note that setting P10-11, P22-23, P26-27, and T0-1 high or low directly serves no useful purpose, since these bits are used to implement the keyboard and mouse ports and are directly controlled by keyboard controller logic.

Table 4. Keyboard Controller Command Codes

Code	Keyboard Command Code Description
20h	Read Control Byte (next byte is Control Byte)
21-3Fh	Read SRAM Data (next byte is Data Byte)
60h	Write Control Byte (next byte is Control Byte)
61-7Fh	Write SRAM Data (next byte is Data Byte)
9xh	Write low nibble (bits 0-3) to P10-P13
A1h	Output Keyboard Controller Version #
A4h	Test if Password is installed (always returns F1h to indicate not installed)
A7h	Disable Mouse Interface
A8h	Enable Mouse Interface
A9h	Mouse Interface Test (puts test results in port 60h) (value: 0=OK, 1=clk stuck low, 2=clk stuck high, 3=data stuck lo, 4=data stuck hi, FF=general error)
AAh	KBC self test (returns 55h if OK, FCh if not)
ABh	Keyboard Interface Test (see A9h Mouse Test)
ADh	Disable Keyboard Interface
AEh	Enable Keyboard Interface
AFh	Return Version #
B0h	Set P10 low
B1h	Set P11 low
B2h	Set P12 low
B3h	Set P13 low
B4h	Set P22 low
B5h	Set P23 low
B6h	Set P14 low
B7h	Set P15 low
B8h	Set P10 high
B9h	Set P11 high
BAh	Set P12 high
BBh	Set P13 high
BCh	Set P22 high
BDh	Set P23 high
BEh	Set P14 high
BFh	Set P15 high
C0h	Read input port (read P10-17 input data to the output buffer)
C1h	Poll input port low (read input data on P11-13 repeatably & put in bits 5-7 of status
C2h	Poll input port high (same except P15-17)
C8h	Unblock P22-23 (use before D1 to change active mode)
C9h	Reblock P22-23 (protection mechanism for D1)
CAh	Read mode (output KBC mode info to port 60 output buffer (bit-0=0 if ISA, 1 if PS/2)
D0h	Read Output Port (copy P10-17 output port values to port 60)
D1h	Write Output Port (data byte following is written to keyboard output port as if it came from keyboard)
D2h	Write Keyboard Output Buffer & clear status bit-5 (write following byte to keyboard)
D3h	Write Mouse Output Buffer & set status bit-5 (write following byte to mouse; put value in mouse input buffer so it appears to have come from the mouse)
D4h	Write Mouse (write following byte to mouse)
E0h	Read test inputs (T0-1 read to bits 0-1 of resp byte)
Exh	Set P23-P21 per command bits 3-1
Fxh	Pulse P23-P20 low for 6usec per command bits 3-0

All other codes not listed are undefined.

DMA Controller I/O Registers

Ports 00-0F - Master DMA Controller

Channels 0-3 of the Master DMA Controller control System DMA Channels 0-3. There are 16 Master DMA Controller registers:

I/O Address Bits 15-0	Register Name	
0000 0000 000x 0000	**Ch 0 Base / Current Address**	**RW**
0000 0000 000x 0001	**Ch 0 Base / Current Count**	**RW**
0000 0000 000x 0010	**Ch 1 Base / Current Address**	**RW**
0000 0000 000x 0011	**Ch 1 Base / Current Count**	**RW**
0000 0000 000x 0100	**Ch 2 Base / Current Address**	**RW**
0000 0000 000x 0101	**Ch 2 Base / Current Count**	**RW**
0000 0000 000x 0110	**Ch 3 Base / Current Address**	**RW**
0000 0000 000x 0111	**Ch 3 Base / Current Count**	**RW**
0000 0000 000x 1000	**Status / Command**	**RW**
0000 0000 000x 1001	**Write Request**	**WO**
0000 0000 000x 1010	**Write Single Mask**	**WO**
0000 0000 000x 1011	**Write Mode**	**WO**
0000 0000 000x 1100	**Clear Byte Pointer F/F**	**WO**
0000 0000 000x 1101	**Master Clear**	**WO**
0000 0000 000x 1110	**Clear Mask**	**WO**
0000 0000 000x 1111	**R/W All Mask Bits**	**RW**

Note that not all bits of the address are decoded.

The Master DMA Controller is compatible with the Intel 8237 DMA Controller chip. Detailed descriptions of 8237 DMA Controller operation can be obtained from the Intel Peripheral Components Data Book and numerous other industry publications.

Ports C0-DF - Slave DMA Controller

Channels 0-3 of the Slave DMA Controller control System DMA Channels 4-7. There are 16 Slave DMA Controller registers:

I/O Address Bits 15-0	Register Name	
0000 0000 1100 000x	**Ch 0 Base / Current Address**	**RW**
0000 0000 1100 001x	**Ch 0 Base / Current Count**	**RW**
0000 0000 1100 010x	**Ch 1 Base / Current Address**	**RW**
0000 0000 1100 011x	**Ch 1 Base / Current Count**	**RW**
0000 0000 1100 100x	**Ch 2 Base / Current Address**	**RW**
0000 0000 1100 101x	**Ch 2 Base / Current Count**	**RW**
0000 0000 1100 110x	**Ch 3 Base / Current Address**	**RW**
0000 0000 1100 111x	**Ch 3 Base / Current Count**	**RW**
0000 0000 1101 000x	**Status / Command**	**RW**
0000 0000 1101 001x	**Write Request**	**WO**
0000 0000 1101 010x	**Write Single Mask**	**WO**
0000 0000 1101 011x	**Write Mode**	**WO**
0000 0000 1101 100x	**Clear Byte Pointer F/F**	**WO**
0000 0000 1101 101x	**Master Clear**	**WO**
0000 0000 1101 110x	**Clear Mask**	**WO**
0000 0000 1101 111x	**Read/Write All Mask Bits**	**WO**

Note that not all bits of the address are decoded.

The Slave DMA Controller is compatible with the Intel 8237 DMA Controller chip. Detailed description of 8237 DMA controller operation can be obtained from the Intel Peripheral Components Data Book and numerous other industry publications.

Ports 80-8F - DMA Page Registers

There are eight DMA Page Registers, one for each DMA channel. These registers provide bits 16-23 of the 24-bit address for each DMA channel (bits 0-15 are stored in registers in the Master and Slave DMA Controllers). They are located at the following I/O Port addresses:

I/O Address Bits 15-0	Register Name
0000 0000 1000 0111	**Channel 0 DMA Page (M-0).....RW**
0000 0000 1000 0011	**Channel 1 DMA Page (M-1).....RW**
0000 0000 1000 0001	**Channel 2 DMA Page (M-2).....RW**
0000 0000 1000 0010	**Channel 3 DMA Page (M-3).....RW**
0000 0000 1000 1111	**Channel 4 DMA Page (S-0) .....RW**
0000 0000 1000 1011	**Channel 5 DMA Page (S-1) .....RW**
0000 0000 1000 1001	**Channel 6 DMA Page (S-2) .....RW**
0000 0000 1000 1010	**Channel 7 DMA Page (S-3) .....RW**

Interrupt Controller Registers

Ports 20-21 - Master Interrupt Controller

The Master Interrupt Controller controls system interrupt channels 0-7. Two registers control the Master Interrupt Controller. They are:

I/O Address Bits 15-0	Register Name	
0000 0000 001x xxx0	**Master Interrupt Control**	**RW**
0000 0000 001x xxx1	**Master Interrupt Mask**	**RW**

Note that not all bits of the address are decoded.

The Master Interrupt Controller is compatible with the Intel 8259 Interrupt Controller chip. Detailed descriptions of 8259 Interrupt Controller operation can be obtained from the Intel Peripheral Components Data Book and numerous other industry publications.

Ports A0-A1 - Slave Interrupt Controller

The Slave Interrupt Controller controls system interrupt channels 8-15. The slave system interrupt controller also occupies two register locations:

I/O Address Bits 15-0	Register Name	
0000 0000 101x xxx0	**Slave Interrupt Control**	**RW**
0000 0000 101x xxx1	**Slave Interrupt Mask**	**RW**

Note that not all address bits are decoded.

The Slave Interrupt Controller is compatible with the Intel 8259 Interrupt Controller chip. Detailed descriptions of 8259 Interrupt Controller operation can be obtained from the Intel Peripheral Components Data Book and numerous other industry publications.

Interrupt Controller Shadow Registers

The following shadow registers are enabled by setting bit 4 of Rx47 to 1 (offset 47h in the PCI-ISA Bridge function 0 register group). If the shadow registers are enabled, they are read back at the indicated I/O port instead of the standard interrupt controller registers (writes to the interrupt controller register ports are directed to the standard interrupt controller registers).

Port 20 - Master Interrupt Control Shadow ..... RO

7-5	**Reserved**	..... always reads 0
4	**OCW3 bit 5**	
3	**OCW2 bit 7**	
2	**ICW4 bit 4**	
1	**ICW4 bit 1**	
0	**ICW1 bit 3**	

Port 21 - Master Interrupt Mask Shadow ..... RO

7-5	**Reserved**	..... always reads 0
4-0	**T7-T3 of Interrupt Vector Address**	

Port A0 - Slave Interrupt Control Shadow ..... RO

7-5	**Reserved**	..... always reads 0
4	**OCW3 bit 5**	
3	**OCW2 bit 7**	
2	**ICW4 bit 4**	
1	**ICW4 bit 1**	
0	**ICW1 bit 3**	

Port A1 - Slave Interrupt Mask Shadow ..... RO

7-5	**Reserved**	..... always reads 0
4-0	**T7-T3 of Interrupt Vector Address**	

Timer / Counter Registers

Ports 40-43 - Timer / Counter Registers

There are 4 Timer / Counter registers:

I/O Address Bits 15-0	Register Name	
0000 0000 010x xx00	**Timer / Counter 0 Count**	**RW**
0000 0000 010x xx01	**Timer / Counter 1 Count**	**RW**
0000 0000 010x xx10	**Timer / Counter 2 Count**	**RW**
0000 0000 010x xx11	**Timer / Counter Cmd Mode**	**WO**

Note that not all bits of the address are decoded.

The Timer / Counters are compatible with the Intel 8254 Timer / Counter chip. Detailed descriptions of 8254 Timer / Counter operation can be obtained from the Intel Peripheral Components Data Book and numerous other industry publications.

CMOS / RTC Registers

Port 70 - CMOS Address..... WO

7 NMI Disable.....WO
- 0 Enable NMI Generation. NMI is asserted on encountering IOCHCK# on the ISA bus or SERR# on the PCI bus.
- 1 Disable NMI Generation .....default

6-0 CMOS Address (lower 128 bytes).....WO

Port 71 - CMOS Data.....RW

7-0 CMOS Data (128 bytes)

Note: Ports 70-71 may be accessed if Rx5A bit-2 is set to one to select the internal RTC. If Rx5A bit-2 is set to zero, accesses to ports 70-71 will be directed to an external RTC.

Port 72 - CMOS Address.....RW

7-0 CMOS Address (256 bytes)..... RW

Port 73 - CMOS Data.....RW

7-0 CMOS Data (256 bytes)

Note: Ports 72-73 may be accessed if Rx5A bit-2 is set to one to select the internal RTC. If Rx5A bit-2 is set to zero, accesses to ports 72-73 will be directed to an external RTC.

Port 74 - CMOS Address.....RW

7-0 CMOS Address (256 bytes)..... RW

Port 75 - CMOS Data.....RW

7-0 CMOS Data (256 bytes)

Note: Ports 74-75 may be accessed only if Function 0 Rx5B bit-1 is set to one to enable the internal RTC SRAM and if Rx48 bit-3 (Port 74/75 Access Enable) is set to one to enable port 74/75 access.

Note: Ports 70-71 are compatible with PC industry-standards and may be used to access the lower 128 bytes of the 256-byte on-chip CMOS RAM. Ports 72-73 may be used to access the full extended 256-byte space. Ports 74-75 may be used to access the full on-chip extended 256-byte space in cases where the on-chip RTC is disabled.

Note: The system Real Time Clock (RTC) is part of the "CMOS" block. The RTC control registers are located at specific offsets in the CMOS data area (0-0Dh and 7D-7Fh). Detailed descriptions of CMOS / RTC operation and programming can be obtained from the VIA VT82887 Data Book or numerous other industry publications. For reference, the definition of the RTC register locations and bits are summarized in the following table:

Offset	Description		Binary Range	BCD Range
00	**Seconds**		00-3Bh	00-59h
01	**Seconds Alarm**		00-3Bh	00-59h
02	**Minutes**		00-3Bh	00-59h
03	**Minutes Alarm**		00-3Bh	00-59h
04	**Hours**	am 12hr:	01-1Ch	01-12h
		pm 12hr:	81-8Ch	81-92h
		24hr:	00-17h	00-23h
05	**Hours Alarm**	am 12hr:	01-1Ch	01-12h
		pm 12hr:	81-8Ch	81-92h
		24hr:	00-17h	00-23h
06	**Day of the Week**	Sun=1:	01-07h	01-07h
07	**Day of the Month**		01-1Fh	01-31h
08	**Month**		01-0Ch	01-12h
09	**Year**		00-63h	00-99h

0A Register A

7	**UIP**	Update In Progress
6-4	**DV2-0**	Divide (010=ena osc & keep time)
3-0	**RS3-0**	Rate Select for Periodic Interrupt

0B Register B

7	**SET**	Inhibit Update Transfers
6	**PIE**	Periodic Interrupt Enable
5	**AIE**	Alarm Interrupt Enable
4	**UIE**	Update Ended Interrupt Enable
3	**SQWE**	No function (read/write bit)
2	**DM**	Data Mode (0=BCD, 1=binary)
1	**24/12**	Hours Byte Format (0=12, 1=24)
0	**DSE**	Daylight Savings Enable

0C Register C

7	**IRQF**	Interrupt Request Flag
6	**PF**	Periodic Interrupt Flag
5	**AF**	Alarm Interrupt Flag
4	**UF**	Update Ended Flag
3-0	**0**	Unused (always read 0)

0D Register D

7	**VRT**	Reads 1 if VBAT voltage is OK
6-0	**0**	Unused (always read 0)

0E-7C Software-Defined Storage Registers (111 Bytes)

Offset	Extended Functions	Binary Range	BCD Range
7D	**Date Alarm**	01-1Fh	01-31h
7E	**Month Alarm**	01-0Ch	01-12h
7F	**Century Field**	13-14h	19-20h

80-FF Software-Defined Storage Registers (128 Bytes)
(See also Function 0 Rx5B[3] and Rx77[2-1])

Table 5. CMOS Register Summary

Function 0 Registers - PCI to ISA Bridge

All registers are located in the function 0 PCI configuration space of the VT82C596B. These registers are accessed through PCI configuration mechanism #1 via I/O address CF8/CFC.

PCI Configuration Space Header

Offset 1-0 - Vendor ID = 1106h ..... RO

Offset 3-2 - Device ID = 0596h ..... RO

Offset 5-4 - Command ..... RW

- **15-8 Reserved** ..... always reads 0
- **7 Address / Data Stepping**
  - 0 Disable
  - 1 Enable .....default
- **6-4 Reserved** ..... always reads 0
- **3 Special Cycle Enable** .....Normally RW†, default = 0
- **2 Bus Master** ..... always reads 1
- **1 Memory Space**..... Normally RO†, reads as 1
- **0 I/O Space** ..... Normally RO†, reads as 1

† If the test bit at offset 46 bit-4 is set, access to the above indicated bits is reversed: bit-3 above becomes read only (reading back 1) and bits 0-1 above become read / write (with a default of 1).

Offset 7-6 - Status ..... RWC

- **15 Detected Parity Error**.....write one to clear
- **14 Signalled System Error**..... always reads 0
- **13 Signalled Master Abort** .....write one to clear
- **12 Received Target Abort** .....write one to clear
- **11 Signalled Target Abort**.....write one to clear
- **10-9 DEVSEL# Timing** ..... fixed at 01 (medium)
- **8 Data Parity Detected**..... always reads 0
- **7 Fast Back-to-Back Capable**..... always reads 0
- **6-0 Reserved** ..... always reads 0

Offset 8 - Revision ID = nn ..... RO

- **7-0 Revision ID (00h is first silicon)**

Offset 9 - Program Interface = 00h ..... RO

Offset A - Sub Class Code = 01h ..... RO

Offset B - Class Code = 06h ..... RO

Offset E - Header Type = 80h ..... RO

- **7-0 Header Type Code.....** 80h (Multifunction Device)

Offset F - BIST = 00h ..... RO

Offset 2F-2C - Subsystem ID ..... RO

Use offset 70-73 to change the value returned.

ISA Bus Control

Offset 40 - ISA Bus Control.....RW

7 ISA Command Delay
- 0 Normal .....default
- 1 Extra

6 Extended ISA Bus Ready
- 0 Disable .....default
- 1 Enable

5 ISA Slave Wait States
- 0 4 Wait States .....default
- 1 5 Wait States

4 Chipset I/O Wait States
- 0 2 Wait States .....default
- 1 4 Wait States

3 I/O Recovery Time
- 0 Disable .....default
- 1 Enable

2 Extend-ALE
- 0 Disable .....default
- 1 Enable

1 ROM Wait States
- 0 1 Wait State.....default
- 1 0 Wait States

0 ROM Write
- 0 Disable .....default
- 1 Enable

Offset 41 - ISA Test Mode .....RW

7 Bus Refresh Arbitration (do not program) default=0

6 XRDY Test Mode (do not program)..... default=0

5 Port 92 Fast Reset
- 0 Disable .....default
- 1 Enable

4 A20G Emulation (do not program)..... default=0

3 Double DMA Clock
- 0 Disable (DMA Clock = ½ ISA Clock) ...default
- 1 Enable (DMA Clock = ISA Clock)

2 SHOLD Lock During INTA (do not program) def=0

1 Refresh Request Test Mode (do not program) def=0

0 ISA Refresh
- 0 Disable .....default
- 1 Enable

Offset 42 - ISA Clock Control..... RW

7 Latch IO16#
- 0 Enable (recommended setting) ..... default
- 1 Disable

6 MS16# Output
- 0 Enable (recommended setting) ..... default
- 1 Disable

5 Master Request Test Mode (do not program)..def=0

4 Reserved (no defined function) .....default = 0

3 ISA CLOCK Select Enable
- 0 ISA Clock = PCICLK/4..... default
- 1 ISA Clock selected per bits 2-0

2-0 ISA Bus Clock Select (if bit-3 = 1)
- 000 PCICLK/3..... default
- 001 PCICLK/2
- 010 PCICLK/4
- 011 PCICLK/6
- 100 PCICLK/5
- 101 PCICLK/10
- 110 PCICLK/12
- 111 OSC

Note: Procedure for ISA CLOCK switching:
1) Set bit 3 to 0; 2) Change value of bit 2-0; 3) Set bit 3 to 1

Offset 43 - ROM Decode Control .....RW

Setting these bits enables the indicated address range to be included in the ROMCS# decode:

7 **FFFE0000h-FFFEFFFFh**..... default=0
6 **FFF80000h-FFFDFFFFh** ..... default=0

5 **FFF00000h-FFF7FFFFh (new)**..... default=0
4 **000E0000h-000EFFFFh (new)** ..... default=0

5 **000E8000h-000EFFFFh (old)**..... default=0
4 **000E0000h-000E7FFFh (old)** ..... default=0

3 **000D8000h-000DFFFFh** ..... default=0
2 **000D0000h-000D7FFFh** ..... default=0
1 **000C8000h-000CFFFFh** ..... default=0
0 **000C0000h-000C7FFFh**..... default=0

Offset 44 - Keyboard Controller Control.....RW

7 **KBC Timeout Test** (do not program) ..... default = 0
6-4 **Reserved** (do not program)..... default = 0
3 **Mouse Lock Enable**
0 Disabled .....default
1 Enabled
2-1 **Reserved** (do not program)..... default = 0
0 **Reserved** (no function)..... default = 0

Offset 45 - Type F DMA Control.....RW

7 **ISA Master / DMA to PCI Line Buffer**.... default=0
6 **DMA type F Timing on Channel 7** ..... default=0
5 **DMA type F Timing on Channel 6** ..... default=0
4 **DMA type F Timing on Channel 5** ..... default=0
3 **DMA type F Timing on Channel 3** ..... default=0
2 **DMA type F Timing on Channel 2** ..... default=0
1 **DMA type F Timing on Channel 1** ..... default=0
0 **DMA type F Timing on Channel 0** ..... default=0

Offset 46 - Miscellaneous Control 1 ..... RW

7 **PCI Master Write Wait States**
0 0 Wait States..... default
1 1 Wait State
6 **Gate INTRQ**
0 Disable..... default
1 Enable
5 **Flush Line Buffer for Int or DMA IOR Cycle**
0 Disable..... default
1 Enable
4 **Config Command Reg Rx04 Access (Test Only)**
0 Normal: Bits 0-1=RO, Bit 3=RW..... default
1 Test Mode: Bits 0-1=RW, Bit-3=RO
3 **Reserved** (do not program).....default = 0
2 **Reserved** (no function) .....default = 0
1 **PCI Burst Read Interruptability**
0 Allow burst reads to be interrupted..... default
1 Don't allow PCI burst reads to be interrupted
0 **Post Memory Write Enable**
0 Disable..... default
1 Enable
The Post Memory Write function is automatically enabled when Delay Transaction (see Rx47 bit-6 below) is enabled, independent of the state of this bit.

Offset 47 - Miscellaneous Control 2 ..... RW

7 **CPU Reset Source**
0 Use CPURST as CPU Reset..... default
1 Use INIT as CPU Reset
6 **PCI Delay Transaction Enable**
0 Disable..... default
1 Enable
The "Post Memory Write" function is automatically enabled when this bit is enabled, independent of the state of Rx46 bit-0 above.
5 **EISA 4D0/4D1 Port Enable**
0 Disable (ignore ports 4D0-1)..... default
1 Enable (ports 4D0-1 per EISA specification)
4 **Interrupt Controller Shadow Register Enable**
0 Disable..... default
1 Enable
3 **Reserved (always program to 0)**.....default = 0
Note: Always mask this bit. This bit may read back as either 0 or 1 but must always be programmed with 0.
2 **Write Delay Transaction Time-Out Timer Enable**
0 Disable..... default
1 Enable
1 **Read Delay Transaction Time-Out Timer Enable**
0 Disable..... default
1 Enable
0 **Software PCI Reset** .....write 1 to generate PCI reset

Offset 48 - Miscellaneous Control 3.....RW

7 Low Voltage CPU Interface
- 0 Disable .....default
- 1 Enable

6-4 Reserved (Do Not Program)..... always reads 0

3 Extra RTC Port 74/75 Enable
- 0 Disable .....default
- 1 Enable

2 Integrated USB Controller Disable
- 0 Enable.....default
- 1 Disable

1 Integrated IDE Controller Disable
- 0 Enable.....default
- 1 Disable

0 512K PCI Memory Decode
- 0 Use Rx4E[15-12] to select top of PCI memory
- 1 Use contents of Rx4E[15-12] plus 512K as top of PCI memory.....default

Offset 4A - IDE Interrupt Routing .....RW

7 Wait for PGNT Before Grant to ISA Master / DMA
- 0 Disable .....default
- 1 Enable **(must be set to 1)**

6 Bus Select for Access to I/O Devices Below 100h
- 0 Access ports 00-FFh via XD bus.....default
- 1 Access ports 00-FFh via SD bus (applies to external devices only; internal devices such as the mouse controller are not effected)

5-4 Reserved (do not program) ..... default = 0

3-2 IDE Second Channel IRQ Routing
- 00 IRQ14
- 01 IRQ15.....default
- 10 IRQ10
- 11 IRQ11

1-0 IDE Primary Channel IRQ Routing
- 00 IRQ14.....default
- 01 IRQ15
- 10 IRQ10
- 11 IRQ11

4C - ISA DMA/Master Memory Access Control 1 ..... RW

7-0 PCI Memory Hole Bottom Address
These bits correspond to HA[23:16] .....default=0

4D - ISA DMA/Master Memory Access Control 2 ..... RW

7-0 PCI Memory Hole Top Address (HA[23:16])
These bits correspond to HA[23:16] .....default=0

Note: Access to the memory defined in the PCI memory hole will not be forwarded to PCI. This function is disabled if the top address less than or equal to the bottom address.

4F-4E - ISA DMA/Master Memory Access Control 3... RW

15-12 Top of PCI Memory for ISA DMA/Master accesses
- 0000 1M ..... default
- 0001 2M
- ... ...
- 1111 16M

Note: All ISA DMA / Masters that access addresses higher than the top of PCI memory will not be directed to the PCI bus.

11 Forward E0000-EFFFF Accesses to PCI.....def=0
10 Forward A0000-BFFFF Accesses to PCI .....def=0
9 Forward 80000-9FFFF Accesses to PCI .....def=1
8 Forward 00000-7FFF Accesses to PCI .....def=1
7 Forward DC000-DFFFF Accesses to PCI .....def=0
6 Forward D8000-DBFFF Accesses to PCI .....def=0
5 Forward D4000-D7FFF Accesses to PCI .....def=0
4 Forward D0000-D3FFF Accesses to PCI .....def=0
3 Forward CC000-CFFFF Accesses to PCI .....def=0
2 Forward C8000-CBFFF Accesses to PCI .....def=0
1 Forward C4000-C7FFF Accesses to PCI .....def=0
0 Forward C0000-C3FFF Accesses to PCI .....def=0

Plug and Play Control

Offset 50 - Reserved (Do Not Program) .....RW

7-0 Reserved ..... default = 24h

Offset 54 - PCI IRQ Polarity.....RW

7-4 Reserved ..... always reads 0

3 PIRQA#
- 0 Non-invert (Level).....default
- 1 Invert (Edge)

2 PIRQB#
- 0 Non-invert (Level).....default
- 1 Invert (Edge)

1 PIRQC#
- 0 Non-invert (Level).....default
- 1 Invert (Edge)

0 PIRQD#
- 0 Non-invert (Level).....default
- 1 Invert (Edge)

Note: PIRQA-D# normally connect to PCI interrupt pins INTA-D# (see pin definitions for more information).

Offset 55 - PNP IRQ Routing 1.....RW

7-4 PIRQA# Routing (see PnP IRQ routing table)
3-0 PIRQ0 Routing (see PnP IRQ routing table)

Offset 56 - PNP IRQ Routing 2.....RW

7-4 PIRQC# Routing (see PnP IRQ routing table)
3-0 PIRQB# Routing (see PnP IRQ routing table)

Offset 57 - PNP IRQ Routing 3.....RW

7-4 PIRQD# Routing (see PnP IRQ routing table)
3-0 PIRQ1 Routing (see PnP IRQ routing table)

Offset 58 - PNP IRQ Routing 4 ..... RW

7-4 Reserved .....always reads 0
3-0 PIRQ2 Routing (see PnP IRQ routing table)

PnP IRQ Routing Table

0000 Disabled..... default
0001 IRQ1
0010 Reserved
0011 IRQ3
0100 IRQ4
0101 IRQ5
0110 IRQ6
0111 IRQ7
1000 Reserved
1001 IRQ9
1010 IRQ10
1011 IRQ11
1100 IRQ12
1101 Reserved
1110 IRQ14
1111 IRQ15

Offset 59 - PIRQ Pin Configuration (04h)..... RW

7-3 Reserved .....always reads 0

2 PIRQ2 / GPI21 Selection (Pin G3)
- 0 PIRQ2
- 1 GPI21 ..... default

1 PIRQ1 / KEYLOCK Selection (Pin J4)
- 0 PIRQ1..... default
- 1 KEYLOCK

0 PIRQ0 / GPI20 Selection (Pin H5)
- 0 PIRQ0..... default
- 1 GPI20

Offset 5A – KBC / RTC Control .....RW

Bits 7-4 of this register are latched from pins SD7-4 at power-up but are read/write accessible so may be changed after power-up to change the default strap setting:

- **7** **Keyboard RP16**..... latched from SD7
- **6** **Keyboard RP15** ..... latched from SD6
- **5** **Keyboard RP14** ..... latched from SD5
- **4** **Keyboard RP13** ..... latched from SD4
- **3** **Reserved** ..... always reads 0
- **2** **Internal RTC Enable**
  - 0 Disable
  - 1 Enable .....default
- **1** **Internal PS2 Mouse Enable**
  - 0 Disable .....default
  - 1 Enable
- **0** **Internal KBC Enable**
  - 0 Disable .....default
  - 1 Enable

Note: External strap option values may be set by connecting the indicated external pin to a 4.7K ohm pullup (for 1) or driving it low during reset with a 7407 TTL open collector buffer (for 0) as shown in the suggested circuit below:

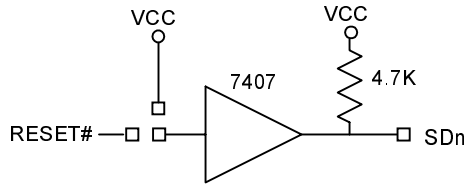


Figure 5. Strap Option Circuit

Offset 5B - Internal RTC Test Mode ..... RW

- **7-4** **Reserved** .....always reads 0
- **3** **RTC Map Rx32 to Rx7F Century Byte**
  - 0 Disable..... default
  - 1 Enable
- **2** **RTC Reset Enable** (do not program) .....default=0
- **1** **RTC SRAM Access Enable**
  - 0 Disable..... default
  - 1 Enable

  This bit is set if the internal RTC is disabled but it is desired to still be able to access the internal RTC SRAM via ports 74-75. If the internal RTC is enabled, setting this bit does nothing (the internal RTC SRAM should be accessed at either ports 70/71 or 72/73.
- **0** **RTC Test Mode Enable** (do not program) .default=0

Offset 5C - DMA Control..... RW

- **7** **Gate Port 61 Command Output**
  - 0 Disable..... default
  - 1 Enable
- **6** **Passive Release**
  - 0 Disable..... default
  - 1 Enable
- **5** **Internal Passive Release**
  - 0 Disable..... default
  - 1 Enable
- **4** **Dummy Request**
  - 0 Disable..... default
  - 1 Enable
- **3** **Extended DMA Command and TC**
  - 0 Disable..... default
  - 1 Enable
- **2** **External APIC Configuration**
  - 0 External APIC on XD Bus..... default
  - 1 External APIC on SD Bus (disable XOE# for APIC cycles)
- **1** **Reserved** .....always reads 0
- **0** **DMA Line Buffer Disable**
  - 0 DMA cycles can be to/from line buffer ..... def
  - 1 Disable DMA Line Buffer

Distributed DMA / Serial IRQ Control

Offset 61-60 - Distributed DMA Ch 0 Base / Enable.....RW

15-4 Channel 0 Base Address Bits 15-4 ..... default = 0

3 Channel 0 Enable
- 0 Disable .....default
- 1 Enable

2-0 Reserved ..... always reads 0

Offset 63-62 - Distributed DMA Ch 1 Base / Enable.....RW

15-4 Channel 1 Base Address Bits 15-4 ..... default = 0

3 Channel 1 Enable
- 0 Disable .....default
- 1 Enable

2-0 Reserved ..... always reads 0

Offset 65-64 - Distributed DMA Ch 2 Base / Enable.....RW

15-4 Channel 2 Base Address Bits 15-4 ..... default = 0

3 Channel 2 Enable
- 0 Disable .....default
- 1 Enable

2-0 Reserved ..... always reads 0

Offset 67-66 - Distributed DMA Ch 3 Base / Enable.....RW

15-4 Channel 3 Base Address Bits 15-4 ..... default = 0

3 Channel 3 Enable
- 0 Disable .....default
- 1 Enable

2-0 Reserved ..... always reads 0

Offset 69-68 – Serial IRQ Control .....RW

15-4 Reserved ..... always reads 0

3 Serial IRQ Enable
- 0 Disable .....default
- 1 Enable

2 Serial IRQ Mode
- 0 Continuous Mode .....default
- 1 Quiet Mode

1-0 Start-Frame Width
- 00 4 PCI Clocks .....default
- 01 6 PCI Clocks
- 10 8 PCI Clocks
- 11 -reserved-

The frame size is fixed at 21 PCI clocks.

Offset 6B-6A - Distributed DMA Ch 5 Base / Enable.... RW

15-4 Channel 5 Base Address Bits 15-4.....default = 0

3 Channel 5 Enable
- 0 Disable..... default
- 1 Enable

2-0 Reserved .....always reads 0

Offset 6D-6C - Distributed DMA Ch 6 Base / Enable ... RW

15-4 Channel 6 Base Address Bits 15-4.....default = 0

3 Channel 6 Enable
- 0 Disable..... default
- 1 Enable

2-0 Reserved .....always reads 0

Offset 6F-6E - Distributed DMA Ch 7 Base / Enable .... RW

15-4 Channel 7 Base Address Bits 15-4.....default = 0

3 Channel 7 Enable
- 0 Disable..... default
- 1 Enable

2-0 Reserved .....always reads 0

Miscellaneous / General Purpose I/O

Offset 73-70 - Subsystem ID ..... WO

31-0 Subsystem ID and Subsystem Vendor ID
Write Only. Always reads back 0.
Contents may be read at offset 2C.

Offset 77-74 – GPIO / Chip Select Control .....RW

31-30 Reserved ..... always reads 0

29 PCS1# For Internal I/O (Pin N5)
0 Disable .....default
1 Enable

28 PCS0# For Internal I/O (Pin L4)
0 Disable .....default
1 Enable

27 RTC Rx32 Remap to Rx7F Century Byte
0 Disable .....default
1 Enable

26 RTC Rx32 Write Protect
0 Disable .....default
1 Enable

25 RTC Rx0D Write Protect
0 Disable .....default
1 Enable

24 DMA Controller Shadow Registers
0 Disable .....default
1 Enable

23-22 Reserved ..... always reads 0

21 PCS1# Enable (Pin N5)
0 Disable .....default
1 Enable

20 PCS0# Enable (Pin L4)
0 Disable .....default
1 Enable

19 MCCS# Enable (Pin N4)
0 Disable .....default
1 Enable

18 GPO26 Enable (Pin K1)
0 Disable .....default
1 Enable

17 GPO25 Enable (Pin L1)
0 Disable .....default
1 Enable

16 GPO24 Enable (Pin M2)
0 Disable .....default
1 Enable

15 GPO23 Enable (Pin M4)
0 Disable .....default
1 Enable

14 GPO22 Enable (Pin M3)
0 Disable .....default
1 Enable

13 GPO21 Enable
0 Disable..... default
1 Enable

12 GPO20 Enable
0 Disable..... default
1 Enable

11 GPO19 Enable (Pin K16)
0 Disable..... default
1 Enable

10 GPO18 Enable (Pin R2)
0 Disable..... default
1 Enable

9 GPO17 Enable (Pin R1)
0 Disable..... default
1 Enable

8 Decode
0 Subtractive..... default
1 Positive

7 APIC Enable
0 Disable..... default
1 Enable

6 GPI12 Enable (Pin P18)
0 Disable..... default
1 Enable

5 GPI11 Enable (Pin N17)
0 Disable..... default
1 Enable

4 GPI10 Enable (Pin P16)
0 Disable..... default
1 Enable

3 GPI9 Enable (Pin U19)
0 Disable..... default
1 Enable

2 GPI8 Enable (Pin H19)
0 Disable..... default
1 Enable

1 Internal APIC
0 Disable..... default
1 Enable

0 GPI0/IOCHCK, GPO[7-1]/LA[23-17] Select
0 GPI0, GPO[7-1]..... default
1 IOCHCK, LA[23-17]

Bits 18-0 also control multi-function pin definitions. Refer to the General Purpose Inputs and Outputs sections of the pin descriptions for more information.

Offset 7B-78 – Programmable Chip Select Control .....RW

31-16 PCS1 I/O Port Address [15-0]
15-0 PCS0 I/O Port Address [15-0]

Offset 7F-7C – PC/PCI Control .....RW

31-11 Reserved ..... always reads 0
10 PCI DMA Pair C Enable
0 Disable .....default
1 Enable
9 PCI DMA Pair B Enable
0 Disable .....default
1 Enable
8 PCI DMA Pair A Enable
0 Disable .....default
1 Enable
7 PCI DMA Channel 7 Enable
0 Disable .....default
1 Enable
6 PCI DMA Channel 6 Enable
0 Disable .....default
1 Enable
5 PCI DMA Channel 5 Enable
0 Disable .....default
1 Enable
4 Reserved ..... always reads 0
3 PCI DMA Channel 3 Enable
0 Disable .....default
1 Enable
2 PCI DMA Channel 2 Enable
0 Disable .....default
1 Enable
1 PCI DMA Channel 1 Enable
0 Disable .....default
1 Enable
0 PCI DMA Channel 0 Enable
0 Disable .....default
1 Enable

Offset 80 – Programmable Chip Select Mask ..... RW

7-4 PCS1 I/O Port Address Mask bits 3-0
3-0 PCS0 I/O Port Address Mask bits 3-0

Offset 81 – ISA Positive Decoding Control 1 .....RW

7 On-Board I/O Port Positive Decoding
- 0 Disable .....default
- 1 Enable

6 Microsoft-Sound System I/O Port Positive Decoding
- 0 Disable .....default
- 1 Enable

5-4 Microsoft-Sound System I/O Decode Range
- 00 0530h-0537h .....default
- 01 0604h-060Bh
- 10 0E80-0E87h
- 11 0F40h-0F47h

3 APIC Positive Decoding
- 0 Disable .....default
- 1 Enable

2 BIOS ROM Positive Decoding
- 0 Disable .....default
- 1 Enable

1 PCS1 Positive Decoding
- 0 Disable .....default
- 1 Enable

0 PCS0 Positive Decoding
- 0 Disable .....default
- 1 Enable

Offset 82 – ISA Positive Decoding Control 2..... RW

7 FDC Positive Decoding
- 0 Disable..... default
- 1 Enable

6 LPT Positive Decoding
- 0 Disable..... default
- 1 Enable

5-4 LPT Decode Range
- 00 3BCh-3BFh, 7BCh-7BEh..... default
- 01 378h-37Fh, 778h-77Ah
- 10 278h-27Fh, 678h-67Ah
- 11 -reserved-

3 Game Port Positive Decoding
- 0 Disable..... default
- 1 Enable

2 MIDI Positive Decoding
- 0 Disable..... default
- 1 Enable

1-0 MIDI Decode Range
- 00 300h-303h..... default
- 01 310h-313h
- 10 320h-323h
- 11 330h-333h

Offset 83 – ISA Positive Decoding Control 3 .....RW

7 COM Port B Positive Decoding
- 0 Disable .....default
- 1 Enable

6-4 COM-Port B Decode Range
- 000 3F8h-3FFh (COM1) .....default
- 001 2F8h-2FFh (COM2)
- 010 220h-227h
- 011 228h-22Fh
- 100 238h-23Fh
- 101 2E8h-2EFh (COM4)
- 110 338h-33Fh
- 111 3E8h-3EFh (COM3)

3 COM Port A Positive Decoding
- 0 Disable .....default
- 1 Enable

2-0 COM-Port A Decode Range
- 000 3F8h-3FFh (COM1) .....default
- 001 2F8h-2FFh (COM2)
- 010 220h-227h
- 011 228h-22Fh
- 100 238h-23Fh
- 101 2E8h-2EFh (COM4)
- 110 338h-33Fh
- 111 3E8h-3EFh (COM3)

Offset 84 – ISA Positive Decoding Control 4..... RW

7-4 Reserved .....always reads 0

3 FDC Decoding Range
- 0 Primary ..... default
- 1 Secondary

2 Sound Blaster Positive Decoding
- 0 Disable..... default
- 1 Enable

1-0 Sound Blaster Decode Range
- 00 220h-22Fh, 230h-233h ..... default
- 01 240h-24Fh, 250h-253h
- 10 260h-26Fh, 270h-273h
- 11 280h-28Fh, 290h-293h

Offset 87 – Test 1 ..... RW

7 UltraDMA-66 Test
- 0 Disable .....default
- 1 Enable

6 USB Port Test
- 0 Disable .....default
- 1 Enable

5-4 USB Port Test Select

3-0 Reserved ..... always reads 0

Offset 88 – Test 2 ..... RW

7-5 Reserved ..... always reads 0

4 PLL PU
- 0 Enable.....default
- 1 Disable

3 PLL Test Mode
- 0 Disable .....default
- 1 Enable

2-0 PLL Test Mode Select

Offset 89 – PLL Control..... RW

7-4 Reserved .....always reads 0

3-2 PLL PCLK Input Delay Select

1-0 PLL CLK66 Feedback Delay Select

Function 1 Registers - Enhanced IDE Controller

This Enhanced IDE controller interface is fully compatible with the SFF 8038i v.1.0 specification. There are two sets of software accessible registers -- PCI configuration registers and Bus Master IDE I/O registers. The PCI configuration registers are located in the function 1 PCI configuration space of the VT82C596B. The Bus Master IDE I/O registers are defined in the SFF8038i v1.0 specification.

PCI Configuration Space Header

Offset 1-0 - Vendor ID (1106h=VIA).....RO

Offset 3-2 - Device ID (0571h=IDE Controller).....RO

Offset 5-4 - Command.....RW

- **15-10 Reserved** ..... always reads 0
- **9 Fast Back to Back Cycles** .....fixed at 0 (disabled)
- **8 SERR# Enable**.....fixed at 0 (disabled)
- **7 Address Stepping** ..... default=**1 (enabled)**
  VIA recommends that this bit always be set to 1 to provide additional address decode time to IDE devices.
- **6 Parity Error Response**.....fixed at 0 (disabled)
- **5 VGA Palette Snoop**.....fixed at 0 (disabled)
- **4 Memory Write & Invalidate** .....fixed at 0 (disabled)
- **3 Special Cycles**.....fixed at 0 (disabled)
- **2 Bus Master** ..... default = 0 (disabled)
  S/G operation can be issued only when the "Bus Master" bit is enabled.
- **1 Memory Space**.....fixed at 0 (disabled)
- **0 I/O Space** ..... default = 0 (disabled)
  When the "I/O Space" bit is disabled, the device will not respond to any I/O addresses for both compatible and native mode.

Offset 7-6 - Status.....RWC

- **15 Detected Parity Error**..... default=0
- **14 Signalled System Error**..... default=0
- **13 Received Master Abort**..... default=0
- **12 Received Target Abort** ..... default=0
- **11 Signalled Target Abort**.....Fixed at 0
- **10-9 DEVSEL# Timing** .....default = 01 (medium)
- **8 Data Parity Detected**..... default=0
- **7 Fast Back to Back** .....Fixed at 1
- **6-0 Reserved** ..... always reads 0

Offset 8 - Revision ID.....RO

- **0-7 Revision Code for IDE Controller Logic Block**

Offset 9 - Programming Interface ..... RW

- **7 Master IDE Capability**..... fixed at 1 (Supported)
- **6-4 Reserved** .....always reads 0
- **3 Programmable Indicator - Secondary** ..... fixed at 1
  Supports both modes (may be set to either mode by writing bit-2)
- **2 Channel Operating Mode - Secondary**
  - 0 Compatibility Mode (fixed addressing)
  - 1 Native PCI Mode (flexible addressing) ..... def
- **1 Programmable Indicator - Primary**..... fixed at 1
  Supports both modes (may be set to either mode by writing bit-0)
- **0 Channel Operating Mode - Primary**
  - 0 Compatibility Mode (fixed addressing)
  - 1 Native PCI Mode (flexible addressing) ..... def

Compatibility Mode (fixed IRQs and I/O addresses):

Channel	Command Block Registers	Control Block Registers	IRQ
Pri	1F0-1F7	3F6	14
Sec	170-177	376	15

Native PCI Mode (registers are programmable in I/O space)

Channel	Command Block Registers	Control Block Registers
Pri	BA @offset 10h	BA @offset 14h
Sec	BA @offset 18h	BA @offset 1Ch

Command register blocks are 8 bytes of I/O space
Control registers are 4 bytes of I/O space (only byte 2 is used)

Offset A - Sub Class Code (01h=IDE Controller) ..... RO

Offset B - Base Class Code (01h=Mass Storage Ctrlr)... RO

Offset D - Latency Timer (00h) ..... RW

- **7-4 Latency Timer**.....default=0
- **3-0 Reserved** .....always reads 0

Offset E - Header Type (00h).....RO

Offset F - BIST (00h).....RO

Offset 13-10 - Pri Data / Command Base Address.....RW

Specifies an 8 byte I/O address space.

31-16	**Reserved**	always read 0
15-3	**Port Address**	default=01F0h
2-0	**Fixed at 001b**	fixed

Offset 17-14 - Pri Control / Status Base Address.....RW

Specifies a 4 byte I/O address space of which only the third byte is active (i.e., 3F6h for the default base address of 3F4h).

31-16	**Reserved**	always read 0
15-2	**Port Address**	default=03F4h
1-0	**Fixed at 01b**	fixed

Offset 1B-18 - Sec Data / Command Base Address .....RW

Specifies an 8 byte I/O address space.

31-16	**Reserved**	always read 0
15-3	**Port Address**	default=0170h
2-0	**Fixed at 001b**	fixed

Offset 1F-1C - Sec Control / Status Base Address.....RW

Specifies a 4 byte I/O address space of which only the third byte is active (i.e., 376h for the default base address of 374h).

31-16	**Reserved**	always read 0
15-2	**Port Address**	default=0374h
1-0	**Fixed at 01b**	fixed

Offset 23-20 - Bus Master Control Regs Base Address..RW

Specifies a 16 byte I/O address space compliant with the **SFF-8038**i **rev 1.0** specification.

31-16	**Reserved**	always read 0
15-4	**Port Address**	default=CC0h
3-0	**Fixed at 0001b**	fixed

Offset 3C - Interrupt Line (0Eh) ..... RW

Offset 3D - Interrupt Pin (00h)..... RO

7-0 Interrupt Routing Mode

00h Legacy mode interrupt routing..... default

01h Native mode interrupt routing

Offset 3E - Min Gnt (00h) ..... RO

Offset 3F - Max Latency (00h)..... RO

IDE-Controller-Specific Confiiguration Registers

Offset 40 - Chip Enable.....RW

- **7-4 Reserved** ..... always reads 0
- **3-2 Reserved (Do Not Program)**.....R/W, default = 0
- **1 Primary Channel Enable**..... default = 0 (disabled)
- **0 Secondary Channel Enable** .... default = 0 (disabled)

Offset 41 - IDE Configuration.....RW

- **7 Primary IDE Read Prefetch Buffer**
  - 0 Disable .....default
  - 1 Enable
- **6 Primary IDE Post Write Buffer**
  - 0 Disable .....default
  - 1 Enable
- **5 Secondary IDE Read Prefetch Buffer**
  - 0 Disable .....default
  - 1 Enable
- **4 Secondary IDE Post Write Buffer**
  - 0 Disable .....default
  - 1 Enable
- **3 Reserved (Do Not Change)**..... default=0
- **2 Reserved (Do Not Change)**..... default=1
- **1 Reserved (Do Not Change)**..... default=1
- **0 Reserved (Do Not Change)**..... default=0

Offset 42 - Reserved (Do Not Program) .....RW

- **7-2 Reserved** ..... always reads 0
- **1-0 Reserved (Do Not Program)**..... default = 0

Offset 43 - FIFO Configuration..... RW

- **7-4 Reserved** .....always reads 0
- **3-2 Threshold for Primary Channel**
  - 00 1
  - 01 1/4
  - 10 1/2 ..... default
  - 11 3/4
- **1-0 Threshold for Secondary Channel**
  - 00 1
  - 01 1/4
  - 10 1/2 ..... default
  - 11 3/4

Offset 44 - Miscellaneous Control 1.....RW

7 Reserved ..... always reads 0

6 Master Read Cycle IRDY# Wait States
- 0 0 wait states
- 1 1 wait state.....default

5 Master Write Cycle IRDY# Wait States
- 0 0 wait states
- 1 1 wait state.....default

4 Reserved (Do Not Program).....R/W, default = 0

3 Bus Master IDE Status Register Read Retry

Retry bus master IDE status register read when master write operation for DMA read is not complete
- 0 Disabled
- 1 Enabled.....default

2-1 Reserved (Do Not Program).....R/W, default = 0

0 UltraDMA Host Must Wait for First Strobe Before Termination
- 0 Enabled.....default
- 1 Disabled

Offset 45 - Miscellaneous Control 2.....RW

7 Reserved ..... always reads 0

6 Interrupt Steering Swap
- 0 Don't swap channel interrupts.....default
- 1 Swap interrupts between the two channels

5-4 Reserved ..... always reads 0

3 Memory Read Multiple Command
- 0 Disable .....default
- 1 Enable

2 Memory Read and Invalidate Command
- 0 Disable .....default
- 1 Enable

1 Secondary Channel Threshold Enable
- 0 Disable (data transfer starts immediately if FIFO is not empty)
- 1 Enable (data transfer will not start until the FIFO is filled to the threshold set in bits 1-0 of Rx43) .....default

0 Primary Channel Threshold Enable
- 0 Disable (data transfer starts immediately if FIFO is not empty)
- 1 Enable (data transfer will not start until the FIFO is filled to the threshold set in bits 3-2 of Rx43) .....default

Offset 46 - Miscellaneous Control 3 ..... RW

7 Primary Channel Read DMA FIFO Flush

1 = Enable FIFO flush for read DMA when interrupt asserts primary channel. .....default=1 (enabled)

6 Secondary Channel Read DMA FIFO Flush

1 = Enable FIFO flush for Read DMA when interrupt asserts secondary channel. .....Default=1 (enabled)

5 Primary Channel End-of-Sector FIFO Flush

1 = Enable FIFO flush at the end of each sector for the primary channel. ..... Default=0 (disabled)

4 Secondary Channel End-of-Sector FIFO Flush

1 = Enable FIFO flush at the end of each sector for the secondary channel..... Default=0 (disabled)

3-2 Reserved .....always reads 0

1-0 Max DRDY Pulse Width

Maximum DRDY# pulse width after the cycle count. Command will deassert in spite of DRDY# status to avoid system ready hang.
- 00 No limitation..... default
- 01 64 PCI clocks
- 10 128 PCI clocks
- 11 192 PCI clocks

Offset 4B-48 - Drive Timing Control.....RW

The following fields define the Active Pulse Width and Recovery Time for the IDE DIOR# and DIOW# signals:

31-28 Primary Drive 0 Active Pulse Width..... def=1010b
27-24 Primary Drive 0 Recovery Time..... def=1000b
23-20 Primary Drive 1 Active Pulse Width..... def=1010b
19-16 Primary Drive 1 Recovery Time..... def=1000b
15-12 Secondary Drive 0 Active Pulse Width .. def=1010b
11-8 Secondary Drive 0 Recovery Time ..... def=1000b
7-4 Secondary Drive 1 Active Pulse Width .. def=1010b
3-0 Secondary Drive 1 Recovery Time ..... def=1000b

The actual value for each field is the encoded value in the field plus one and indicates the number of PCI clocks.

Offset 4C - Address Setup Time.....RW

7-6 Primary Drive 0 Address Setup Time
5-4 Primary Drive 1 Address Setup Time
3-2 Secondary Drive 0 Address Setup Time
1-0 Secondary Drive 1 Address Setup Time

For each field above:

00 1T
01 2T
10 3T
11 4T .....default

Offset 4E - Secondary Non-1F0 Port Access Timing.....RW

7-4 DIOR#/DIOW# Active Pulse Width..... def=1111b
3-0 DIOR#/DIOW# Recovery Time..... def=1111b

The actual value for each field is the encoded value in the field plus one and indicates the number of PCI clocks.

Offset 4F - Primary Non-1F0 Port Access Timing` .....RW

7-4 DIOR#/DIOW# Active Pulse Width..... def=1111b
3-0 DIOR#/DIOW# Recovery Time..... def=1111b

The actual value for each field is the encoded value in the field plus one and indicates the number of PCI clocks.

Offset 53-50 - UltraDMA Extended Timing Control..... RW

31 Pri Drive 0 UltraDMA-Mode Enable Method
0 Enable by using “Set Feature” command..... def
1 Enable by setting bit-30 of this register
30 Pri Drive 0 UltraDMA-Mode Enable
0 Disable..... default
1 Enable UltraDMA-Mode Operation
29 Pri Drive 0 Transfer Mode
0 Based on DMA or PIO Mode ..... default
1 Based on UltraDMA Mode
28-26 Reserved .....always reads 0
25-24 Pri Drive 0 Cycle Time (T = 30nsec @33MHz)
00 2T
01 3T
10 4T
11 5T ..... default

23 Pri Drive 1 UltraDMA-Mode Enable Method
22 Pri Drive 1 UltraDMA-Mode Enable
21 Pri Drive 1 Transfer Mode
20 Reserved .....always reads 0
19 Pri Clock Source
0 33 MHz..... default
1 66 MHz
18 Reserved .....always reads 0
17-16 Pri Drive 1 Cycle Time

15 Sec Drive 0 UltraDMA-Mode Enable Method
14 Sec Drive 0 UltraDMA-Mode Enable
13 Sec Drive 0 Transfer Mode
12-10 Reserved .....always reads 0
9-8 Sec Drive 0 Cycle Time

7 Sec Drive 1 UltraDMA-Mode Enable Method
6 Sec Drive 1 UltraDMA-Mode Enable
5 Sec Drive 1 Transfer Mode
4 Reserved .....always reads 0
3 Sec Clock Source
0 33 MHz..... default
1 66 MHz
2 Reserved .....always reads 0
1-0 Sec Drive 1 Cycle Time

Each byte defines UltraDMA operation for the indicated drive. The bit definitions are the same within each byte.

Offset 54 – UltraDMA FIFO Control.....RW

7-5 Reserved (Do Not Program).....RW, default=0

4 Split REQ Change Channel
- 0 Enable .....default
- 1 Disable

3 Reserved ..... always reads 0

2 Change Drive to Clear All FIFO & Internal States
- 0 Disabled
- 1 Enabled .....default

1 Add Dummy FIFO Push After End of Transfer
- 0 Enabled
- 1 Disabled .....default

This bit is normally set to 0 for effective handling of transfer lengths that are not doubleword multiples

0 Complete DMA Cycle with Transfer Size Less Than FIFO Size
- 0 Enabled.....default
- 1 Disabled

Offset 61-60 - Primary Sector Size ..... RW

15-12 Reserved .....always reads 0

11-0 Number of Bytes Per Sector .....default=200h

Offset 69-68 - Secondary Sector Size ..... RW

15-12 Reserved .....always reads 0

11-0 Number of Bytes Per Sector ...def=200h (512 bytes)

Offset 70 – Primary IDE Status .....RW

7	**Interrupt Status**	
6	**Prefetch Buffer Status**	
5	**Post Write Buffer Status**	
4	**DMA Read Prefetch Status**	
3	**DMA Write Prefetch Status**	
2	**S/G Operation Complete**	
1-0	**Reserved**	always reads 0

Offset 71 – Primary Interrupt Control.....RW

7-1	**Reserved**	always reads 0
0	**Flush FIFO Before Generating IDE Interrupt**	
	0 Desable.....	default
	1 Enable	

Offset 74 – Primary IDE Command 1 .....RW

7	**Reload Sector Size After Last Command Register Write**	
6-0	**Reserved**	always reads 0

Offset 75 – Primary IDE Command 2 .....RW

7	**Set Controller to Perform PIO Mode Data Port Prefetch**	
6	**Set Controller to Perform PIO Mode Data Port Buffer Write**	
5	**Set Controller to Perform DMA Mode Read Pipeline Operation**	
4	**Set Controller to Perform DMA Mode Write Pipeline Operation**	
3	**Stop S/G Bus Master**	
2-0	**Reserved**	always reads 0

Offset 78 – Secondary IDE Status ..... RW

7	**Interrupt Status**	
6	**Prefetch Buffer Status**	
5	**Post Write Buffer Status**	
4	**DMA Read Prefetch Status**	
3	**DMA Write Prefetch Status**	
2	**S/G Operation Complete**	
1-0	**Reserved**	always reads 0

Offset 79 - Secondary Interrupt Control ..... RW

7-1	**Reserved**	always reads 0
0	**Flush FIFO Before Generating IDE Interrupt**	
	0 Desable	default
	1 Enable	

Offset 7C – Secondary IDE Command 1 ..... RW

7	**Reload Sector Size After Last Command Register Write**	
6-0	**Reserved**	always reads 0

Offset 7D – Secondary IDE Command 2 ..... RW

7	**Set Controller to Perform PIO Mode Data Port Prefetch**	
6	**Set Controller to Perform PIO Mode Data Port Buffer Write**	
5	**Set Controller to Perform DMA Mode Read Pipeline Operation**	
4	**Set Controller to Perform DMA Mode Write Pipeline Operation**	
3	**Stop S/G Bus Master**	
2-0	**Reserved**	always reads 0

Offset 83-80 – Primary S/G Descriptor Address .....RW

Offset 8B-88 – Secondary S/G Descriptor Address .....RW

IDE I/O Registers

These registers are compliant with the SFF 8038I v1.0 standard. Refer to the SFF 8038I v1.0 specification for further details.

I/O Offset 0 - Primary Channel Command

I/O Offset 2 - Primary Channel Status

I/O Offset 4-7 - Primary Channel PRD Table Address

I/O Offset 8 - Secondary Channel Command

I/O Offset A - Secondary Channel Status

I/O Offset C-F - Secondary Channel PRD Table Address

Function 2 Registers - Universal Serial Bus Controller

This USB host controller interface is fully compatible with UHCI specification v1.1. There are two sets of software accessible registers: PCI configuration registers and USB I/O registers. The PCI configuration registers are located in the function 2 PCI configuration space of the VT82C596B. The USB I/O registers are defined in the UHCI v1.1 specification.

PCI Configuration Space Header

Offset 1-0 - Vendor ID ..... RO

0-7 Vendor ID ..... (1106h = VIA Technologies)

Offset 3-2 - Device ID ..... RO

0-7 Device ID (3038h = VT82C596B USB Controller)

Offset 5-4 - Command ..... RW

15-8 Reserved ..... always reads 0
7 Address Stepping ..... default=0 (disabled)
6 Reserved (parity error response) ..... fixed at 0
5 Reserved (VGA palette snoop) ..... fixed at 0
4 Memory Write and Invalidate . default=0 (disabled)
3 Reserved (special cycle monitoring) ..... fixed at 0
2 Bus Master ..... default=0 (disabled)
1 Memory Space ..... default=0 (disabled)
0 I/O Space ..... default=0 (disabled)

Offset 7-6 - Status ..... RWC

15 Reserved (detected parity error) ..... always reads 0
14 Signalled System Error ..... default=0
13 Received Master Abort ..... default=0
12 Received Target Abort ..... default=0
11 Signalled Target Abort ..... default=0
10-9 DEVSEL# Timing
00 Fast
01 Medium ..... default (fixed)
10 Slow
11 Reserved
8-0 Reserved ..... always reads 0

Offset 8 - Revision ID (nnh) ..... RO

7-0 Silicon Revision Code (0 indicates first silicon)

Offset 9 - Programming Interface (00h) ..... RO

Offset A - Sub Class Code (03h) ..... RO

Offset B - Base Class Code (0Ch) ..... RO

Offset 0D - Latency Timer ..... RW

7-0 Timer Value ..... default = 16h

Offset 0E - Header Type (00h) ..... RO

Offset 23-20 - USB I/O Register Base Address ..... RW

31-16 Reserved ..... always reads 0
15-5 USB I/O Register Base Address. Port Address for the base of the 32-byte USB I/O Register block, corresponding to AD[15:5]
4-0 00001b

Offset 3C - Interrupt Line (00h) ..... RW

7-4 Reserved ..... always reads 0
3-0 USB Interrupt Routing ..... default = 16h
0000 Disabled ..... default
0001 IRQ1
0010 Reserved
0011 IRQ3
0100 IRQ4
0101 IRQ5
0110 IRQ6
0111 IRQ7
1000 IRQ8
1001 IRQ9
1010 IRQ10
1011 IRQ11
1100 IRQ12
1101 IRQ13
1110 IRQ14
1111 Disabled

Offset 3D - Interrupt Pin (04h) ..... RO

USB-Specific Configuration Registers

Offset 40 - Miscellaneous Control 1.....RW

7 PCI Memory Command Option
- 0 Support Memory-Read-Line, Memory-Read-Multiple, and Memory-Write-and-Invalidate ....default
- 1 Only support Memory Read, Memory Write Commands

6 Babble Option
- 0 Automatically disable babbled port when EOF babble occurs.....default
- 1 Don't disable babbled port

5 PCI Parity Check Option
- 0 Disable PERR# generation.....default
- 1 Enable parity check and PERR# generation

4 Reserved ..... always reads 0

3 USB Data Length Option
- 0 Support TD length up to 1280.....default
- 1 Support TD length up to 1023

2 USB Power Management
- 0 Disable USB power management.....default
- 1 Enable USB power management

1 DMA Option
- 0 16 DW burst access.....default
- 1 8 DW burst access

0 PCI Wait States
- 0 Zero wait .....default
- 1 One wait

Offset 41 - Miscellaneous Control 2 ..... RW

7 USB 1.1 Improvement for EOP
- 0 USB Specification 1.1 Compliant..... default
  If a bit stuffing error occurs before EOP, the receiver will accept the packet
- 1 USB Specification 1.0 Compliant
  If a bit stuffing error occurs before EOP, the receiver will ignore the packet

6 Patch Read / Resume Issue
- 0 Enable (Fix the Bug) (Normal Setting).. default
- 1 Disable (when one USB port is in reset or resume status, the controller may not see the device attached at the other USB port)

5 Patch 1 Bit-Time EOP

The USB spec says that the device must assert an EOP in at least two bit times.
- 0 Enable (accept 1 bit-time EOP) ..... default
- 1 Disable (require 2 bit-time EOP)

4 Hold PCI Request for Successive Accesses
- 0 Disable
- 1 Enable ..... default

Setting this bit to "enable" causes the system to treat the USB request as higher priority

3 Frame Counter Test Mode
- 0 Disable ..... default
- 1 Enable

2 Trap Option
- 0 Set trap 60/64 status bits only when trap 60/64 enable bits are set..... default
- 1 Set trap 60/64 status bits without checking enable bits

1 A20gate Pass Through Option
- 0 Pass through A20GATE command sequence defined in UHCI ..... default
- 1 Don't pass through Write I/O port 64 (ff)

0 Reserved ..... always reads 0

Offset 60 - Serial Bus Release Number.....RO

7-0 Release Number..... always reads 10h

Offset C1-C0 - Legacy Support.....RO

15-0 UHCI v1.1 Compliant..... always reads 2000h

USB I/O Registers

These registers are compliant with the UHCI v1.1 standard. Refer to the UHCI v1.1 specification for further details.

I/O Offset 1-0 - USB Command

I/O Offset 3-2 - USB Status

I/O Offset 5-4 - USB Interrupt Enable

I/O Offset 7-6 - Frame Number

I/O Offset B-8 - Frame List Base Address

I/O Offset 0C - Start Of Frame Modify

I/O Offset 11-10 - Port 1 Status / Control

I/O Offset 13-12 - Port 2 Status / Control

I/O Offset 1F-14 - Reserved

Function 3 Registers - Power Management and SMBus

This section describes the ACPI (Advanced Configuration and Power Interface) Power Management system of the VT82C596B which includes a System Management Bus (SMBus) interface controller. The power management system of the VT82C596B supports both ACPI and legacy power management functions and is compatible with the APM v1.2 and ACPI v1.0 specifications.

PCI Configuration Space Header

Offset 1-0 - Vendor ID ..... RO

0-7 Vendor ID ..... (1106h = VIA Technologies)

Offset 3-2 - Device ID ..... RO

0-7 Device ID ..... (3050h = ACPI Power Mgmt)

Offset 5-4 - Command ..... RW

15-8 Reserved ..... always reads 0
7 Address Stepping ..... fixed at 0
6 Reserved (parity error response) ..... fixed at 0
5 Reserved (VGA palette snoop) ..... fixed at 0
4 Memory Write and Invalidate ..... fixed at 0
3 Reserved (special cycle monitoring) ..... fixed at 0
2 Bus Master ..... fixed at 0
1 Memory Space ..... fixed at 0
0 I/O Space ..... fixed at 0

Offset 7-6 - Status ..... RWC

15 Detected Parity Error ..... always reads 0
14 Signalled System Error ..... always reads 0
13 Received Master Abort ..... always reads 0
12 Received Target Abort ..... always reads 0
11 Signalled Target Abort ..... always reads 0
10-9 DEVSEL# Timing
00 Fast
01 Medium ..... default (fixed)
10 Slow
11 Reserved
8 Data Parity Detected ..... always reads 0
7 Fast Back to Back Capable ..... always reads 1
6-0 Reserved ..... always reads 0

Offset 8 - Revision ID (nnh) ..... RO

7-0 Silicon Revision Code ..... default = 20h

Offset 9 - Programming Interface (00h) ..... RO

The value returned by this register may be changed by writing the desired value to PCI Configuration Function 3 offset 61h.

Offset A - Sub Class Code (00h) ..... RO

The value returned by this register may be changed by writing the desired value to PCI Configuration Function 3 offset 62h.

Offset B - Base Class Code (00h) ..... RO

The value returned by this register may be changed by writing the desired value to PCI Configuration Function 3 offset 63h.

Offset 0D - Latency Timer ..... RW

7-0 Timer Value ..... default = 0

Offset 0E - Header Type (00h) ..... RO

Power Management-Specific PCI Configuration Registers

Offset 40 - Debounce Control.....RW

7-6 Reserved ..... always reads 0

5 Debounce LID and PWRBTN# Inputs for 200us

0 Disable .....default

1 Enable

4-0 Reserved ..... always reads 0

Offset 41 - General Configuration (00h)..... RW

7 I/O Enable for ACPI I/O Base

0 Disable access to ACPI I/O block..... default

1 Allow access to Power Management I/O Register Block (see offset 4B-48 to set the base address for this register block). The definitions of the registers in the Power Management I/O Register Block are included later in this document, following the Power Management Subsystem overview.

6 ACPI Timer Reset

0 Disable..... default

1 Enable

5-4 Reserved (Do Not Program).....default = 0

3 ACPI Timer Count Select

0 24-bit Timer..... default

1 32-bit Timer

2 RTC Enable Signal Gated with PSON (SUSC#) in Soft-Off Mode

0 Disable..... default

1 Enable

1 Clock Throttling Clock Selection

0 32 usec (512 usec cycle time)..... default

1 1 msec (16 msec cycle time)

0 Reserved (Do Not Program).....default = 0

Offset 42 - SCI Interrupt Configuration (00h) .....RW

7 ATX/AT Power Indicator.....RO
- 0 ATX .....default
- 1 AT

6 SUSC State .....RO

5 Reserved ..... always reads 0

4 SUSC Default Off Enable Status .....RO

3-0 SCI Interrupt Assignment
- 0000 Disabled .....default
- 0001 IRQ1
- 0010 Reserved
- 0011 IRQ3
- 0100 IRQ4
- 0101 IRQ5
- 0110 IRQ6
- 0111 IRQ7
- 1000 IRQ8
- 1001 IRQ9
- 1010 IRQ10
- 1011 IRQ11
- 1100 IRQ12
- 1101 IRQ13
- 1110 IRQ14
- 1111 IRQ15

Offset 45-44 - Primary Interrupt Channel (0000h) ..... RW

15 1/0 = Ena/Disa IRQ15 as Primary Intrpt Channel
14 1/0 = Ena/Disa IRQ14 as Primary Intrpt Channel
13 1/0 = Ena/Disa IRQ13 as Primary Intrpt Channel
12 1/0 = Ena/Disa IRQ12 as Primary Intrpt Channel
11 1/0 = Ena/Disa IRQ11 as Primary Intrpt Channel
10 1/0 = Ena/Disa IRQ10 as Primary Intrpt Channel
9 1/0 = Ena/Disa IRQ9 as Primary Intrpt Channel
8 1/0 = Ena/Disa IRQ8 as Primary Intrpt Channel
7 1/0 = Ena/Disa IRQ7 as Primary Intrpt Channel
6 1/0 = Ena/Disa IRQ6 as Primary Intrpt Channel
5 1/0 = Ena/Disa IRQ5 as Primary Intrpt Channel
4 1/0 = Ena/Disa IRQ4 as Primary Intrpt Channel
3 1/0 = Ena/Disa IRQ3 as Primary Intrpt Channel
2 Reserved .....always reads 0
1 1/0 = Ena/Disa IRQ1 as Primary Intrpt Channel
0 1/0 = Ena/Disa IRQ0 as Primary Intrpt Channel

Offset 47-46 - Secondary Interrupt Channel (0000h).... RW

15 1/0 = Ena/Disa IRQ15 as Secondary Intr Channel
14 1/0 = Ena/Disa IRQ14 as Secondary Intr Channel
13 1/0 = Ena/Disa IRQ13 as Secondary Intr Channel
12 1/0 = Ena/Disa IRQ12 as Secondary Intr Channel
11 1/0 = Ena/Disa IRQ11 as Secondary Intr Channel
10 1/0 = Ena/Disa IRQ10 as Secondary Intr Channel
9 1/0 = Ena/Disa IRQ9 as Secondary Intr Channel
8 1/0 = Ena/Disa IRQ8 as Secondary Intr Channel
7 1/0 = Ena/Disa IRQ7 as Secondary Intr Channel
6 1/0 = Ena/Disa IRQ6 as Secondary Intr Channel
5 1/0 = Ena/Disa IRQ5 as Secondary Intr Channel
4 1/0 = Ena/Disa IRQ4 as Secondary Intr Channel
3 1/0 = Ena/Disa IRQ3 as Secondary Intr Channel
2 Reserved .....always reads 0
1 1/0 = Ena/Disa IRQ1 as Secondary Intr Channel
0 1/0 = Ena/Disa IRQ0 as Secondary Intr Channel

Offset 4B-48 – Power Management I/O Base .....RW

31-16 Reserved ..... always reads 0

15-7 Power Management I/O Register Base Address. Port Address for the base of the 128-byte Power Management I/O Register block, corresponding to AD[15:7]. The "I/O Space" bit at offset 41 bit-7 enables access to this register block. The definitions of the registers in the Power Management I/O Register Block are included later in this document, following the Power-Management-Specific PCI Configuration register descriptions and the Power Management Subsystem overview.

6-0 0000001b

Offset 4C – Host Bus Power Management Control.....RW

7-4 Thermal Duty Cycle (THM_DTY)

This 4-bit field determines the duty cycle of the STPCLK# signal when the THRM# pin is asserted low. The field is decoded as follows:

0000 Reserved
0001 0-6.25%
0010 6.25-12.50%
0011 18.75-25.00%
0100 31.25-37.50%
0101 37.50-43.75%
0110 43.75-50.00%
0111 50.00-56.25%
1000 56.25-62.50%
1001 62.50-68.75%
1010 68.75-75.00%
1011 75.00-87.50%
1100 75.00-81.25%
1101 81.25-87.50%
1110 87.50-93.75%
1111 93.75-100%

3-2 Reserved ..... always reads 0

1 SRAM ZZ

0 Disable .....default
1 Enable (power down the cache SRAM)

0 CPU Stop Grant Cycle Select

0 From Halt and Stop Grant Cycle .....default
1 From Stop Grant Cycle

This bit is combined with I/O space Rx2C[3] for controlling the start of STPCLK# assertion during system suspend mode:

Rx2C[3] Function 3 I/O Space	Rx4C[0] Function 3 Cfg Space	STPCLK# Assertion
0	x	Immediate
1	0	Wait for CPU Halt / Stop Grant cycle
1	1	Wait for CPU Stop Grant cycle

Offset 4D – Clock Stop Control..... RW

7-3 Reserved .....always reads 0

2 Internal Clock Stop for PCI Idle

0 Disable..... default
1 Enable

1 Internal Clock Stop During C3

0 Disable..... default
1 Enable

0 Internal Clock Stop During Suspend

0 Disable..... default
1 Enable

Offset 53-50 – GP0/1 Timer Control (0000 0000h).....RW

31-30 Conserve Mode Timer Count Value
- 00 1/16 second .....default
- 01 1/8 second
- 10 1 second
- 11 1 minute

29 Conserve Mode Status
This bit reads 1 when in Conserve Mode

28 Conserve Mode Enable
- 0 Disable .....default
- 1 Enable

27-26 Secondary Event Timer Count Value
- 00 2 milliseconds.....default
- 01 64 milliseconds
- 10 ½ second
- 11 by EOI + 0.25 milliseconds

25 Secondary Event Occurred Status
This bit reads 1 to indicate that a secondary event has occurred (to resume the system from suspend) and the secondary event timer is counting down.

24 Secondary Event Timer Enable
- 0 Disable .....default
- 1 Enable

23-16 GP1 Timer Count Value (base defined by bits 5-4)
Write to load count value; Read to get current count

15-8 GP0 Timer Count Value (base defined by bits 1-0)
Write to load count value; Read to get current count

7 GP1 Timer Start
On setting this bit to 1, the GP1 timer loads the value defined by bits 23-16 of this register and starts counting down. The GP1 timer is reloaded at the occurrence of certain peripheral events enabled in the GP Timer Reload Enable Register (Power Management I/O Space Offset 38h). If no such event occurs and the GP1 timer counts down to zero, then the GP1 Timer Timeout Status bit is set to one (bit-3 of the Global Status register at Power Management Register I/O Space Offset 28h). Additionally, if the GP1 Timer Timeout Enable bit is set (bit-3 of the Global Enable register at Power Management Register I/O Space Offset 2Ah), then an SMI is generated.

6 GP1 Timer Automatic Reload
This bit is set to one to enable the GP1 timer to reload automatically after counting down to 0.

5-4 GP1 Timer Base
- 00 Disable .....default
- 01 1/4 msec
- 10 1 second
- 11 1 minute

3 GP0 Timer Start
On setting this bit to 1, the GP0 timer loads the value defined by bits 15-8 of this register and starts counting down. The GP0 timer is reloaded at the occurrence of certain peripheral events enabled in the GP Timer Reload Enable Register (Power Management I/O Space Offset 38h). If no such event occurs and the GP0 timer counts down to zero, then the GP0 Timer Timeout Status bit is set to one (bit-2 of the Global Status register at Power Management Register I/O Space Offset 28h). Additionally, if the GP0 Timer Timeout Enable bit is set (bit-2 of the Global Enable register at Power Management Register I/O Space Offset 2Ah), then an SMI is generated.

2 GP0 Timer Automatic Reload
This bit is set to one to enable the GP0 timer to reload automatically after counting down to 0.

1-0 GP0 Timer Base
- 00 Disable..... default
- 01 1/16 second
- 10 1 second
- 11 1 minute

Offset 54 – GPIO Select .....RW

7 GPO21 Pin Function (Pin T18)
- 0 SUSST2#.....default
- 1 GPO21

6 Power Well Output Gating for STR
- 0 Disable .....default
- 1 Enable

5 SUSC# Level for STR
- 0 SUSC# = 1 for STR.....default
- 1 SUSC# = 0 for STR

4 GPO20 Pin Function (Pin T17)
- 0 SUSST1#.....default
- 1 GPO20

3 GPO15 Pin Function (Pin V19)
- 0 SUSB#.....default
- 1 GPO15

2 GPO16 Pin Function (Pin U18)
- 0 SUSC#.....default
- 1 GPO16

1-0 GPO8 Pin Function (Pin T19)
- 00 GPO8 (ACPI Rx4C[8] .....default
- 01 1 Hz Output
- 10 2 Hz Output
- 11 4 Hz Output

Offset 55 – Wakeup Control ..... RW

7-1 Reserved .....always reads 0

0 USB Wakeup for STR / STD / Soft Off
- 0 Disable..... default
- 1 Enable

Offset 5B-58 – GP2/3 Timer Control (0000 0000h) .....RW

31-24 Reserved ..... always reads 0

23-16 GP3 Timer Count Value (base defined by bits 5-4)
Write to load count value; Read to get current count

15-8 GP2 Timer Count Value (base defined by bits 1-0)
Write to load count value; Read to get current count

7 GP3 Timer Start
On setting this bit to 1, the GP3 timer loads the value defined by bits 23-16 of this register and starts counting down. The GP3 timer is reloaded at the occurrence of certain peripheral events enabled in the GP Timer Reload Enable Register (Power Management I/O Space Offset 38h). If no such event occurs and the GP3 timer counts down to zero, then the GP3 Timer Timeout Status bit is set to one (bit-13 of the Global Status register at Power Management Register I/O Space Offset 28h). Additionally, if the GP3 Timer Timeout Enable bit is set (bit-13 of the Global Enable register at Power Management Register I/O Space Offset 2Ah), then an SMI is generated.

6 GP3 Timer Automatic Reload
This bit is set to one to enable the GP3 timer to reload automatically after counting down to 0.

5-4 GP3 Timer Base
00 Disable .....default
01 1/4 msec
10 1 second
11 1 minute

3 GP2 Timer Start
On setting this bit to 1, the GP2 timer loads the value defined by bits 15-8 of this register and starts counting down. The GP2 timer is reloaded at the occurrence of certain peripheral events enabled in the GP Timer Reload Enable Register (Power Management I/O Space Offset 38h). If no such event occurs and the GP2 timer counts down to zero, then the GP2 Timer Timeout Status bit is set to one (bit-12 of the Global Status register at Power Management Register I/O Space Offset 28h). Additionally, if the GP2 Timer Timeout Enable bit is set (bit-12 of the Global Enable register at Power Management Register I/O Space Offset 2Ah), then an SMI is generated.

2 GP2 Timer Automatic Reload
This bit is set to one to enable the GP2 timer to reload automatically after counting down to 0.

1-0 GP2 Timer Base
00 Disable .....default
01 1/16 second
10 1 second
11 1 minute

Offset 61 - Programming Interface Read Value .....WO

7-0 Rx09 Read Value
The value returned by the register at offset 9h (Programming Interface) may be changed by writing the desired value to this location.

Offset 62 - Sub Class Read Value.....WO

7-0 Rx0A Read Value
The value returned by the register at offset 0Ah (Sub Class Code) may be changed by writing the desired value to this location.

Offset 63 - Base Class Read Value.....WO

7-0 Rx0B Read Value
The value returned by the register at offset 0Bh (Base Class Code) may be changed by writing the desired value to this location.

System Management Bus-Specific Configuration Registers

Offset 93-90 – SMBus I/O Base.....RW

31-16 Fixed ..... always reads 00h
15-4 I/O Base ..... default = 00h
3-0 Fixed ..... always reads 0001b

Offset D2 – SMBus Control.....RW

7-4 Reserved ..... always reads 0
3 SMBus Interrupt Select
0 SMI .....default
1 SCI
2-1 Reserved ..... always reads 0
0 SMBus Controller Enable
0 Disable .....default
1 Enable

Offset D3 – SMBus Host Slave Command..... RW

7-0 SMBus Host Slave Command Code.....default=0

Offset D4 – SMBus Slave Address for Port 1..... RW

7-1 SMBus Slave Address for Port 1.....default=0
0 R/W for Shadow Port 1
0 Disable..... default
1 Enable

Offset D5 – SMBus Slave Address for Port 2..... RW

7-1 SMBus Slave Address for Port 2.....default=0
0 R/W for Shadow Port 2
0 Disable..... default
1 Enable

Offset D6 – SMBus Revision ID ..... RO

7-0 SMBus Revision Code

System Management Bus I/O-Space Registers

I/O Offset 00 – SMBus Host Status.....RWC

7-5 Reserved ..... always reads 0

4 Failed Bus Transaction.....**RWC**
- 0 SMBus interrupt not caused by failed bus transaction .....default
- 1 SMBus interrupt caused by failed bus transaction. This bit may be set when the KILL bit (I/O Rx02[1]) is set and can be cleared by writing a 1 to this bit position.

3 Bus Collision.....**RWC**
- 0 SMBus interrupt not caused by transaction collision.....default
- 1 SMBus interrupt caused by transaction collision. This bit is only set by hardware and can be cleared by writing a 1 to this bit position.

2 Device Error.....**RWC**
- 0 SMBus interrupt not caused by generation of an SMBus transaction error.....default
- 1 SMBus interrupt caused by generation of an SMBus transaction error (illegal command field, unclaimed host-initiated cycle, or host device timeout). This bit is only set by hardware and can be cleared by writing a 1 to this bit position.

1 SMBus Interrupt.....**RWC**
- 0 SMBus interrupt not caused by host command completion.....default
- 1 SMBus interrupt caused by host command completion. This bit is only set by hardware and can be cleared by writing a 1 to this bit position.

0 Host Busy .....**RO**
- 0 SMBus controller host interface is not processing a coimmand .....default
- 1 SMBus host controller is busy processing a coimmand. None of the other SMBus registers should be accessed if this bit is set.

I/O Offset 01h – SMBus Slave Status..... RWC

7-6 Reserved .....always reads 0

5 Alert Status ..... **RWC**
- 0 SMBus interrupt not caused by SMBALERT# signal ..... default
- 1 SMBus interrupt caused by SMBALERT# signal. This bit will be set only if the Alert Enable bit is set in the SMBus Slave Control Register at I/O Offset R08[3]. This bit is only set by hardware and can be cleared by writing a 1 to this bit position.

4 Shadow 2 Status..... **RWC**
- 0 SMBus interrupt not caused by address match to SMBus Shadow Address Port 2..... default
- 1 SMBus interrupt or resume event caused by slave cycle address match to SMBus Shadow Address Port 2. This bit is only set by hardware and can be cleared by writing a 1 to this bit position.

3 Shadow 1 Status..... **RWC**
- 0 SMBus interrupt not caused by address match to SMBus Shadow Address Port 1..... default
- 1 SMBus interrupt or resume event caused by slave cycle address match to SMBus Shadow Address Port 1. This bit is only set by hardware and can be cleared by writing a 1 to this bit position.

2 Slave Status ..... **RWC**
- 0 SMBus interrupt not caused by slave event match ..... default
- 1 SMBus interrupt or resume event caused by slave cycle event match of the SMBus Slave Command Register at PCI Function 3 Configuration Offset 85h (command match) and the SMBus Slave Event Register at SMBus Base + Offset 0Ah (data event match). This bit is only set by hardware and can be cleared by writing a 1 to this bit position.

1 Reserved .....always reads 0

0 Slave Busy ..... **RO**
- 0 SMBus controller slave interface is not processing data ..... default
- 1 SMBus controller slave interface is busy receiving data. None of the other SMBus registers should be accessed if this bit is set.

I/O Offset 02h – SMBus Host Control.....RW

7 Reserved ..... always reads 0

6 Start ..... always reads 0

0 Writing 0 has no effect .....default

1 Start Execution of Command

Writing a 1 to this bit causes the SMBus controller host interface to initiate execution of the command programmed in the SMBus Host Command Register (I/O offset 3). All necessary registers should be programmed prior to writing a 1 to this bit. The Host Busy bit (SMBus Host Status Register bit-0) can be used to identify when the SMBus controller has completed command execution.

5 Reserved ..... always reads 0

4-2 SMBus Command Protocol

000 Quick Read or Write .....default

001 Byte Read or Write

010 Byte Data Read or Write

011 Word Data Read or Write

100 Reserved

101 Block Read or Write

110 Reserved

111 Reserved

1 Kill

0 Normal host controller operation .....default

1 Stop the host transaction currently in progress

Setting this bit to 1 also sets the FAILED status bit (Host Status bit-4) and asserts the interrupt selected by the SMB Interrupt Select bit (Function 3 SMBus Host Configuration Register Rx84[1]).

0 Interrupt Enable

0 Disable interrupt generation .....default

1 Enable generation of interrupts on the completion of the current host transaction.

I/O Offset 03h – SMBus Host Command..... RW

7-0 SMBUS Host Command .....default = 0

This field contains the data transmitted in the command field of the SMBus host transaction.

I/O Offset 04h – SMBus Host Address..... RW

The contents of this register are transmitted in the address field of the SMBus host transaction.

7-1 SMBUS Address .....default = 0

This field contains the 7-bit address of the targeted slave device.

0 SMBUS Read or Write .....default = 0

0 Execute a WRITE command ..... default

1 Execute a READ command

I/O Offset 05h – SMBus Host Data 0 ..... RW

The contents of this register are transmitted in the Data 0 field of SMBus host transaction writes. On reads, Data 0 bytes are stored here.

7-0 SMBUS Data 0.....default = 0

For Block Write commands, this field is programmed with the block transfer count (a value between 1 and 32). Counts of 0 or greater than 32 are undefined. For Block Read commands, the count received from the SMBus device is stored here.

I/O Offset 06h – SMBus Host Data 1 ..... RW

The contents of this register are transmitted in the Data 1 field of SMBus host transaction writes. On reads, Data 1 bytes are stored here.

7-0 SMBUS Data 1.....default = 0

I/O Offset 07h – SMBus Block Data ..... RW

Reads and writes to this register are used to access the 32-byte block data storage array. An internal index pointer is used to address the array. It is reset to 0 by reads of the SMBus Host Control register (I/O Offset 2) and incremented automatically by each access to this register. The transfer of block data into (read) or out of (write) this storage array during an SMBus transaction always starts at index address 0.

7-0 SMBUS Block Data .....default = 0

I/O Offset 08h – SMBus Slave Control.....RW

7-4 Reserved ..... always reads 0

3 SMBus Alert Enable

0 Disable .....default

1 Enable generation of an interrupt or resume event on the assertion of the SMBALERT# signal

2 SMBus Shadow Port 2 Enable

0 Disable .....default

1 Enable generation of an interrupt or resume event on external SMBus master generation of a transaction with an address that matches the SMBus Slave Shadow Port 2 register (PCI function 3 configuration register Rx87).

1 SMBus Shadow Port 1 Enable

0 Disable .....default

1 Enable generation of an interrupt or resume event on external SMBus master generation of a transaction with an address that matches the SMBus Slave Shadow Port 1 register (PCI function 3 configuration register Rx86).

0 SlaveEnable

0 Disable .....default

1 Enable generation of an interrupt or resume event on external SMBus master generation of a transaction with an address that matches the SMBus host controller slave port of 10h, a command field which matches the SMBus Slave Command register (PCI function 3 configuration register Rx85), and a match of one of the corresponding enabled events in the SMBus Slave Event Register (I/O Offset 0Ah).

I/O Offset 09h – SMBus Shadow Command ..... RO

This register is used to store command values for external SMBus master accesses to the host slave and slave shadow ports.

7-0 Shadow Command.....default = 0

This field contains the command value which was received during an external SMBus master access whose address field matched the host slave address (10h) or one of the slave shadow port addresses.

I/O Offset 0Ah – SMBus Slave Event .....RW

This register is used to enable generation of interrupt or resume events for accesses to the host controller's slave port.

15-0 SMBus Slave Event..... default = 0
This field contains data bits used to compare against incoming data to the SMBus Slave Data Register (I/O Offset 0Ch). When a bit in this register is set and the corresponding bit the Slave Data register is also set, an interrupt or resume event will be generated if the command value matches the value in the SMBus Slave Command register and the access was to SMBus host address 10h.

I/O Offset 0Ch – SMBus Slave Data ..... RO

This register is used to store data values for external SMBus master accesses to the shadow ports or the SMBus host controller's slave port.

15-0 SMBus Slave Data.....default = 0
This field contains the data value which was transmitted during an external SMBus master access whose address field matched one of the slave shadow port addresses or the SMBus host controller slave port address of 10h.

Power Management I/O-Space Registers

Basic Power Management Control and Status

I/O Offset 1-0 - Power Management Status .....RWC

The bits in this register are set only by hardware and can be reset by software by writing a one to the desired bit position.

15 **Wakeup Status** (WAK_STS) ..... default = 0
This bit is set when the system is in the suspend state and an enabled resume event occurs. Upon setting this bit, the system automatically transitions from the suspend state to the normal working state (from C3 to C0 for the processor).

14-12 **Reserved** ..... always reads 0

11 **Power Status** (PWR_STS)..... default = 0
This bit is set by abnormal power off.

10 **RTC Status** (RTC_STS) ..... default = 0
This bit is set when the RTC generates an alarm (on assertion of the RTC IRQ signal).

9 **Sleep Button Status** (SB_STS)..... default = 0
This bit is set when the sleep button (SLPBTN# / GPI13) is pressed.

8 **Power Button Status** (PB_STS)..... default = 0
This bit is set when the PWRBTN# signal is asserted LOW. If the PWRBTN# signal is held LOW for more than four seconds, this bit is cleared and the system will transition into the soft off state.

7-6 **Reserved** ..... always reads 0

5 **Global Status** (GBL_STS)..... default = 0
This bit is set by hardware when BIOS_RLS is set (typically by an SMI routine to release control of the SCI/SMI lock). When this bit is cleared by software (by writing a one to this bit position) the BIOS_RLS bit is also cleared at the same time by hardware.

4 **Bus Master Status** (BM_STS) ..... default = 0
This bit is set when a system bus master requests the system bus. All PCI master, ISA master and ISA DMA devices are included.

3-1 **Reserved** ..... always reads 0

0 **Timer Carry Status** (TMR_STS)..... default = 0
The bit is set when the 23rd (31st) bit of the 24 (32) bit ACPI power management timer changes.

I/O Offset 3-2 - Power Management Enable ..... RW

The bits in this register correspond to the bits in the Power Management Status Register at offset 1-0.

15 **Reserved** .....always reads 0

14-11 **Reserved** .....always reads 0

10 **RTC Enable** (RTC_EN).....default = 0
This bit may be set to trigger either an SCI or an SMI (depending on the setting of the SCI_EN bit) to be generated when the RTC_STS bit is set.

9 **Sleep Button Enable** (SB_EN) .....default = 0
This bit may be set to trigger either an SCI or SMI when the SB_STS bit is set.

8 **Power Button Enable** (PB_EN) ..... **default = 1**
This bit may be set to trigger either an SCI or an SMI (depending on the setting of the SCI_EN bit) to be generated when the PB_STS bit is set.

7-6 **Reserved** .....always reads 0

5 **Global Enable** (GBL_EN).....default = 0
This bit may be set to trigger either an SCI or an SMI (depending on the setting of the SCI_EN bit) to be generated when the GBL_STS bit is set.

4 **Reserved** .....always reads 0

3-1 **Reserved** .....always reads 0

0 **ACPI Timer Enable** (TMR_EN) .....default = 0
This bit may be set to trigger either an SCI or an SMI (depending on the setting of the SCI_EN bit) to be generated when the TMR_STS bit is set.

I/O Offset 5-4 - Power Management Control .....RW

15-14 Reserved ..... always reads 0

13 Sleep Enable (SLP_EN)..... always reads 0
This is a write-only bit; reads from this bit always return zero. Writing a one to this bit causes the system to sequence into the sleep (suspend) state defined by the SLP_TYP field.

12-10 Sleep Type (SLP_TYP)
- 000 Normal On
- 001 Suspend to DRAM
- 010 Suspend to Disk (also called Soft Off). The VCC power plane is turned off while the VCCSUS and VCCRTC planes remain on.
- 011 Reserved
- 100 Power On Suspend without Reset
- 101 Power On Suspend with CPU Reset
- 110 Power On Suspend with CPU/PCI Reset
- 111 Reserved

In any sleep state, there is minimal interface between powered and non-powered planes so that the effort for hardware design may be well managed.

9-3 Reserved ..... always reads 0

2 Global Release (GBL_RLS) ..... **WO**, default = 0
This bit is set by ACPI software to indicate the release of the SCI / SMI lock. Upon setting of this bit, the hardware automatically sets the BIOS_STS bit. The bit is cleared by hardware when the BIOS_STS bit is cleared by software. Note that the setting of this bit will cause an SMI to be generated if the BIOS_EN bit is set (bit-5 of the Global Enable register at offset 2Ah).

1 Bus Master Reload (BMS_RLD)..... default = 0
This bit is used to enable the occurrence of a bus master request to transition the processor from the C3 state to the C0 state.

0 SCI Enable (SCI_EN)..... default = 0
Selects the power management event to generate either an SCI or SMI:
- 0 Generate SMI
- 1 Generate SCI

Note that certain power management events can be programmed individually to generate an SCI or SMI independent of the setting of this bit (refer to the General Purpose SCI Enable and General Purpose SMI Enable registers at offsets 22 and 24). Also, TMR_STS & GBL_STS always generate SCI and BIOS_STS always generates SMI.

I/O Offset 0B-08 - Power Management Timer..... RW

31-24 Extended Timer Value (ETM_VAL)
This field reads back 0 if the 24-bit timer option is selected (Rx41 bit-3).

23-0 Timer Value (TMR_VAL)
This read-only field returns the running count of the power management timer. This is a 24/32-bit counter that runs off a 3.579545 MHz clock, and counts while in the S0 (working) system state. The timer is reset to an initial value of zero during a reset, and then continues counting until the 14.31818 MHz input to the chip is stopped. If the clock is restarted without a reset, then the counter will continue counting from where it stopped.

Processor Power Management Registers

I/O Offset 13-10 - Processor & PCI Bus Control.....RW

31-12 Reserved ..... always reads 0

11 PCI Stop (PCISTP# asserted) when PCKRUN# is Deasserted (PCI_STP)

0 Enable.....default
1 Disable

10 PCI Bus Clock Run Without Stop (PCI_RUN)

0 PCKRUN# will be de-activated after the PCI bus is idle for 26 clocks.....default
1 PCKRUN# is always asserted

9 Host Clock Stop Enable (HOST_STP)

0 STPCLK# will be asserted in the C3 state, but the CPU clock is not stopped .....default
1 CPU clock is stopped in the C3 state

8 Assertion of SLP# for LVL3 Read

0 Disable .....default
1 Enable

Used in Slot-1 systems only.

7-5 Reserved ..... always reads 0

4 Throttling Enable (THT_EN).
Setting this bit starts clock throttling (modulating the STPCLK# signal) regardless of the CPU state. The throttling duty cycle is determined by bits 3-0 of this register.

3-0 Throttling Duty Cycle (THT_DTY)
This 4-bit field determines the duty cycle of the STPCLK# signal when the system is in throttling mode (the "Throttling Enable" bit is set to one). The duty cycle indicates the percentage of time the STPCLK# signal is asserted while the Throttling Enable bit is set. The field is decoded as follows:

0000 Reserved
0001 0-6.25%
0010 6.25-12.50%
0011 18.75-25.00%
0100 31.25-37.50%
0101 37.50-43.75%
0110 43.75-50.00%
0111 50.00-56.25%
1000 56.25-62.50%
1001 62.50-68.75%
1010 68.75-75.00%
1011 75.00-87.50%
1100 75.00-81.25%
1101 81.25-87.50%
1110 87.50-93.75%
1111 93.75-100%

I/O Offset 14 - Processor Level 2 (P_LVL2)..... RO

7-0 Level 2 .....always reads 0
Reads from this register put the processor into the Stop Grant state (the VT82C596B asserts STPCLK# to suspend the processor). Wake up from Stop Grant state is by interrupt (INTR, SMI, and SCI).

Reads from this register return all zeros; writes to this register have no effect.

I/O Offset 15 - Processor Level 3 (P_LVL3)..... RO

7-0 Level 3 .....always reads 0
Reads from this register put the processor in the C3 clock state with the STPCLK# signal asserted. If Rx10[9] = 1 then the CPU clock is also stopped by asserting CPUSTP#. Wake up from the C3 state is by interrupt (INTR, SMI, and SCI).

Reads from this register return all zeros; writes to this register have no effect.

General Purpose Power Management Registers

I/O Offset 21-20 - General Purpose Status (GP_STS). RWC

15 Reserved ..... always reads 0

14 USB Wakeup Status for STR/STD/Soff (UW_STS)

13 Reserved ..... always reads 0

12 Battery Low Status (BL_STS)
This bit is set when the BATLOW# input is asserted low.

11 Notebook Lid Status (LID_STS)
This bit is set when the LID input detects the edge selected by Rx2C bit-7 (0=rising, 1=falling).

10 Thermal Detect Status (THRM_STS)
This bit is set when the THRM# input detects the edge selected by Rx2C bit-6 (0=rising, 1=falling).

9 USB Resume Status (USB_STS)
This bit is set when a USB peripheral generates a resume event.

8 Ring Status (RI_STS)
This bit is set when the RI# input is asserted low.

7 EXTSMI7 Toggle Status (XSMI7_STS)
This bit is set when the GPI17 pin is toggled.

6 EXTSMI6 Toggle Status (XSMI6_STS)
This bit is set when the GPI16 pin is toggled.

5 EXTSMI5 Toggle Status (XSMI5_STS)
This bit is set when the GPI15 pin is toggled.

4 EXTSMI4 Toggle Status (XSMI4_STS)
This bit is set when the GPI4 pin is toggled.

3 EXTSMI3 Toggle Status (XSMI3_STS)
This bit is set when the GPI3 pin is toggled.

2 EXTSMI2 Toggle Status (XSMI2_STS)
This bit is set when the GPI2 pin is toggled.

1 PME# Status (PME_STS)
This bit is set when the GPI1 pin is asserted high.

0 EXTSMI# Status (EXT_STS)
This bit is set when the EXTSMI# pin is asserted low.

Note that the above bits correspond one for one with the bits of the General Purpose SCI Enable and General Purpose SMI Enable registers at offsets 22 and 24: an SCI or SMI is generated if the corresponding bit of the General Purpose SCI or SMI Enable registers, respectively, is set to one.

The above bits are set by hardware only and can only be cleared by writing a one to the desired bit.

I/O Offset 23-22 - General Purpose SCI Enable ..... RW

15 Reserved ..... always reads 0

14 Enable SCI on setting of the UW_STS bit ..... def=0

13 Reserved ..... always reads 0

12 Enable SCI on setting of the BL_STS bit ..... def=0

11 Enable SCI on setting of the LID_STS bit ..... def=0

10 Enable SCI on setting of the THRM_STS bit def=0

9 Enable SCI on setting of the USB_STS bit .... def=0

8 Enable SCI on setting of the RI_STS bit ..... def=0

7 Enable SCI on setting of the XSMI7_STS bit def=0

6 Enable SCI on setting of the XSMI6_STS bit def=0

5 Enable SCI on setting of the XSMI5_STS bit def=0

4 Enable SCI on setting of the XSMI4_STS bit def=0

3 Enable SCI on setting of the XSMI3_STS bit def=0

2 Enable SCI on setting of the XSMI2_STS bit def=0

1 Enable SCI on setting of the PME_STS bit.... def=0

0 Enable SCI on setting of the EXT_STS bit .... def=0

These bits allow generation of an SCI using a separate set of conditions from those used for generating an SMI.

I/O Offset 25-24 - General Purpose SMI Enable ..... RW

15 Reserved ..... always reads 0

14 Enable SMI on setting of the UW_STS bit .... def=0

13 Reserved ..... always reads 0

12 Enable SMI on setting of the BL_STS bit ..... def=0

11 Enable SMI on setting of the LID_STS bit .... def=0

10 Enable SMI on setting of the THRM_STS bit def=0

9 Enable SMI on setting of the USB_STS bit ... def=0

8 Enable SMI on setting of the RI_STS bit ..... def=0

7 Enable SMI on setting of the XSMI7_STS bit def=0

6 Enable SMI on setting of the XSMI6_STS bit def=0

5 Enable SMI on setting of the XSMI5_STS bit def=0

4 Enable SMI on setting of the XSMI4_STS bit def=0

3 Enable SMI on setting of the XSMI3_STS bit def=0

2 Enable SMI on setting of the XSMI2_STS bit def=0

1 Enable SMI on setting of the PME_STS bit... def=0

0 Enable SMI on setting of the EXT_STS bit.... def=0

These bits allow generation of an SMI using a separate set of conditions from those used for generating an SCI.

Generic Power Management Registers

I/O Offset 29-28 - Global Status.....RWC

- **15 GPIO Range 1 Access Status (GP_R1_STS)**.. def=0
- **14 GPIO Range 0 Access Status (GP_R0_STS)**.. def=0
- **13 GP3 Timer Timeout Status (GP3_TO_STS)**.. def=0
- **12 GP2 Timer Timeout Status (GP3_TO_STS)**.. def=0
- **11 SerIRQ SMI Status (SIRQ_SM_STS)**..... def=0
- **10-9 Reserved** ..... always reads 0
- **8 PCKRUN# Resume Status (PR_RSM_STS)**.. def=0
  This bit is set when PCI bus peripherals wake up the system by asserting PCKRUN#
- **7 Primary IRQ Resume Status (PI_RSM_STS)** def=0
  This bit is set at the occurrence of primary IRQs as defined in Rx45-44 of PCI configuration space
- **6 Software SMI Status (SW_SMI_STS)**..... def=0
  This bit is set when the SMI_CMD port (offset 2F) is written.
- **5 BIOS Status (BIOS_STS)**..... def=0
  This bit is set when the GBL_RLS bit is set to one (typically by the ACPI software to release control of the SCI/SMI lock). When this bit is reset (by writing a one to this bit position) the GBL_RLS bit is reset at the same time by hardware.
- **4 Legacy USB Status (LEG_USB_STS)**..... def=0
  This bit is set when a legacy USB event occurs.
- **3 GP1 Timer Time Out Status (GP1_TO_STS)** def=0
  This bit is set when the GP1 timer times out.
- **2 GP0 Timer Time Out Status (GP0_TO_STS)** def=0
  This bit is set when the GP0 timer times out.
- **1 Secondary Event Timer Time Out Status (ST_TO_STS)**..... def=0
  This bit is set when the secondary event timer times out.
- **0 Primary Activity Status (PACT_STS)**..... def=0
  This bit is set at the occurrence of any enabled primary system activity (see the Primary Activity Detect Status register at offset 30h and the Primary Activity Detect Enable register at offset 34h). After checking this bit, software can check the status bits in the Primary Activity Detect Status register at offset 30h to identify the specific source of the primary event. Note that setting this bit can be enabled to reload the GP0 timer (see bit-0 of the GP Timer Reload Enable register at offset 38).

Note that SMI can be generated based on the setting of any of the above bits (see the offset 2Ah Global Enable register bit descriptions in the right hand column of this page).

The bits in this register are set by hardware only and can only be cleared by writing a one to the desired bit position.

I/O Offset 2B-2A - Global Enable ..... RW

- **15 GPIO Range 1 Access Enable (GP_R1_EN)** ..def=0
- **14 GPIO Range 0 Access Enable (GP_R0_EN)** ..def=0
- **13 GP3 Timer Timeout Enable (GP3_TO_EN)** ..def=0
- **12 GP2 Timer Timeout Enable (GP3_TO_EN)** ..def=0
- **11 SerIRQ SMI Enable (SIRQ_SM_EN)** .....def=0
- **10-9 Reserved** .....always reads 0
- **8 PCKRUN# Resume Enable (PR_RSM_EN)** ..def=0
  This bit may be set to trigger an SMI to be generated when the PR_RSM_STS bit is set.
- **7 Primary IRQ Resume Enable (PI_RSM_EN)** def=0
  This bit may be set to trigger an SMI to be generated when the PI_RSM_STS bit is set.
- **6 Software SMI Enable (SW_SMI_EN)** .....def=0
  This bit may be set to trigger an SMI to be generated when the SW_SMI_STS bit is set.
- **5 BIOS Enable (BIOS_EN)**.....def=0
  This bit may be set to trigger an SMI to be generated when the BIOS_STS bit is set.
- **4 Legacy USB Enable (LEG_USB_EN)**.....def=0
  This bit may be set to trigger an SMI to be generated when the LEG_USB_STS bit is set.
- **3 GP1 Timer Time Out Enable (GP1_TO_EN)** def=0
  This bit may be set to trigger an SMI to be generated when the GP1_TO_STS bit is set.
- **2 GP0 Timer Time Out Enable (GP0_TO_EN)** def=0
  This bit may be set to trigger an SMI to be generated when the GP0_TO_STS bit is set.
- **1 Secondary Event Timer Time Out Enable (ST_TO_EN)**.....def=0
  This bit may be set to trigger an SMI to be generated when the ST_TO_STS bit is set.
- **0 Primary Activity Enable (PACT_EN)** .....def=0
  This bit may be set to trigger an SMI to be generated when the PACT_STS bit is set.

I/O Offset 2D-2C - Global Control (GBL_CTL) .....RW

15-12 Reserved ..... always reads 0

11 IDE Secondary Bus Power Off
- 0 Disable .....default
- 1 Enable

10 IDE Primary Bus Power Off
- 0 Disable .....default
- 1 Enable

9 Reserved ..... always reads 0

8 SMI Active (INSMI)
- 0 SMI Inactive.....default
- 1 SMI Active. If the SMIIG bit is set, this bit needs to be written with a 1 to clear it before the next SMI can be generated.

7 LID Triggering Polarity
- 0 Rising Edge .....default
- 1 Falling Edge

6 THRM# Triggering Polarity
- 0 Rising Edge .....default
- 1 Falling Edge

5 Disable Battery Low Resume
- 0 Enable resume .....default
- 1 Disable resume from suspend when BATLOW# is asserted

4 SMI Lock (SMIIG)
- 0 Disable SMI Lock
- 1 Enable SMI Lock (SMI low to gate for the next SMI) .....default

3 Wait for Halt / Stop Grant Cycle for STPCLK# Assertion
- 0 Don't wait.....default
- 1 Wait

This bit works with Rx4C[7] of PCI configuration space to control the start of STPCLK# assertion.

2 Power Button Triggering
- 0 SCI/SMI generated by PWRBTN# rising edge
- 1 SCI/SMI generated by PWRBTN# low level

Must be set to 1 for ACPI v0.9 compliance.

1 BIOS Release (BIOS_RLS)

This bit is set by legacy software to indicate release of the SCI/SMI lock. Upon setting of this bit, hardware automatically sets the GBL_STS bit. This bit is cleared by hardware when the GBL_STS bit cleared by software.

Note that if the GBL_EN bit is set (bit-5 of the Power Management Enable register at offset 2), then setting this bit causes an SCI to be generated (because setting this bit causes the GBL_STS bit to be set).

0 SMI Enable (SMI_EN)
- 0 Disable all SMI generation
- 1 Enable SMI generation

I/O Offset 2F - SMI Command (SMI_CMD) ..... RW

7-0 SMI Command

Writing to this port sets the SW_SMI_STS bit. Note that if the SW_SMI_EN bit is set (see bit-6 of the Global Enable register at offset 2Ah), then an SMI is generated.

I/O Offset 33-30 - Primary Activity Detect Status.....RWC

These bits correspond to the Primary Activity Detect Enable bits in offset 37-34.

31-11 Reserved .....always read 0

10 Audio Controller Access Status ..... (AUD_STS)
Set if the audio controller is accessed.

9 Keyboard Controller Access Status..... (KBC_STS)
Set if the keyboard controller is accessed via I/O port 60h.

8 VGA Access Status..... (VGA_STS)
Set if the VGA port is accessed via I/O ports 3B0-3DFh or memory space A0000-BFFFFh.

7 Parallel Port Access Status.....(PAR_STS)
Set if the parallel port is accessed via I/.O ports 278-27Fh or 378-37Fh (LPT2 or LPT1).

6 Serial Port B Access Status ..... (COMB_STS)
Set if serial port B is accessed via I/O ports 2F8-2FFh or 2E8-2EFh.

5 Serial Port A Access Status ..... (COMA_STS)
Set if serial port A is accessed via I/O ports 3F8-3FFh or 3E8-3EFh.

4 Floppy Access Status..... (FLP_STS)
Set if the floppy devices are accessed via I/O ports 3F0-3F5h or 3F7h.

3 Secondary IDE Access Status.....(SIDE_STS)
Set if the secondary IDE port is accessed via I/O ports 170-177h or 376h.

2 Primary IDE Access Status ..... (PIDE_STS)
Set if the primary IDE port is accessed via I/O ports 1F0-1F7h or 3F6h.

1 Primary Interrupt Activity Status..... (PIRQ_STS)
Set on the occurrence of a primary interrupt (enabled via the "Primary Interrupt Channel" register at Function 3 PCI configuration register offset 44h).

0 PCI Master Activity Status ..... (PCI_STS)
Set on the occurrence of PCI master activity.

Note: The bits above correspond to the bits of the Primary Activity Detect Enable register at offset 34 (see right hand column of this page): if the corresponding bit is set in that register, setting of the above bits will cause the PACT_STS bit to be set (bit-0 of the Global Status register at offset 28). Setting of PACT_STS may be set up to enable a "Primary Activity Event": an SMI will be generated if PACT_EN is set (bit-0 of the Global Enable register at offset 2Ah) and/or the GP0 timer will be reloaded if the "GP0 Timer Reload on Primary Activity" bit is set (bit-0 of the GP Timer Reload Enable register at offset 38 on this page).

Note: Bits above also correspond to bits of the GP Timer Reload Enable register at offset 38: if the corresponding bit is set in that register, setting the bit in this register will cause the indicated timer to be reloaded.

Bits in this register are set by hardware only and may only be cleared by writing a 1 to the desired bit. All bits default to 0.

I/O Offset 37-34 - Primary Activity Detect Enable..... RW

These bits correspond to the Primary Activity Detect Status bits in offset 33-30.

31-11 Reserved ..... always read 0

10 Audio Controller Status Enable..... (AUD_EN)
0 Don't set PACT_STS if AUD_STS is set .... def
1 Set PACT_STS if AUD_STS is set

9 Keyboard Controller Status Enable ..... (KBC_EN)
0 Don't set PACT_STS if KBC_STS is set..... def
1 Set PACT_STS if KBC_STS is set

8 VGA Status Enable ..... (VGA_EN)
0 Don't set PACT_STS if VGA_STS is set .... def
1 Set PACT_STS if VGA_STS is set

7 Parallel Port Status Enable .....(PAR_EN)
0 Don't set PACT_STS if PAR_STS is set ..... def
1 Set PACT_STS if PAR_STS is set

6 Serial Port B Status Enable .....(COMB_EN)
0 Don't set PACT_STS if COMB_STS is set . def
1 Set PACT_STS if COMB_STS is set

5 Serial Port A Status Enable..... (COMA_EN)
0 Don't set PACT_STS if COMA_STS is set . def
1 Set PACT_STS if COMA_STS is set

4 Floppy Status Enable ..... (FLP_EN)
0 Don't set PACT_STS if FLP_STS is set..... def
1 Set PACT_STS if FLP_STS is set

3 Secondary IDE Status Enable .....(SIDE_EN)
0 Don't set PACT_STS if SIDE_STS is set .... def
1 Set PACT_STS if SIDE_STS is set

2 Primary IDE Status Enable.....(PIDE_EN)
0 Don't set PACT_STS if PIDE_STS is set .... def
1 Set PACT_STS if PIDE_STS is set

1 Primary INTR Status Enable ..... (PIRQ_EN)
0 Don't set PACT_STS if PIRQ_STS is set.... def
1 Set PACT_STS if PIRQ_STS is set

0 PCI Master Status Enable ..... (DRQ_EN)
0 Don't set PACT_STS if PCI_STS is set..... def
1 Set PACT_STS if PCI_STS is set

Note: Setting of any of the above bits also sets the PACT_STS bit (bit-0 of offset 28) which causes the GP0 timer to be reloaded (if PACT_GP0_EN is set) or generates an SMI (if PACT_EN is set).

I/O Offset 3B-38 - GP Timer Reload Enable .....RW

All bits in this register default to 0 on power up.

31-11 Reserved .....always read 0

7 Enable GP1 Timer Reload on KBC Access
1 = setting of KBC_STS causes GP1 timer to reload.

6 Enable GP1 Timer Reload on Serial Port Access
1 = setting of COMA_STS or COMB_STScauses GP1 timer to reload.

5 Reserved .....always read 0

4 Enable GP1 Timer Reload on VGA Access
1 = setting of VGA_STS causes GP1 timer to reload.

3 Enable GP1 Timer Reload on IDE/Floppy Access
1 = setting of FLP_STS, PIDE_STS, or SIDE_STS causes GP1 timer to reload.

2 Ena GP3 Timer Reload on GPIO Range 1 Access
1 = setting of GR1_STS causes GP3 timer to reload.

1 Ena GP2 Timer Reload on GPIO Range 0 Access
1 = setting of GR0_STS causes GP2 timer to reload.

0 Enable GP0 Timer Reload on Primary Activity
1 = setting of PACT_STS causes GP0 timer to reload. Primary activities are enabled via the Primary Activity Detect Enable register (offset 37-34) with status recorded in the Primary Activity Detect Status register (offset 33-30).

General Purpose I/O Registers

I/O Offset 45-44 – External SMI Input Value (EXTSMI_VAL) .....RO

Depending on the configuration, up to 8 external SCI/SMI ports are available as indicated below. The state of these inputs may be read in this register.

15-11 Reserved .....always reads 0
10 Hardware Monitor IRQ Status
9 SMBus IRQ Status
8 SMBus Resume Status
7 RI# (GPI12 Pin) Input Value
6 SMBALRT# (GPI11 Pin) Input Value
5 Reserved .....always reads 0
4 SLPBTN# (GPI13 Pin) Input Value
3 LID (GPI10 Pin) Input Value
2 BATLOW# (GPI9 Pin) Input Value
1 PME# (GPI1 Pin) Input Value
0 EXTSMI# Input Value

I/O Offset 4B-48 - GPI Port Input Value (GPI_VAL).... RO

31-22 Reserved ..... always read 0
21-0 GPI[21-0] Input Value ..... Read Only

I/O Offset 4F-4C - GPO Port Output Value (GPO_VAL)RW

Reads from this register return the last value written (held on chip)

31 Reserved .....always reads 0
30-0 GPO[30-0] Output Value.....default = 7FFFFFFh

FUNCTIONAL DESCRIPTIONS

Power Management

Power Management Subsystem Overview

The power management function of the VT82C596B is indicated in the following block diagram:

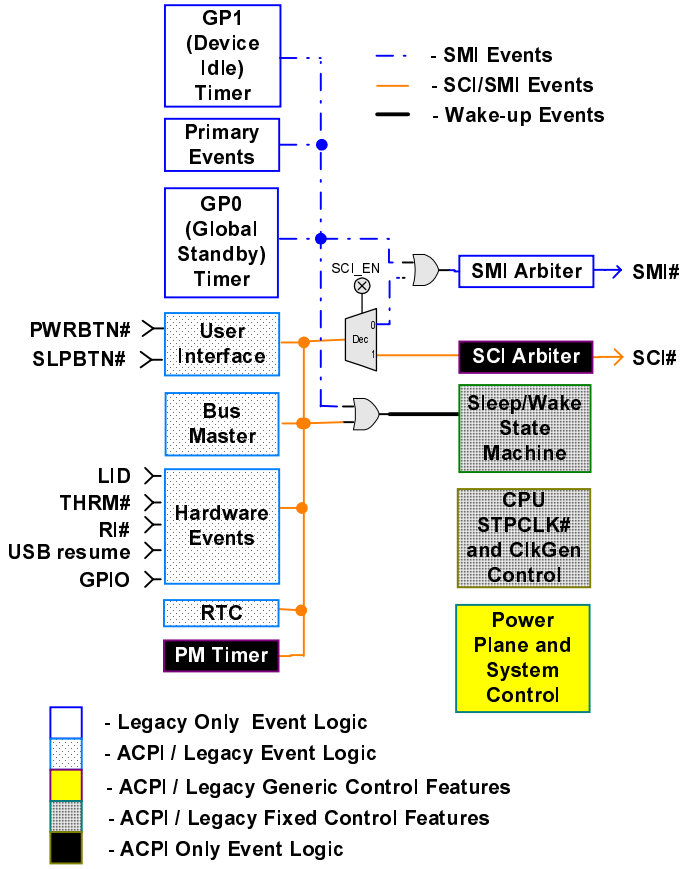


Figure 6. Power Management Subsystem Block Diagram

Refer to ACPI Specification v1.0 and APM specification v1.2 for additional information.

Processor Bus States

The VT82C596B supports the complete set of C0 to C3 processor states as specified in the Advanced Configuration and Power Interface (ACPI) specification (and defined in ACPI I/O space Registers 10-15):

C0: Normal Operation

C1: CPU Halt (controlled by software).

C2: Stop Clock. Entered when the P_LVL2 register is read. The STPCLK# signal is asserted to put the processor in the Stop Grant State. If the SRAM_ZZ bit is set to 1, then the ZZ pin is also asserted (after the acknowledgement of the stop grant bus cycle) for powering down the cache SRAM. The CPUSTP# signal is not asserted so that host clocks remain running. To exit this state, the chip negates the ZZ signal and then negates STPCLK#.

C3: Suspend. Entered when the P_LVL3 register is read. In addition to STPCLK# and ZZ assertion as in the C2 state, the SUSST1# (suspend status 1) signal is asserted to tell the north bridge to switch to "Suspend DRAM Refresh" mode based on the 32KHz suspend clock (SUSCLK) provided by the VT82C596B. If the HOST_STP bit is enabled, then CPUSTP# is also asserted to stop clock generation and put the CPU into Stop Clock State. To exit this state, the chip negates CPUSTP# and allows time for the processor PLL to lock. Then the SUSST1#, ZZ, and STPCLK# signals are negated to resume to normal operation.

During normal operation, two mechanisms are provided to modulate CPU execution and control power consumption by throttling the duty cycle of STPCLK#:

a. Setting the THT_EN bit to 1, the duty cycle defined in THT_DTY (IO space Rx10) is used.

b. THRM# pin assertion enables automatic clock throttling with duty cycle pre-configured in THM_DTY (PCI configuration Rx4C).

System Suspend States and Power Plane Control

There are three power planes inside the VT82C596B. The first power plane (VCCSUS) is always on unless turned off by the mechanical switch. The second power plane (VCC) is controlled by chip output SUSC# (also called "PSON"). The third plane (VCCRTC) is powered by the combination of the VCCSUS and the external battery (VBAT) for the integrated real time clock. Most of the circuitry inside the VT82C596B is powered by VCC. The amount of logic powered by VCCSUS is very small; its main function is to control the supply of VCC and other power planes. VCCRTC is always on unless both the mechanical switch and VBAT are removed.

The VT82C596B supports multiple system suspend states by configuring the SLP_TYP field of ACPI I/O space register Rx4-5:

a) **POS (Power On Suspend):** Most devices in the system remain powered. The host bus is put into an equivalent of the C3 state. In particular, the CPU is put into the Stop Grant State or Stop Clock State depending on the setting of the HOST_STP bit. SUSST1# is asserted to tell the north bridge to switch to "Suspend DRAM Refresh" mode based on the 32KHz SUSCLK provided by the VT82C596B. As to the PCI bus, setting the PCLK_RUN bit to 0 enables the CLKRUN protocol defined in the PCI Mobile Design Guide. That is, the PCKRUN# pin will be de-activated after the PCI bus is idle for 26 clocks. Any PCI bus masters including the north bridge may resume PCI clock operation by pulling the PCKRUN# pin low. During the PCKRUN# de-activation period, the PCISTP# pin may be activated to disable the output of the PCI clock generator if the PCI_STP bit is enabled. When the system resumes from POS, the VT82C496 can optionally resume without resetting the system, can reset the processor only, or can reset the entire system. When no reset is performed, the chip only needs to wait for the clock synthesizer and processor PLL to lock before the system is resumed, which typically takes 20ms.

b) **STR (Suspend to DRAM):** Power is removed from most of the system except the system DRAM. Power is supplied to the suspend refresh logic in the north bridge (VTT of VT82C598AT) and the suspend logic of the VT82C596B (VCCSUS). The VT82C596B provides a 32KHz suspend clock to the north bridge for it to use to continue DRAM refresh.

c) **STD (Suspend to Disk, also called Soft-off):** Power is removed from most of the system except the suspend logic of VT82C596B (VCCSUS).

d) **Mechanical Off:** This is not a suspend state. All power in the system is removed except the RTC battery.

The suspend state is entered by setting the SLP_EN bit to 1. Three power plane control signals (SUSA#, SUSB# and SUSC#) are provided to turn off more system power planes as the system moves to deeper power-down states, i.e., from normal operation to POS (only SUSA# asserted), to STR (both SUSA# and SUSB# asserted), and to STD (all three SUS# signals asserted). In particular, the assertion of SUSC# can be used to turn off the VCC supply to the VT82C596B.

Two suspend status indicators (SUSST1-2#) are provided to inform the north bridge and the rest of the system of the processor and system suspend states. SUSST2# is asserted when the system enters any suspend state. SUSST1# is asserted when the system enters the suspend state or the processor enters the C3 state. SUSST1# is connected to the north bridge to switch between normal and suspend-DRAM-refresh modes.

General Purpose I/O Ports

As ACPI compliant hardware, the VT82C596B includes PWRBTN#, SLPBTN#, and RI# pins to implement power button, sleep button, and ring indicator functionality, respectively. Furthermore, the VT82C596B offers many general-purpose I/O ports with the following capabilities:

- **I^2C/SMB Support**
- **Thermal Detect**
- **Notebook Lid Open/Close Detect**
- **Battery Low Detect**
- **Twenty-two General Purpose Input Ports** (10 dedicated and 12 multiplexed with other functions).
- **Thirty-one General Purpose Output Ports** (6 dedicated and 25 multiplexed with other functions)

In addition, the VT82C596B provides eight external SMI pins (one dedicated EXTSMI# pin and seven pins shared with general purpose input pins). Once enabled, each of the external SMI inputs triggers an SCI or SMI at both the rising and falling edges of the corresponding input signal. Software can check the status of the input pins and take appropriate actions.

Power Management Events

Three types of power management events are supported:

1) **ACPI-required Fixed Events** defined in the PM1a_STS and PM1a_EN registers. These events can trigger either SCI or SMI depending on the SCI_EN bit:
   - PWRBTN# Triggering
   - RTC Alarm
   - Sleep Button
   - ACPI Power Management Timer Carry (always SCI)
   - BIOS Release (always SCI)

2) **ACPI-aware General Purpose Function Events** defined in the GP_STS and GP_SCI_EN, and GP_SMI_EN registers. These events can trigger either SCI or SMI depending on the setting of individual SMI and SCI enable bits:
   - External SMI triggering
   - USB Resume
   - Ring Indicator (RI#)
   - Battery Low Detect (BATLOW#)
   - Notebook Lid Open/Close Detect (LID)
   - Thermal Detect (THRM#)

3) **Generic Global Events** defined in the GBL_STS and GBL_EN registers. These registers are mainly used for SMI:
   - PCI Bus Clock Run Resume
   - Primary Interrupt Occurance
   - GP0 and GP1 Timer Time Out
   - Secondary Event Timer Time Out
   - Occurrence of Primary Events (defined in register PACT_STS and PACT_EN)
   - Legacy USB accesses (keyboard and mouse)
   - Software SMI

System and Processor Resume Events

Depending on the system suspend state, different features can be enabled to resume the system. There are two classes of resume events:

a) VCCSUS-based events. Event logic resides in the VCCSUS plane and thus can resume the system from any suspend state. Such events include PWRBTN#, RI#, BATLOW#, LID, SMBus resume event, RTC alarm, EXTSMI#, and GP1 (EXTSMI1#).

b) VCC-Based Events. Event logic resides in the VCC plane and thus can only resume the system from the POS state. Such events include the ACPI PM timer, USB resume, and EXTSMI2-7#.

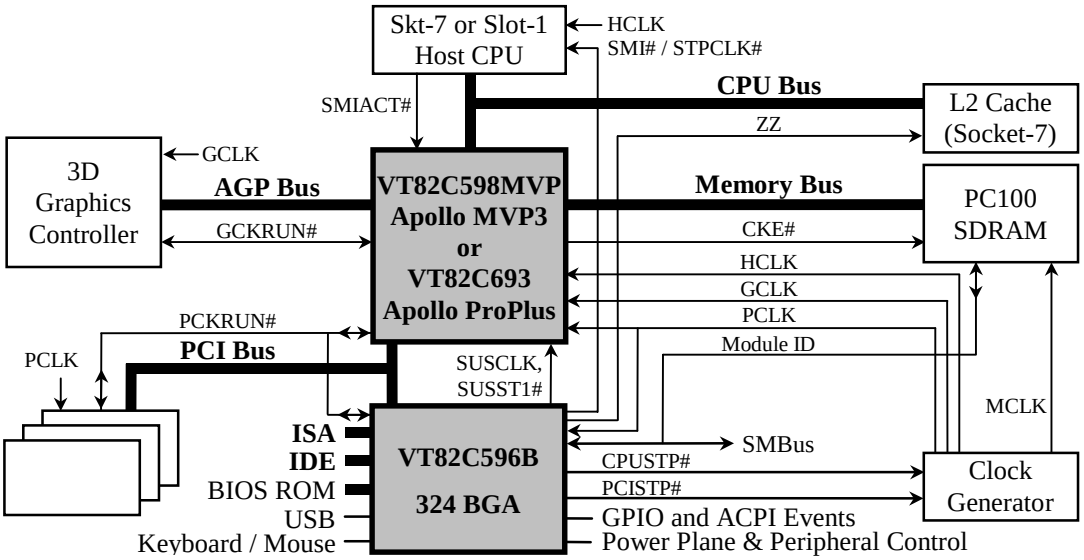


Figure 7. Apollo MVP3 System Block Diagram Using the VT82C596B South Bridge

Legacy Power Management Timers

In addition to the ACPI power management timer, the VT82C596B includes the following four legacy power management timers:

GP0 Timer: general purpose timer with primary event

GP1 Timer: general purpose timer with peripheral event reload

Secondary Event Timer: to monitor secondary events

Conserve Mode Timer: Hardware-controlled return to standby

The normal sequence of operations for a general purpose timer (GP0 or GP1) is to

1) First program the time base and timer value of the initial count (register GP_TIM_CNT).
2) Then activate counting by setting the GP0_START or GP1_START bit to one: the timer will start with the initial count and count down towards 0.
3) When the timer counts down to zero, an SMI will be generated if enabled (GP0TO_EN and GP1TO_EN in the GBL_EN register) with status recorded (GP0TO_STS and GP1TO_STS in the GBL_STS register).
4) Each timer can also be programmed to reload the initial count and restart counting automatically after counting down to 0. This feature is not used in standard VIA BIOS.

The GP0 and GP1 timers can be used just as the general purpose timers described above. However, they can also be programmed to reload the initial count by system primary events or peripheral events thus used as primary event (global standby) timer and peripheral timer, respectively. The secondary event timer is solely used to monitor secondary events.

System Primary and Secondary Events

Primary system events are distinguished in the PRI_ACT_STS and PRI_ACT_EN registers:

Bit	Event	Trigger
7	**Keyboard Access**	I/O port 60h
6	**Serial Port Access**	I/O ports 3F8h-3FFh, 2F8h-2FFh, 3E8h-3EFh, or 2E8h-2EFh
5	**Parallel Port Access**	I/O ports 378h-37Fh or 278h-27Fh
4	**Video Access**	I/O ports 3B0h-3DFh or memory A/B segments
3	**IDE/Floppy Access**	I/O ports 1F0h-1F7h, 170h-177h, or 3F5h
2	**Reserved**	
1	**Primary Interrupts**	Each channel of the interrupt controller can be programmed to be a primary or secondary interrupt
0	**ISA Master/DMA Activity**	

Each category can be enabled as a primary event by setting the corresponding bit of the PRI_ACT_EN register to 1. If enabled, the occurrence of the primary event reloads the GP0 timer if the PACT_GP0_EN bit is also set to 1. The cause of the timer reload is recorded in the corresponding bit of PRI_ACT_STS register while the timer is reloaded. If no enabled primary event occurs during the count down, the GP0 timer will time out (count down to 0) and the system can be programmed (setting the GP0TO_EN bit in the GBL_EN register to one) to trigger an SMI to switch the system to a power down mode.

The VT82C596B distinguishes two kinds of interrupt requests as far as power management is concerned: the primary and secondary interrupts. Like other primary events, the occurrence of a primary interrupt demands that the system be restored to full processing capability. Secondary interrupts, however, are typically used for housekeeping tasks in the background unnoticeable to the user. The VT82C596B allows each channel of interrupt request to be declared as either primary, secondary, or ignorable in the PIRQ_CH and SIRQ_CH registers. Secondary interrupts are the only system secondary events defined in the VT82C596B.

Like primary events, primary interrupts can be made to reload the GP0 timer by setting the PIRQ_EN bit to 1. Secondary interrupts do not reload the GP0 timer. Therefore the GP0 timer will time out and the SMI routine can put the system into power down mode if no events other than secondary interrupts are happening periodically in the background.

Primary events can be programmed to trigger an SMI (setting of the PACT_EN bit). Typically, this SMI triggering is turned off during normal system operation to avoid degrading system performance. Triggering is turned on by the SMI routine before entering the power down mode so that the system may be returned to normal operation at the occurrence of primary events. At the same time, the GP0 timer is reloaded and the count down process is restarted.

Peripheral Events

Primary and secondary events define system events in general and the response is typically expressed in terms of system events. Individual peripheral events can also be monitored by the VT82C596B through the GP1 timer. The following four categories of peripheral events are distinguished (via register GP_RLD_EN):

Bit-7 **Keyboard Access**
Bit-6 **Serial Port Access**
Bit-4 **Video Access**
Bit-3 **IDE/Floppy Access**

The four categories are subsets of the primary events as defined in PRI_ACT_EN and the occurrence of these events can be checked through a common register PRI_ACT_STS. As a peripheral timer, GP1 can be used to monitor one (or more than one) of the above four device types by programming the corresponding bit to one and the other bits to zero. Time out of the GP1 timer indicates no activity of the corresponding device type and appropriate action can be taken as a result.

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Min	Max	Unit
Ambient operating temperature	0	70	^{o}C
Storage temperature	-55	125	^{o}C
Input voltage	-0.5	5.5	Volts
Output voltage (V_{CC} = 5V)	-0.5	5.5	Volts
Output voltage (V_{CC} = 3.1 - 3.6V)	-0.5	V_{CC} + 0.5	Volts

Note: Stress above the conditions listed may cause permanent damage to the device. Functional operation of this device should be restricted to the conditions described under operating conditions.

DC Characteristics

TA-0-70^{o}C, V_{CC}=5V+/-5%, GND=0V

Symbol	Parameter	Min	Max	Unit	Condition
V_{IL}	Input low voltage	-0.50	0.8	V	
V_{IH}	Input high voltage	2.0	V_{CC}+0.5	V	
V_{OL}	Output low voltage	-	0.45	V	I_{OL}=4.0mA
V_{OH}	Output high voltage	2.4	-	V	I_{OH}=-1.0mA
I_{IL}	Input leakage current	-	+/-10	uA	$0<V_{IN}<V_{CC}$
I_{OZ}	Tristate leakage current	-	+/-20	uA	$0.45<V_{OUT}<V_{CC}$
I_{CC}	Power supply current	-	80	mA	

AC Timing Specifications

Table 6. AC Characteristics - PCI Cycle Timing

	Parameter	Min	Max	Unit	Notes
T_S	AD[31:0] Setup Time to PCLK Rising	7		ns	
T_S	FRAME#,TRDY#,IRDY# Setup Time to PCLK Rising	7		ns	
T_S	CBE[3:0]#, STOP#,DEVSEL# Setup Time to PCLK Rising	7		ns	
T_S	PGNT# Setup Time to PCLK Rising	12		ns	
T_H	AD[31:0] Hold Time from PCLK Rising	0		ns	
T_H	FRAME#,TRDY#,IRDY# Hold Time from PCLK Rising	0		ns	
T_H	CBE[3:0]#, STOP#,DEVSEL# Hold Time from PCLK Rising	0		ns	
T_H	PGNT# Hold Time from PCLK Rising	0		ns	
T_{VD}	AD[31:0] Valid Delay from PCLK Rising (address phase)	2	11	ns	0pf on min, 50pf on max
T_{VD}	AD[31:0] Valid Delay from PCLK Rising (data phase)	2	11	ns	0pf on min, 50pf on max
T_{VD}	FRAME#,TRDY#,IRDY# Valid Delay from PCLK Rising	2	11	ns	0pf on min, 50pf on max
T_{VD}	CBE[3:0]#, STOP#,DEVSEL# Valid Delay from PCLK Rising	2	11	ns	0pf on min, 50pf on max
T_{VD}	PREQ# Valid Delay from PCLK Rising	2	12	ns	0pf on min, 50pf on max
T_{FD}	FRAME#,TRDY#,IRDY# Float Delay from PCLK Rising		28	ns	0pf on min, 50pf on max
T_{FD}	CBE[3:0]#, STOP#,DEVSEL# Float Delay from PCLK Rising		28	ns	0pf on min, 50pf on max

Table 7. AC Characteristics - UltraDMA-33 IDE Bus Interface Timing

Symbol	Description	Timing	Unit
T_{ENV1}	Envelope time for read initial	29.3	ns
T_{DS1}	Data setup time for read initial	1.1	ns
T_{DH1}	Data hold time for read initial (rise)	2.3	ns
T_{ENV2}	Envelope time for write initial (rise)	29.3	ns
T_{DVS2}	Data setup time for write initial (fall)	42.2	ns
T_{DVH2}	Data hold time for write initial (fall)	17.8	ns
T_{DVS2}	Data setup time for write initial	42.0	ns
T_{DVH2}	Data hold time for write initial	17.2	ns
T_{RFS}	READY to final STROBE time	21.3	ns
T_{RP}	READY to Pause time	180.0	ns
T_{LI4}	Limited interlock time (to STOP)	95.1	ns
T_{LI4}	Limited interlock time (to Host DMARDY)	125.3	ns
T_{ZA4}	Delay time required for output drives turning on	102.0	ns
T_{DVS4}	Data setup time for read terminating	55.3	ns
T_{DVH4}	Data hold time for read terminating	31.6	ns
T_{LI5}	Limited interlock time (to STOP)	125.3	ns
T_{LI5}	Limited interlock time (to Host STROBE)	95.2	ns
T_{MIL5}	Limited interlock time with minimum	120.6	ns
T_{DVS5}	Data setup time for write terminating	57.7	ns
T_{DVH5}	Data hold time for write terminating	31.8	ns
T_{MIL6}	Limited interlock time with minimum	155.8	ns
T_{ZA6}	Delay time required for output drives turning on	68.5	ns
T_{LI5}	Limited interlock time	65.2	ns
T_{MIL5}	Limited interlock time with minimum	90.6	ns
T_2	Delay time of PCLK to DCS3,1#	4.8	ns
T_3	Delay time of PCLK to DA[2:0]	5.3	ns
T_4	Delay time of PCLK to DIOW#	9.3	ns
T_5	Delay time of PCLK to DIOR#	9.2	ns
T_{WDS}	Data setup time during PIO write	85.5	ns
T_{WDH}	Data hold time during PIO write	31.7	ns
T_{RDS}	Data setup time during PIO read	0.4	ns
T_{RDH}	Data hold time during PIO read	2.1	ns

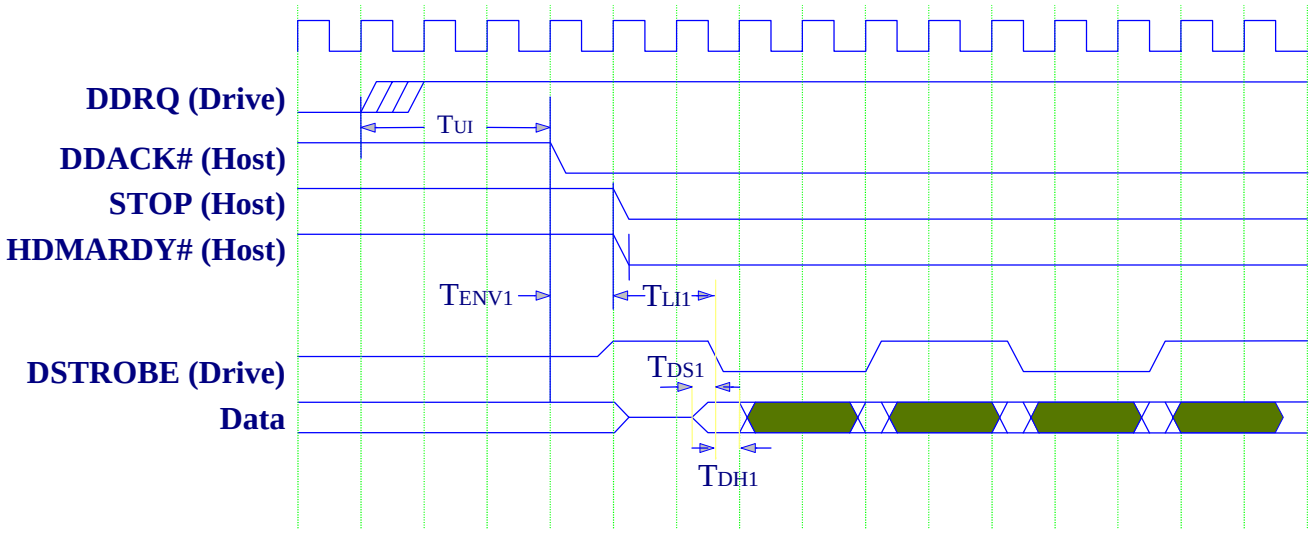


Figure 8. UltraDMA-33 IDE Timing - Drive Initiating DMA Burst for Read Command

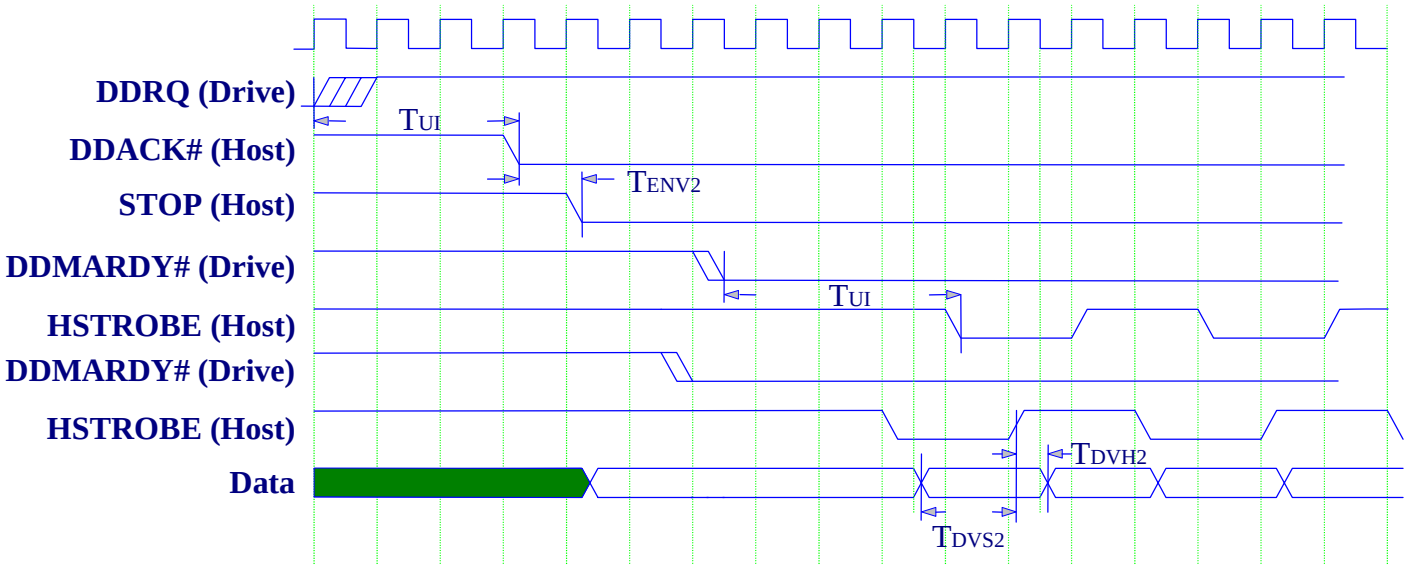


Figure 9. UltraDMA-33 IDE Timing - Drive Initiating Burst for Write Command

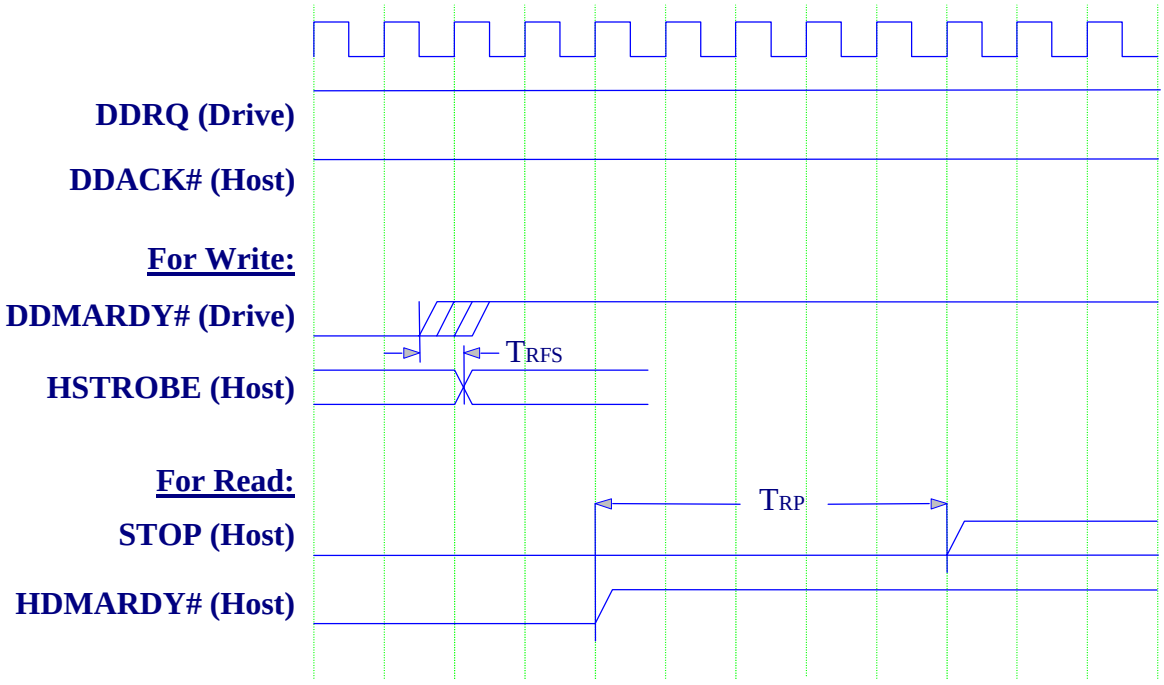


Figure 10. UltraDMA-33 IDE Timing - Pausing a DMA Burst

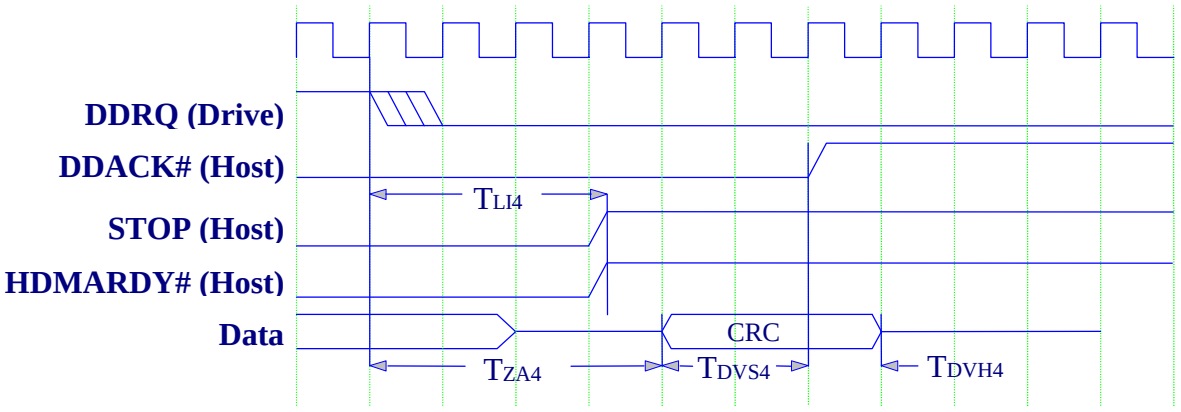


Figure 11. UltraDMA-33 IDE Timing - Drive Terminating DMA Burst During Read Command

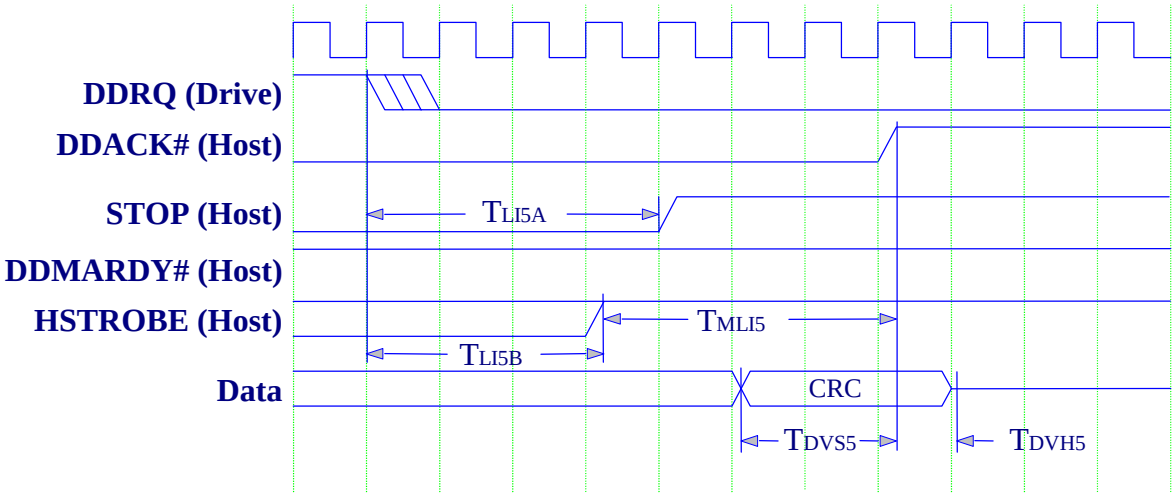


Figure 12. UltraDMA-33 IDE Timing - Drive Terminating DMA Burst During Write Command

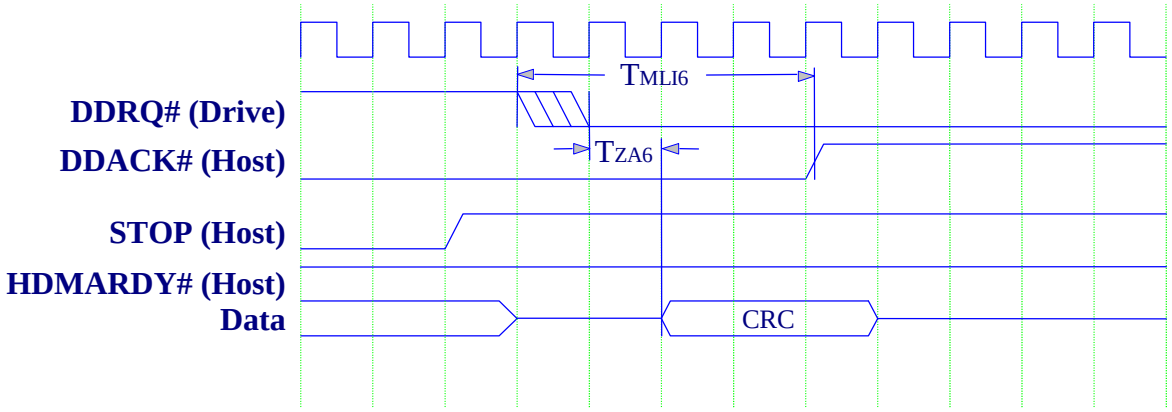


Figure 13. UltraDMA-33 IDE Timing - Host Terminating DMA Burst During Read Command

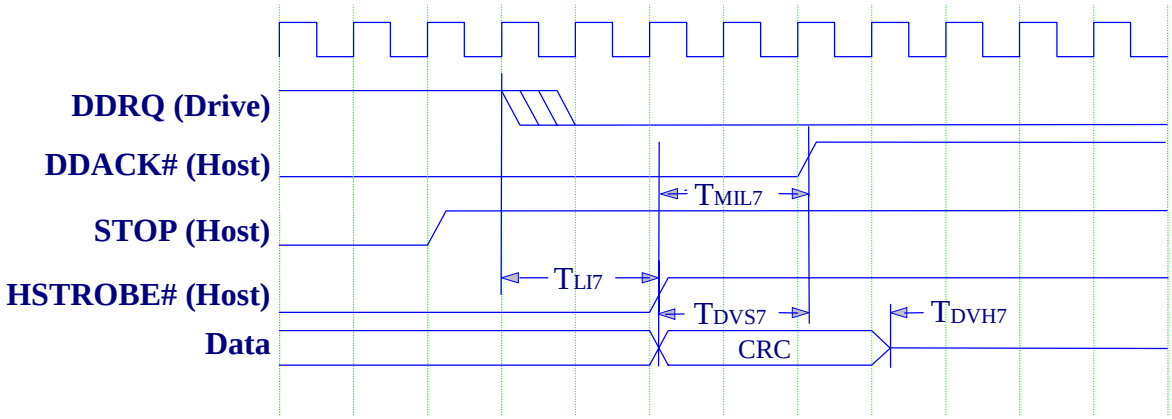


Figure 14. UltraDMA-33 IDE Timing - Host Terminating DMA Burst During Write Command

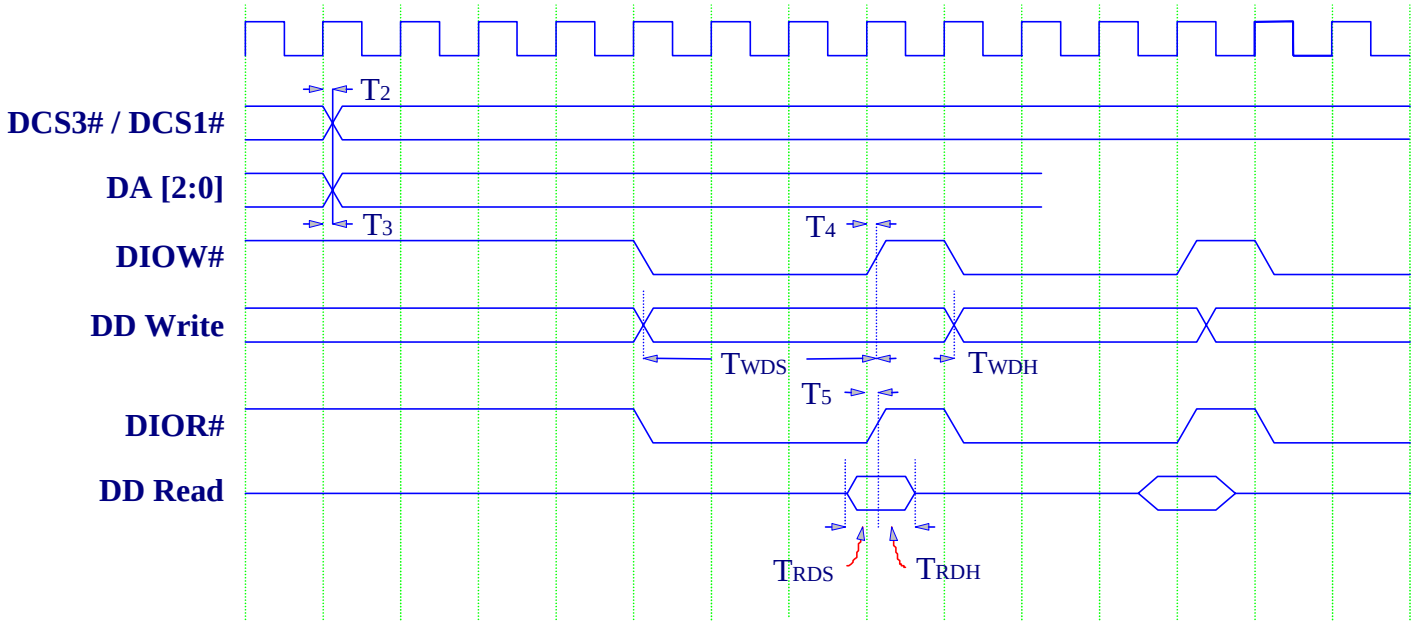


Figure 15. UltraDMA-33 IDE Timing - PIO Cycle

PACKAGE MECHANICAL SPECIFICATIONS

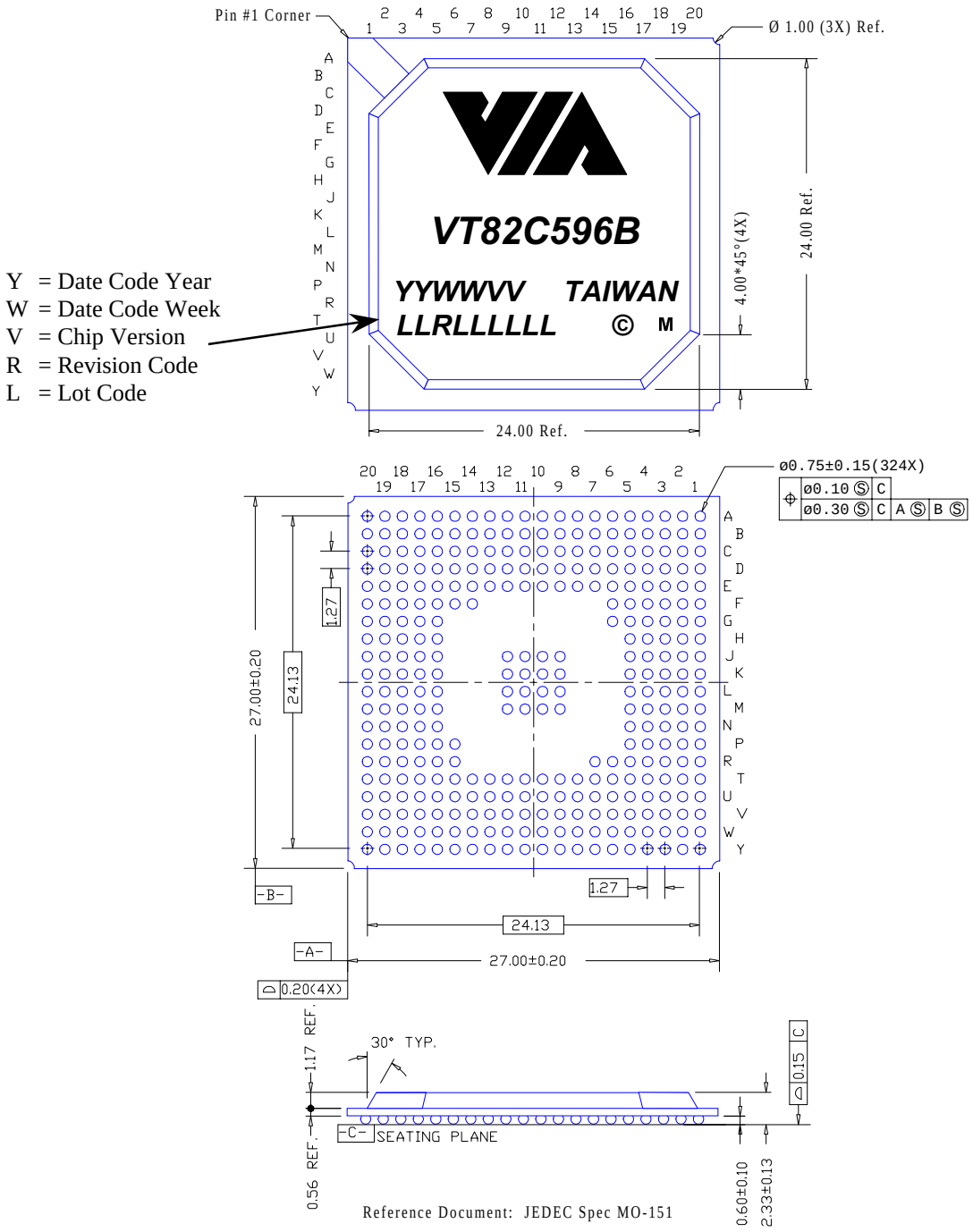


Figure 16. Mechanical Specifications - 324-Pin Ball Grid Array Package