HMC745LC3

13 Gbps, FAST RISE TIME XOR / XNOR GATE w/ PROGRAMMABLE OUTPUT VOLTAGE & POSITIVE SUPPLY

Typical Applications

The HMC745LC3 is ideal for:

- RF ATE Applications
- Broadband Test & Measurement
- Serial Data Transmission up to 13 Gbps
- Digital Logic Systems up to 13 GHz

Features

Inputs Terminated Internally in 50 Ohms

Differential & Singe-Ended Operation

Fast Rise and Fall Times: 21 / 19 ps

Low Power Consumption: 240 mW typ.

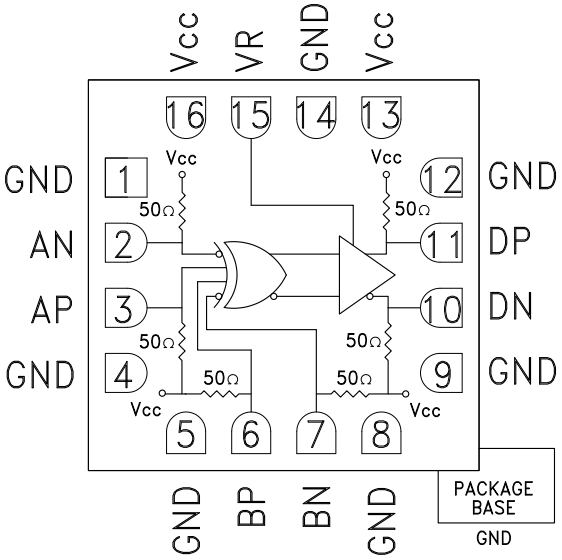
Programmable Differential
Output Voltage Swing: 600 - 1200 mV

Propagation Delay: 95 ps

Single Supply: +3.3 V

16 Lead Ceramic 3x3 mm SMT Package: 9 mm^2

Functional Diagram



General Description

The HMC745LC3 is a XOR/XNOR gate function designed to support data transmission rates of up to 13 Gbps, and clock frequencies as high as 13 GHz. The HMC745LC3 also features an output level control pin, VR, which allows for loss compensation or for signal level optimization.

All input and output signals to the HMC745LC3 are terminated with 50 Ohms to Vcc on-chip, and may be either AC or DC coupled. Inputs or outputs can be connected directly to a 50 Ohm to Vcc terminated system, while DC blocking capacitors may be used if the terminating system is 50 Ohms to ground. The HMC745LC3 operates from a single +3.3 V DC supply, and is available in a ceramic RoHS compliant 3x3 mm SMT package.

Electrical Specifications, T_A = +25 °C, Vcc = +3.3 V

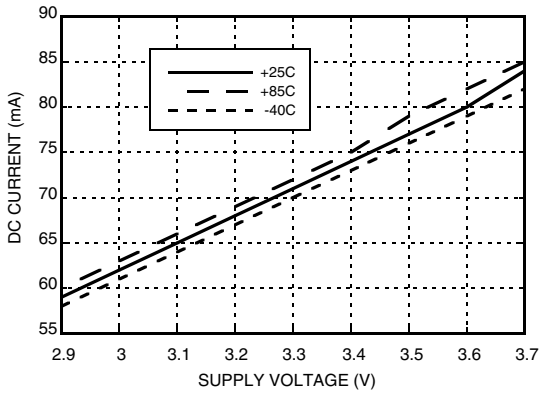
Parameter	Conditions	Min.	Typ.	Max	Units
Power Supply Voltage		3.0	3.3	3.6	V
Power Supply Current			72		mA
Maximum Data Rate			13		Gbps
Maximum Clock Rate			13		GHz
Input High Voltage		2.8		3.8	V
Input Low Voltage		2.1		3.3	V
Input Return Loss	Frequency <13 GHz		10		dB
Output Amplitude	Single-Ended, peak-to-peak		550		mVp-p
	Differential, peak-to-peak		1100		mVp-p
Output High Voltage			3.25		V
Output Low Voltage			2		V
Output Rise / Fall Time	Differential, 20% - 80%		21 / 19		ps

Electrical Specifications (continued)

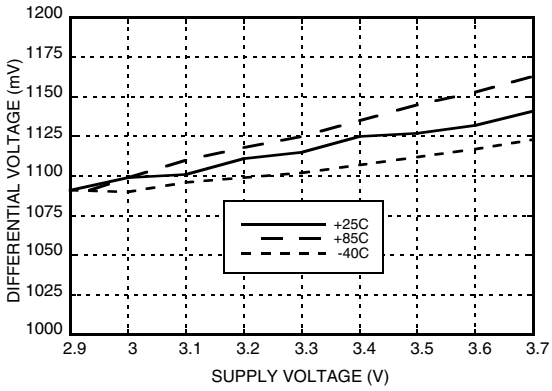
Parameter	Conditions	Min.	Typ.	Max	Units
Output Return Loss	Frequency <13 GHz		10		dB
Small Signal Gain			27		dB
Random Jitter Jr	rms			0.2	ps rms
Deterministic Jitter, Jd	peak-to-peak, 2^{15}-1 PRBS input [1]		2		ps, p-p
Propagation Delay, td			95		ps

[1] Deterministic jitter calculated by simultaneously measuring the jitter of a 300 mV, 13 GHz, 2^{15}-1 PRBS input, and a single-ended output

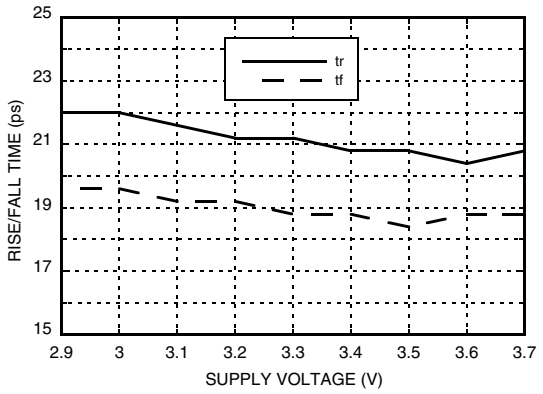
DC Current vs. Supply Voltage [1][2]



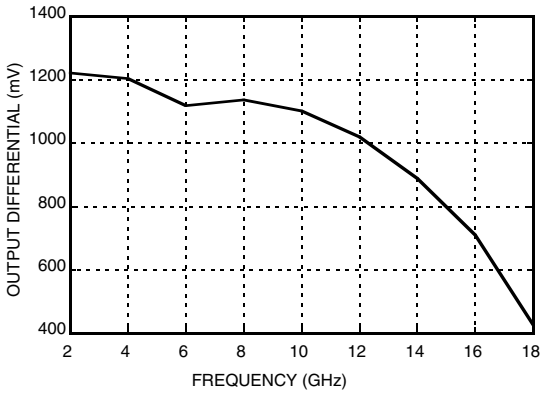
Output Differential vs. Supply Voltage [1][2]



Rise / Fall Time vs. Supply Voltage [2]



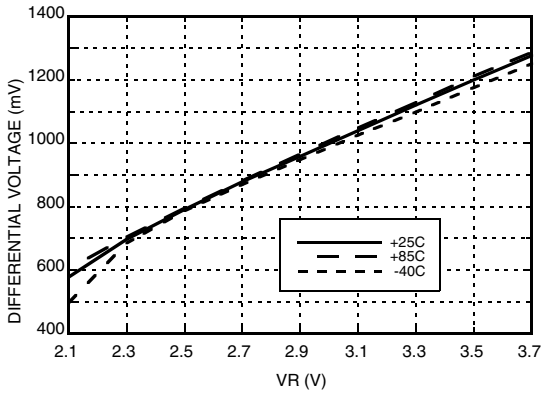
Output Differential vs. Frequency [1]



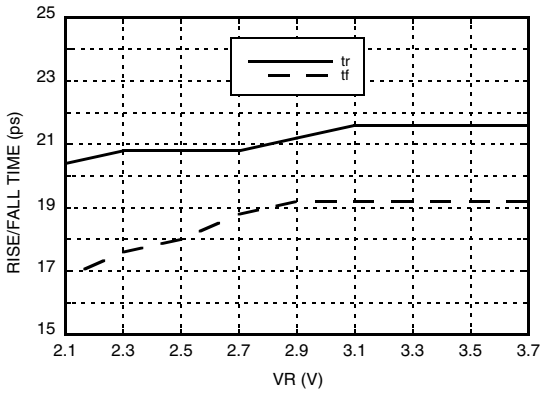
[1] VR = +3.3 V [2] Frequency = 13 GHz

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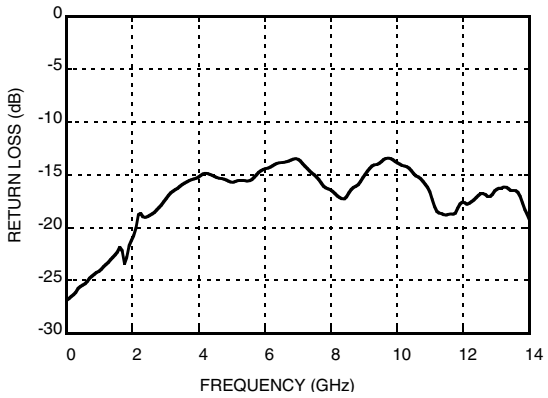
Output Differential vs. VR [2]



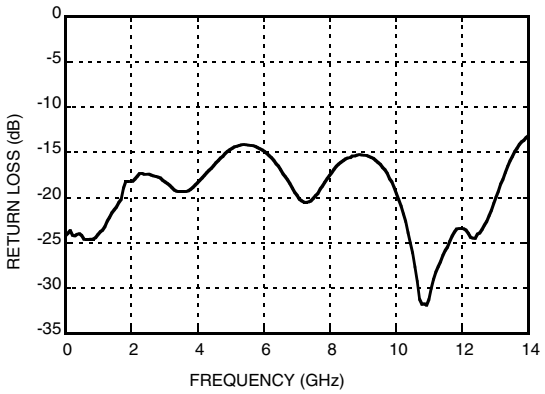
Rise / Fall Time vs. VR [2]



Input Return Loss vs. Frequency

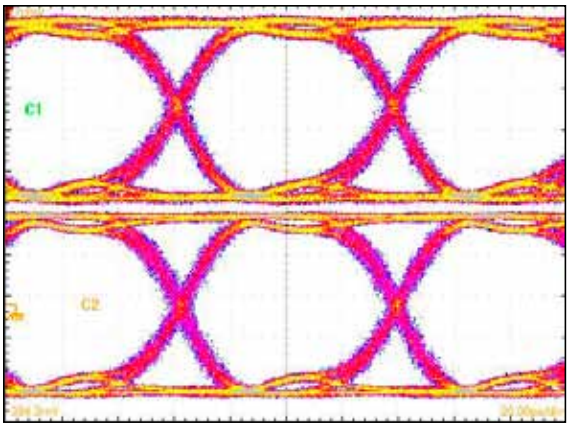


Output Return Loss vs. Frequency



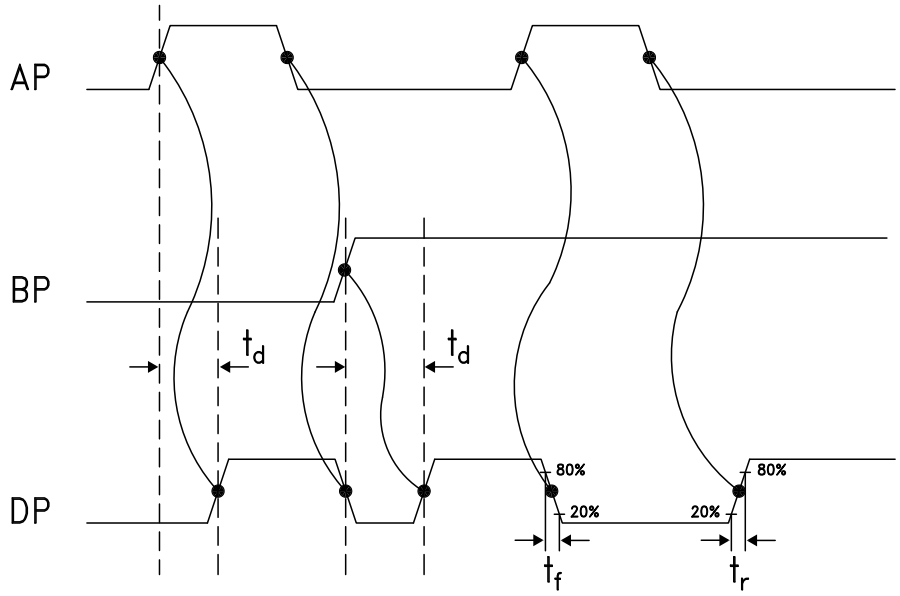
[1] VR = +3.3 V [2] Frequency = 13 GHz

Eye Diagram



[1] Test Conditions:
Waveform generated with an Agilent N4903A J-Bert. Rate = 13 Gbps.
Eye diagram data presented on a Tektronix CSA 8000. Device is AC coupled to scope.

Timing Diagram



Truth Table

Input		Outputs
A	B	D
L	L	L
L	H	H
H	L	H
H	H	L
Notes: A = AP - AN B = BP - BN D = DP - DN	H - Positive voltage level L - Negative voltage level	

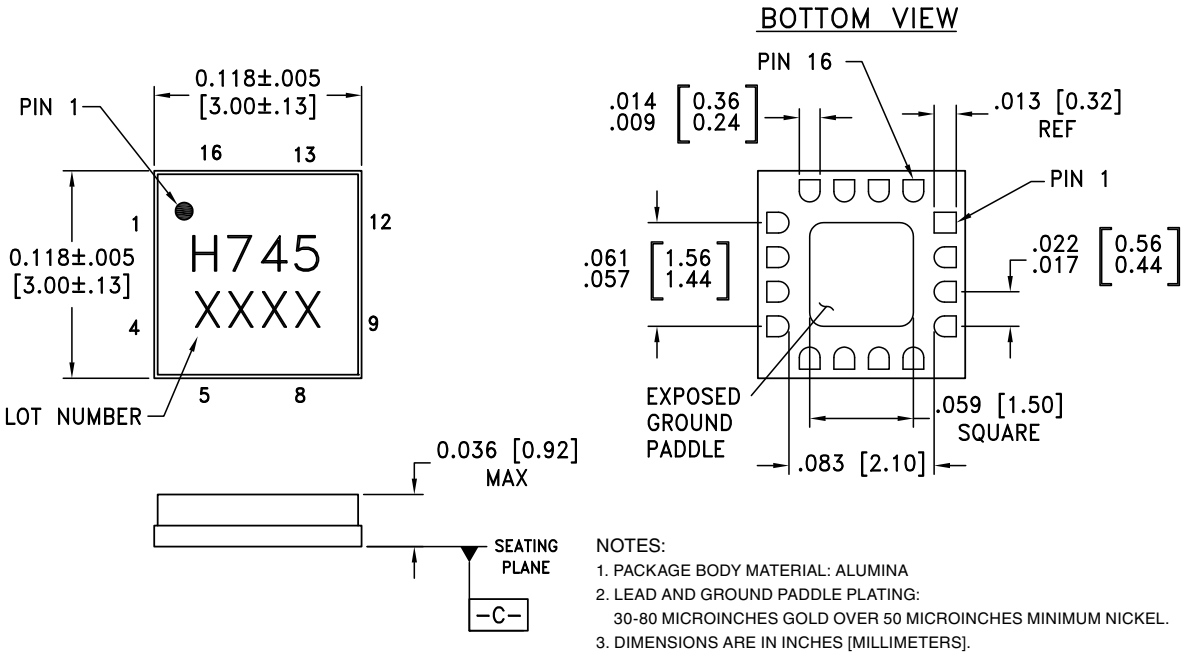
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Absolute Maximum Ratings

Power Supply Voltage (Vee)	-3.75 V to +0.5 V
Input Signals	-2 V to +0.5 V
Output Signals	-1.5 V to +1 V
Continuous Pdiss (T = 85 °C) (derate 17 mW/°C above 85 °C)	0.68 W
Thermal Resistance ($R_{th\ j\text{-}p}$) Worst case junction to package paddle	59 °C/W
Maximum Junction Temperature	125 °C
Storage Temperature	-65 °C to +150 °C
Operating Temperature	-40 °C to +85 °C

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

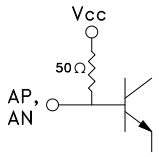
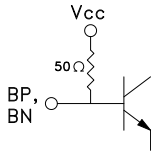
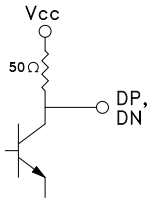
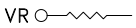
Outline Drawing



NOTES:
1. PACKAGE BODY MATERIAL: ALUMINA
2. LEAD AND GROUND PADDLE PLATING:
   30-80 MICROINCHES GOLD OVER 50 MICROINCHES MINIMUM NICKEL.
3. DIMENSIONS ARE IN INCHES [MILLIMETERS].
4. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
5. PACKAGE WARP SHALL NOT EXCEED 0.05 mm DATUM -C-
6. ALL GROUND LEADS MUST BE SOLDERED TO PCB RF GROUND.
7. PADDLE MUST BE SOLDERED TO GND.

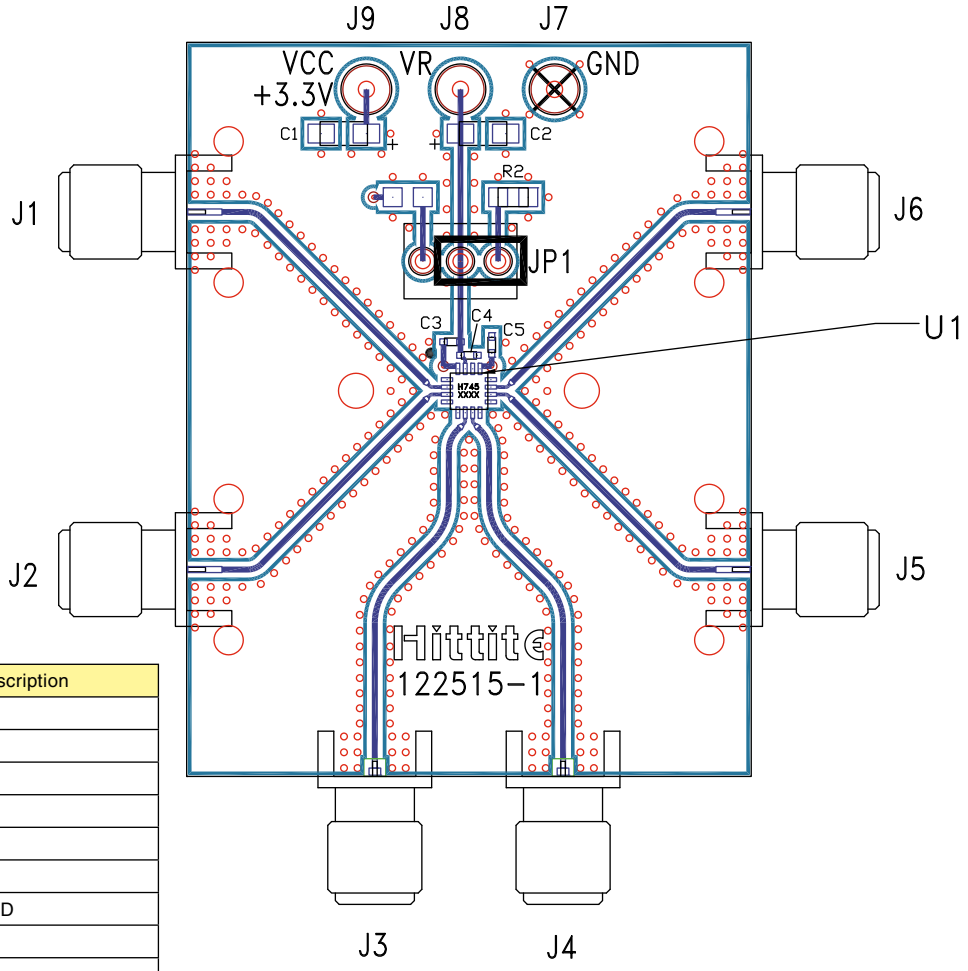
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Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 4, 5, 8, 9, 12	GND	Signal Grounds	
2, 3	AN, AP	Clock / Data Input A	
6, 7	BP, BN	Clock / Data Input B	
10, 11	DN, DP	Clock / Data Output	
13, 16	Vcc	Positive Supply	
14, Package Base	GND	Supply Ground	
15	VR	Output level control. Output level may be adjusted by applying a voltage to VR per "Output Differential vs. VR" plot.	

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Evaluation PCB



Item	Description
J1	AN
J2	AP
J3	BP
J4	BN
J5	DN
J6	DP
J7	GND
J8	VR
J9	Vcc

List of Materials for Evaluation PCB 122517 [1]

Item	Description
J1 - J6	PCB Mount SMA RF Connectors
J7 - J9	DC Pin
JP1	Shorting Jumper
C1, C2	4.7 µF Capacitor, Tantalum
C3 - C5	100 pF Capacitor, 0402 Pkg.
R2	10 Ohm Resistor, 0603 Pkg.
U1	HMC745LC3 High Speed Logic, XOR / XNOR
PCB [2]	122515 Evaluation Board

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Arlon 25FR

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads should be connected directly to the ground plane similar to that shown. The exposed package base should be connected to GND. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

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Application Circuit

