PTN36242L

Dual port SuperSpeed USB 3.0 redriver

Rev. 3 — 24 January 2014 Product data sheet

1. General description

The PTN36242L is a dual port SuperSpeed USB 3.0 redriver IC that enhances signal quality by performing receive equalization on the deteriorated input signal followed by transmit de-emphasis maximizing system link performance. With its superior differential signal conditioning and enhancement capability, the device delivers significant flexibility and performance scaling for various systems with different PCB trace and cable channel conditions and still benefit from optimum power consumption.

The PTN36242L is a dual port device that supports data signaling rate of 5 Gbit/s through each channel. PTN36242L has four channels (two ports): one port has two channels. Port 1 has A1 and B1 channels and Port 2 has A2 and B2 channels. The data flow of one channel is facing the USB host and another channel is facing the USB peripheral or device. Each channel consists of a high-speed Transmit (Tx) differential lane and a high-speed Receive (Rx) differential lane.

The PTN36242L has built-in advanced power management capability that enables significant power saving under various different USB 3.0 Low-power modes (U2/U3). It detects LFPS signaling and link electrical conditions and can dynamically activate/de-activate internal circuitry and logic. The device performs these actions without host software intervention and conserves power.

The PTN36242L is powered from a 3.3 V supply and it is available in HVQFN32 3 mm $\times$ 6 mm $\times$ 0.85 mm package with 0.4 mm pitch.

2. Features and benefits

- Supports USB 3.0 specification (SuperSpeed only)
- Support of two ports (Port 1 has A1 and B1 channels; Port 2 has A2 and B2 channels)
- Each channel supports a receive equalizer and a transmit de-emphasis function
- Selectable receive equalization on each channel to recover from InterSymbol Interference (ISI) and high-frequency losses, with the ability to choose equalization gain settings per channel
- Selectable transmit de-emphasis and output swing on each channel delivers pre-compensation suited to channel conditions
- Integrated termination resistors provide impedance matching on both transmit and receive paths
- Automatic receiver termination indication and detection
- Low active power: 743 mW/225 mA (typical) for both ports with V_{os} = 1000 mV; equalization = 6 dB; de-emphasis = −3.5 dB and V_{DD} = 3.3 V

- Power-saving states:
  - 60 mW/20 mA (typical) when in U2/U3 states
  - 26 mW/8 mA (typical) when no connection detected
  - 0.5 mW/150 μA (typical) when in deep power-saving state
- Hot plug capable
- Power supply: 3.3 V ± 10 %
- HVQFN32 3 mm × 6 mm × 0.85 mm package with 0.4 mm pitch, exposed center pad for thermal relief and electrical ground
- ESD: 8 kV HBM, 1 kV CDM for high-speed pins
- Operating temperature range: 0 °C to 85 °C

3. Applications

- Notebook/netbook/net top platforms
- Docking stations
- Desktop and AIO platforms
- Server and storage platforms
- USB 3.0 peripherals such as consumer/storage devices, printers, or USB 3.0 capable hubs/repeaters

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4. System context diagrams

The system context diagrams in Figure 1 illustrate PTN36242L usage.

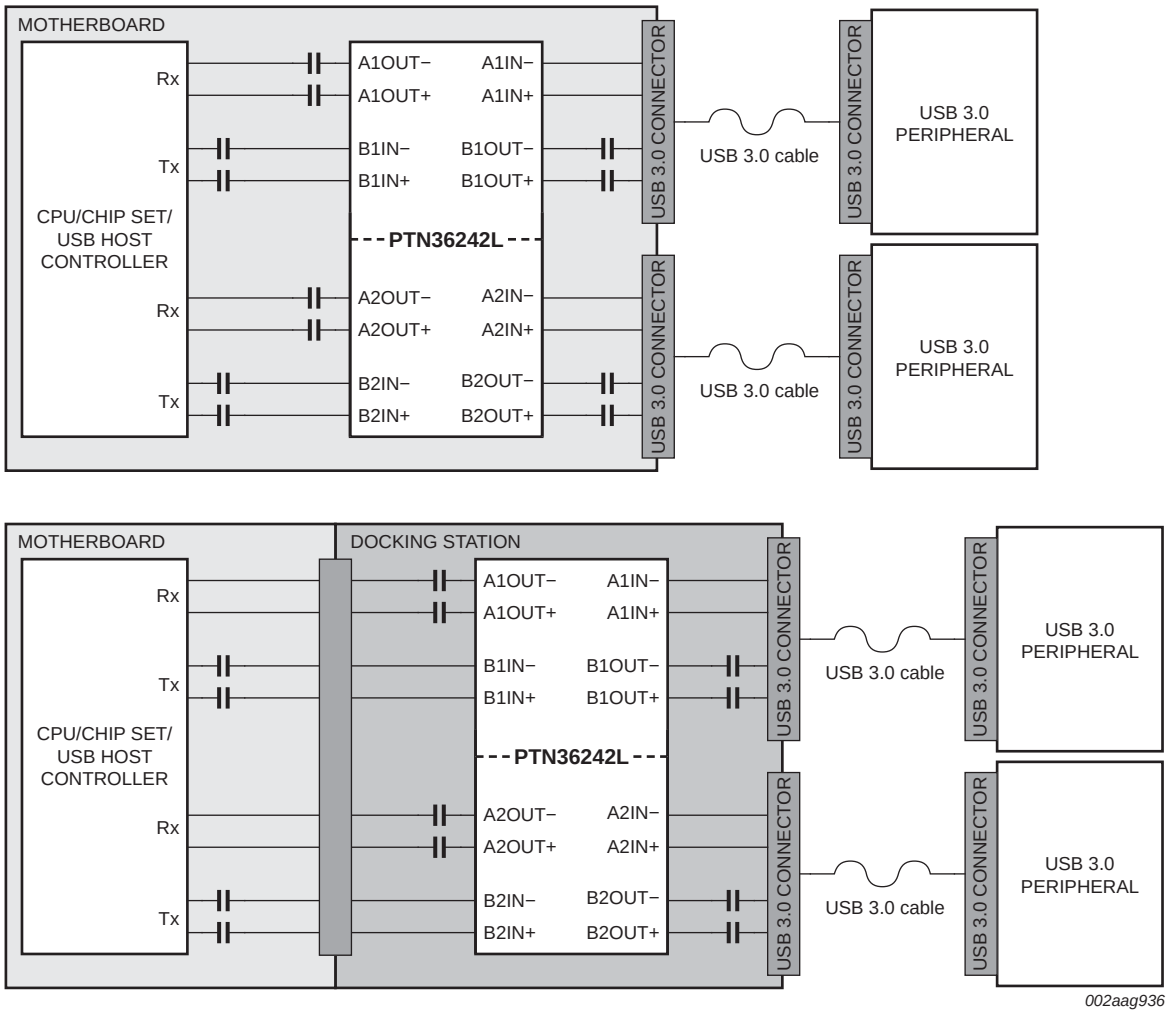


Fig 1. PTN36242L context diagrams

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5. Ordering information

Table 1. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
PTN36242LBS	36242L	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 3 × 6 × 0.85 mm[1]	SOT1185-1
PTN36242LBS/S900	36242L	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 3 × 6 × 0.85 mm[1]	SOT1185-1

[1] Maximum package height is 1 mm.

5.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
PTN36242LBS	PTN36242LBS,518	HVQFN32	Reel 13” Q1/T1 *standard mark SMD dry pack[1]	5000	T_{amb} = 0 °C to 85 °C
PTN36242LBS/S900	PTN36242LBS/S900Y	HVQFN32	Reel 13” Q1/T1 *standard mark SMD dry pack[2]	5000	T_{amb} = 0 °C to 85 °C

[1] 16 mm wide carrier tape.

[2] 12 mm wide carrier tape.

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6. Block diagram

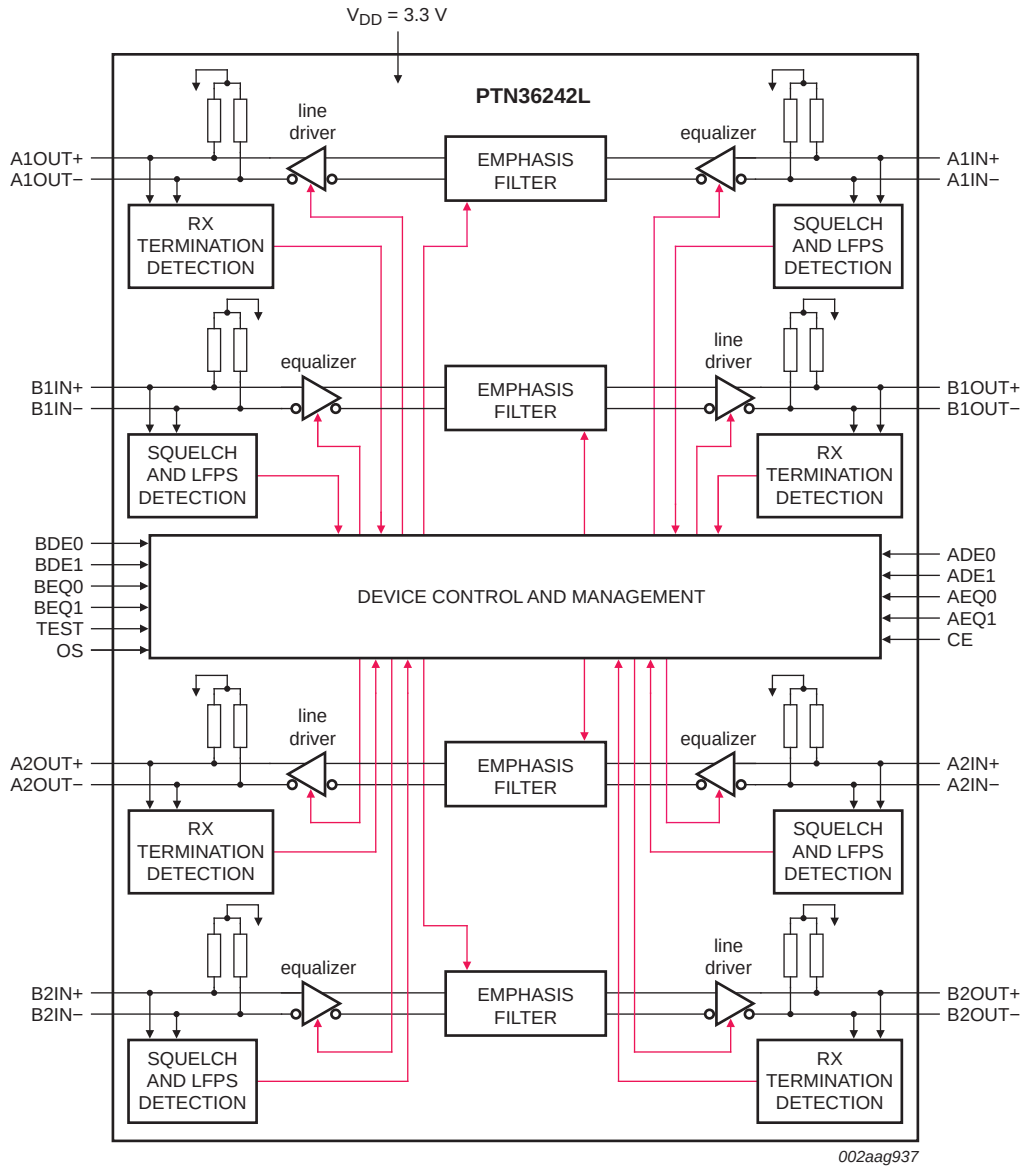


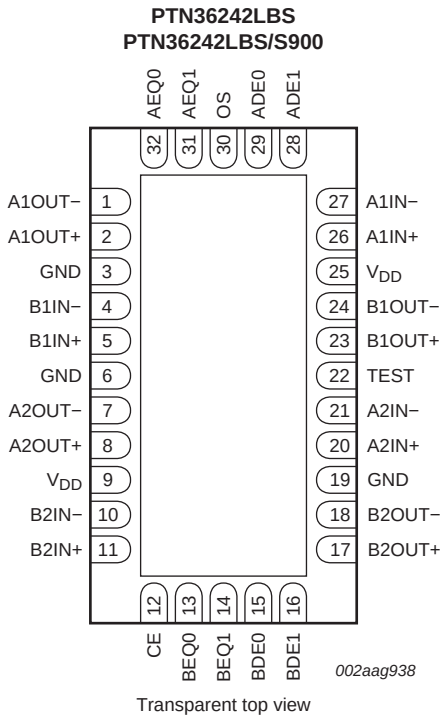
Fig 2. Block diagram of PTN36242L

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7. Pinning information

7.1 Pinning



Transparent top view

Center pad is connected to PCB ground plane for electrical grounding and thermal relief.

Refer to Section 12 for package-related information.

Fig 3. Pin configuration for HVQFN32

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Type	Description
High-speed differential signals			
A1IN+	26	self-biasing differential input	Differential signal from SuperSpeed USB 3.0 transmitter. A1IN+ makes a differential pair with A1IN−. The input to this pin must be AC-coupled externally.
A1IN−	27	self-biasing differential input	Differential signal from SuperSpeed USB 3.0 transmitter. A1IN− makes a differential pair with A1IN+. The input to this pin must be AC-coupled externally.
B1OUT+	23	self-biasing differential output	Differential signal to SuperSpeed USB 3.0 receiver. B1OUT+ makes a differential pair with B1OUT−. The output of this pin must be AC-coupled externally.
B1OUT−	24	self-biasing differential output	Differential signal to SuperSpeed USB 3.0 receiver. B1OUT− makes a differential pair with B1OUT+. The output of this pin must be AC-coupled externally.

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Table 3. Pin description *...continued*

Symbol	Pin	Type	Description
A1OUT+	2	self-biasing differential output	Differential signal to SuperSpeed USB 3.0 receiver. A1OUT+ makes a differential pair with A1OUT−. The output of this pin must be AC-coupled externally.
A1OUT−	1	self-biasing differential output	Differential signal to SuperSpeed USB 3.0 receiver. A1OUT− makes a differential pair with A1OUT+. The output of this pin must be AC-coupled externally.
B1IN+	5	self-biasing differential input	Differential signal from SuperSpeed USB 3.0 transmitter. B1IN+ makes a differential pair with B1IN−. The input to this pin must be AC-coupled externally.
B1IN−	4	self-biasing differential input	Differential signal from SuperSpeed USB 3.0 transmitter. B1IN− makes a differential pair with B1IN+. The input to this pin must be AC-coupled externally.
A2IN+	20	self-biasing differential input	Differential signal from SuperSpeed USB 3.0 transmitter. A2IN+ makes a differential pair with A2IN−. The input to this pin must be AC-coupled externally.
A2IN−	21	self-biasing differential input	Differential signal from SuperSpeed USB 3.0 transmitter. A2IN− makes a differential pair with A2IN+. The input to this pin must be AC-coupled externally.
B2OUT+	17	self-biasing differential output	Differential signal to SuperSpeed USB 3.0 receiver. B2OUT+ makes a differential pair with B2OUT−. The output of this pin must be AC-coupled externally.
B2OUT−	18	self-biasing differential output	Differential signal to SuperSpeed USB 3.0 receiver. B2OUT− makes a differential pair with B2OUT+. The output of this pin must be AC-coupled externally.
A2OUT+	8	self-biasing differential output	Differential signal to SuperSpeed USB 3.0 receiver. A2OUT+ makes a differential pair with A2OUT−. The output of this pin must be AC-coupled externally.
A2OUT−	7	self-biasing differential output	Differential signal to SuperSpeed USB 3.0 receiver. A2OUT− makes a differential pair with A2OUT+. The output of this pin must be AC-coupled externally.
B2IN+	11	self-biasing differential input	Differential signal from SuperSpeed USB 3.0 transmitter. B2IN+ makes a differential pair with B2IN−. The input to this pin must be AC-coupled externally.
B2IN−	10	self-biasing differential input	Differential signal from SuperSpeed USB 3.0 transmitter. B2IN− makes a differential pair with B2IN+. The input to this pin must be AC-coupled externally.
Control and configuration signals			
CE	12	CMOS input	Chip Enable input (active HIGH); internally pulled-up. If CE is LOW, then the device is in deep power-saving state even if supply rail is ON. For the device to be able to operate, the CE pin must be HIGH.
TEST	22	CMOS input	When TEST = HIGH, device is in Test mode, otherwise the device is in USB functional mode (default). Internally pulled down to GND.

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Table 3. Pin description *...continued*

Symbol	Pin	Type	Description
OS	30	Analog	External resistor for output swing adjustment. This pin shall be left open, internally generated bias current will be used and the output is at default swing setting. This pin shall be connected to a 4.99 kΩ resistor to GND. The output swing will be at the default value with reference to the external resistor. For output swing of 1000 mV, leave OS pin open or use resistor of 4.99 kΩ. For output swing of 1100 mV, short OS pin to ground through a 3.75 kΩ resistor. For output swing of 900 mV, short OS pin to ground through a 6.25 kΩ resistor.
AEQ0	32	CMOS input	Equalizer control for channel A of port 1 and port 2. Internally pulled down through 50 kΩ resistor. [AEQ1, AEQ0] = 00: 9 dB 01: 3 dB 10: 6 dB 11: 7.5 dB
AEQ1	31		
ADE0	29	CMOS input	Programmable output de-emphasis level setting for channel A of port 1 and port 2. Internally pulled down through 50 kΩ resistor. [ADE1, ADE0] = 00: −3.5 dB 01: 0 dB 10: −7 dB 11: −5 dB
ADE1	28		
BEQ0	13	CMOS input	Equalizer control for channel B of port 1 and port 2. Internally pulled down through 50 kΩ resistor. [BEQ1, BEQ0] = 00: 9 dB 01: 3 dB 10: 6 dB 11: 7.5 dB
BEQ1	14		
BDE0	15	CMOS input	Programmable output de-emphasis level setting for channel B of port 1 and port 2. Internally pulled down through 50 kΩ resistor. [BDE1, BDE0] = 00: −3.5 dB 01: 0 dB 10: −7 dB 11: −5 dB
BDE1	16		
Supply voltage			
V_{DD}	9, 25	Power	3.3 V supply.

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Table 3. Pin description *...continued*

Symbol	Pin	Type	Description
Ground connections			
GND	3, 19, 6	Ground	Ground supply (0 V).
GND	center pad	Ground	the center pad must be connected to GND plane for both electrical grounding and thermal relief.

8. Functional description

Refer to Figure 2 “Block diagram of PTN36242L”.

PTN36242L is a dual port SuperSpeed USB 3.0 redriver meant to be used for signal integrity enhancement on various platforms — notebooks, docking station, desktop, AIO, peripheral devices, etc. With its high fidelity differential signal conditioning capability and wide configurability, this chip is flexible enough for use under various system environments.

The following sections describe the individual block functions and capabilities of the device in more detail.

8.1 Receive equalization

On the high-speed signal path, the device performs receive equalization providing frequency selective gain to configuration pins AEQ0, AEQ1, BEQ0 and BEQ1 setting. Table 4 lists the configuration options available in this device.

Table 4. AEQ0/AEQ1 (channel A), BEQ0/BEQ1 (channel B) configuration options

AEQ1/AEQ0, BEQ1/BEQ0	SuperSpeed USB 3.0 signal equalization gain at 2.5 GHz
LL	9 dB
LH	3 dB
HL	6 dB
HH	7.5 dB

8.2 Transmit de-emphasis

The PTN36242L device enhances High Frequency (HF) signal content further by performing de-emphasis on the high-speed signals. In addition, the device provides flat frequency gain by boosting output signal. Both flat and frequency selective gains prepare the system to cover up for losses further down the link. Table 5 lists de-emphasis configuration options of PTN36242L.

Table 5. ADE0/ADE1 (channel A), BDE0/BDE1 (channel B) configuration options

ADE1/ADE0, BDE1/BDE0	SuperSpeed USB 3.0 signal de-emphasis gain
LL	−3.5 dB
LH	0
HL	−7 dB
HH	−5 dB

Figure 4 illustrates de-emphasis as a function of time.

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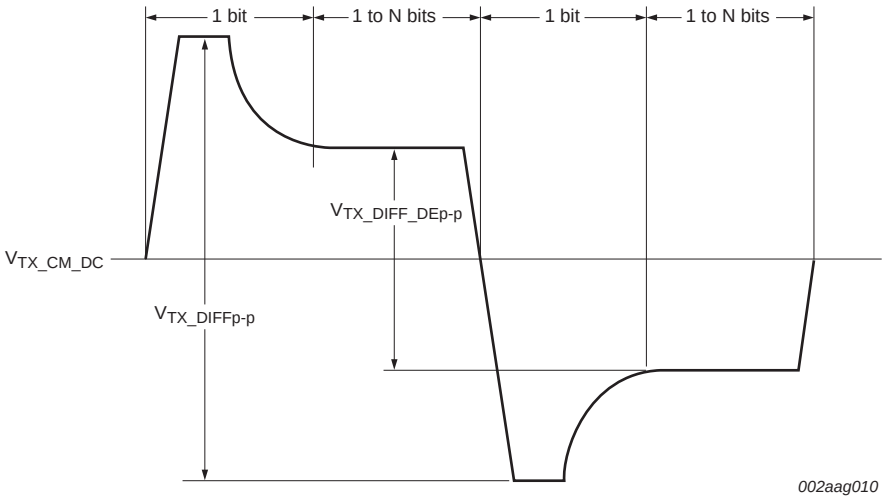


Fig 4. Differential output with de-emphasis

8.3 Device states and power management

PTN36242L has implemented an advanced power management scheme that operates in tune with USB 3.0 bus electrical condition. Though the device does not decode USB power management commands (related to USB 3.0 U1/U2/U3 transitions) exchanged between USB 3.0 host and peripheral/device, it relies on bus electrical conditions to decide to be in one of the following states:

- **Active state** wherein device is fully operational, USB data is transported on port 1 and port 2. In this state, USB connection exists, but there is no need for Receive Termination detection.
- **Power-saving** state wherein the channels A1, A2, B1 and B2 are kept enabled. In this state, squelching, LFPS detection and/or Receive termination detection circuitry are active. Based on USB connection, there are 2 possibilities:
  - No USB connection:

    Receive Termination detection circuitry keeps polling periodically.

    DC common-mode voltage level is not maintained.
  - When USB connection exists and when the link is in USB 3.0 U2/U3 mode:

    Receive Termination detection circuitry keeps polling periodically.

    DC Common mode voltage level is maintained.
- **Deep power-saving** or **Shutdown state** wherein the channel is in Deep power-saving/Shutdown condition enabling significant power saving.
  - DC common-mode voltage level is not maintained.
  - Tx and Rx terminations are put to high-impedance condition.
  - Transitioning to Active state would take several tens of milliseconds.

When CE is LOW, both port 1 and port 2 are put in Deep power-saving state.

The Receive Termination Detection circuitry is implemented as part of a transmitter and detect whether a load device with equivalent DC impedance Z_{RX_DC} is present.

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9. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage		[1]	−0.3	+4.6	V
V_I	input voltage	3.3 V CMOS inputs	[1]	−0.3	V_{DD} + 0.5	V
T_{stg}	storage temperature			−65	+150	°C
V_{ESD}	electrostatic discharge voltage	HBM for high-speed pins	[2]	-	8000	V
		HBM for control pins	[2]	-	4000	V
		CDM for high-speed pins	[3]	-	1000	V
		CDM for control pins	[3]	-	500	V

[1] All voltage values (except differential voltages) are with respect to network ground terminal.

[2] Human Body Model: ANSI/EOS/ESD-S5.1-1994, standard for ESD sensitivity testing, Human Body Model - Component level; Electrostatic Discharge Association, Rome, NY, USA.

[3] Charged Device Model; ANSI/EOS/ESD-S5.3.1-1999, standard for ESD sensitivity testing, Charged Device Model - Component level; Electrostatic Discharge Association, Rome, NY, USA.

10. Recommended operating conditions

Table 7. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage	3.3 V supply option	3.0	3.3	3.6	V
V_I	input voltage	control and configuration pins (for example, AEQ0, AEQ1, BEQ0, BEQ1, ADE0, ADE1, BDE0, BDE1, CE, TEST)	-	V_{DD}	3.6	V
T_{amb}	ambient temperature	operating in free air	0	-	85	°C

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11. Characteristics

11.1 Device characteristics

Table 8. Device characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{startup}$	start-up time	supply voltage within operating range to specified operating characteristics	-	-	20	ms
$t_{s(HL)}$	HIGH to LOW settling time	enable to disable; CE HIGH → LOW change to specified operating characteristics; device is supplied with valid supply voltage	-	-	1	ms
$t_{s(LH)}$	LOW to HIGH settling time	disable to enable; CE LOW → HIGH change to specified operating characteristics; device is supplied with valid supply voltage	-	-	20	ms
t_{rcfg}	reconfiguration time	any configuration pin change (from one setting to another setting) to specified operating characteristics; device is supplied with valid supply voltage	-	-	100	ms
$t_{PD(dif)}$	differential propagation delay	between 50 % level at input and output; see Figure 5	-	-	0.4	ns
t_{idle}	idle time	default wait time to wait before getting into Power-saving state	-	300	400	ms
$t_{d(pwrsave-act)}$	delay time from power-save to active	time for exiting from Power-saving state and get into Active state; see Figure 7	-	10	-	µs
$t_{d(act-idle)}$	delay time from active to idle	reaction time for squelch detection circuit and transmitter output buffer; see Figure 6	-	9	14	ns
$t_{d(idle-act)}$	delay time from idle to active	reaction time for squelch detection circuit and transmitter output buffer; see Figure 6	-	5	11	ns
I_{DD}	supply current	Active state; Tx de-emphasis = −3.5 dB; Rx equalization gain = 6 dB; Tx output signal swing (peak-to-peak) = 1000 mV	-	225	-	mA
		U2/U3 Power-saving state	-	20		mA
		no USB connection state	-	8		mA
		Deep power-saving state; CE = LOW	-	150		µA

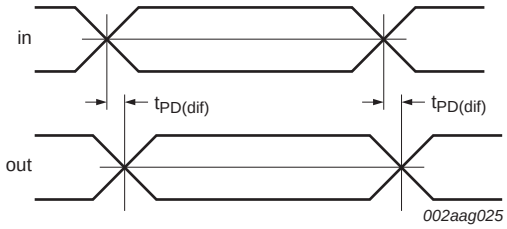


Fig 5. Propagation delay

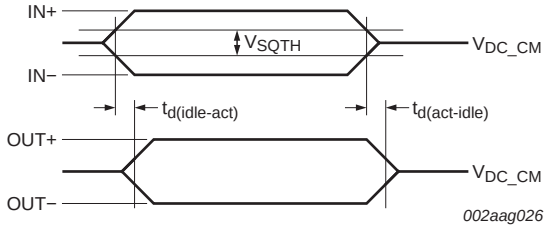


Fig 6. Electrical idle transitions in U0/U1 modes

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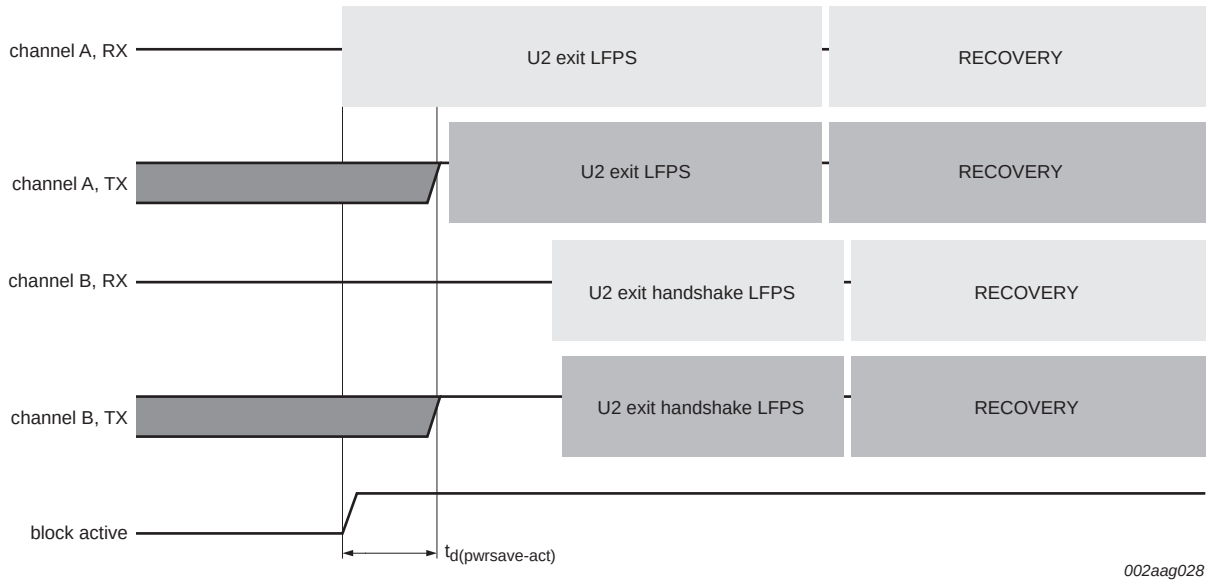


Fig 7. U2/U3 exit behavior

11.2 Receiver AC/DC characteristics

Table 9. Receiver AC/DC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Z_{RX_DC}	receiver DC common-mode impedance		18	-	30	Ω
$Z_{RX_DIFF_DC}$	DC differential impedance	RX pair	72	-	120	Ω
Z_{IH}	HIGH-level input impedance	DC input; common-mode	25	-	-	kΩ
$V_{RX_DIFFp-p}$	differential input peak-to-peak voltage		100	-	1200	mV
$V_{RX_DC_CM}$	RX DC common mode voltage		-	1.8	-	V
$V_{RX_CM_AC_P}$	RX AC common-mode voltage	peak	-	-	150	mV
$V_{th(i)}$	input threshold voltage	differential peak-to-peak value	100	-	-	mV

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11.3 Transmitter AC/DC characteristics

Table 10. Transmitter AC/DC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Z_{TX_DC}	transmitter DC common-mode impedance		18	-	30	Ω
$Z_{TX_DIFF_DC}$	DC differential impedance		72	-	120	Ω
$V_{TX_DIFFp-p}$	differential peak-to-peak output voltage	R_L = 100 Ω				
		OS = 4.99 kΩ or not connected	800	1000	1200	mV
		OS = 3.75 kΩ	800	1100	1200	mV
		OS = 6.25 kΩ	800	900	1200	mV
$V_{TX_DC_CM}$	transmitter DC common-mode voltage		-	-	1.8	V
$V_{TX_CM_ACpp_ACTIV}$	TX AC common-mode peak-to-peak output voltage (active state)	device input fed with differential signal	-	-	100	mV
$V_{TX_IDL_DIFF_ACpp}$	electrical idle differential peak-to-peak output voltage	when link is in electrical idle	-	-	10	mV
$V_{TX_RCV_DETECT}$	voltage change allowed during receiver detection	positive voltage swing to sense the receiver termination detection	-	-	600	mV
$t_{r(tx)}$	transmit rise time	measured using 20 % and 80 % levels; see Figure 8	60	70	80	ps
$t_{f(tx)}$	transmit fall time	measured using 80 % and 20 % levels; see Figure 8	60	70	80	ps
$t_{(r-f)tx}$	difference between transmit rise and fall time	measured using 20 % and 80 % levels	-	-	20	ps

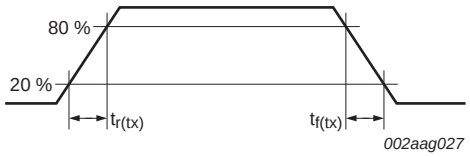


Fig 8. Output rise and fall times

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11.4 Jitter performance

Table 11 provides jitter performance of PTN36242L under a specific set of conditions, illustrated by Figure 9.

Table 11. Jitter performance characteristics

Unit Interval (UI) = 200 ps.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{jit(o)(p-p)}$	peak-to-peak output jitter time	total jitter at test point C	[1]	-	0.14	-	UI
$t_{jit(dtrm)(p-p)}$	peak-to-peak deterministic jitter time		[1]	-	0.06	-	UI
$t_{jit(rndm)(p-p)}$	peak-to-peak random jitter time		[1][2]	-	0.08	-	UI

[1] Measured at test point C with K28.5 pattern, V_{ID} = 1000 mV (peak-to-peak), 5 Gbit/s; –3.5 dB de-emphasis from source.

[2] Random jitter calculated as 14.069 times the RMS random jitter for 10^{-12} bit error rate.

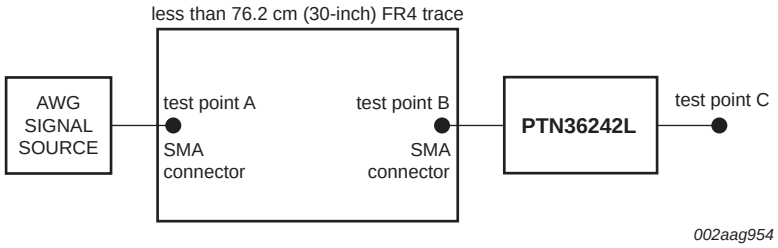


Fig 9. Jitter measurement setup

11.5 Control inputs

Table 12. Control input characteristics

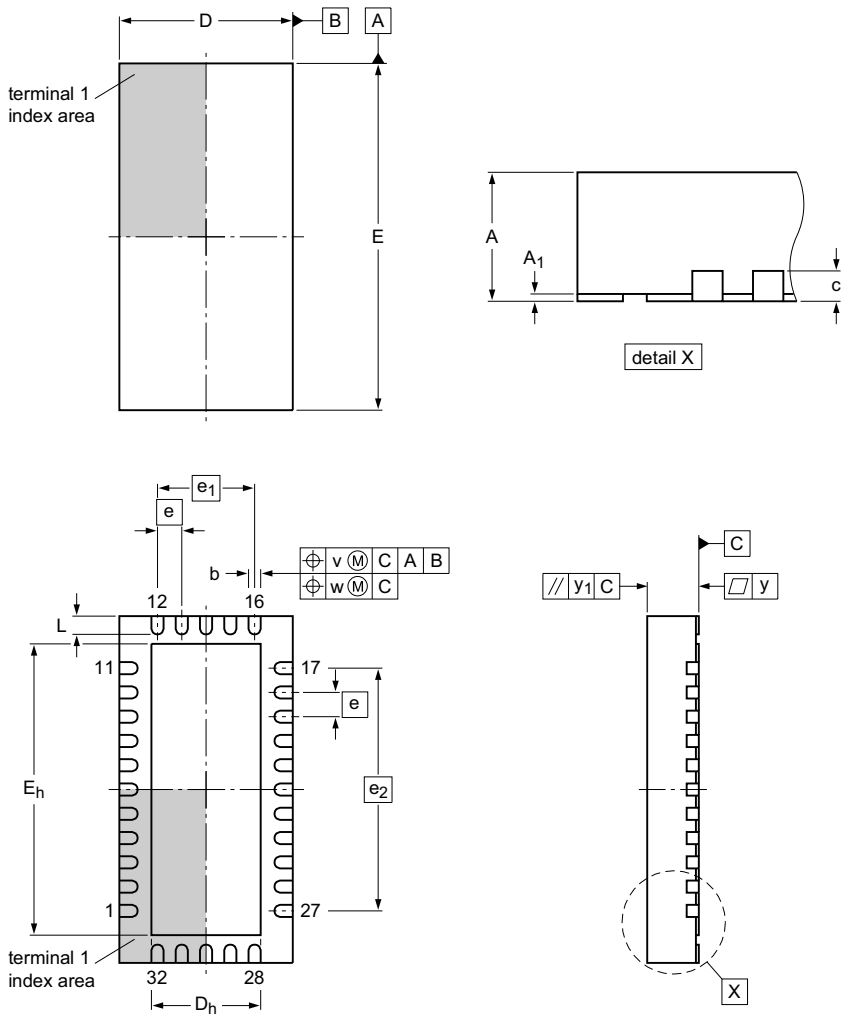
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage		0.65 × $V_{DD(3V3)}$	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.35 × $V_{DD(3V3)}$	V
I_{LI}	input leakage current	measured with input at $V_{IH(max)}$ and $V_{IL(min)}$ when CE = 0 and excluding OS pin	-	10	-	µA

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12. Package outline

HVQFN32: plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; 3 x 6 x 0.85 mm **SOT1185-1**



Dimensions

Unit		$A^{(1)}$	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	L	v	w	y	y_1
	max	1.00	0.05	0.25		3.1	1.9	6.1	4.9				0.4				
mm	nom	0.85	0.02	0.20	0.2	3.0	1.8	6.0	4.8	0.4	1.6	4	0.3	0.07	0.05	0.08	0.1
	min	0.80	0.00	0.15		2.9	1.7	5.9	4.7				0.2				

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot1185-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1185-1	- - -	- - -	- - -			~~10-07-26~~ 10-08-09

Fig 10. Package outline SOT1185-1 (HVQFN32)

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13. Packing information

13.1 Packing method

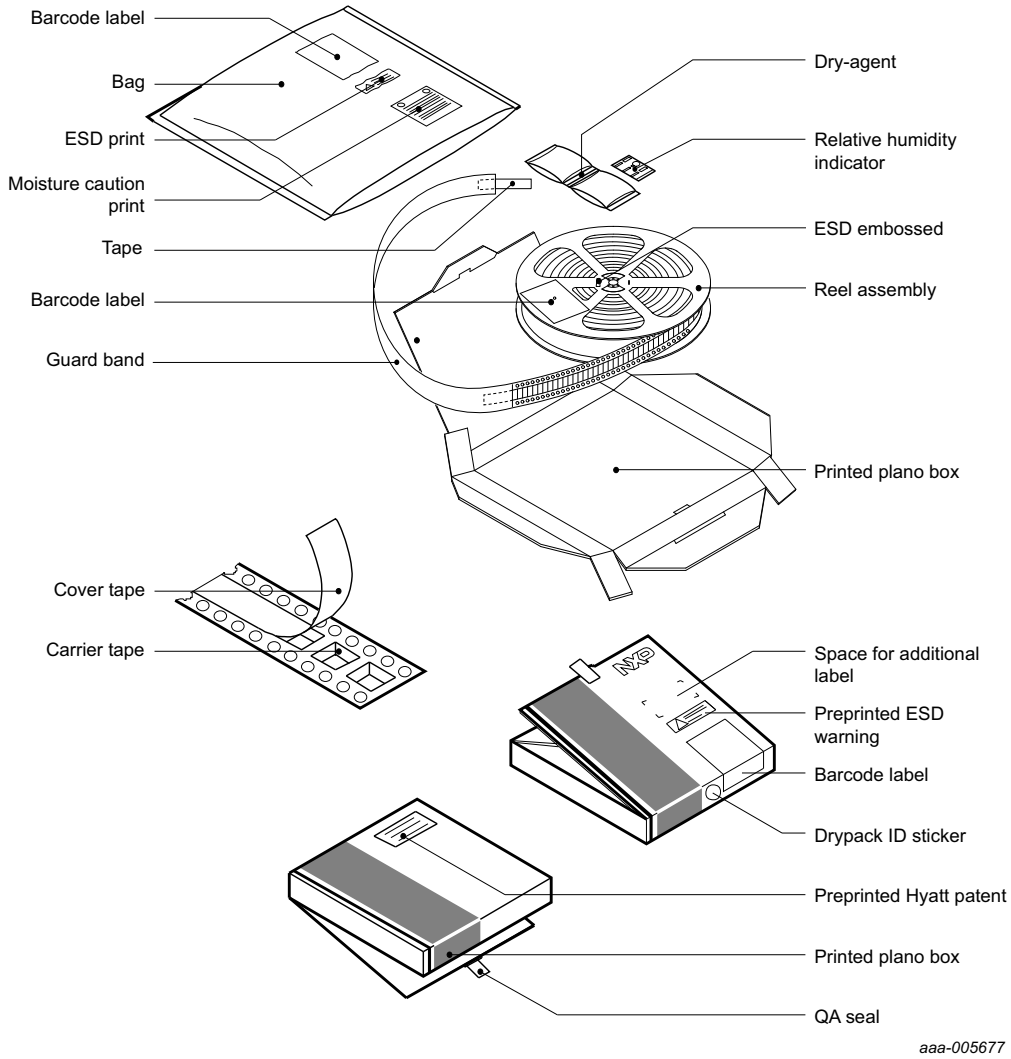


Fig 11. Dry reel pack for SMD

Table 13. Dimensions and quantities

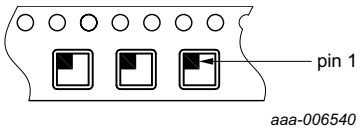
Orderable part number	Reel dimensions d × w (mm) [1]	SPQ/PQ (pcs)	Reels per box	Outer box dimensions l × w × h (mm)
PTN36242LBS,518	330 × 16	5000	1	339 × 335 × 43
PTN36242LBS/S900Y	330 × 12	5000	1	339 × 335 × 33

[1] d = reel diameter; w = tape width.

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13.2 Product orientation



Pin 1 is in quadrant 1.

Fig 12. Product orientation in carrier tape

13.3 Carrier tape dimensions

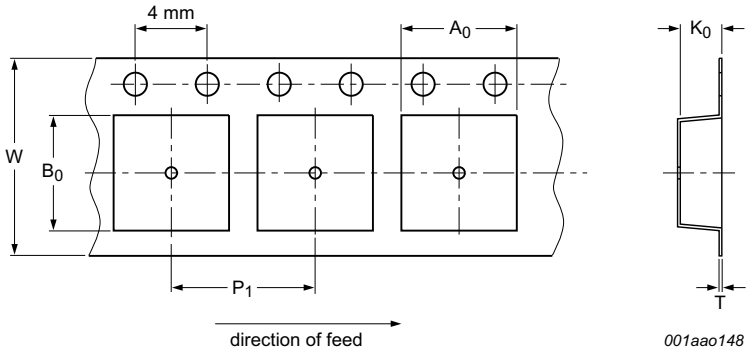


Fig 13. Carrier tape dimensions

Table 14. Carrier tape dimensions

Orderable part number	A_0 (mm)	B_0 (mm)	K_0 (mm)	T (mm)	P_1 (mm)	W (mm)
PTN36242LBS,518	3.3 ± 0.10	6.3 ± 0.10	1.0 ± 0.10	-	8 ± 0.10	16 ± 0.30
PTN36242LBS/S900Y	3.3 ± 0.10	6.3 ± 0.10	1.2 ± 0.10	-	8 ± 0.10	12 ± 0.30

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13.4 Reel dimensions

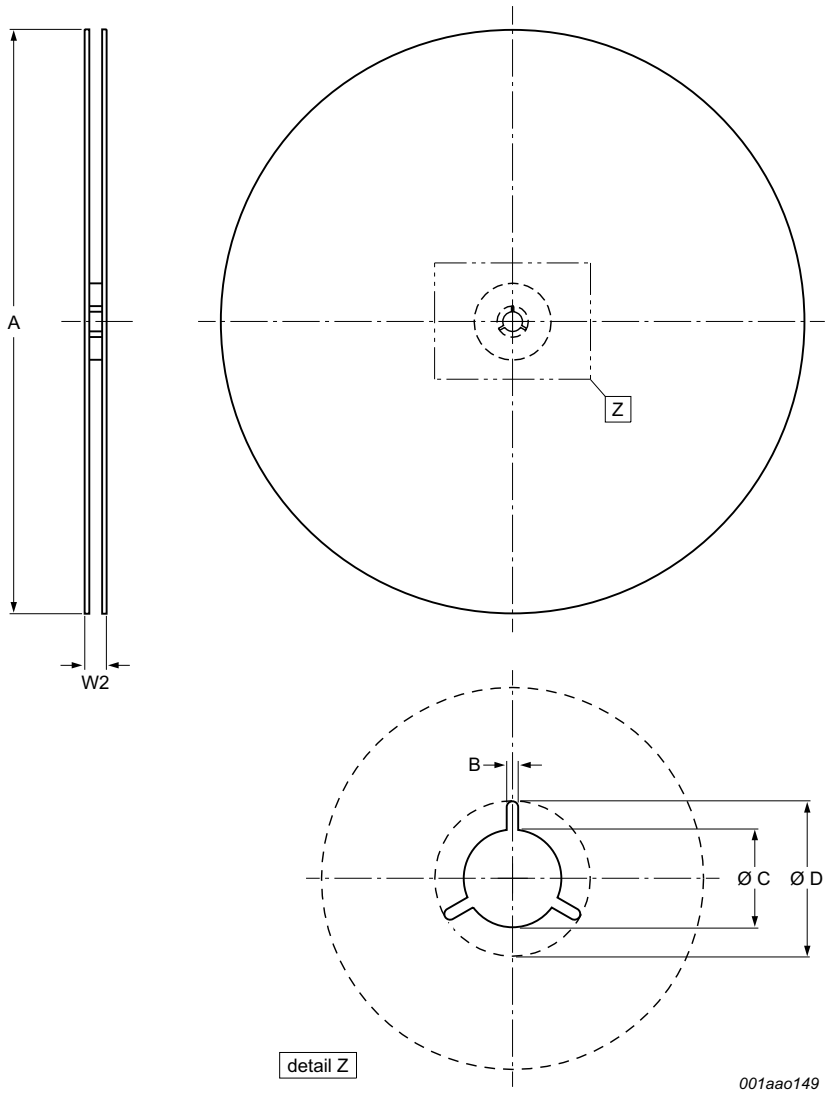


Fig 14. Schematic view of reel

Table 15. Reel dimensions

Orderable part number	A [nom] (mm)	W2 [max] (mm)	B [min] (mm)	C [min] (mm)	D [min] (mm)
PTN36242LBS,518	330	22.4	1.5	12.8	20.2
PTN36242LBS/S900Y	330	14.5	1.5	12.8	20.2

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13.5 Barcode label

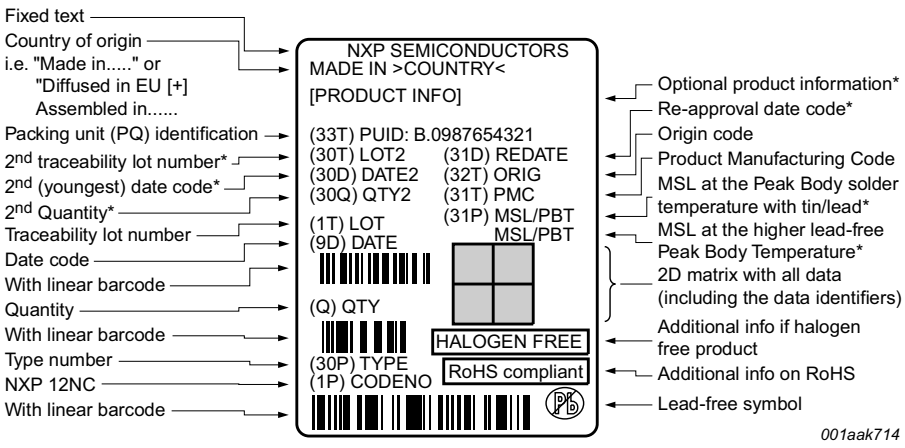


Fig 15. Box and reel information barcode

Table 16. Barcode dimensions

Box barcode label l × w (mm)	Reel barcode label l × w (mm)
100 × 75	100 × 75

14. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

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Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 16) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 17 and 18

Table 17. SnPb eutectic process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

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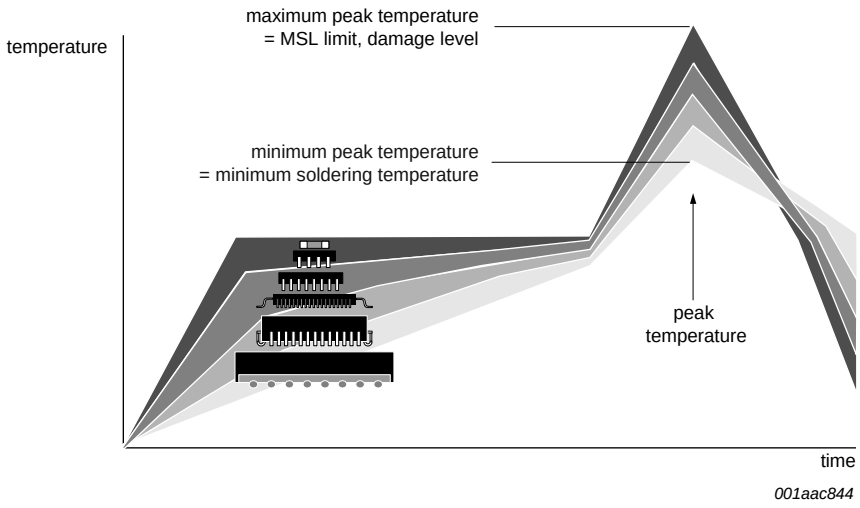
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Table 18. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 16.



MSL: Moisture Sensitivity Level

Fig 16. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

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15. Abbreviations

Table 19. Abbreviations

Acronym	Description
AIO	All In One computer platform
CDM	Charged-Device Model
HBM	Human Body Model
I^2C-bus	Inter-Integrated Circuit bus
IC	Integrated Circuit
LFPS	Low Frequency Periodic Sampling
PCB	Printed-Circuit Board
Rx	Receive
SI	Signal Integrity
Tx	Transmit
USB	Universal Serial Bus

16. Revision history

Table 20. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PTN36242L v.3	20140124	Product data sheet	-	PTN36242L v.2
Modifications:	• Table 1 “Ordering information”: – added Type number PTN36242LBS/S900 • Table 2 “Ordering options”: – added Table note [1] and its reference at PTN36242LBS packing method – added Table note [2] and its reference at PTN36242LBS/S900 packing method • Added Section 13 “Packing information”			
PTN36242L v.2	20130619	Product data sheet	-	PTN36242L v.1
PTN36242L v.1	20130411	Product data sheet	-	-

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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