3V Single Chip 10-Bit Data Acquisition System

FEATURES

- Single Supply 3.3V or ±3.3V Operation
- Software Programmable Features:
  - Unipolar/Bipolar Conversions
  - 4 Differential/8 Single-Ended Inputs
  - MSB- or LSB-First Data Sequence
  - Variable Data Word Length
- Built-In Sample-and-Hold
- Direct 4-Wire Interface to Most MPU Serial Ports and all MPU Parallel Ports
- 15kHz Maximum Throughput Rate

KEY SPECIFICATIONS

- Minimum Guaranteed Supply Voltage: 3V
- Resolution: 10 Bits
- Offset Error: ±0.5LSB Max
- Linearity Error: ±0.5LSB Max
- Gain Error (LTC1283A): ±1LSB Max
- Conversion Time: 44µs
- Supply Current: 350µA Max, 150µA Typ

DESCRIPTION

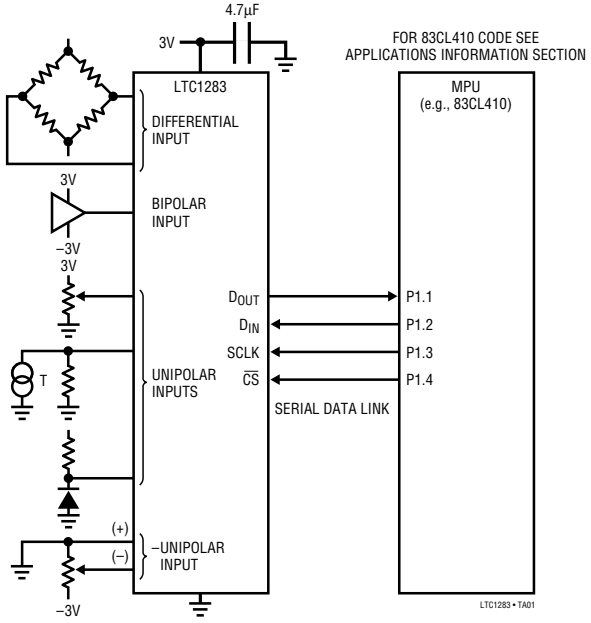
The LTC1283 is a 3V data acquisition component which contains a serial I/O successive approximation A/D converter. It uses LTCMOS™ switched capacitor technology to perform either 10-bit unipolar, or 9-bit plus sign bipolar A/D conversions. The 8-channel input multiplexer can be configured for either single-ended or differential inputs (or combinations thereof). An on-chip sample-and-hold is included for all single-ended input channels.

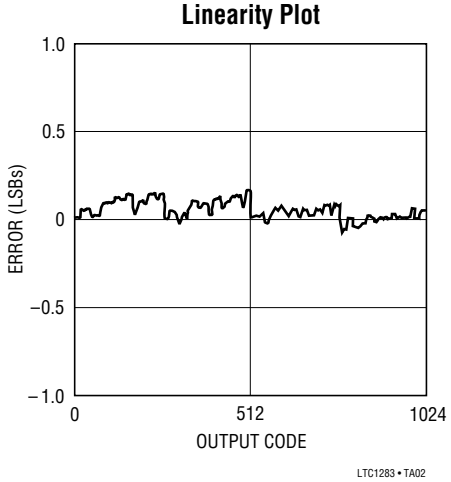
The serial I/O is designed to be compatible with industry-standard full-duplex serial interfaces. It allows either MSB- or LSB-first data and automatically provides 2's complement output coding in the bipolar mode. The output data word can be programmed for a length of 8-, 10-, 12-, or 16-bit. This allows easy interface to shift registers and a variety of processors.

Both the LTC1283A and LTC1283 are specified with offset and linearity errors less than ±0.5LSB. The LTC1283A has a gain error limit of ±1LSB. The 1283 is specified with a gain error limit of ±2LSB for applications where gain is adjustable or less critcial.

LTCMOS is a trademark of Linear Technology Corp.

TYPICAL APPLICATION



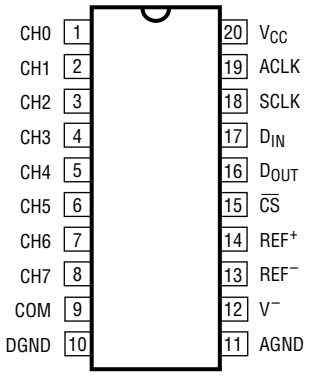


ABSOLUTE MAXIMUM RATINGS (Notes 1 and 2)

Supply Voltage (V_{CC}) to GND or V^- 12V
Voltage
  Analog and Reference
  Inputs ..... (V^-) –0.3V to V_{CC} + 0.3V
  Digital Inputs ..... –0.3V to 12V
  Digital Outputs ..... –0.3V to V_{CC} + 0.3V
Negative Supply Voltage (V–) ..... –6V to GND
Power Dissipation 500mW
Operating Temperature
  LTC1283AC, LTC1283C ..... 0°C to 70°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION

TOP VIEW



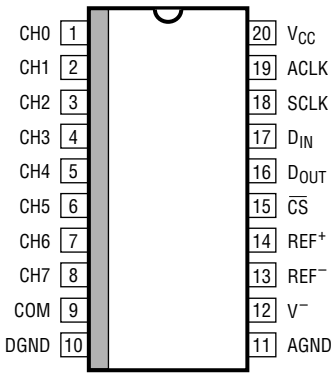
N PACKAGE
20-LEAD PLASTIC DIP

$T_{J\,MAX}$ = 150°C, θ_{JA} = 100°C/W

ORDER PART NUMBER

LTC1283ACN
LTC1283CN

TOP VIEW



S PACKAGE
20-LEAD PLASTIC SOL

$T_{J\,MAX}$ = 150°C, θ_{JA} = 130°C/W

ORDER PART NUMBER

LTC1283ACS
LTC1283CS

Consult factory for Industrial and Military grade parts

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LTC1283/LTC1283A MIN	TYP	MAX	UNITS
V_{CC}	Positive Supply Voltage	V^- = 0V	3.0		3.6	V
V^-	Negative Supply Voltage	V_{CC} = 3.3V	–3.6		0	V
f_{SCLK}	Shift Clock Frequency	V_{CC} = 3V	0		500	kHz
f_{ACLK}	A/D Clock Frequency	V_{CC} = 3V $T_A \le 25°C$ $T_A \le 70°C$	 0.01 0.05		 1.00 1.00	 MHz MHz
t_{CYC}	Total Cycle Time	See Operating Sequence	10 SCLK + 48 ACLK			Cycles
$t_{h\overline{CS}}$	Hold Time, $\overline{CS}$ Low After Last SCLK↓	V_{CC} = 3V	0			ns
t_{hDI}	Hold Time, D_{IN} After SCLK↑	V_{CC} = 3V	200			ns
$t_{su\overline{CS}}$	Setup Time $\overline{CS}$↓ Before Clocking in First Address Bit (Note 8)	V_{CC} = 3V	2 ACLK Cycles + 1µs			
t_{suDI}	Setup Time, D_{IN} Stable Before SCLK↑	V_{CC} = 3V	400			ns
t_{WHACLK}	ACLK High Time	V_{CC} = 3V	250			ns
t_{WLACLK}	ACLK Low Time	V_{CC} = 3V	400			ns
$t_{WH\overline{CS}}$	$\overline{CS}$ High Time During Conversion	V_{CC} = 3V	44			ACLK Cycles

CONVERTER AND MULTIPLEXER CHARACTERISTICS (Note 3)

PARAMETER	CONDITIONS		LTC1283A MIN	LTC1283A TYP	LTC1283A MAX	LTC1283 MIN	LTC1283 TYP	LTC1283 MAX	UNITS
Offset Error	(Note 4)	●			±0.5			±0.5	LSB
Linearity Error	(Notes 4 and 5)	●			±0.5			±0.5	LSB
Gain Error	(Note 4)	●			±1.0			±2.0	LSB
Minimum Resolution for Which No Missing Codes are Guaranteed		●			10			10	Bits
Reference Input Resistance				10			10		kΩ
Analog and REF Input Range	(Note 6)			(V^-) – 0.05V to V_{CC} + 0.05V					V
On Channel Leakage Current (Note 7)	On Channel = 3V Off Channel = 0V	●			1			1	µA
	On Channel = 0V Off Channel = 3V	●			–1			–1	µA
Off Channel Leakage Current (Note 7)	On Channel = 3V Off Channel = 0V	●			–1			–1	µA
	On Channel = 0V Off Channel = 3V	●			1			1	µA

AC CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS		LTC1283/LTC1283A MIN	LTC1283/LTC1283A TYP	LTC1283/LTC1283A MAX	UNITS
t_{ACC}	Delay Time From $\overline{CS}\downarrow$ to D_{OUT} Data Valid	(Note 8)			2		ACLK Cycles
t_{SMPL}	Analog Input Sample Time	See Operating Sequence			5		SCLK Cycles
t_{CONV}	Conversion Time	See Operating Sequence			44		ACLK Cycles
t_{dDO}	Delay Time, SCLK↓ to D_{OUT} Data Valid	See Test Circuts	●		400	900	ns
t_{dis}	Delay Time, $\overline{CS}\uparrow$ to D_{OUT} Hi-Z	See Test Circuits	●		240	500	ns
t_{en}	Delay Time, 2nd CLK↓ to D_{OUT} Enabled	See Test Circuits	●		300	800	ns
t_{hDO}	Time Output Data Remains Valid After SCLK↓				75		ns
t_f	D_{OUT} Fall Time	See Test Circuits	●		90	300	ns
t_r	D_{OUT} Rise Time	See Test Circuits	●		80	300	ns
C_{IN}	Input Capacitance	Analog Inputs On Channel Off Channel Digital Inputs			65 5 5		pF pF pF

DIGITAL AND DC ELECTRICAL CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS		LTC1283/LTC1283A MIN	LTC1283/LTC1283A TYP	LTC1283/LTC1283A MAX	UNITS
V_{IH}	High Level Input Voltage	V_{CC} = 3.6V	●	1.7			V
V_{IL}	Low Level Input Voltage	V_{CC} = 3V	●			0.45	V
I_{IH}	High Level Input Current	$V_{IN} = V_{CC}$	●			2.5	µA
I_{IL}	Low Level Input Current	V_{IN} = 0V	●			–2.5	µA
V_{OH}	High Level Output Voltage	V_{CC} = 3V, I_O = –20µA I_O = –200µA	 ●	2.6 2.0	2.8		V V
V_{OL}	Low Level Output Voltage	V_{CC} = 3V, I_O = 20µA I_O = 400µA	 ●		0.05 0.10	 0.30	V V

DIGITAL AND DC ELECTRICAL CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS		LTC1283/LTC1283A MIN	TYP	MAX	UNITS
I_{OZ}	Hi-Z Output Leakage	$V_{OUT} = V_{CC}$, $\overline{CS}$ High $V_{OUT} = 0V$, CS High	● ●			3 –3	µA µA
I_{SOURCE}	Output Source Current	$V_{OUT} = 0V$			–4.5		mA
I_{SINK}	Output Sink Current	$V_{OUT} = V_{CC}$			4.5		mA
I_{CC}	Positive Supply Current	$\overline{CS}$ High, REF^+ Open	●		150	350	µA
I_{REF}	Reference Current	$V_{REF} = 2.5V$	●		250	500	µA
I^-	Negative Supply Current	$\overline{CS}$ High, $V^- = –3V$	●		–1	–50	µA

The ● denotes specifications which apply over the operating temperature range; all other limits and typicals $T_A = 25°C$.

Note 1: Absolute maximum ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to ground with DGND, AGND and REF^- wired together (unless otherwise noted).

Note 3: $V_{CC} = 3V$, $V_{REF}^+ = 2.5V$, $V_{REF}^- = 0V$, $V^- = 0V$ for unipolar mode and –3V for bipolar mode, ACLK = 1MHz, SCLK = 0.25MHz unless otherwise specified.

Note 4: These specifications apply for both unipolar and bipolar modes. In bipolar mode, one LSB is equal to the bipolar input span ($2V_{REF}$) divided by 1024. For example, when $V_{REF} = 2.5V$, 1LSB (bipolar) = 2(2.5V)/1024 = 4.88mV.

Note 5: Linearity error is the deviation from ideal of the slope between the two end points of the transfer curve.

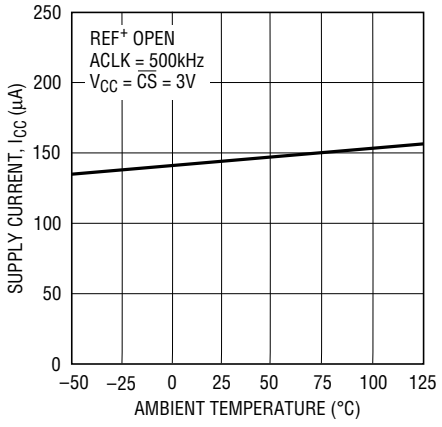
Note 6: Two on-chip diodes are tied to each reference and analog input which will conduct for reference or analog input voltages one diode drop below V^- or one diode drop above V_{CC}. Be careful during testing at low V_{CC} levels, as high level reference or analog inputs can cause this input diode to conduct, especially at elevated temperatures, and cause errors for inputs near full scale. This spec allows 50mV forward bias of either diode. This means that as long as the reference or analog input does not exceed the supply voltage by more than 50mV, the output code will be correct.

Note 7: Channel leakage current is measured after the channel selection.

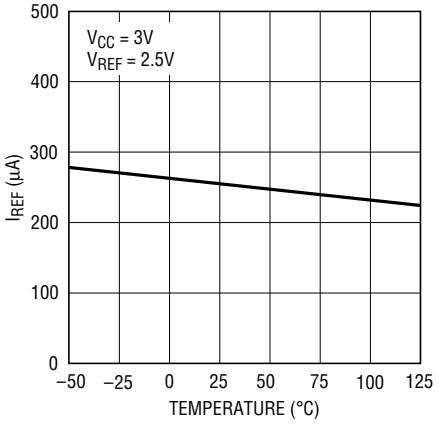
Note 8: To minimize errors caused by noise at the chip select input, the internal circuitry waits for two ACLK falling edges after a chip select falling edge is detected before responding to control input signals. Therefore, no attempt should be made to clock an address in or data out until the minimum chip select setup time has elapsed.

TYPICAL PERFORMANCE CHARACTERISTICS

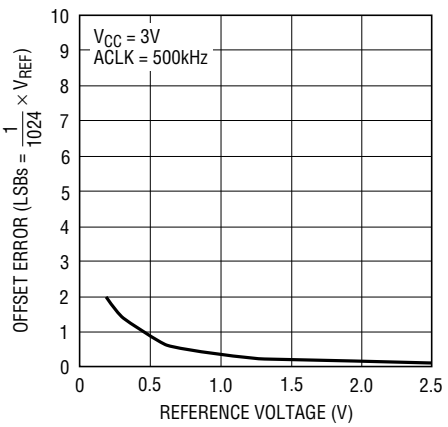
Supply Current vs Temperature



Reference Current vs Temperature

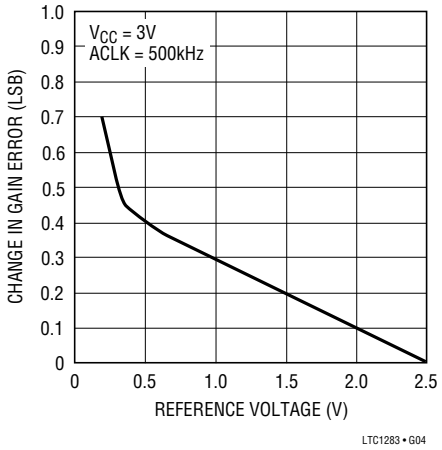


Unadjusted Offset Error vs Reference Voltage

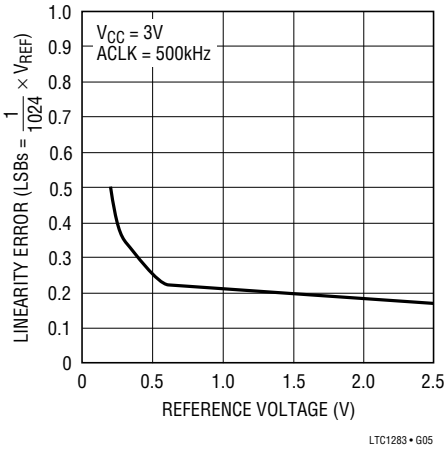


TYPICAL PERFORMANCE CHARACTERISTICS

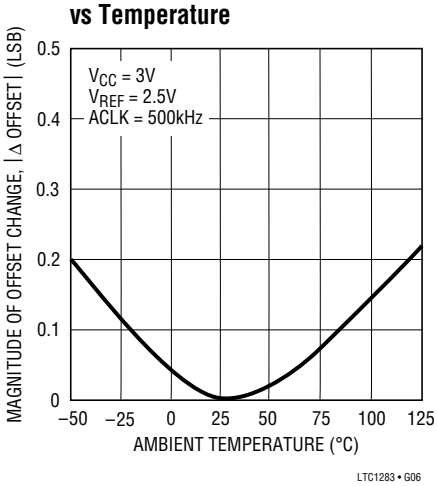
Change in Full-Scale Error vs Reference Voltage



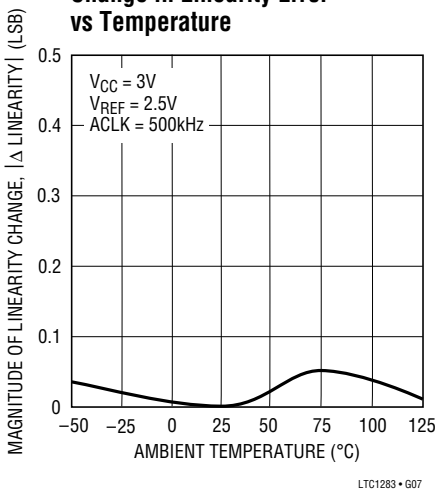
Linearity Error vs Reference Voltage



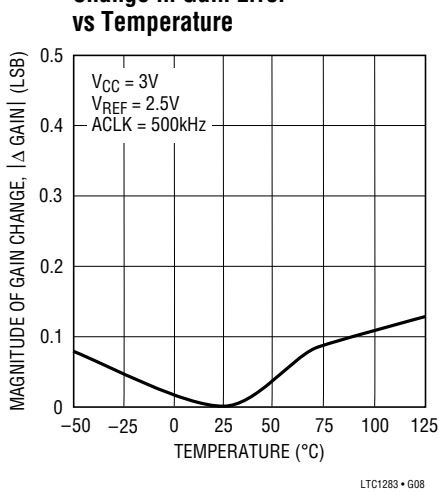
Change in Offset Error vs Temperature



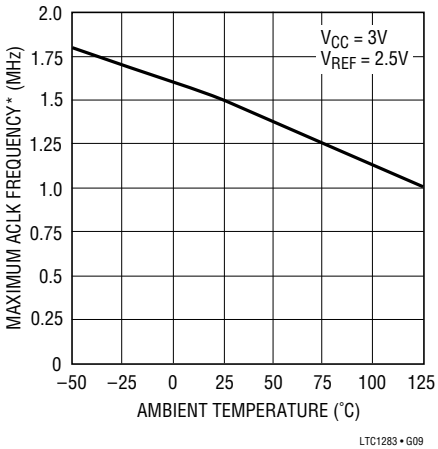
Change in Linearity Error vs Temperature



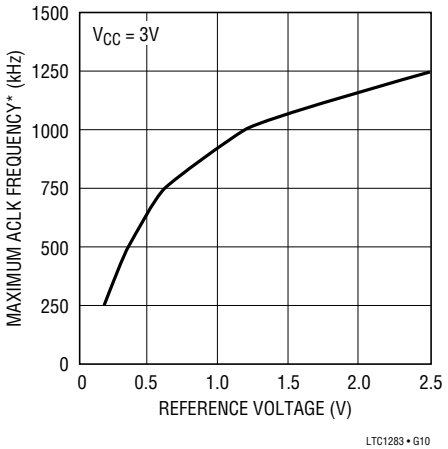
Change in Gain Error vs Temperature



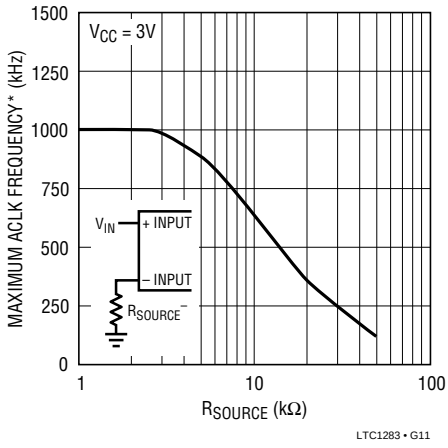
Maximum Conversion Clock Rate vs Temperature



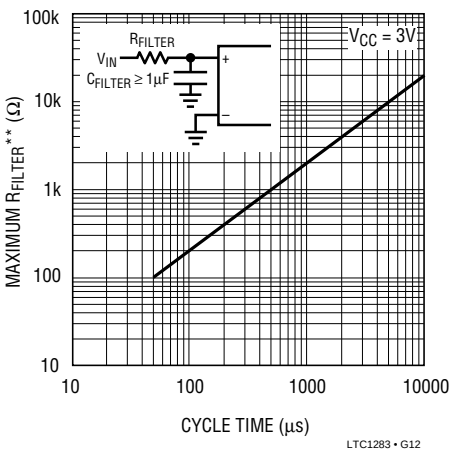
Maximum Conversion Clock Rate vs Reference Voltage



Maximum Conversion Clock Rate vs Source Resistance



Maximum Filter Resistor vs Cycle Time

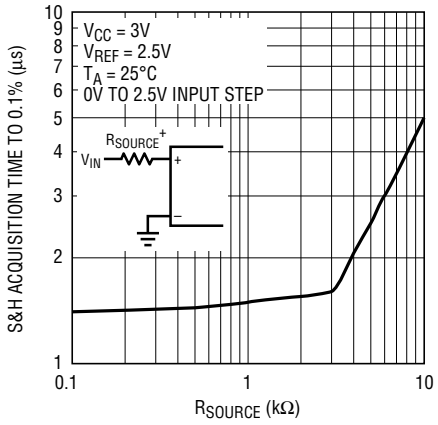


*Maximum ACLK frequency represents the ACLK frequency at which a 0.1LSB shift in the error at any code transition from its 100kHz value is first detected.

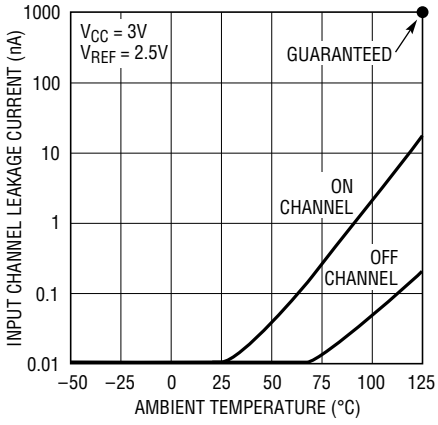
**Maximum R_{FILTER} represents the filter resistor value at which a 0.1LSB change in full-scale error from its value at R_{FILTER} = 0 is first detected.

TYPICAL PERFORMANCE CHARACTERISTICS

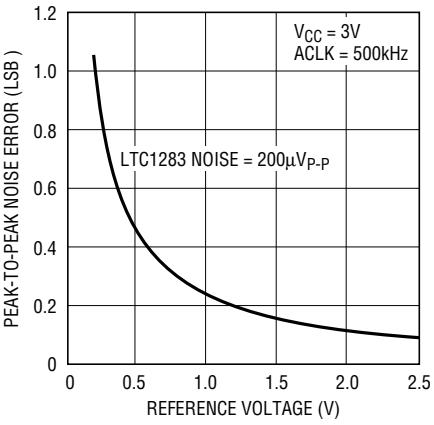
Sample-and-Hold Acquisition Time vs Source Resistance



Input Channel Leakage Current vs Temperature



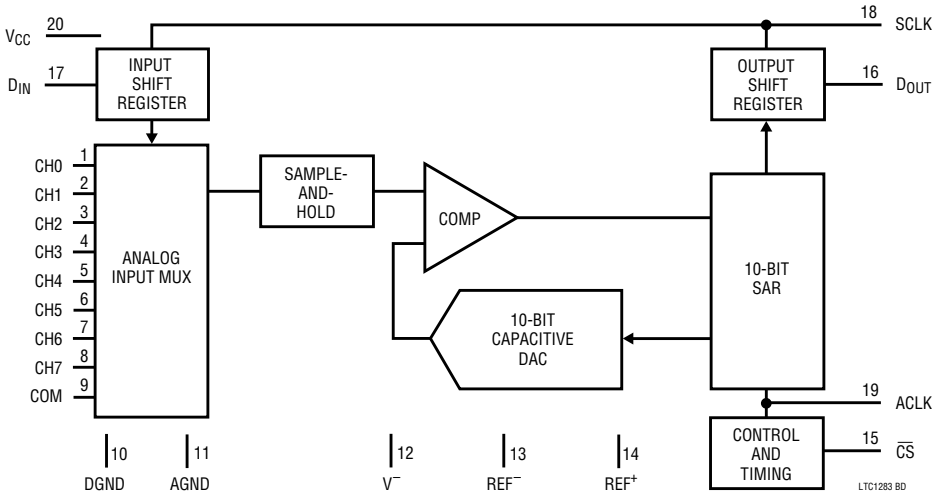
Noise Error vs Reference Voltage



PIN FUNCTIONS

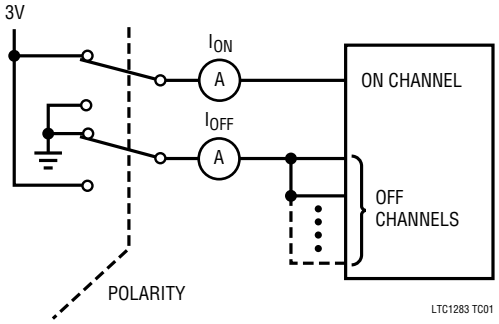
#	PIN	FUNCTION	DESCRIPTION
1-8	CH0-CH7	Analog Inputs	The analog inputs must be free of noise with respect to AGND.
9	COM	Common	The common pin defines the zero reference point for all single-ended inputs. It must be free of noise and is usually tied to the analog ground plane.
10	DGND	Digital Ground	This is the ground for the internal logic. Tie to the ground plane.
11	AGND	Analog Ground	AGND should be tied directly to the analog ground plane.
12	V^-	Negative Supply	Tie V^- to most negative potential in the circuit. (Ground in single supply applications.)
13, 14	$\overline{REF}^-$, REF^+	Reference Inputs	The reference inputs must be kept free of noise with respect to AGND.
15	$\overline{CS}$	Chip Select Input	A logic low on this input enables data transfer.
16	D_{OUT}	Digital Data Output	The A/D conversion result is shifted out of this output.
17	D_{IN}	Data Input	The A/D configuration word is shifted into this input.
18	SCLK	Shift Clock	This clock synchronizes the serial data transfer.
19	ACLK	A/D Conversion Clock	This clock controls the A/D conversion process.
20	V_{CC}	Positive Supply	This supply must be kept free of noise and ripple by bypassing directly to the analog ground plane.

BLOCK DIAGRAM

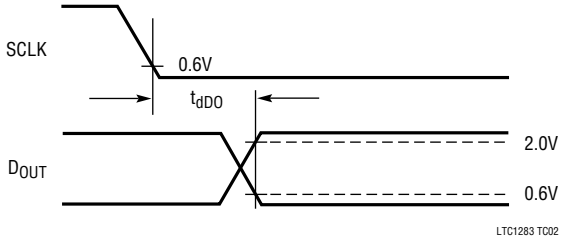


TEST CIRCUITS

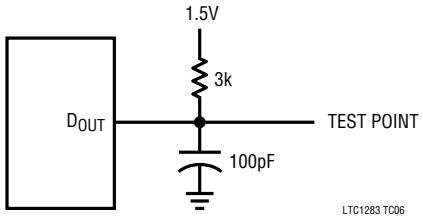
On and Off Channel Leakage Current



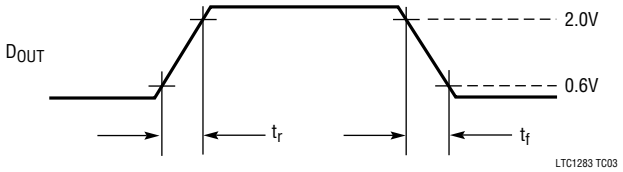
Voltage Waveforms for D_{OUT} Delay Time, t_{dDO}



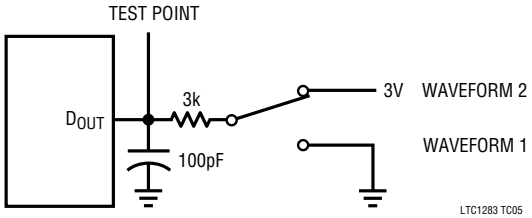
Load Circuit for t_{dDO}, t_r, t_f and t_{en}



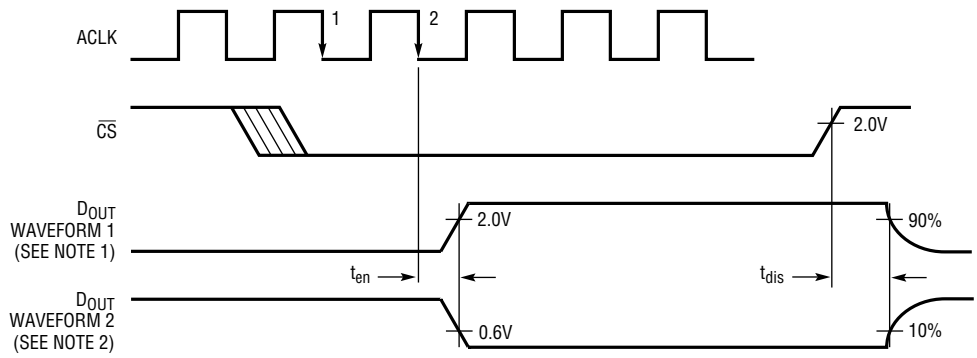
Voltage Waveform for D_{OUT} Rise and Fall Times, t_r and t_f



Load Circuit for t_{dis}



Voltage Waveforms for t_{en} and t_{dis}



NOTE 1: WAVEFORM 1 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS HIGH UNLESS DISABLED BY THE OUTPUT CONTROL.

NOTE 2: WAVEFORM 2 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS LOW UNLESS DISABLED BY THE OUTPUT CONTROL.

LTC1283 TC04

APPLICATIONS INFORMATION

The LTC1283 is a 3V data acquisition component which contains the following functional blocks:

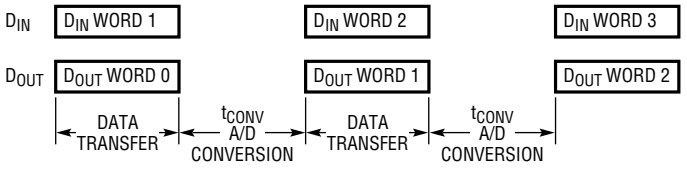
1. 10-bit successive approximation capacitive A/D converter
2. Analog multiplexer (MUX)
3. Sample-and-hold (S&H)
4. Synchronous, full duplex serial interface
5. Control and timing logic

DIGITAL CONSIDERATIONS

1. Serial Interface

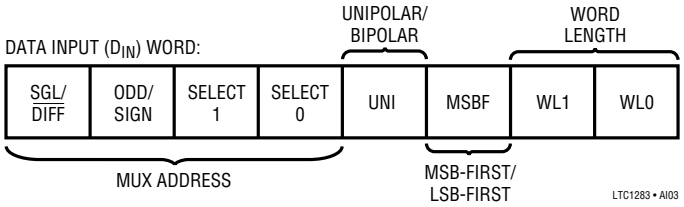
The LTC1283 communicates with microprocessors and other external circuitry via a synchronous, full duplex, 4-wire serial interface (see Operating Sequence). The shift clock (SCLK) synchronizes the data transfer with each bit being transmitted on the falling SCLK edge and captured on the rising SCLK edge in both transmitting and receiving systems. The data is transmitted and received simultaneously (full duplex).

Data transfer is initiated by a falling chip select ($\overline{CS}$) signal. After the falling $\overline{CS}$ is recognized, an 8-bit input word is shifted into the D_{IN} input which configures the LTC1283 for the next conversion. Simultaneously, the result of the previous conversion is output on the D_{OUT} line. At the end of the data exchange the requested conversion begins and $\overline{CS}$ should be brought high. After t_{CONV}, the conversion is complete and the results will be available on the next data transfer cycle. As shown below, the result of a conversion is delayed by one $\overline{CS}$ cycle from the input word requesting it.

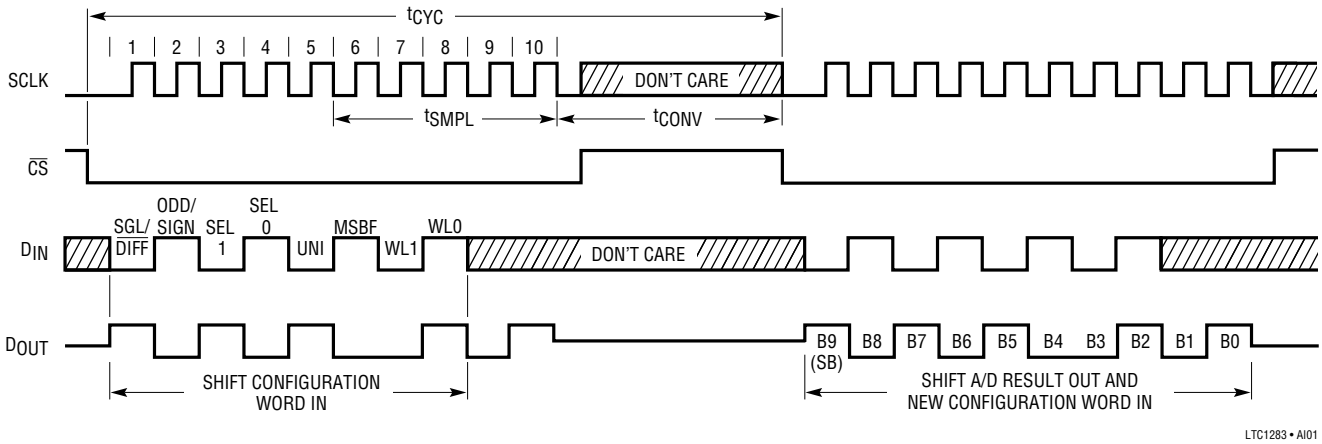


2. Input Data Word

The LTC1283 8-bit input data word is clocked into the D_{IN} input on the first eight rising SCLK edges after chip select is recognized. Further inputs on the D_{IN} pin are then ignored until the next $\overline{CS}$ cycle. The eight bits of the input word are defined as follows:



Operating Sequence
(Example: Differential Inputs (CH3-CH2), Bipolar, MSB-First and 10-Bit Word Length)



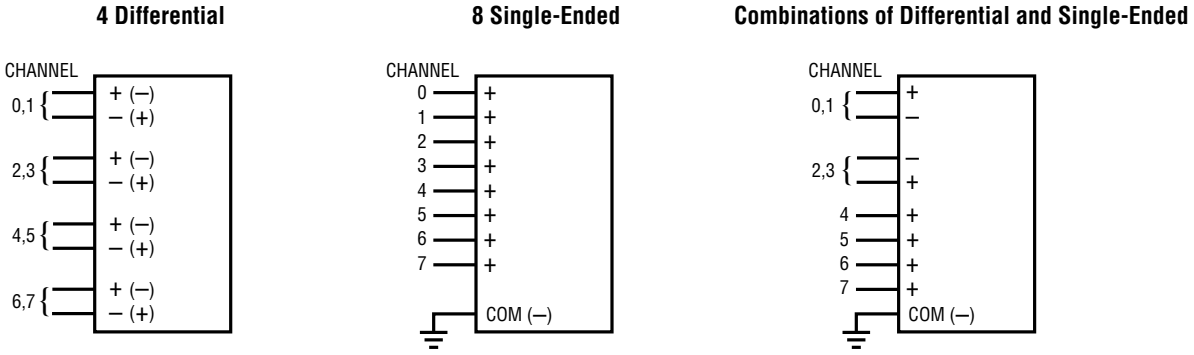
APPLICATIONS INFORMATION

Multiplexer (MUX) Address

The first four bits of the input word assign the MUX configuration for the requested conversion. For a given channel selection, the converter will measure the voltage between the two channels indicted by the + and – signs in the selected row of Table 1. Note that in differential mode (SGL/$\overline{\text{DIFF}}$ = 0) measurements are limited to four adjacent input pairs with either polarity. In single-ended mode, all input channels are measured with respect to COM. Figure 1 shows some examples of multiplexer assignments.

Table 1. Multiplexer Channel Selection

MUX ADDRESS				DIFFERENTIAL CHANNEL SELECTION								MUX ADDRESS				SINGLE-ENDED CHANNEL SELECTION								
SGL/ $\overline{\text{DIFF}}$	ODD/ SIGN	SELECT 1	0	0	1	2	3	4	5	6	7	SGL/ $\overline{\text{DIFF}}$	ODD/ SIGN	SELECT 1	0	0	1	2	3	4	5	6	7	COM
0	0	0	0	+	–							1	0	0	0	+								–
0	0	0	1			+	–					1	0	0	1			+						–
0	0	1	0					+	–			1	0	1	0					+				–
0	0	1	1							+	–	1	0	1	1							+		–
0	1	0	0	–	+							1	1	0	0		+							–
0	1	0	1			–	+					1	1	0	1				+					–
0	1	1	0					–	+			1	1	1	0						+			–
0	1	1	1							–	+	1	1	1	1								+	–



Changing the MUX Assignment "On the Fly"

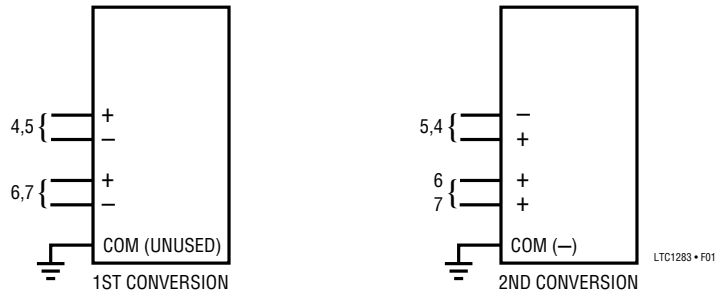


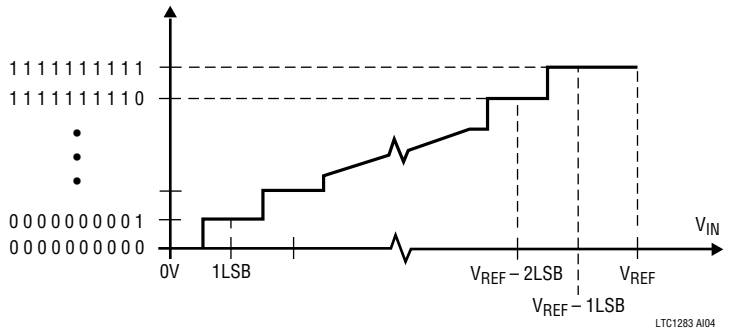
Figure 1. Examples of Multiplexer Options on the LTC1283

APPLICATIONS INFORMATION

Unipolar/Bipolar (UNI)

The fifth input bit (UNI) determines whether the conversion will be unipolar or bipolar. When UNI is a logical one, a unipolar conversion will be performed on the selected input voltage. When UNI is a logical zero, a bipolar conversion will result. The input span and code assignment for each conversion type are shown in the figures below.

Unipolar Transfer Curve (UNI = 1)

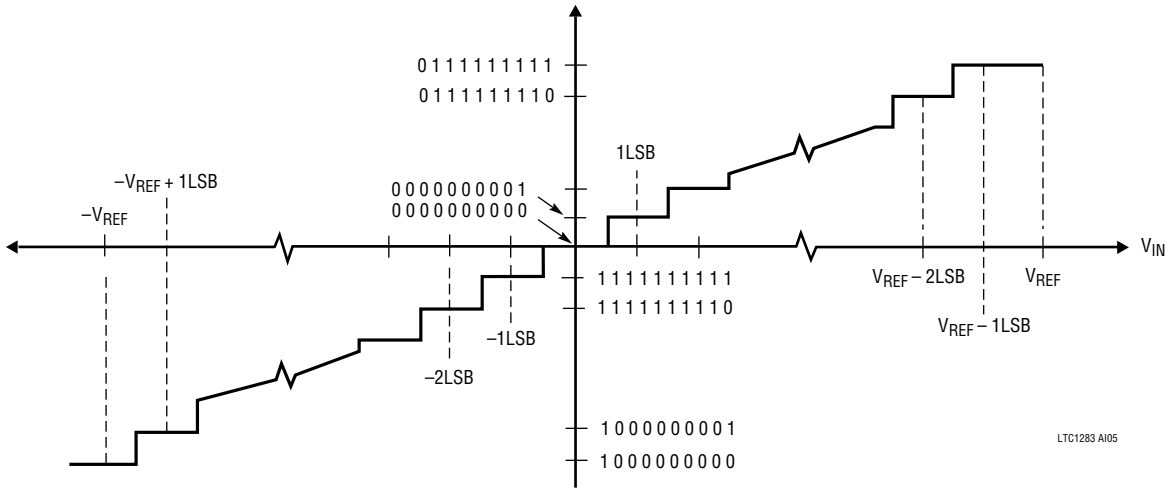


Unipolar Output Code (UNI = 1)

OUTPUT CODE	INPUT VOLTAGE	INPUT VOLTAGE (V_{REF} = 2.5V)
1111111111	V_{REF} – 1LSB	2.4976V
1111111110	V_{REF} – 2LSB	2.4951V
•	•	•
•	•	•
•	•	•
0000000001	1LSB	0.0024V
0000000000	0V	0V

LTC1283 AI06

Bipolar Transfer Curve (UNI = 0)



Bipolar Output Code (UNI = 0)

OUTPUT CODE	INPUT VOLTAGE	INPUT VOLTAGE (V_{REF} = 2.5V)
0111111111	V_{REF} – 1LSB	2.4951V
0111111110	V_{REF} – 2LSB	2.4902V
•	•	•
•	•	•
•	•	•
0000000001	1LSB	0.0049V
0000000000	0V	0V
1111111111	–1LSB	–0.0049V
1111111110	–2LSB	–0.0098V
•	•	•
•	•	•
•	•	•
1000000001	–(V_{REF}) + 1LSB	–2.4951V
1000000000	–(V_{REF})	–2.5000V

LTC1283 AI07

APPLICATIONS INFORMATION

MSB-First/LSB-First Format (MSBF)

The output data of the LTC1283 is programmed for MSB-first or LSB-first sequence using the MSBF bit. For MSB-first output data the input word clocked to the LTC1283 should always contain a logical one in the sixth bit location (MSBF bit). Likewise for LSB-first output data, the input word clocked to the LTC1283 should always contain a zero in the MSBF bit location. The MSBF bit in a given D_{IN} word will control the order of the next D_{OUT} word. The MSBF bit affects only the order of the output data word. The order of the input word is unaffected by this bit.

MSBF	OUTPUT FORMAT
0	LSB-First
1	MSB-First

LTC1283 AI08

Word Length (WL1, WL0)

The last two bits of the input word (WL1 and WL0) program the output data word length of the LTC1283. Word lengths of 8-, 10-, 12- or 16-bit can be selected according to the following table. The WL1 and WL0 bits in a given D_{IN} word control the length of the present, not the next, D_{OUT} word. **WL1 and WL2 are never "don't cares"** and must be set for the correct D_{OUT} word length even when a "dummy" D_{IN} word is sent. On any transfer cycle, the word length should be made equal to the number of SCLK cycles sent by the MPU.

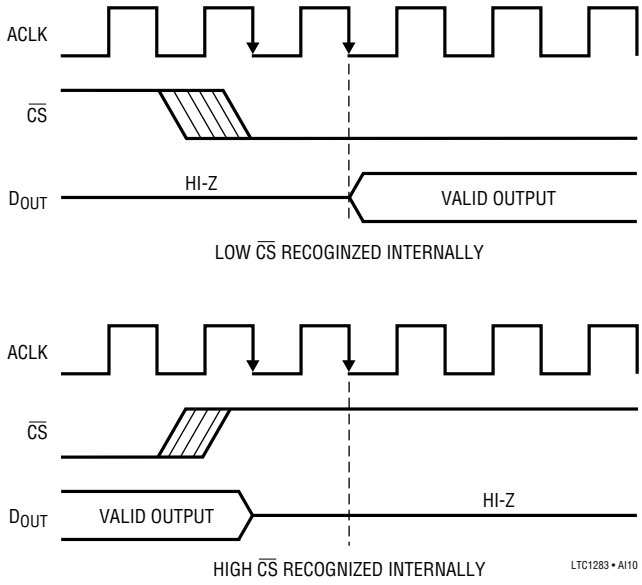
WL1	WL0	OUTPUT WORD LENGTH
0	0	8 Bits
0	1	10 Bits
1	0	12 Bits
1	1	16 Bits

LTC1283 • AI09

Figure 2 shows how the data output (D_{OUT}) timing can be controlled with word length selection and MSB/LSB-first format selection.

3. Deglitcher

A deglitching circuit has been added to the chip select input of the LTC1283 to minimize the effects of errors caused by noise on that input. This circuit ignores changes in state on the $\overline{CS}$ input that are shorter in duration than 1 ACLK cycle. After a change of state on the $\overline{CS}$ input, the LTC1283 waits for two falling edges of the ACLK before recognizing a valid chip select. One indication of $\overline{CS}$ low recognition is the D_{OUT} line becoming active (leaving the Hi-Z state). Note that the deglitching applies to both the rising and falling $\overline{CS}$ edges.



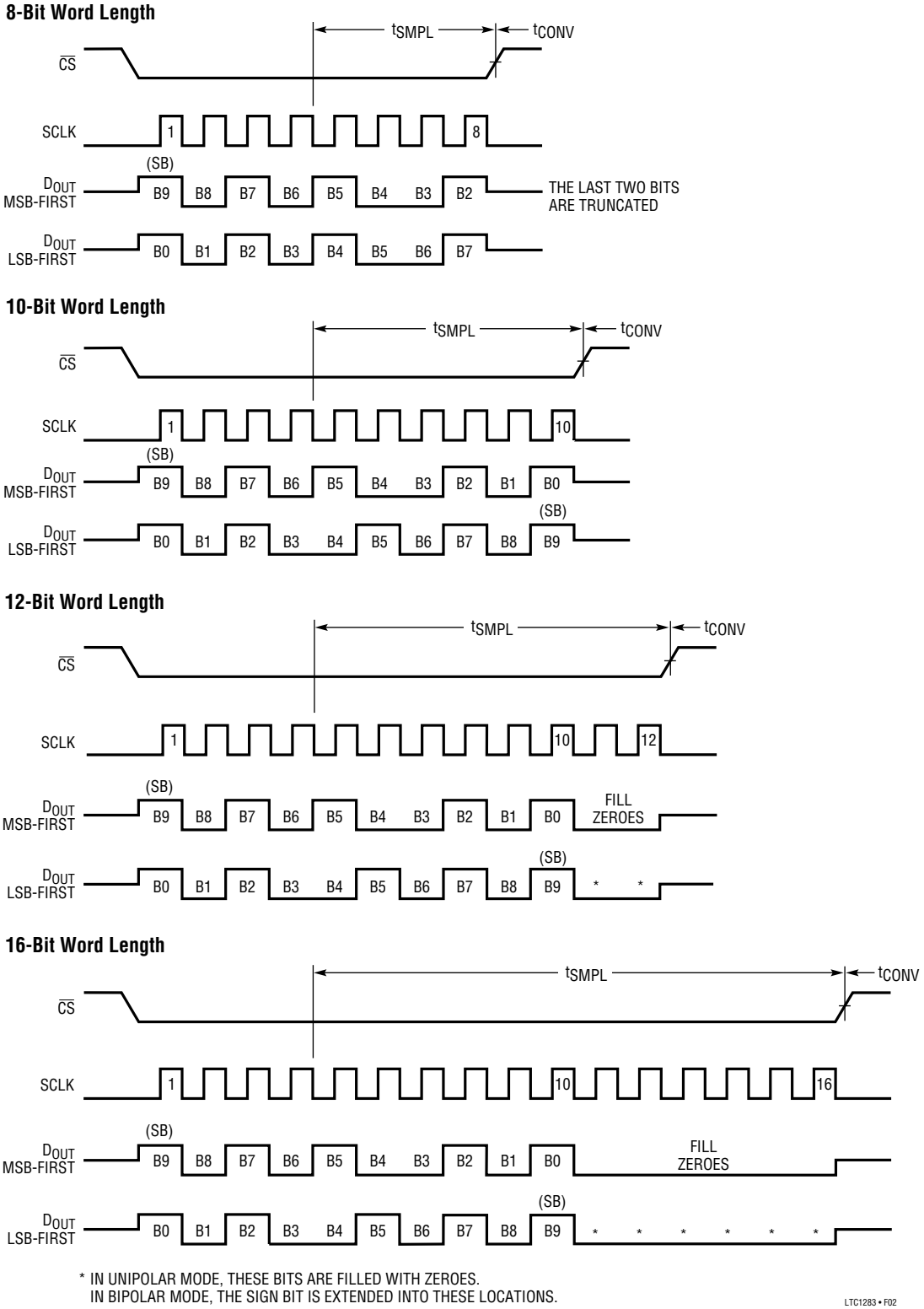
4. $\overline{CS}$ Low During Conversion

In the normal mode of operation, $\overline{CS}$ is brought high during the conversion time (see Figure 3). The serial port ignores any SCLK activity while $\overline{CS}$ is high. The LTC1283 will also operate with $\overline{CS}$ low during the conversion. In this mode, SCLK must remain low during the conversion as shown in Figure 4. After the conversion is complete, the D_{OUT} line will become active with the first output bit. Then the data transfer can begin as normal.

5. Microprocessor Interfaces

The LTC1283 can interface directly (without external hardware) to most popular microprocessor (MPU) synchronous serial formats (see Table 2). If an MPU without a serial interface is used, then four of the MPU's parallel port lines can be programmed to form the serial link to the LTC1283. Included here are three serial interface examples and one example showing a parallel port programmed to form the serial interface.

APPLICATIONS INFORMATION



* IN UNIPOLAR MODE, THESE BITS ARE FILLED WITH ZEROES.
IN BIPOLAR MODE, THE SIGN BIT IS EXTENDED INTO THESE LOCATIONS.

LTC1283 • F02

Figure 2. Data Output (D_{OUT}) Timing with Different Word Lengths

APPLICATIONS INFORMATION

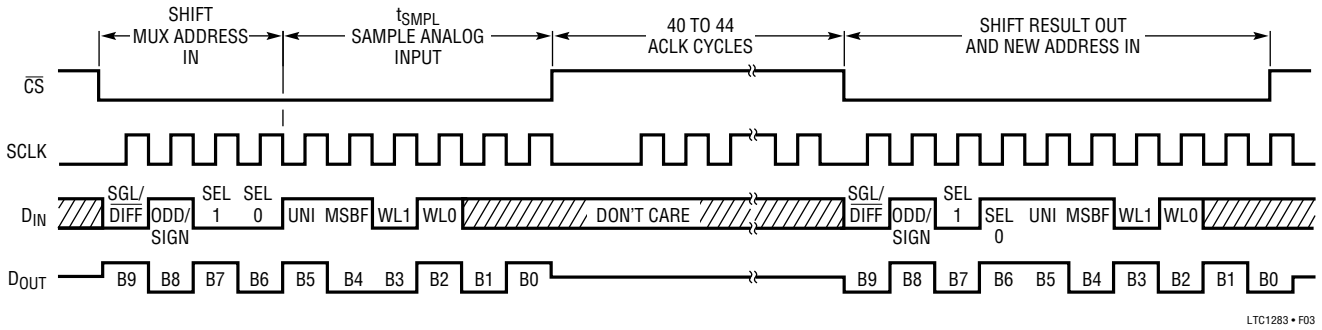


Figure 3. $\overline{CS}$ High During Conversion

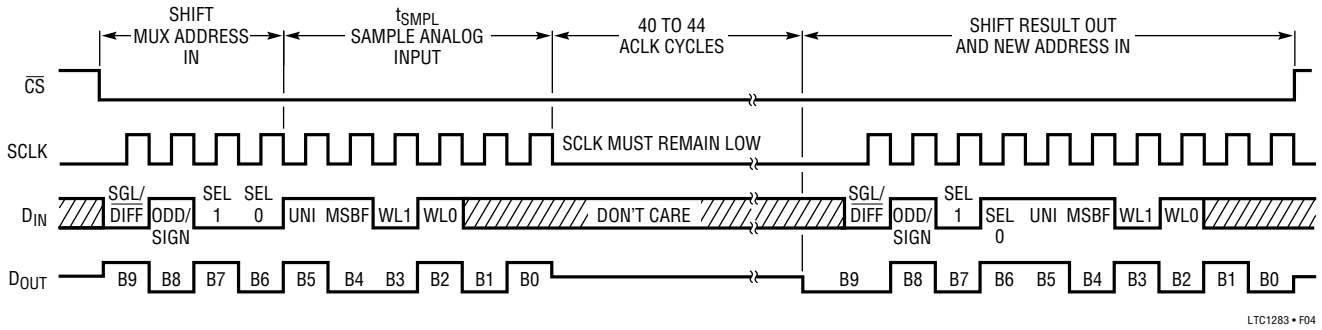


Figure 4. $\overline{CS}$ Low During Conversion

Table 2. 3V Microprocessor with Hardware Serial Interfaces Compatible with the LTC1283*

PART NUMBER	TYPE OF INTERFACE
Motorola	
MC68HC11	SPI
MC68HC05	SPI
RCA	
CDP68HC05	SPI
National Semiconductor	
COP800 Family	MICROWIRE/PLUS†
HPC16000 Family	MICROWIRE/PLUS†
Texas Instruments	
TMS70C02	Serial Port
TMS70C42	Serial Port

*Contact factory for interface information for processors not on this list
†MICROWIRE/PLUS is a trademark of National Semiconductor Corp.

Serial Port Microprocessors

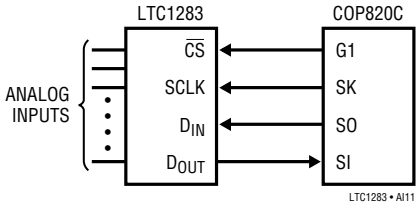
Most synchronous serial formats contain a shift clock (SCLK) and two data lines, one for transmitting and one for receiving. In most cases data bits are transmitted on the falling edge of the clock (SCLK) and captured on the rising edge. However, serial port formats vary among MPU manufacturers as to the smallest number of bits that can be sent in one group (e.g., 4-bit, 8-bit or 16-bit transfers). They also vary as to the order in which the bits are transmitted (LSB- or MSB-first). The following examples show how the LTC1283 accommodates these differences.

National MICROWIRE (COP820C)

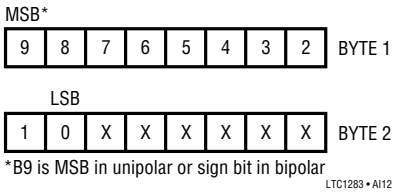
The COP820C transfers data MSB-first and in 8-bit increments. This is easily accommodated by setting the LTC1283 to MSB-first format and 10-bit word length. The data output word is then received by the COP820C in one 8-bit block and one 2-bit block.

APPLICATIONS INFORMATION

Hardware and Software Interface to National Semiconductor COP820C Processor



D_{OUT} from LTC1283 stored in COP820C RAM

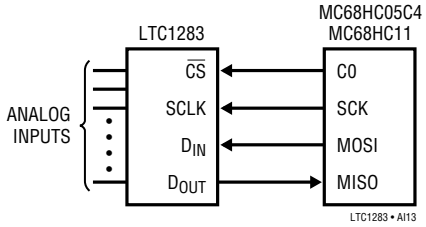


MNEMONIC	COMMENTS	MNEMONIC	COMMENTS
LD (F0)←0D	LOAD 0D INTO F0 (D_{IN})	X(A)←→(E9)	LOAD D_{OUT} INTO ACC
LD (D5)←32	CONFIGURE PORT G	SBIT 2	TRANSFER CONTINUES
LD (EE)←8	CONFIGURE CONTROL REG.	X (A)←→(F3)	LOAD D_{OUT} IN ADDR F3
LD (B)←D4	PORT G DATA REG. INTO B	RBIT 2	STOP TRANSFER
LD (A)←(F0)	LOAD D_{IN} INTO ACC	LD (B)←D4	PUT PORT G ADDR IN B
RBIT 1	G1 RESET ($\overline{CS}$ GOES LOW)	SBIT 1	G1 SET ($\overline{CS}$ GOES HIGH)
X (A)←→(E9)	LOAD D_{IN} INTO SHIFT REG.	X (A)←→(E9)	LOAD D_{OUT} INTO ACC
LD (B)←EF	LOAD PSW REG. ADDR IN B	RC	CLEAR CARRY
SBIT 2	TRANSFER BEGINS	RRCA	SHIFT RIGHT THRU CARRY
↑		RRCA	SHIFT RIGHT THRU CARRY
NOP	15 NOPs FOR TIMING	RRCA	SHIFT RIGHT THRU CARRY
↓		X (A)←→(F4)	LOAD D_{OUT} IN ADDR F4

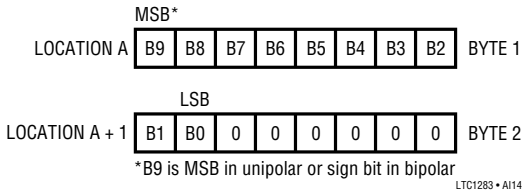
Motorola SPI (MC68HC05C4, MC68HC11)

The MC68HC05C4 and MC68HC11 transfer data MSB-first and in 8-bit increments. Programming the LTC1283 for MSB-first format and 16-bit word length allows the 10-bit data output to be received by the MPU as two 8-bit bytes with the final 6 unused bits filled with zeroes by the LTC1283.

Hardware and Software Interface to Motorola MC68HC05C4 and MC68HC11 Processors



D_{OUT} from LTC1283 stored in MC68HC05C4 or MC68HC11 RAM



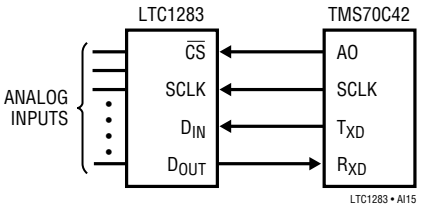
MNEMONIC	COMMENTS	MNEMONIC	COMMENTS
BCLR n	C0 IS CLEARED ($\overline{CS}$ GOES LOW)	STA	START NEXT SPI CYCLE
LDA	LOAD D_{IN} FOR LTC1283 INTO ACC	↑	
STA	LOAD D_{IN} FROM ACC TO SPI DATA REG. START SCK	NOP	6 NOPs FOR TIMING
↑		↓	
NOP	8 NOPs FOR TIMING	BSET n	C0 IS SET ($\overline{CS}$ GOES HIGH)
↓		LDA	LOAD CONTENTS OF SPI STATUS REG. INTO ACC
LDA	LOAD CONTENTS OF SPI STATUS REG. INTO ACC	LDA	LOAD LTC1283 D_{OUT} FROM SPI DATA REG.
LDA	LOAD LTC1283 D_{OUT} FROM SPI DATA REG. INTO ACC (BYTE 1)		INT ACC (BYTE 2)
		STA	LOAD LTC1283 INTO RAM (LOCATION A +1)
STA	LOAD LTC1283 D_{OUT} INTO RAM (LOCATION A)		

APPLICATIONS INFORMATION

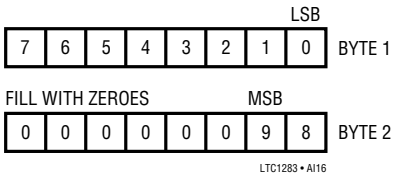
Texas Instruments TMS70C42

The TMS70C42 transfers serial data in 8-bit increments, LSB-first. To accommodate this, the LTC1283 is programmed for 16-bit word length and LSB-first format. The 10-bit output data is received by the processor as two 8-bit bytes, LSB-first. The LTC1283 fills the final 6 unused bits (after the MSB) with zeroes.

Hardware and Software Interface to TI TMS70C42 Processor



D_{OUT} from LTC1283 stored in TMS70C42 RAM

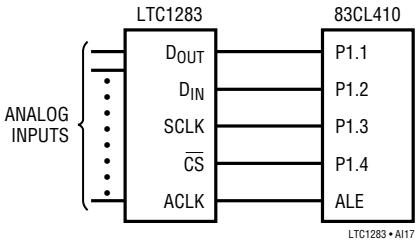


LABEL	MNEMONIC		DESCRIPTION
START	DINT		DISABLES ALL INTERRUPTS
	MOVP	% > 2A, P0	DISABLE INTERRUPT FLAGS
	MOVP	% > 02, P16	DISABLE INTERRUPT FLAGS
	MOV	% > 60, B	ADDRESS OF STACK
	LDSP		PUT ADDRESS INTO POINTER
	MOVP	% > DF, P5	CONFIGURE PORT A
	MOVP	% > 08, P6	ENABLE Tx BY SETTING B3 = 1
	MOVP	% > 40, P21	RESET THE SERIAL PORT
	MOVP	% > 0C, P20	CONFIGURE THE SERIAL PORT
	MOVP	% > 00, P24	TURN START BIT OFF
	MOVP	% > 00, P21	ENABLE THE SERIAL PORT
	MOVP	% > 00, P23	SET SCLK RATE (TIMER 3)
	MOVP	% > C0, P24	START TIMER
LOOP	MOV	% > DF, A	LOAD D_{IN} WORD IN A
	CALL	SXTNBIT	ROUTINE THAT SHIFTS DATA
	MOV	B, R5	PUT FIRST 8 LSBs IN R5
	MOV	A, R6	PUT MSBs IN R6
SXTNBIT	ANDP	% > FE, P4	A0 CLEARED (CS GOES LOW)
	MOVP	A, P26	PUT D_{IN} INTO TXBUF
	MOVP	% > 40, P24	SCLK OFF (TIMER 3 DISABLED)
	MOVP	% > 17, P21	ENABLE SERIAL PORT
	MOVP	% > C0, P24	SCLK ON (TRANSFER BEGINS)
	MOVP	% > 16, P21	TXEN GOES LOW
	MOV	% > 02, A	LOAD COUNTER
WAIT1	DJNZ	A, WAIT1	LOOP WHILE SHIFT OCCURS
	NOP		DELAY
	MOVP	P25, B	PUT D_{OUT} IN B
	MOVP	A, P26	LOAD TXBUF
	MOVP	% > 40, P24	SCLK OFF (TIMER 3 DISABLE)
	MOVP	% > 17, P21	ENABLE SERIAL PORT
	MOVP	% > C0, P24	SCLK ON (TRANSFER BEGINS)
	MOVP	% > 16, P21	TXEN GOES LOW
	MOV	% > 02, A	LOAD COUNTER
WAIT2	DJNZ	A, WAIT2	LOOP WHILE SHIFT OCCURS
	NOP		DELAY
	MOVP	P25, A	PUT D_{OUT} IN A
	ORP	% > 01, P4	A0 SET (CS GOES HIGH)
	RETS		RETURN TO MAIN PROGRAM

Parallel Port Microprocessors

When interfacing the LTC1283 to an MPU which has a parallel port, the serial signals are created on the port with software. Three MPU port lines are programmed to create the CS, SCLK and D_{IN} signals for the LTC1283. A fourth port line reads the D_{OUT} line. An example is made of the Signetics 83CL410.

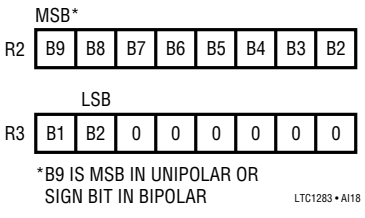
Hardware and Software Interface to Signetics 83CL410 Processor



Signetics 83CL410

To interface to the 83CL410, (a 3V version of the 80C51) the LTC1283 is programmed for MSB-first format and 10-bit word length. The 83CL410 generates CS, SCLK and D_{IN} on three port lines and reads D_{OUT} on the fourth.

D_{OUT} from LTC1283 stored in 83CL410 RAM



APPLICATIONS INFORMATION

83CL410 Code

MNEMONIC		DESCRIPTION	MNEMONIC		DESCRIPTION
	MOV P1, #02H	INITIALIZE PORT 1 (BIT 1 IS MADE AN INPUT)		MOV C, P1.1	READ DATA BIT INTO CARRY
				CLR A	CLEAR ACC
	CLR P1.3	SCLK GOES LOW		RLC A	ROTATE DATA BIT INTO ACC
	SETB P1.4	$\overline{CS}$ GOES LOW		SETB P1.3	SCLK GOES HIGH
CONTINUE:	MOV A, #0DH	D_{IN} WORD FOR THE LTC1283 IS PLACED IN ACC		CLR P1.3	SCLK GOES LOW
				MOV C, P1.1	READ DATA BIT IN CARRY
	CLR P1.4	$\overline{CS}$ GOES LOW		RRC A	ROTATE RIGHT INTO ACC
	MOV R4, #08	LOAD COUNTER		RRC A	ROTATE RIGHT INTO ACC
	NOP	DELAY FOR DEGLITCHER		MOV R3, A	STORE LSBs IN R3
LOOP:	MOV C, P1.1	READ DATA BIT INTO CARRY		SETB P1.3	SCLK GOES HIGH
	RLC A	ROTATE DATA BIT INTO ACC		CLR P1.3	SCLK GOES LOW
	MOV P1.2, C	OUTPUT D_{IN} BIT TO LTC1283		SETB P1.4	$\overline{CS}$ GOES HIGH
	SETB P1.3	SCLK GOES HIGH		MOV R5, #07H	LOAD COUNTER
	CLR P1.3	SCLK GOES LOW	DELAY:	DJNZ R5, DELAY	DELAY FOR LTC1283 TO PERFORM CONVERSION
	DJNZ R4, LOOP	NEXT BIT			
	MOV R2, A	STORE MSBs IN R2		AJMP CONTINUE	REPEAT PROGRAM

6. Sharing the Serial Interface

The LTC1283 can share the same 3-wire serial interface with other peripheral components or other LTC1283s (see Figure 5). In this case, the $\overline{CS}$ signals decide which LTC1283 is being addressed by the MPU.

ANALOG CONSIDERATIONS

1. Grounding

The LTC1283 should be used with an analog ground plane and single point grounding techniques.

Pin 11 (AGND) should be tied directly to this ground plane.

Pin 10 (DGND) can also be tied directly to this ground plane because minimal digital noise is generated within the chip itself.

Pin 20 (V_{CC}) should be bypassed to the ground plane with a 4.7µF tantalum with leads as short as possible. Pin 12 (V^-) should be bypassed with a 0.1µF ceramic disk. For single supply applications, V^- can be tied to the ground plane.

It is also recommended that pin 13 (REF^-) and pin 9 (COM) be tied directly to the ground plane. All analog inputs should be referenced directly to the single point ground. Digital inputs and outputs should be shielded from and/or routed away from the reference and analog circuitry.

Figure 6 shows an example of an ideal ground plane design for a two-sided board. Of course this much ground plane will not always be possible, but users should strive to get as close to this ideal as possible.

2. Bypassing

For good performance, V_{CC} must be free of noise and ripple. Any changes in the V_{CC} voltage with respect to analog ground during a conversion cycle can induce errors

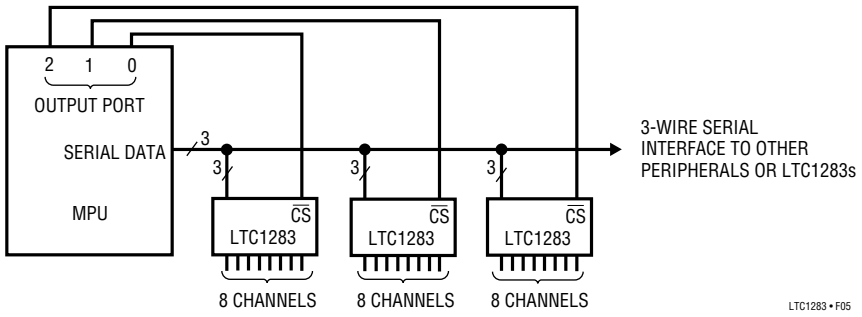


Figure 5. Several LTC1283s Sharing One 3-Wire Serial Interface

APPLICATIONS INFORMATION

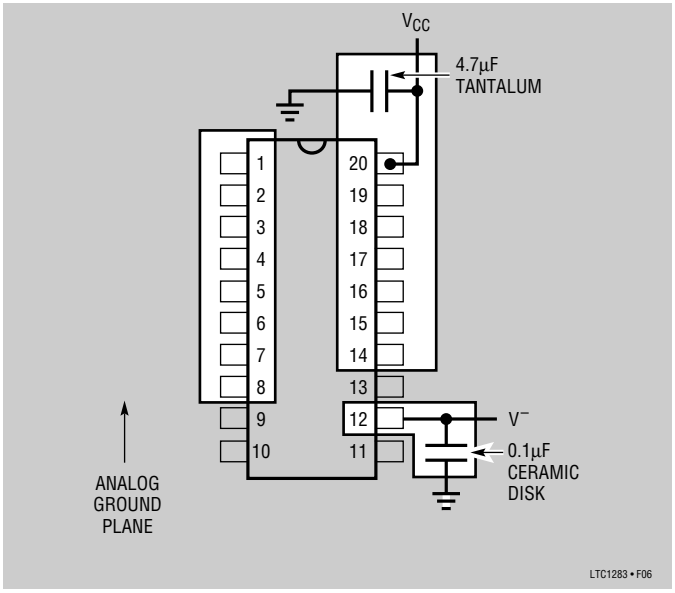


Figure 6. Example Ground Plane for the LTC1283

or noise in the output code. V_{CC} noise and ripple can be kept below 1mV by bypassing the V_{CC} pin directly to the analog ground plane with a 4.7µF tantalum with leads as short as possible. Figures 7 and 8 show the effects of good and poor V_{CC} bypassing.

3. Analog Inputs

Because of the capacitive redistribution A/D conversion techniques used, the analog inputs of the LTC1283 have capacitive switching input current spikes. These current spikes settle quickly and do not cause a problem.

However, if large source resistances are used or if slow settling op amps drive the inputs, care must be taken to insure that the transients caused by the current spikes settle completely before the conversion begins.

Source Resistance

The analog inputs of the LTC1283 look like 65pF capacitor (C_{IN}) in series with a 500Ω resistor (R_{ON}) as shown in Figure 9. C_{IN} gets switched between the selected "+" and "–" inputs once during each conversion cycle. Large external source resistors and capacitances will slow the settling of the inputs. It is important that the overall RC time constants be short enough to allow the analog inputs to completely settle within the allowed time.

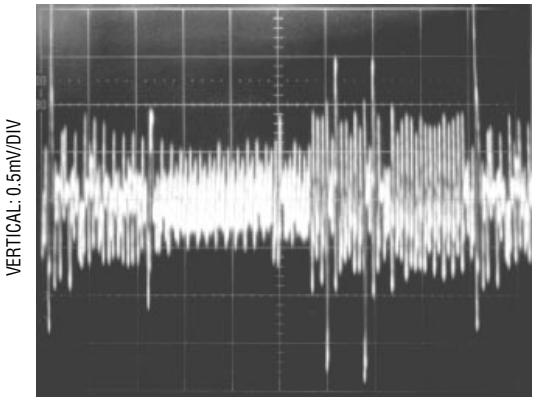


Figure 7. Poor V_{CC} Bypassing. Noise and Ripple can Cause A/D Errors

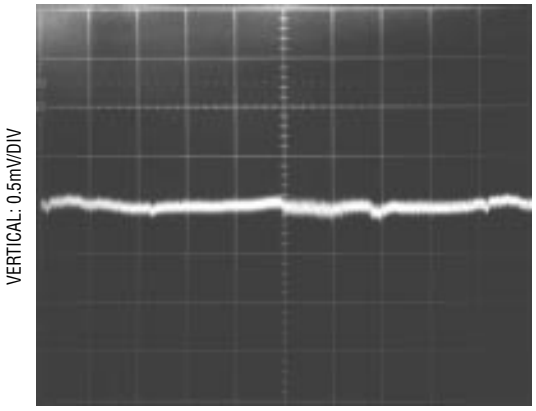


Figure 8. Good V_{CC} Bypassing Keeps Noise and Ripple on V_{CC} Below 1mV

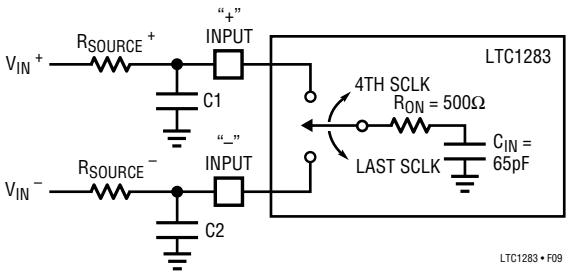


Figure 9. Analog Input Equivalent Circuit

APPLICATIONS INFORMATION

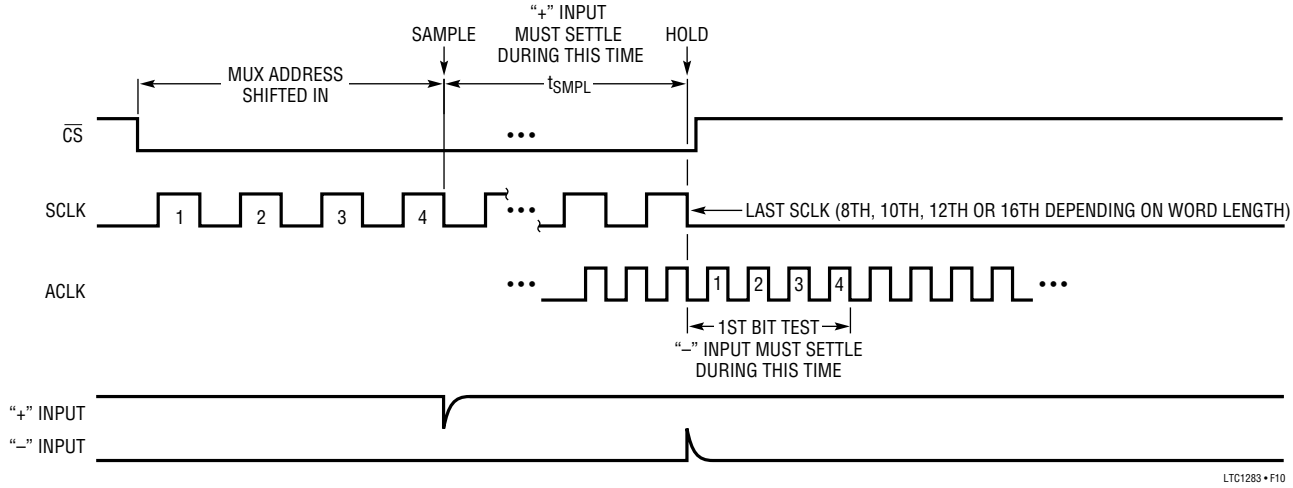


Figure 10. "+" and "–" Input Settling Windows

"+" Input Settling

This input capacitor is switched onto the "+" input during the sample phase (t_{SMPL}, see Figure 10). The sample phase starts at the 4th SCLK cycle and lasts until the falling edge of the last SCLK (the 8th, 10th, 12th or 16th SCLK cycle depending on the selected word length). The voltage on the "+" input must settle completely within this sample time. Minimizing R_{SOURCE}^+ and C1 will improve the input settling time. If large "+" input source resistance must be used, the sample time can be increased by using a slower SCLK frequency or selecting a longer word length. With the minimum possible sample time of 8µs, **R_{SOURCE}^+ < 2k and C1 < 20pF will provide adequate settling.**

"–" Input Settling

At the end of the sample phase the input capacitor switches to the "–" input and the conversion starts (see Figure 10). During the conversion, the "+" input voltage is effectively "held" by the sample-and-hold and will not affect the conversion result. However, it is critical that the "–" input voltage be free of noise and settle completely during the first four ACLK cycles of the conversion time. Minimizing R_{SOURCE}^- and C2 will improve settling time. If large "–" input source resistance must be used, the time allowed for settling can be extended by using a slower ACLK frequency. At the maximum ACLK rate of 1MHz, **R_{SOURCE}^- < 1k and C2 < 20pF will provide adequate settling.**

Input Op Amps

When driving the analog inputs with an op amp it is important that the op amp settle within the allowed time (see Figure 10). Again, the "+" and "–" input sampling times can be extended as described above to accommodate slower op amps. Most op amps including the LT1006 and LT1013 single supply op amps can be made to settle well even with the minimum settling windows of 8µs ("+" input) and 4µs ("–" input) which occur at the maximum clock rates (ACLK = 1MHz and SCLK = 0.5MHz). Figures 11 and 12 show examples of adequate and poor op amp settling.

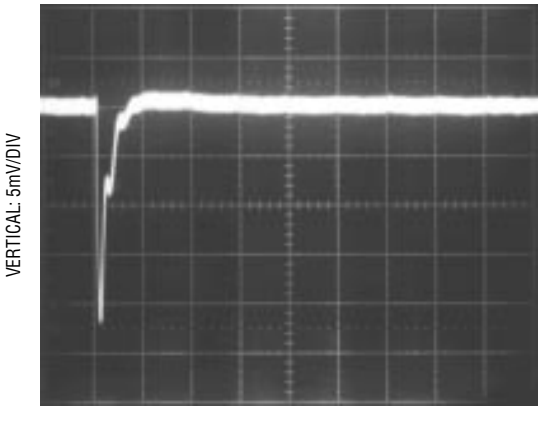


Figure 11. Adequate Settling of Op Amp Driving Analog Input

APPLICATIONS INFORMATION

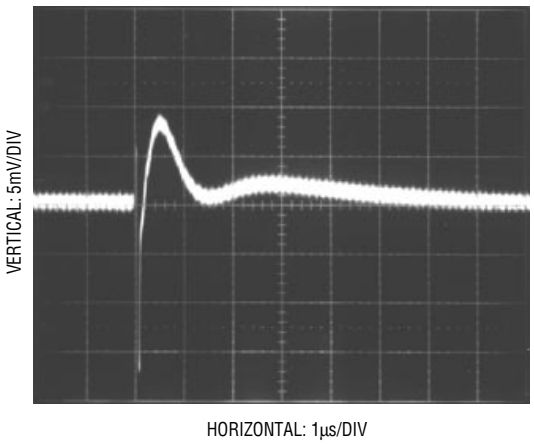


Figure 12. Poor Op Amp Settling Can Cause A/D Errors

RC Input Filtering

It is possible to filter the inputs with an RC network as shown in Figure 13. For large values of C_F (e.g., 1µF), the capacitive input switching currents are averaged into a net DC current. Therefore, a filter should be chosen with small resistor and large capacitor to prevent DC drops across the resistor. The magnitude of the DC current is approximately $I_{DC} = 65pF \times V_{IN}/t_{CYC}$ and is roughly proportional to V_{IN}. When running at the minimum cycle time of 68µs, the input current equals 2.5µA at V_{IN} = 2.5V. In this case, a filter resistor of 100Ω will cause 0.1LSB of full-scale error. If a larger filter resistor must be used, errors can be eliminated by increasing the cycle time as shown in the typical curve Maximum Filter Resistor vs Cycle Time.

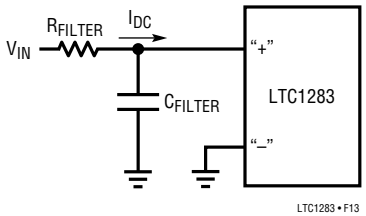


Figure 13. RC Input Filtering

Input Leakage Current

Input leakage currents can also create errors if the source resistance gets too large. For instance, the maximum input leakage specification of 1µA (at 125°C) flowing through a source resistance of 1k will cause a voltage drop of 1mV or 0.4LSB. This error will be much reduced at lower temperatures because leakage drops rapidly (see typical curve of Input Channel Leakage Current vs Temperature).

Noise Coupling into Inputs

High source resistance input signals (>500Ω) are more sensitive to coupling from external sources. It is preferable to use channels near the center of the package (i.e., CH2-CH7) for signals which have the highest output resistance because they are essentially shielded by the pins of the package ends (DGND and CH0). Grounding any unused inputs (especially the end pin, CH0) will also reduce outside coupling into high source resistances.

4. Sample-and-Hold

Single-Ended Inputs

The LTC1283 provides a built-in sample-and-hold (S&H) function for all signals acquired in the single-ended mode (COM pin grounded). This sample-and-hold allows the LTC1283 to convert rapidly varying signals (see typical curve of S&H Acquisition Time vs Source Resistance). The input voltage is sampled during the t_{SMPL} time as shown in Figure 10. The sampling interval begins after the fourth MUX address bit is shifted in and continues during the remainder of the data transfer. On the falling edge of the final SCLK, the S&H goes into hold mode and the conversion begins. The voltage will be held on either the 8th, 10th, 12th or 16th falling edge of the SCLK depending on the word length selected.

Differential Inputs

With differential inputs, or when the COM pin is not tied to ground, the A/D no longer converts just a single voltage but rather the difference between two voltages. In these cases, the voltage on the selected "+" input is still sampled and held and therefore may be rapidly time varying just as in single-ended mode. However, the voltage on the selected "–" input must remain constant and be free of noise and ripple throughout the conversion time. Otherwise, the

APPLICATIONS INFORMATION

differencing operation may not be performed accurately. The conversion time is 44 ACLK cycles. Therefore, a change in the "–" input voltage during this interval can cause conversion errors. For a sinusoidal voltage on the "–" input this error would be:

$$V_{ERROR\ (MAX)} = V_{PEAK} \times 2 \times \pi \times f("-") \times 44/f_{ACLK}$$

Where f("–") is the frequency of the "–" input voltage, V_{PEAK} is its peak amplitude and f_{ACLK} is the frequency of the ACLK. In most cases V_{ERROR} will not be significant. For a 60Hz signal on the "–" input to generate a 1/4LSB error (0.61mV) with the converter running at ACLK = 1MHz, its peak value would have to be 38mV.

5. Reference Inputs

The voltage between the reference inputs of the LTC1283 defines the voltage span of the A/D converter. The reference inputs look primarily like a 10k resistor but will have transient capacitive switching currents due to the switched-capacitor conversion technique (see Figure 14). During each bit test of the conversion (every 4 ACLK cycles), a capacitive current spike will be generated on the reference pins by the A/D. These current spikes settle quickly and do not cause a problem. However, if slow settling circuitry is used to drive the reference inputs, care must be taken to insure that transients caused by these current spikes settle completely during each bit test of the conversion.

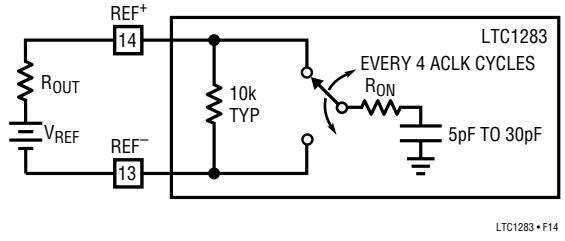


Figure 14. Reference Input Equivalent Circuit

When driving the reference inputs, three things should be kept in mind:

1. The source resistance (R_{OUT}) driving the reference inputs should be low (less than 1Ω) to prevent DC drops caused by the 300μA maximum reference current (I_{REF}).
2. Transients on the reference inputs caused by the capacitive switching currents must settle completely during each bit test (each 4 ACLK cycles). Figures 15 and 16 show examples of both adequate and poor settling. Using a slower ACLK will allow more time for the reference to settle. However, even at the maximum ACLK rate of 1MHz most references and op amps can be made to settle within the 4μs bit time.
3. It is recommended that the REF^- input be tied directly to the analog ground plane. If REF^- is biased at a voltage other than ground, the voltage must not change during a conversion cycle. This voltage must also be free of noise and ripple with respect to analog ground.

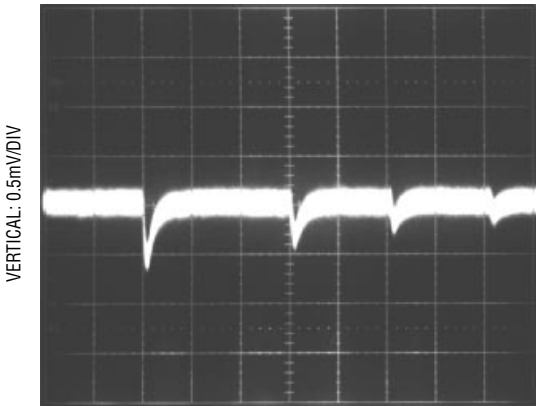


Figure 15. Adequate Reference Settling

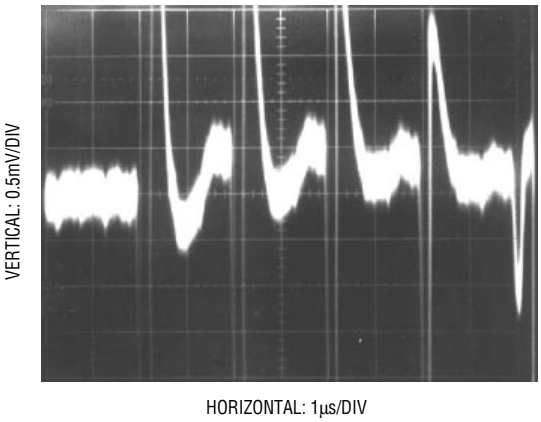


Figure 16. Poor Reference Settling Can Cause A/D Errors

6. Reduced Reference Operation

The effective resolution to the LTC1283 can be increased by reducing the input span of the converter. The LTC1283 exhibits good linearity and gain over a wide range of reference voltages (see typical curves of Linearity and Gain Error vs Reference Voltage). However, care must be taken

APPLICATIONS INFORMATION

when operating at low values of V_{REF} because of the reduced LSB step size and the resulting higher accuracy requirement placed on the converter. The following factors must be considered when operating at low V_{REF} values.

1. Conversion speed (ACLK frequency)
2. Offset
3. Noise

Conversion Speed with Reduced V_{REF}

With reduced reference voltages, the LSB step size is reduced and the LTC1283 internal comparator overdrive is reduced. With less overdrive, more time is required to perform a conversion. Therefore, the maximum ACLK frequency should be reduced when low values of V_{REF} are used. This is shown in the typical curve of Maximum Conversion Clock Rate vs Reference Voltage.

Offset with Reduced V_{REF}

The offset of the LTC1283 has a larger effect on the output code when the A/D is operated with reduced reference voltage. The offset (which is typically a fixed voltage) becomes a larger fraction of an LSB as the size of the LSB is reduced. The typical curve of Unadjusted Offset Error vs Reference Voltage shows how offset in LSBs is related to reference voltage for a typical value of V_{OS}. For example, a V_{OS} of 0.5mV which is 0.2LSB with a 2.5V reference becomes 0.5LSB with a 1V reference and 2.5LSBs with a 0.2V reference. If this offset is unacceptable, it can be corrected digitally by the receiving system or by offsetting the "–" input to the LTC1283.

Noise with Reduced V_{REF}

The total input referred noise of the LTC1283 can be reduced to approximately 200μV peak-to-peak using a ground plane, good bypassing, good layout techniques and minimizing noise on the reference inputs. This noise is insignificant with a 2.5V reference but will become a larger fraction of an LSB as the size of the LSB is reduced. The typical curve of Noise Error vs Reference Voltage shows the LSB contribution of this 200μV of noise.

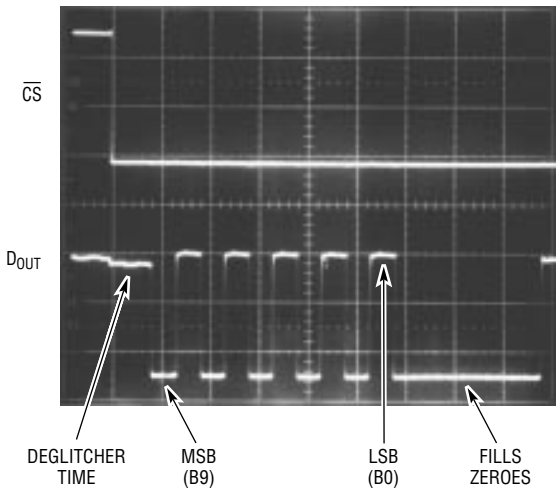
For operation with a 2.5V reference, the 200μV noise is only 0.08LSB peak-to-peak. In this case, the LTC1283 noise will contribute virtually no uncertainty to the output code. However, for reduced references, the noise may become a significant fraction of an LSB and cause undesirable jitter in the output code. For example, with a 1V reference, this same 200μV noise is 0.2LSB peak-to-peak. This will reduce the range of input voltages over which a stable output code can be achieved by 0.2LSB. If the reference is further reduced to 200mV, the 200μV noise becomes equal to one LSB and a stable code may be difficult to achieve. In this case averaging readings may be necessary.

This noise data was taken in a very clean setup. Any setup induced noise (noise or ripple on V_{CC}, V_{REF}, V_{IN} or V^-) will add to the internal noise. The lower the reference voltage to be used, the more critical it becomes to have a clean, noise-free setup.

A "Quick Look" Circuit for the LTC1283

Users can get a quick look at the function and timing of the LTC1283 by using the following simple circuit. REF^+ and D_{IN} are tied to V_{CC} selecting a 3V input span, CH7 as a single-ended input, unipolar mode, MSB-first format and 16-bit word length. ACLK and SCLK are tied together and driven by an external clock. $\overline{CS}$ is driven at 1/64 the clock rate by the CD4520 and D_{OUT} outputs the data. All other pins are tied to a ground plane. The output data from the D_{OUT} pin can be viewed on an oscilloscope which is set up to trigger on the falling edge of $\overline{CS}$.

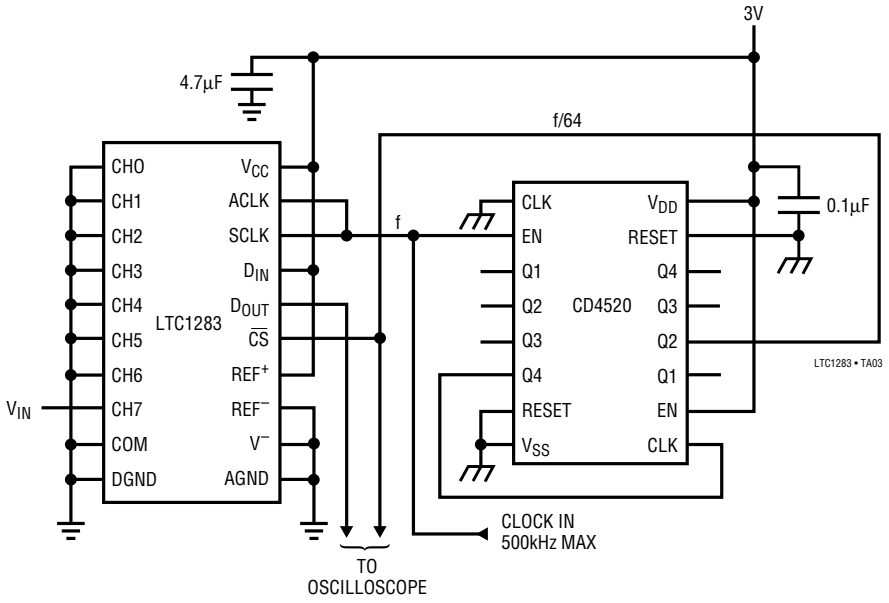
Scope Trace of LTC1283 "Quick Look" Circuit Showing A/D Output of 0101010101 (155_{HEX})



VERTICAL: 1V/DIV, HORIZONTAL: 5μs/DIV

TYPICAL APPLICATIONS

A "Quick Look" Circuit for the LTC1283

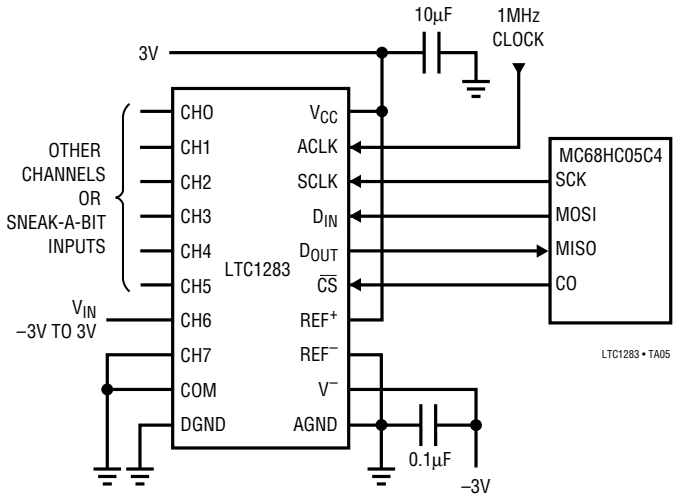


SNEAK-A-BIT™

The LTC1283's unique ability to software select the polarity of the differential inputs and the output word length is used to achieve one more bit of resolution. Using the circuit below with two conversions and some software, a 2's complement 10-bit + sign word is returned to memory inside the MPU. The MC68HC05C4 was chosen as an example; however, any processor could be used.

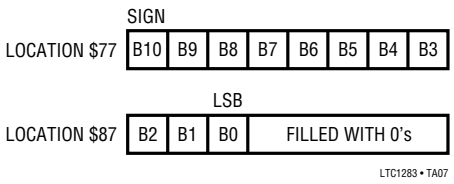
Two 10-bit unipolar conversions are performed: the first over a 0V to 3V span and the second over a 0V to –3V span (by reversing the polarity of the inputs). The sign of the input is determined by which of the two spans contain it. Then the resulting number (ranging from –1023 to 1023 decimal) is converted to 2's complement notation and stored in RAM.

SNEAK-A-BIT Circuit

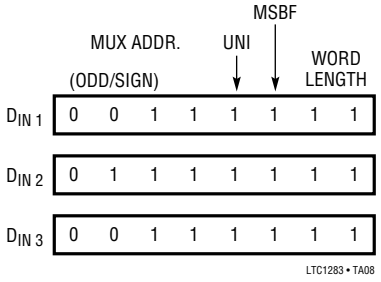


SNEAK-A-BIT Code

D_{OUT} from LTC1283 in MC68HC05C4



D_{IN} Words for LTC1283



SNEAK-A-BIT is a trademark of Linear Technology Corp.

TYPICAL APPLICATIONS

Sneak-A-Bit Code for the LTC1283 Using the MC68HC05C4

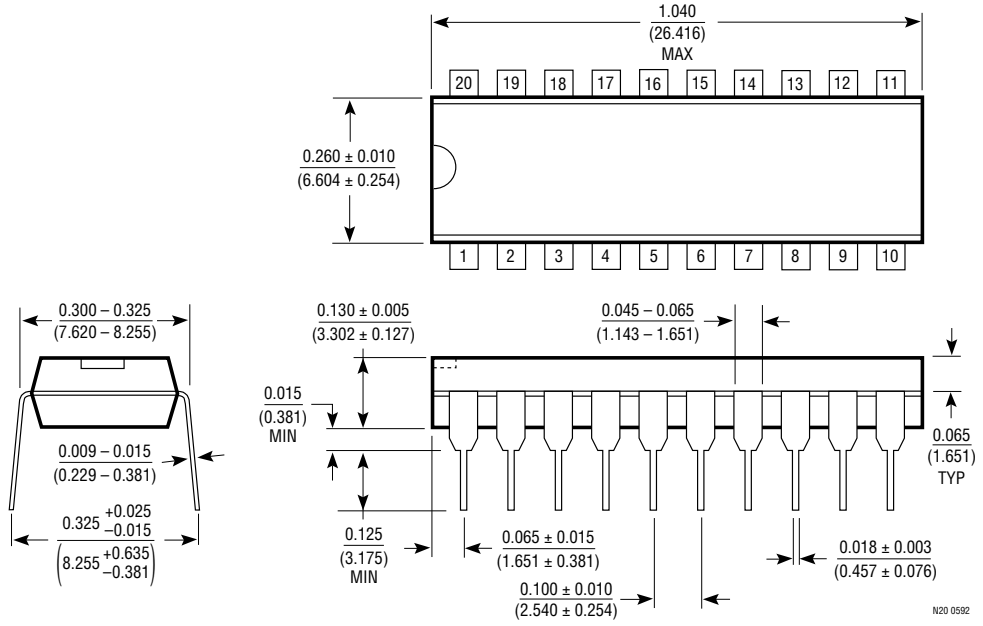
MNEMONIC			DESCRIPTION
	LDA	#$50	CONFIGURATION DATA FOR SPCR
	STA	$0A	LOAD CONFIGURATION DATA INTO $0A
	LDA	#$FF	CONFIGURATION DATA FOR PORT C DDR
	STA	$06	LOAD CONFIGURATION DATA INTO PORT C DDR
	BSET	0, $02	MAKE SURE $\overline{CS}$ IS HIGH
	JSR	READ –/+	DUMMY READ CONFIGURES LTC1283 FOR NEXT READ
	JSR	READ +/–	READ CH6 WITH RESPECT TO CH7
	JSR	READ –/+	READ CH7 WITH RESPECT TO CH6
	JSR	CHK SIGN	DETERMINES WHICH READING HAS VALID DATA, CONVERTS TO 2's COMPLEMENT AND STORES IN RAM
READ –/+:	LDA	#$3F	LOAD D_{IN} WORD FOR LTC1283 INTO ACC
	JSR	TRANSFER	READ LTC1283 ROUTINE
	LDA	$60	LOAD MSBs FROM LTC1283 INTO ACC
	STA	$71	STORE MSBs IN $71
	LDA	$61	LOAD LSBs FROM LTC1283 INTO ACC
	STA	$72	STORE LSBs IN $72
	RTS		RETURN
Read +/–:	LDA	#$7F	LOAD D_{IN} WORD FOR LTC1283 INTO ACC
	JSR	TRANSFER	READ LTC1283 ROUTINE
	LDA	$60	LOAD MSBs FROM LTC1283 INTO ACC
	STA	$73	STORE MSBs IN $73
	LDA	$61	LOAD LSBs FROM LTC1283 INTO ACC
	STA	$74	STORE LSBs IN $74
	RTS		RETURN
TRANSFER:	BCLR	0, $02	$\overline{CS}$ GOES LOW
	STA	$0C	LOAD D_{IN} INTO SPI. START TRANSFER
LOOP 1:	TST	$0B	TEST STATUS OF SPIF
	BPL	LOOP 1	LOOP TO PREVIOUS INSTRUCTION IF NOT DONE
	LDA	$0C	LOAD CONTENTS OF SPI DATA REG. INTO ACC
	STA	$0C	START NEXT CYCLE
	STA	$60	STORE MSBs IN $60
LOOP 2:	TST	$0B	TEST STATUS OF SPIF
	BPL	LOOP 2	LOOP TO PREVIOUS INSTRUCTION IF NOT DONE
	BSET	0, $02	$\overline{CS}$ GOES HIGH
	LDA	$0C	LOAD CONTENTS OF SPI DATA REG. INTO ACC
	STA	$61	STORE LSBs IN $61
	RTS		RETURN
CHK SIGN:	LDA	$73	LOAD MSBs OF +/– READ INTO ACC
	ORA	$74	OR ACC (MSBs) WITH LSBs OF +/– read
	BEQ	MINUS	IF RESULT IS 0 GOTO MINUS
	CLC		CLEAR CARRY
	ROR	$73	ROTATE RIGHT $73 THROUGH CARRY
	ROR	$74	ROTATE RIGHT $74 THROUGH CARRY
	LDA	$73	LOAD MSBs OF +/– READ INTO ACC
	STA	$77	STORE MSBs IN RAM LOCATION $77
	LDA	$74	LOAD LSBs OF +/– READ INTO ACC
	STA	$87	STORE LSBs IN RAM LOCATION $87
	BRA	END	GOTO END OF ROUTINE
MINUS:	CLC		CLEAR CARRY
	ROR	$71	SHIFT MSBs OF –/+ READ RIGHT
	ROR	$72	SHIFT LSBs –/+ READ RIGHT
	COM	$71	1's COMPLEMENT OF MSBs
	COM	$72	1's COMPLEMENT OF LSBs
	LDA	$72	LOAD LSBs INTO ACC
	ADD	#$01	ADD 1 TO LSBs
	STA	$72	STORE ACC IN $72
	CLRA		CLEAR ACC
	ADC	$71	ADD WITH CARRY TO MSBs. RESULT IN ACC
	STA	$71	STORE ACC IN $71
	STA	$77	STORE MSBs IN RAM LOCATION $77
	LDA	$72	LOAD LSBs IN ACC
	STA	$87	STORE LSBs IN RAM LOCATION $87
END:	RTS		RETURN

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of circuits as described herein will not infringe on existing patent rights.

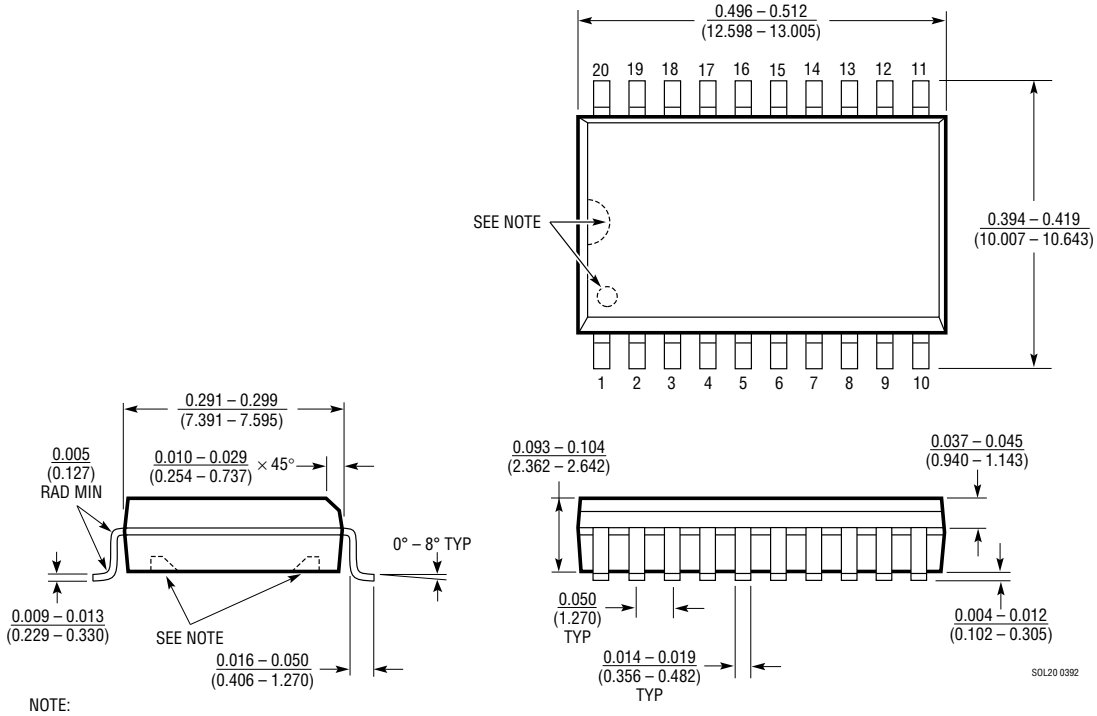
PACKAGE DESCRIPTION

Dimensions are in inches (millimeters) unless otherwise noted.

N Package
20-Lead Plastic DIP



S Package
20-Lead Plastic SOL



NOTE:
PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS.
THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS.

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