Document No.	853-1487
ECN No.	00730
Date of Issue	October 17, 1990
Status	Product Specification
ACL Products	

AC11014: Product Specification
ACT11014: Objective Specification

FEATURES

- Output capability: ±24 mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50Ω incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: SSI

DESCRIPTION

The 74AC/ACT11014 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11014 provides six separate inverters which are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have greater noise margin than conventional inverters.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/t_{PHL}	Propagation delay A, B, to $\overline{Y}$	C_L = 50pF	3.6	8.5	ns
C_{PD}	Power dissipation capacitance per gate[1]	f = 1MHz; C_L = 50pF	27	36	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4.0	4.0	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA

Note:

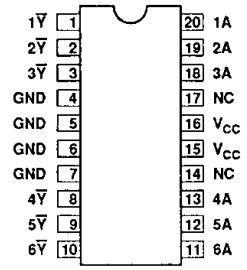
1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

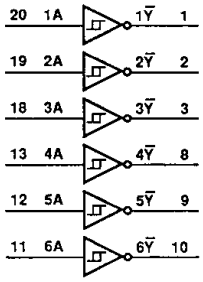
PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11014N 74ACT11014N
20-pin plastic SOL (300mil-wide)	-40°C to +85°C	74AC11014D 74ACT11014D

PIN CONFIGURATION

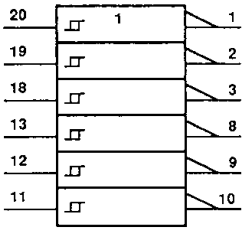
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Hex inverter Schmitt-trigger

74AC/ACT11014

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
20, 19, 18, 13, 12, 11	1A - 6A	Data inputs
1, 2, 3, 8, 9, 10	$1\overline{Y}$ - $6\overline{Y}$	Data outputs
4, 5, 6, 7	GND	Ground (0V)
15, 16	V_{CC}	Positive supply voltage

INPUT	OUTPUT
nA	$n\overline{Y}$
L	H
H	L

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11014			74ACT11014			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		100	0		100	ns/V
T_{amb}	Operating free-air temperature range	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 TO +7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DCoutput voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±150	mA
	DC ground current		±150	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package	Above 70°C; derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C; derate linearly by 8mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

Hex inverter Schmitt-trigger 74AC/ACT11014

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11014				74ACT11014				UNIT
					T_{amb} = +25°C		T_{amb} = -40°C to +85°C		T_{amb} = +25°C		T_{amb} = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{T+}	Positive-going threshold			3.0		2.2		2.2					V
				4.5		3.2		3.2		2.0		2.0	
				5.5		3.9		3.9		2.0		2.0	
V_{T-}	Negative-going threshold			3.0	0.5		0.5						V
				4.5	0.9		0.9			0.8		0.8	
				5.5	1.1		1.1			0.8		0.8	
ΔV_T	Hysteresis ($V_{T+} - V_{T-}$)			3.0	0.3	1.2	0.3	1.2					V
				4.5	0.4	1.4	0.4	1.4	0.4	1.2	0.4	1.2	
				5.5	0.5	1.6	0.5	1.6	0.4	1.2	0.4	1.2	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	$V_I = V_{IL}$ or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	$V_I = V_{IL}$ or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		3.6		0.44					
			I_{OL} = 24mA	4.5		3.6		0.44		3.6		0.44	
				5.5		3.6		0.44		3.6		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	$V_I = V_{CC}$ or GND		5.5		±0.1		±0.1		±0.1		±0.1	μA
I_{CC}	Quiescent supply current	$V_I = V_{CC}$ or GND, I_O = 0mA		5.5		4.0		4.0		4.0		4.0	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

Hex inverter Schmitt-trigger

74AC/ACT11014

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	WAVEFORM	74AC11014					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB to n$\overline{Y}$	1	1.2 1.7	5.4 6.0	9.2 8.5	1.2 1.7	9.8 9.3	ns

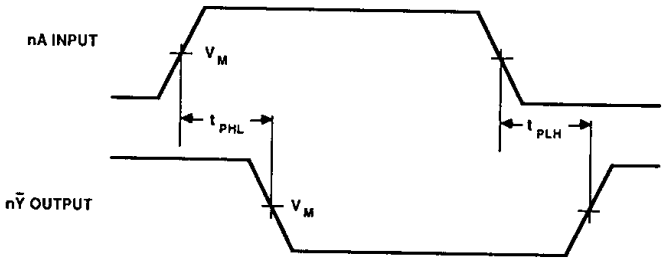
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	WAVEFORM	74AC11014					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB to n$\overline{Y}$	1	1.1 1.5	3.6 4.1	6.8 6.7	1.1 1.5	7.1 7.4	ns

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	WAVEFORM	74ACT11014					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB to n$\overline{Y}$	1	1.5 1.5			1.5 1.5		ns

AC WAVEFORMS

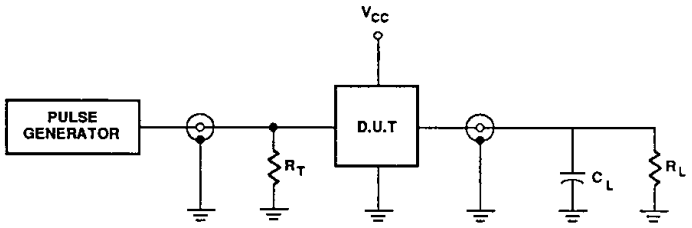


Waveform 1. Waveforms Showing the Input (nA) to Output (n$\overline{Y}$) Propagation Delays

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

Document No.	
ECN No.	
Date of Issue	October 17, 1990
Status	Preliminary Specification
ACL Products	

74AC/ACT11873

Dual 4-bit D-type transparent latch with clear (3–State)

FEATURES

- 3-State output buffers
- Asynchronous clear
- Output capability: ±24 mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50Ω incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: MSI

DESCRIPTION

The 74AC/ACT11873 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11873 devices are dual 4-bit D-type latches with asynchronous resets, making them suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The dual 4-bit latches are transparent D-type. When the latch enable inputs (1LE, 2LE) are High, the data on the D

(continued)

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/ t_{PHL}	Propagation delay nD_n to nQ_n	C_L = 50pF		5.5	6.9	ns
C_{PD}	Power dissipation capacitance per flip-flop[1]	f = 1MHz; C_L = 50pF	Enabled	43	40	pF
			Disabled	9	7	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.5	4.5	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}; Disabled		13.5	13.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA

Note:

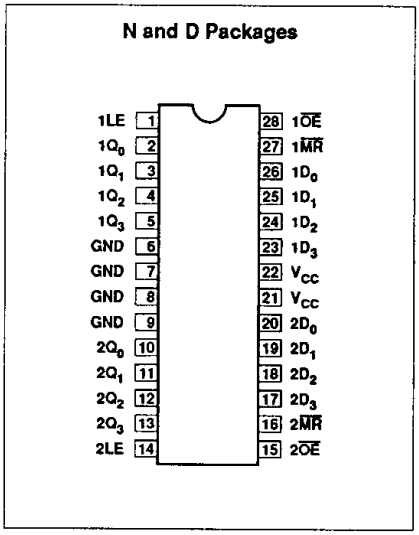
1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

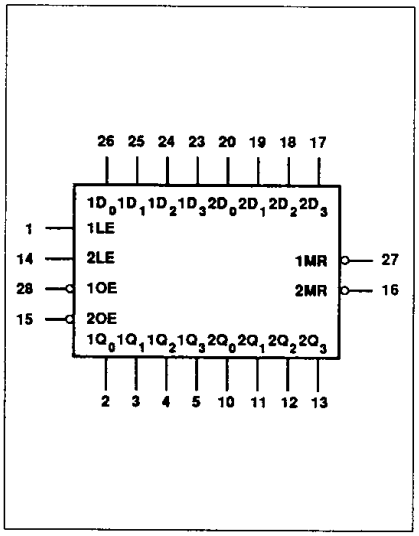
PACKAGES	TEMPERATURE RANGE	ORDER CODE
28-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11873N 74ACT11873N
28-pin plastic SOL (300mil-wide)	-40°C to +85°C	74AC11873D 74ACT11873D

PIN CONFIGURATION

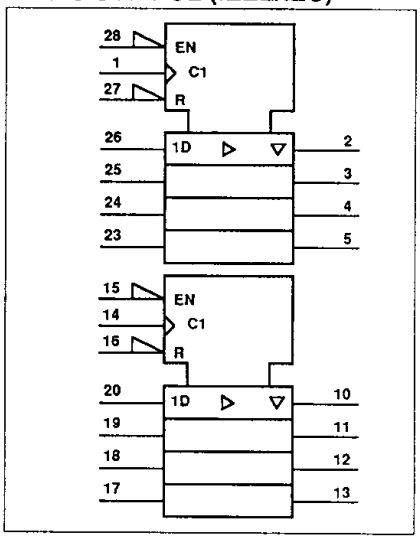
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Dual 4-bit D-type transparent latch with clear (3–State)

74AC/ACT11873

inputs is transferreded to the latch outputs (Q_0 - Q_3). The latches remain transparent to the data input while LE is High and store the data that is present one setup time before the High-to-Low latch enable transition. All four Q outputs will be forced low, independent of clock or data inputs, by taking $\overline{MR}$ Low.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active-Low Output Enable (OE) controls all eight 3-State buffers independent of the latch operation.

When the $\overline{OE}$ inputs are Low, the latched or transparent data appears at the outputs. When the $\overline{OE}$ inputs are high, the outputs are in the High-impedance "OFF" state, which means they will neither drive nor load the bus.

PIN DESCRIPTION

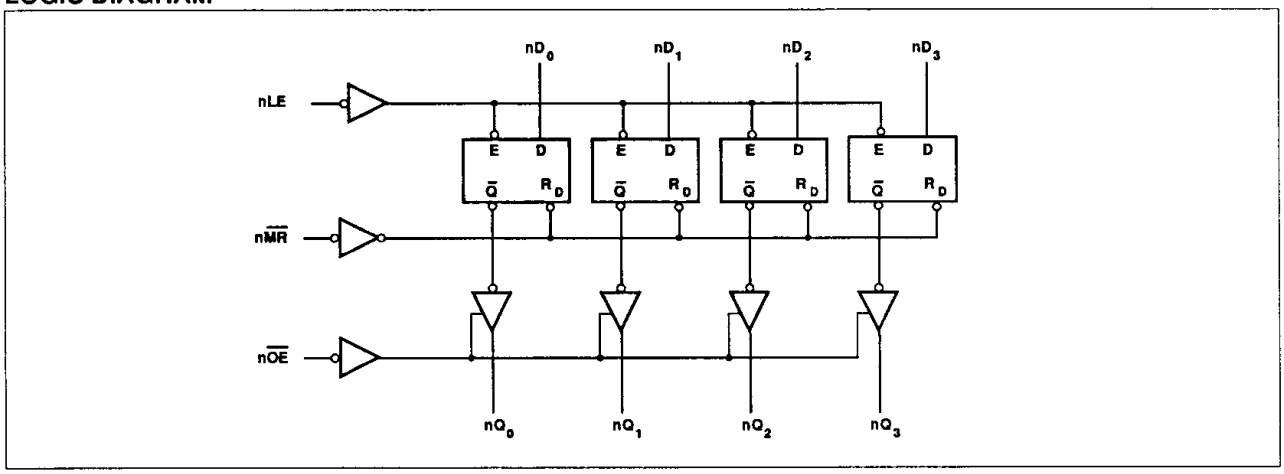
PIN NUMBER	SYMBOL	NAME AND FUNCTION
28, 15	$1\overline{OE}$, $2\overline{OE}$	Output enables
26, 25, 24, 23, 20, 19, 18, 17	$1D_0$ - $1D_3$, $2D_0$ - $2D_3$	Data inputs
2, 3, 4, 5 10, 11, 12, 13	$1Q_0$ - $1Q_3$, $2Q_0$ - $2Q_3$	Data outputs
1, 14	1LE, 2LE	Latch enable inputs
27, 16	$1\overline{MR}$, $2\overline{MR}$	Master reset inputs
6, 7, 8, 9	GND	Ground (0V)
22, 21	V_{CC}	Positive supply voltage

FUNCTION TABLE

OPERATING MODES	INPUTS				INTERNAL REGISTER	OUTPUTS
	$\overline{MR}$	$n\overline{OE}$	nLE	nD_n		nQ_n
Reset (clear)	L	L	X	X	X	L
Enable and read register	H H	L L	H H	L H	L H	L H
Latch and read register	H H	L L	↓ ↓	l h	L H	L H
Hold	H	L	L	X	NC	NC
Disable outputs	X	H	X	X	X	Z

H = High voltage level steady state
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level steady state
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
NC = No change
Z = High-Impedance "OFF" state
↓ = Low-to-High transition

LOGIC DIAGRAM



Dual 4-bit D-type transparent latch with clear (3–State)

74AC/ACT11873

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11873			74ACT11873			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_{amb}	Operating free-air temperature range	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 TO +7.0	V
I_{IK} or V_I	DC input diode current[2]	V_I < 0	-20	mA
		V_I > V_{CC}	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	V_O < 0	-50	mA
		V_O > V_{CC}	50	
	DCoutput voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package	Above 70°C; derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C; derate linearly by 8mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

Dual 4-bit D-type transparent latch with clear (3–State)

74AC/ACT11873

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11873				74ACT11873				UNIT
					T_{amb} = +25°C		T_{amb} = -40°C to +85°C		T_{amb} = +25°C		T_{amb} = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	$V_I = V_{IL}$ or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	$V_I = V_{IL}$ or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	$V_I = V_{CC}$ or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off–state current	$V_I = V_{IL}$ or V_{IH}, $V_O = V_{CC}$ or GND		5.5		±0.5		5.0		±0.5		5.0	μA
I_{CC}	Quiescent supply current	$V_I = V_{CC}$ or GND, I_O = 0mA		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

Dual 4-bit D-type transparent latch with clear (3–State)

74AC/ACT11873

AC ELECTRICAL CHARACTERISTICS AT 3.0V ±0.3V

SYMBOL	PARAMETER		WAVEFORM	74AC11873					UNIT
				T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nD_n to nQ_n		1	2.8 2.8	8.8 9.0	11.2 11.2	2.8 2.8	13.0 12.7	ns
t_{PLH} t_{PHL}	Propagation delay nLE to nQ_n		5	3.0 2.9	9.4 9.4	11.8 11.7	3.0 2.9	13.6 13.2	ns
t_{PHL}	Propagation delay $n\overline{MR}$ to nQ_n		4	2.3	8.2	10.3	2.3	11.5	ns
t_{PZH} t_{PZL}	Output enable time to High or Low level		2	1.8 2.7	6.4 9.9	8.4 12.5	1.8 2.7	9.7 14.4	ns
t_{PHZ} t_{PLZ}	Output disable time from High or Low level		2	3.8 3.5	6.8 6.8	8.4 8.5	3.8 3.5	9.0 9.1	ns
t_W	nLE pulse width High or Low		5	5.0			5.0		ns
t_W	$n\overline{MR}$ pulse width Low		4	5.0			5.0		ns
t_S	Setup time nD_n to nLE	Data High	3	3.0			3.0		ns
		Data Low		4.0			4.0		
t_H	Hold time nD_n to nLE	Data High	3	1.0			1.0		ns
		Data Low		1.0			1.0		

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER		WAVEFORM	74AC11873					UNIT
				T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nD_n to nQ_n		1	2.2 2.1	5.5 5.5	7.3 7.2	2.2 2.1	8.4 8.2	ns
t_{PLH} t_{PHL}	Propagation delay nLE to nQ_n		5	2.4 2.2	5.9 5.8	7.8 7.6	2.4 2.2	8.9 8.7	ns
t_{PHL}	Propagation delay $n\overline{MR}$ to nQ_n		4	1.7	5.1	6.8	1.7	7.6	ns
t_{PZH} t_{PZL}	Output enable time to High or Low level		2	1.2 1.9	4.1 5.5	5.6 7.3	1.2 1.9	6.4 8.5	ns
t_{PHZ} t_{PLZ}	Output disable time from High or Low level		2	3.5 3.3	5.9 5.5	7.4 7.0	3.5 3.3	7.9 7.6	ns
t_W	nLE pulse width High or Low		5	5.0			5.0		ns
t_W	$n\overline{MR}$ pulse width Low		4	5.0			5.0		ns
t_S	Setup time nD_n to nLE	Data High	3	2.0			2.0		ns
		Data Low		3.0			3.0		
t_H	Hold time nD_n to nLE	Data High	3	1.0			1.0		ns
		Data Low		1.0			1.0		

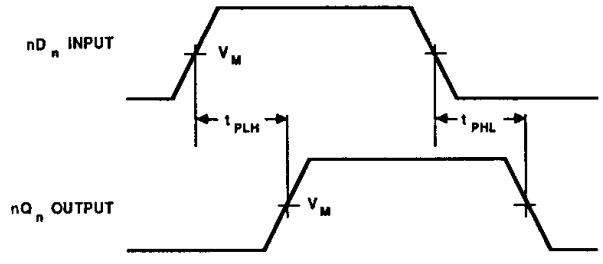
Dual 4-bit D-type transparent latch with clear (3–State)

74AC/ACT11873

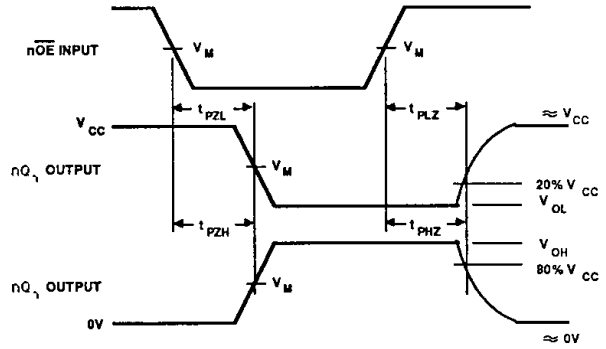
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER		WAVEFORM	74ACT11873					UNIT
				T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nD_n to nQ_n		1	4.4 3.0	7.2 6.6	8.8 9.1	4.4 3.0	10.0 10.2	ns
t_{PLH} t_{PHL}	Propagation delay nLE to nQ_n		5	4.7 5.2	8.1 8.9	10.0 10.9	4.7 5.2	11.3 12.3	ns
t_{PHL}	Propagation delay $n\overline{MR}$ to nQ_n		4	2.9	6.5	9.0	2.9	10.0	ns
t_{PZH} t_{PZL}	Output enable time to High or Low level		2	1.9 2.7	4.9 6.4	7.1 9.1	1.9 2.7	8.0 10.3	ns
t_{PHZ} t_{PLZ}	Output disable time from High or Low level		2	5.7 5.2	8.0 7.8	9.5 9.1	5.7 5.2	10.2 9.8	ns
t_W	nLE pulse width High or Low		5	5.0			5.0		ns
t_W	$n\overline{MR}$ pulse width Low		4	5.0			5.0		ns
t_S	Setup time nD_n to nLE	Data High	3	6.0			6.0		ns
		Data Low		3.0			3.0		
t_H	Hold time nD_n to nLE	Data High	3	0.0			0.0		ns
		Data Low		0.0			0.0		

AC WAVEFORMS



Waveform 1. Waveforms Showing the Input (nD_n) to Output (nQ_n) Propagation Delays

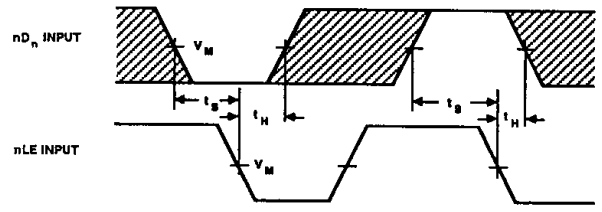


Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

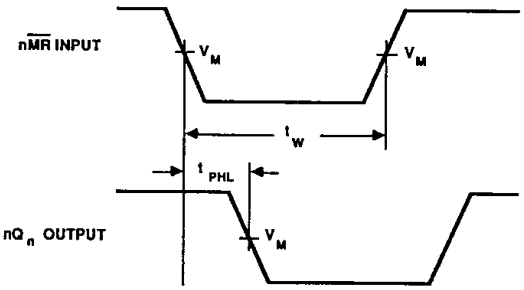
Dual 4-bit D-type transparent latch with clear (3–State)

74AC/ACT11873

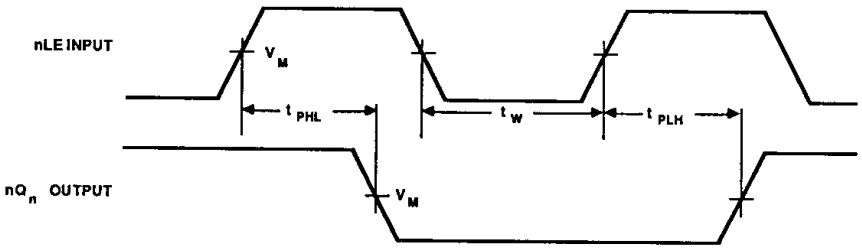
WAVEFORMS (continued)



Waveform 3. Waveforms Showing the Data Setup and Hold Times for nD$_n$ Input to nLE Input



Waveform 4. Waveforms Showing Master Reset (nMR) Pulse Width and Master Reset to Output Delay

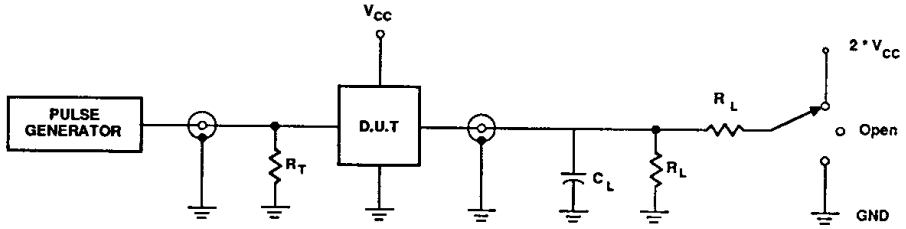


Waveform 5. Waveforms Showing the Latch Enable Input (nLE) Pulse Width and the Latch Enable Input to Output (nQ$_n$) Propagation Delays

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2*V_{CC}
t_{PHZ}/t_{PZH}	GND

SWITCH POSITION

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns