2GB – 2x128Mx72 DDR2 SDRAM REGISTERED, w/PLL

FEATURES

- 240-pin, dual in-line memory module
- Fast data transfer rates: PC2-4200 and PC2-3200
- Utilizes 533 and 400 Mb/s DDR2 SDRAM components
- $V_{CC} = V_{CCQ} = 1.8V \pm 0.1V$
- $V_{CCSPD} = 1.7V$ to $3.6V$
- JEDEC standard 1.8V I/O (SSTL_18-compatible)
- Differential data strobe (DQS, DQS#) option
- Four-bit prefetch architecture
- DLL to align DQ and DQS transitions with CK
- Multiple internal device banks for concurrent operation
- Supports duplicate output strobe (RDQS/RDQS#)
- Programmable CAS# latency (CL): 3 and 4
- Adjustable data-output drive strength
- On-die termination (ODT)
- Serial Presence Detect (SPD) with EEPROM
- 64ms: 8,192 cycle refresh
- Gold edge contacts
- Product is lead-free
- RoHS compliant
- Dual Rank
- Package option
  - 240 Pin DIMM
  - PCB – 29.97mm (1.18")

DESCRIPTION

The WV3HG2128M72AER is a 128Mx72 Double Data Rate DDR2 SDRAM high density module. This memory module consists of thirty six 128Mx4 bit with 4 banks DDR2 Synchronous DRAMs in FBGA packages, mounted on a 240-pin DIMM FR4 substrate.

* This product is under development, is not qualified or characterized and is subject to change or cancellation without notice.

NOTE: Consult factory for availability of:
- Vendor source control options
- Industrial temperature option

OPERATING FREQUENCIES

	PC2-3200	PC2-4200
Clock Speed	200MHz	266MHz
CL-t_{RCD}-t_{RP}	3-3-3	4-4-4

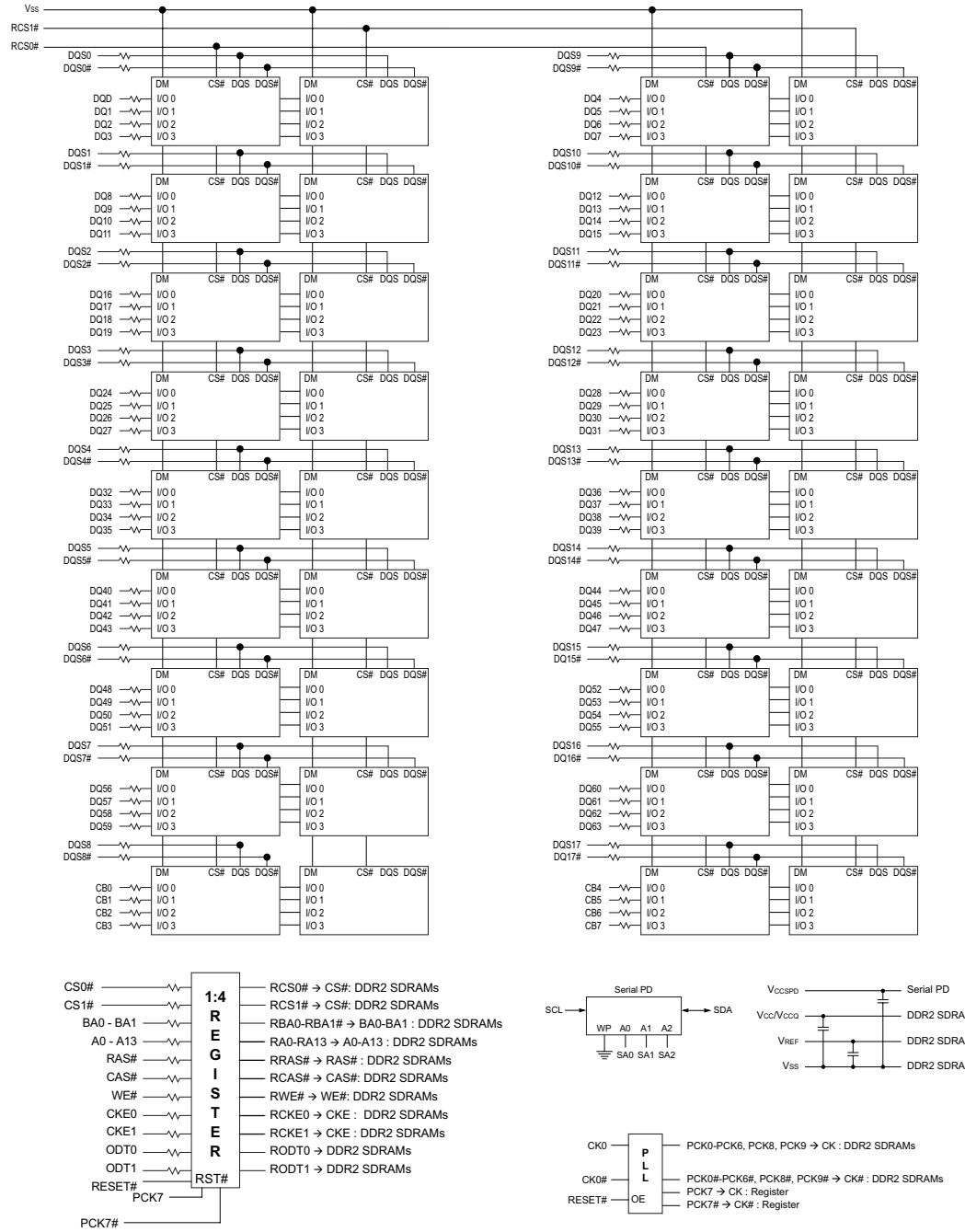
PIN CONFIGURATION

Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol
1	V_{REF}	61	A4	121	V_{SS}	181	V_{CCQ}
2	V_{SS}	62	V_{CCQ}	122	DQ4	182	A3
3	DQ0	63	A2	123	DQ5	183	A1
4	DQ1	64	V_{CC}	124	V_{SS}	184	V_{CC}
5	V_{SS}	65	V_{SS}	125	DQS9	185	CK0
6	DQS0#	66	V_{SS}	126	DQS9#	186	CK0#
7	DQS0	67	V_{CC}	127	V_{SS}	187	V_{CC}
8	V_{SS}	68	NC	128	DQ6	188	A0
9	DQ2	69	V_{CC}	129	DQ7	189	V_{CC}
10	DQ3	70	A10/AP	130	V_{SS}	190	BA1
11	V_{SS}	71	BA0	131	DQ12	191	V_{CCQ}
12	DQ8	72	V_{CCQ}	132	DQ13	192	RAS#
13	DQ9	73	WE#	133	V_{SS}	193	S0#
14	V_{SS}	74	CAS#	134	DQS10	194	V_{CCQ}
15	DQS1#	75	V_{CCQ}	135	DQS10#	195	ODT0
16	DQS1	76	CS1#	136	V_{SS}	196	A13
17	V_{SS}	77	ODT1	137	NC	197	V_{CC}
18	RESET#	78	V_{CCQ}	138	NC	198	V_{SS}
19	NC	79	V_{SS}	139	V_{SS}	199	DQ36
20	V_{SS}	80	DQ32	140	DQ14	200	DQ37
21	DQ10	81	DQ33	141	DQ15	201	V_{SS}
22	DQ11	82	V_{SS}	142	V_{SS}	202	DQS13
23	V_{SS}	83	DQS4#	143	DQ20	203	DQS13#
24	DQ16	84	DQS4	144	DQ21	204	V_{SS}
25	DQ17	85	V_{SS}	145	V_{SS}	205	DQ38
26	V_{SS}	86	DQ34	146	DQS11	206	DQ39
27	DQS2#	87	DQ35	147	DQS11#	207	V_{SS}
28	DQS2	88	V_{SS}	148	V_{SS}	208	DQ44
29	V_{SS}	89	DQ40	149	DQ22	209	DQ45
30	DQ18	90	DQ41	150	DQ23	210	V_{SS}
31	DQ19	91	V_{SS}	151	V_{SS}	211	DQS14
32	V_{SS}	92	DQS5#	152	DQ28	212	DQS14#
33	DQ24	93	DQS5	153	DQ29	213	V_{SS}
34	DQ25	94	V_{SS}	154	V_{SS}	214	DQ46
35	V_{SS}	95	DQ42	155	DQS12	215	DQ47
36	DQS3#	96	DQ43	156	DQS12#	216	V_{SS}
37	DQS3	97	V_{SS}	157	V_{SS}	217	DQ52
38	V_{SS}	98	DQ48	158	DQ30	218	DQ53
39	DQ26	99	DQ49	159	DQ31	219	V_{SS}
40	DQ27	100	V_{SS}	160	V_{SS}	220	NC
41	V_{SS}	101	SA2	161	CB4	221	NC
42	CB0	102	NC	162	CB5	222	V_{SS}
43	CB1	103	V_{SS}	163	V_{SS}	223	DQS15
44	V_{SS}	104	DQS6#	164	DQS17	224	DQS15#
45	DQS8#	105	DQS6	165	DQS17#	225	V_{SS}
46	DQS8	106	V_{SS}	166	V_{SS}	226	DQ54
47	V_{SS}	107	DQ50	167	CB6	227	DQ55
48	CB2	108	DQ51	168	CB7	228	V_{SS}
49	CB3	109	V_{SS}	169	V_{SS}	229	DQ60
50	V_{SS}	110	DQ56	170	V_{CCQ}	230	DQ61
51	V_{CCQ}	111	DQ57	171	CKE1	231	V_{SS}
52	CKE0	112	V_{SS}	172	V_{CC}	232	DQS16
53	V_{CC}	113	DQS7#	173	NC	233	DQS16#
54	NC	114	DQS7	174	NC	234	V_{SS}
55	NC	115	V_{SS}	175	V_{CCQ}	235	DQ62
56	V_{CCQ}	116	DQ58	176	A12	236	DQ63
57	A11	117	DQ59	177	A9	237	V_{SS}
58	A7	118	V_{SS}	178	V_{CC}	238	V_{CC}SPD
59	V_{CC}	119	SDA	179	A8	239	SA0
60	A5	120	SCL	180	A6	240	SA1

PIN NAMES

Pin Name	Function
A0-A13	Address Inputs
BA0,BA1	SDRAM Bank Address
DQ0-DQ63	Data Input/Output
CB0-CB7	Check Bits
DQS0-DQS17	Data strobes
DQS0#-DQS17#	Data strobes complement
ODT0, ODT1	On-die termination control
CK0,CK0#	Clock Inputs, positive line
CKE0, CKE1	Clock Enables
CS0#, CSI#	Chip Selects
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Write Enable
SA0-SA2	SPD Address
V_{CC}	Core and I/O Power (1.8V)
V_{CCQ}	I/O Power (1.8V)
V_{SS}	Ground
A10/AP	Address input/ autoprecharge
V_{REF}	Input/Output Reference
V_{CC}SPD	SPD Power
NC	Spare pins, No connect

FUNCTIONAL BLOCK DIAGRAM



NOTE: All resistor values are 22 ohms unless otherwise specified.

DC OPERATING CONDITIONS

All voltages referenced to V_{SS}

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Supply voltage	V_{CC}	1 .7	1 .8	1 .9	V	1
I/O Supply voltage	V_{CCQ}	1 .7	1 .8	1 .9	V	4
V_{CCL} Supply voltage	V_{CCL}	1 .7	1 .8	1 .9	V	4
I/O Reference voltage	V_{REF}	0.49 x V_{CCQ}	0.50 x V_{CCQ}	0.51 x V_{CCQ}	V	2
I/O Termination voltage	V_{TT}	V_{REF}-0.04	V_{REF}	V_{REF} + 0.04	V	3

Notes:

1. V_{CC} V_{CCQ} must track each other. V_{CCQ} must be less than or equal to V_{CC}.
2. V_{REF} is expected to equal V_{CCQ}/2 of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed ±1 percent of the DC value. Peak-to-peak AC noise on V_{REF} may not exceed ±2 percent of V_{REF}. This measurement is to be taken at the nearest V_{REF} bypass capacitor.
3. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF}.
4. V_{CCQ} tracks with V_{CC}; V_{CCL} track with V_{CC}.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		MIN	MAX	U nit
V_{CC}	Voltage on V_{CC} pin relative to V_{SS}		-1.0	2.3	V
V_{CCQ}	Voltage on V_{CCQ} pin relative to V_{SS}		-0.5	2.3	V
V_{CCL}	Voltage on V_{CCL} pin relative to V_{SS}		-0.5	2.3	V
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}		-0.5	2.3	V
T_{STG}	Storage temperature		-55	100	°C
I_L	Input leakage current; Any input 0V<V_{IN}<V_{CC}; V_{REF} input 0V<V_{IN}<0.95V; Other pins not under test = 0V	Command/Address, RAS#, CAS#, WE#, CS#, CKE CK, CK# DM	-5	5	uA
I_{OZ}	Output leakage current; 0V<V_{OUT}<V_{CCQ}; DQs and ODT are disable	DQ, DQS, DQS#	-10	-10	uA
I_{VREF}	V_{REF} leakage current; V_{REF} = Valid V_{REF} level		-72	72	uA

CAPACITANCE

TA=25°C, f=1MHz, V_{CC} =V_{CCQ} = 1.8V

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0 ~ A1 3, BA0 ~ BA1 ,RAS#,CAS#,WE#)	C_{IN1}	9	11	pF
Input capacitance (CKE0, CKE1), (ODT0, ODT1)	C_{IN2}	9	11	pF
Input capacitance (CS0#, CS1#)	C_{IN3}	14	18	pF
Input capacitance (CK0, CK0#)	C_{IN4}	6	7	pF
Input capacitance (DQS0 ~ DQS8)	C_{IN5}	9	12	pF
Input capacitance (DQ0 ~ DQ63), (CB0 ~ CB7)	C_{OUT1}	9	12	pF

OPERATING TEMPERATURE CONDITION

Parameter	Symbol	Rating	Units	Notes
Operating temperature	T_{OPER}	0 to 85	°C	1, 2

Notes:
1. Operating temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JEDEC JESD51 .2
2. At 0 - 85°C, operation temperature range, all DRAM specification will be supported.

INPUT DC LOGIC LEVEL

All voltages referenced to V_{SS}

Parameter	Symbol	Min	Max	Unit
Input High (Logic 1) Voltage	V_{IH}(DC)	V_{REF} + 0.1 25	V_{REF} + 0.300	V
Input Low (Logic 0) Voltage	V_{IL}(DC)	-0.300	V_{REF} - 0.125	V

INPUT AC LOGIC LEVEL

All voltages referenced to V_{SS}

Parameter	Symbol	Min	Max	Unit
AC Input High (Logic 1) Voltage	V_{IH}(AC)	V_{REF} + 0.250	—	V
AC Input Low (Logic 0) Voltage DDR2-400 & DDR2-533	V_{IL}(AC)	—	V_{REF} - 0.250	V

DDR2 I_{DD} SPECIFICATIONS AND CONDITIONS

Includes DDR2 SDRAM components only

Symbol	Proposed Conditions		534	403	Units
I_{DD0}*	**Operating one bank active-precharge current;** $t_{CK} = t_{CK}(I_{DD})$, $t_{RC} = t_{RC}(I_{DD})$, $t_{RAS} = t_{RAS}min(I_{DD})$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		2284	2284	mA
I_{DD1}*	**Operating one bank active-read-precharge current;** I_{OUT} = 0mA; BL = 4, CL = CL(I_{DD}), AL = 0; $t_{CK} = t_{CK}(I_{DD})$, $t_{RC} = t_{RC}(I_{DD})$, $t_{RAS} = t_{RAS}min(I_{DD})$, $t_{RCD} = t_{RCD}(I_{DD})$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus input are switching; Data pattern is same as I_{DD}6W		2554	2554	mA
I_{DD2P}**	**Precharge power-down current;** All banks idle; $t_{CK} = t_{CK}(I_{DD})$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		988	988	mA
I_{DD2Q}**	**Precharge quiet standby current;** All banks idle; $t_{CK} = t_{CK}(I_{DD})$; CKE is HIGH, CS# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		1780	1780	mA
I_{DD2N}**	**Precharge standby current;** All banks idle; $t_{CK} = t_{CK}(I_{DD})$; CKE is HIGH, CS# is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		1960	1960	mA
I_{DD3P}**	**Active power-down current;** All banks open; $t_{CK} = t_{CK}(I_{DD})$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Fast PDN Exit MRS(12) = 0mA	1780	1780	mA
		Slow PDN Exit MRS(12) = 1mA	1132	1132	mA
I_{DD3N}**	**Active standby current;** All banks open; $t_{CK} = t_{CK}(I_{DD})$, $t_{RC} = t_{RC}(I_{DD})$; $t_{RAS} = t_{RAS}max(I_{DD})$; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		2500	2500	mA
I_{DD4W}*	**Operating burst write current;** All banks open, Continuous burst writes; BL = 4, CL = CL(I_{DD}), AL = 0; $t_{CK} = t_{CK}(I_{DD})$, $t_{RAS} = t_{RAS}max(I_{DD})$, $t_{RP} = t_{RP}(I_{DD})$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		2824	2644	mA
I_{DD4R}*	**Operating burst read current;** All banks open, Continuous burst reads, I_{OUT} = 0mA; BL = 4, CL = CL(I_{DD}), AL = 0; $t_{CK} = t_{CK}(I_{DD})$, $t_{RAS} = t_{RAS}max(I_{DD})$, $t_{RP} = t_{RP}(I_{DD})$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as I_{DD}4W		2914	2734	mA
I_{DD5}**	**Burst auto refresh current;** $t_{CK} = t_{CK}(I_{DD})$; Refresh command at every $t_{RFC}(I_{DD})$ interval; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		5740	5740	mA
I_{DD6}**	**Self refresh current;** CK and CK# at 0V; CKE 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	Normal	288	288	mA
I_{DD7}*	**Operating bank interleave read current;** All bank interleaving reads, I_{OUT} = 0mA; BL = 4, CL = CL(I_{DD}), AL = $t_{RC}D(I_{DD})$-1*$t_{CK}(I_{DD})$; $t_{CK} = t_{CK}(I_{DD})$, $t_{RC} = t_{RC}(I_{DD})$, $t_{RRD} = t_{RRD}(I_{DD})$, $t_{RCD} = 1*t_{CK}(I_{DD})$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data bus imputs are switching.		4804	4804	mA

Notes:

I_{DD} specification is based on **SAMSUNG** components. Other DRAM manufacturers specification may be different.

* Value calculated as one module rank in this operating condition, and all other module ranks in I_{DD2P} (CKE LOW) mode.

** Value calculated reflects all module ranks in this operating condition.

AC TIMING PARAMETERS & SPECIFICATIONS

$0°C \le T_A \le +70°C$; V_{CCQ} = + 1.8V ± 0.1V, V_{CC} = +1.8V ± 0.1V

AC CHARACTERISTICS				534		403		
PARAMETER			SYMBOL	MIN	MAX	MIN	MAX	UNIT
Clock	Clock cycle time	CL = 4	$t_{CK\ (4)}$	3,750	8,000	5,000	8,000	ps
		CL = 3	$t_{CK\ (3)}$	5,000	8,000	5,000	8,000	ps
	CK high-level width		t_{CH}	0.45	0.55	0.45	0.55	t_{CK}
	CK low-level width		t_{CL}	0.45	0.55	0.45	0.55	t_{CK}
	Half clock period		t_{HP}	MIN (t_{CH}, t_{CL})		MIN (t_{CH}, t_{CL})		ps
	Clock jitter		t_{JIT}	TBD		TBD		ps
Data	DQ output access time from CK/CK#		t_{AC}	-500	+500	-600	+600	ps
	Data-out high-impedance window from CK/CK#		t_{HZ}		t_{AC} MAX		t_{AC} MAX	ps
	Data-out low-impedance window from CK/CK#		t_{LZ}	t_{AC} MIN	t_{AC} MAX	t_{AC} MIN	t_{AC} MAX	ps
	DQ and DM input setup time relative to DQS		t_{DS}	100		150		
	DQ and DM input hold time relative to DQS		t_{DH}	225		275		
	A DQ and DM input pulse width (for each input)		t_{DIPW}	0.35		0.35		t_{CK}
	Data hold skew factor		t_{QHS}		400		450	ps
	DQ…DQS hold, DQS to first DQ to go nonvalid, per access		t_{QH}	t_{HP} - t_{QHS}		t_{HP} - t_{QHS}		ps
	Data valid output window (DVW)		t_{DVW}	t_{QH} - t_{DQSQ}		t_{QH} - t_{DQSQ}		ns
Data Strobe	DQS input high pulse width		t_{DQSH}	0.35		0.35		t_{CK}
	DQS input low pulse width		t_{DQSL}	0.35		0.35		t_{CK}
	DQS output access time from CK/CK#		t_{DQSCK}	-450	+450	-500	+500	ps
	DQS falling edge to CK rising … setup time		t_{DSS}	0.2		0.2		t_{CK}
	DQS falling edge from CK rising … hold time		t_{DSH}	0.2		0.2		t_{CK}
	DQS…DQ skew, DQS to last DQ valid, per group, per access		t_{DQSQ}		300		350	ps
	DQS read preamble		t_{RPRE}	0.9	1.1	0.9	1.1	t_{CK}
	DQS read postamble		t_{RPST}	0.4	0.6	0.4	0.6	t_{CK}
	DQS write preamble setup time		t_{WPRES}	0		0		ps
	DQS write preamble		t_{WPRE}	0.35		0.35		t_{CK}
	DQS write postamble		t_{WPST}	0.4	0.6	0.4	0.6	t_{CK}
	Write command to first DQS latching transition		t_{DQSS}	WL - 0.25	WL + 0.25	WL - 0.25	WL + 0.25	t_{CK}

Notes:
AC specification is based on **SAMSUNG** components. Other DRAM manufacturers specification may be different.

Continued on next page

AC TIMING PARAMETERS (cont'd)

$0°C \le T_A \le +70°C$; V_{CCQ} = + 1.8V ± 0.1V, V_{CC} = +1.8V ± 0.1V

AC CHARACTERISTICS			534		403		
	PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	UNIT
Command and Address	Address and control input pulse width for each input	t_{IPW}	0.6		0.6		t_{CK}
	Address and control input setup time	t_{IS}	250		250		ps
	Address and control input hold time	t_{IH}	375		475		ps
	CAS# to CAS# command delay	t_{CCD}	2		2		t_{CK}
	ACTIVE to ACTIVE (same bank) command	t_{RC}	60		65		ns
	ACTIVE bank a to ACTIVE bank b command	t_{RRD}	7.5		7.5		ns
	ACTIVE to READ or WRITE delay	t_{RCD}	15		15		ns
	Four Bank Activate period	t_{FAW}	37.5	37.5	37.5	37.5	ns
	ACTIVE to PRECHARGE command	t_{RAS}	45	70,000	45	70,000	ns
	Internal READ to precharge command delay	t_{RTP}	7.5		7.5		ns
	Write recovery time	t_{WR}	15		15		ns
	Auto precharge write recovery + precharge time	t_{DAL}	$t_{WR} + t_{RP}$		$t_{WR} + t_{RP}$		ns
	Internal WRITE to READ command delay	t_{WTR}	7.5		10		ns
	PRECHARGE command period	t_{RP}	15		15		ns
	PRECHARGE all command period	t_{RPA}	$t_{RP} + t_{CK}$		$t_{RP} + t_{CK}$		ns
	LOAD MODE command cycle time	t_{MRD}	2		2		t_{CK}
	CKE low to CK,CK# uncertainty	t_{DELAY}	4.375		4.375		ns
Self Refresh	REFRESH to REFRESH command interval	t_{RFC}	127.5	70,000	127.5	70,000	ns
	Average periodic refresh interval	t_{REFI}		7.8		7.8	µs
	Exit self refresh to non-READ command	t_{XSNR}	$t_{RFC\ (MIN)} + 10$		$t_{RFC\ (MIN)} + 10$		ns
	Exit self refresh to READ command	t_{XSRD}	200		200		t_{CK}
	Exit self refresh timing reference	t_{ISXR}	t_{IS}		t_{IS}		ps
ODT	ODT turn-on delay	t_{AOND}	2	2	2	2	t_{CK}
	ODT turn-on	t_{AON}	t_{AC} (MIN)	t_{AC} (MAX) + 1000	t_{AC} (MIN)	t_{AC} (MAX) + 1000	ps
	ODT turn-off delay	t_{AOFD}	2.5	2.5	2.5	2.5	t_{CK}
	ODT turn-off	t_{AOF}	t_{AC} (MIN)	t_{AC} (MAX) + 600	t_{AC} (MIN)	t_{AC} (MAX) + 600	ps
	ODT turn-on (power-down mode)	t_{AONPD}	t_{AC} (MIN) + 2000	2 x t_{CK} + t_{AC} (MAX) + 1000	t_{AC} (MIN) + 2000	2 x t_{CK} + t_{AC} (MAX) + 1000	ps
	ODT turn-off (power-down mode)	t_{AOFPD}	t_{AC} (MIN) + 2000	2.5 x t_{CK} + t_{AC} (MAX) + 1000	t_{AC} (MIN) + 2000	2.5 x t_{CK} + t_{AC} (MAX) + 1000	ps
	ODT to power-down entry latency	t_{ANPD}	3		3		t_{CK}
	ODT power-down exit latency	t_{AXPD}	8		8		t_{CK}
Power-Down	Exit active power-down to READ command, MR[bit12=0]	t_{XARD}	2		2		t_{CK}
	Exit active power-down to READ command, MR[bit12=1]	t_{XARDS}	6 - AL		6 - AL		t_{CK}
	A Exit precharge power-down to any non-READ command.	t_{XP}	2		2		t_{CK}
	CKE minimum high/low time	t_{CKE}	3		3		t_{CK}

Notes:
AC specification is based on **SAMSUNG** components. Other DRAM manufacturers specification may be different.

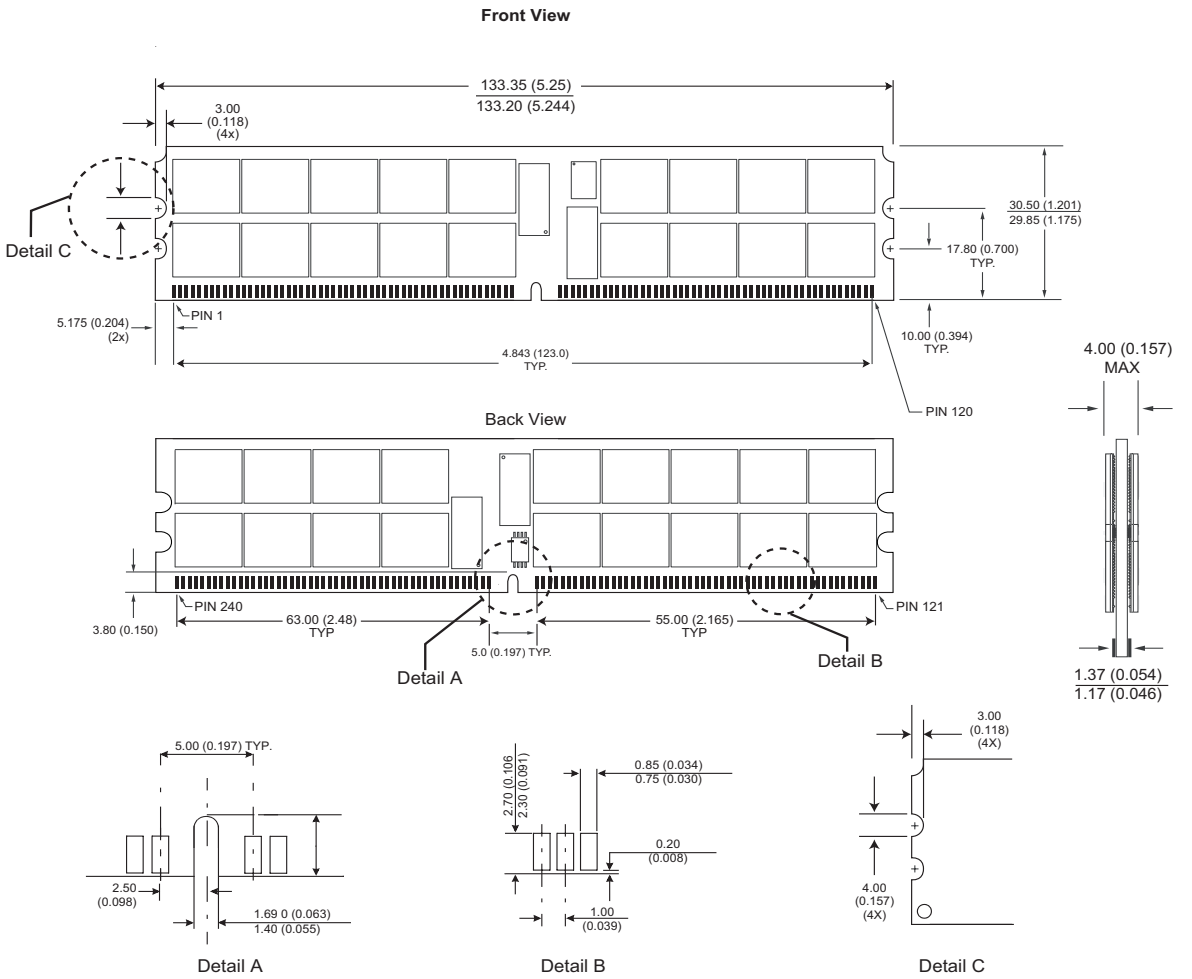
ORDERING INFORMATION FOR D6

Part Number	Speed	CAS Latency	t_{RCD}	t_{RP}	Height*
WV3HG2128M72AER534D6xG	266MHz/533Mb/s	4	4	4	29.97mm (1.18")
WV3HG2128M72AER403D6xG	200MHz/400Mb/s	3	3	3	29.97mm (1.18")

NOTES:

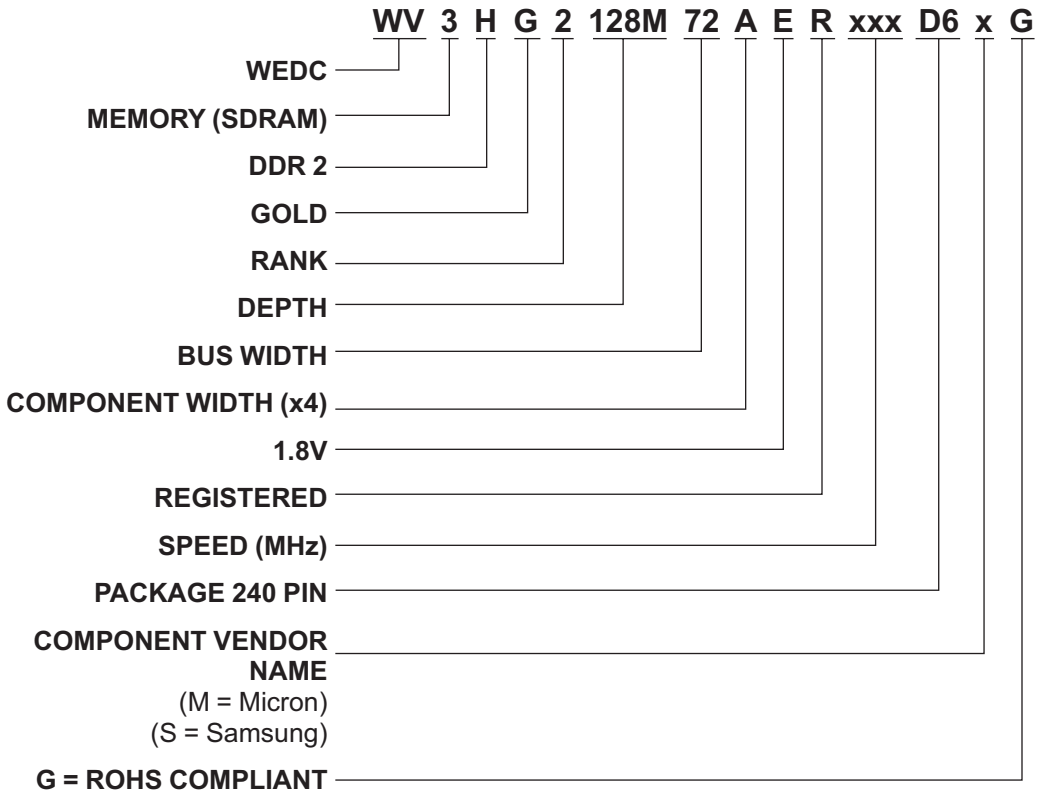
- RoHS products. ("G" = RoHS Compliant)
- Vendor specific part numbers are used to provide memory component source control. The place holder for this is shown as a lower case "x" in the part numbers above and is to be replaced with respective vendors code. Consult factory for qualified sourcing options. (M = Micron, S = Samsung & consult factory for others)
- Consult factory for availability of industrial temperature (-40°C to 85°C) option

PACKAGE DIMENSIONS FOR D6



* ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES)

PART NUMBERING GUIDE



Document Title

2GB – 2x128Mx72 DDR2 SDRAM REGISTERED, w/PLL

Revision History

Rev #	History	Release Date	Status
Rev 0	Created	September 2005	Advanced