Zero Voltage Switching Resonant Power Conversion

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Abstract

The technique of zero voltage switching in modern power conversion is explored. Several ZVS topologies and applications, limitations of the ZVS technique, and a generalized design procedure are featured. Two design examples are presented: a 50 Watt DC/DC converter, and an off-line 300 Watt multiple output power supply. This topic concludes with a performance comparison of ZVS converters to their square wave counterparts, and a summary of typical applications.

Introduction

Advances in resonant and quasi-resonant power conversion technology propose alternative solutions to a conflicting set of square wave conversion design goals; obtaining high efficiency operation at a high switching frequency from a high voltage source. Currently, the conventional approaches are by far, still in the production mainstream. However, an increasing challenge can be witnessed by the emerging resonant technologies, primarily due to their lossless switching merits. The intent of this presentation is to unravel the details of zero voltage switching via a comprehensive analysis of the timing intervals and relevant voltage and current waveforms.

The concept of quasi-resonant, "lossless" switching is not new, most noticeably patented by one individual [1] and publicized by another at various power conferences [2,3]. Numerous efforts focusing on zero current switching ensued, first perceived as the likely candidate for tomorrow's generation of high frequency power converters [4,5,6,7,8]. In theory, the on-off transitions occur at a time in the resonant cycle where the switch current is zero, facilitating zero current, hence zero power switching. And while true, two obvious concerns can impede the quest for high efficiency operation with high voltage inputs.

By nature of the resonant tank and zero current switching limitation, the peak switch current is significantly higher than its square wave counterpart. In fact, the peak of the full load switch current is a minimum of twice that of its square wave kin. In its off state, the switch returns to a blocking a high voltage every cycle. When activated by the next drive pulse, the MOSFET output capacitance (C_{oss}) is discharged by the FET, contributing a significant power loss at high frequencies and high voltages. Instead, both of these losses are avoided by implementing a zero voltage switching technique [9,lO].

Zero Voltage Switching Overview

Zero voltage switching can best be defined as conventional square wave power conversion during the switch's on-time with "resonant" switching transitions. For the most part, it can be considered as square wave power utilizing a constant off-time control which varies the conversion frequency, or on-time to maintain regulation of the output voltage. For a given unit of time, this method is similar to fixed frequency conversion which uses an adjustable duty cycle, as shown in Fig. 1.

Regulation of the output voltage is accomplished by adjusting the effective duty cycle, performed by varying the conversion frequency. This changes the effective on-time in a ZVS design. The foundation of this conversion is simply the volt-second product equating of the input and output. It is virtually identical to that of square wave power conversion, and vastly

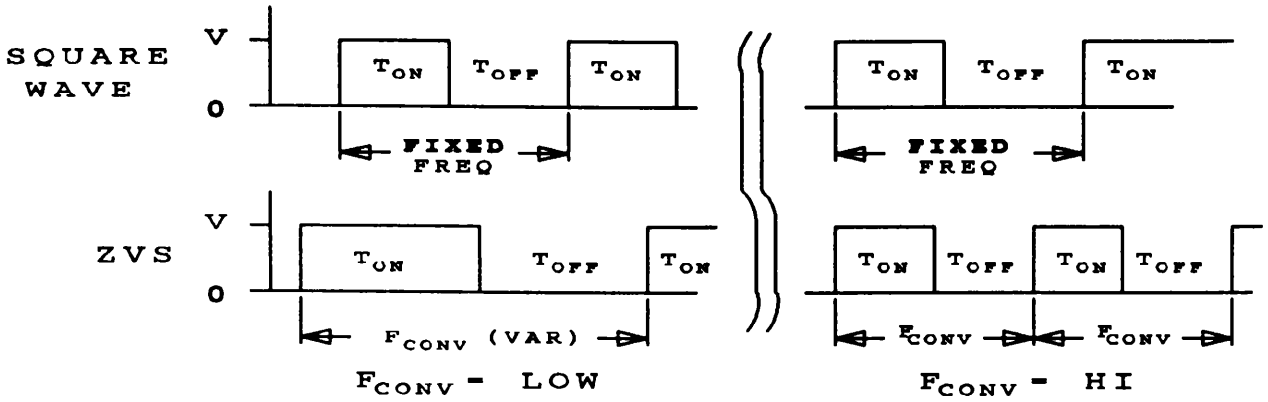


Fig. 1 - Zero Voltage Switching vs. Conventional Square Wave

unlike the energy transfer system of its electrical dual, the zero current switched converter.

During the ZVS switch off-time, the L-C tank circuit resonates. This traverses the voltage across the switch from zero to its peak, and back down again to zero. At this point the switch can be reactivated, and lossless zero voltage switching facilitated. Since the output capacitance of the MOSFET switch (C_{OSS}) has been discharged by the resonant tank, it does not contribute to power loss or dissipation in the switch. Therefore, the MOSFET transition losses go to zero - regardless of operating frequency and input voltage. This could represent a significant savings in power, and result in a substantial improvement in efficiency. Obviously, this attribute makes zero voltage switching a suitable candidate for high frequency, high voltage converter designs. Additionally, the gate drive requirements are somewhat reduced in a ZVS design due to the lack of the gate to drain (Miller) charge, which is deleted when V_{DS} equals zero.

The technique of zero voltage switching is applicable to all switching topologies; the buck regulator and its derivatives (forward, half and full bridge), the flyback, and boost converters, to name a few. This presentation will focus on the continuous output current, buck derived topologies, however a list of references describing the others has been included in the appendix.

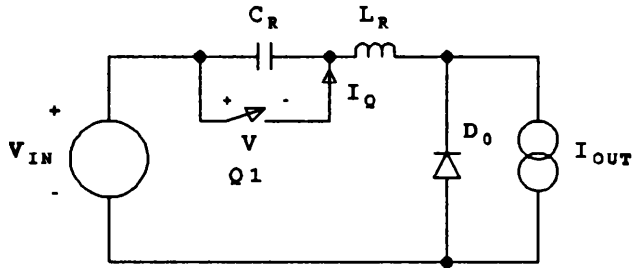


Fig. 2 - Resonant Switch Implementation

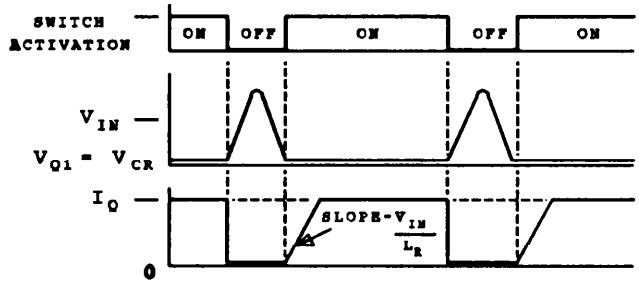


Fig. 3 - General Waveforms

ZVS Benefits

- Zero power “Lossless” switching transitions
- Reduced EMI / RFI at transitions
- No power loss due to discharging C_{OSS}
- No higher peak currents, (ie. ZCS) same as square wave systems
- High efficiency with high voltage inputs at any frequency
- Can incorporate parasitic circuit and component ***L & C***

- Reduced gate drive requirements (no "Miller" effects)

Short circuit tolerant

ZVS Differences:

- Variable frequency operation (in general)
- Higher off-state voltages in single switch, unclamped topologies
- Relatively new technology - users must climb the learning curve
- Conversion frequency is inversely proportional to load current
- A more sophisticated control circuit may be required

ZVS Design Equations

A zero voltage switched Buck regulator will be used to develop the design equations for the various voltages, currents and time intervals associated with each of the conversion periods which occur during one complete switching cycle. The circuit schematic, component references, and relevant polarities are shown in Fig. 4.

Typical design procedure guidelines and "shortcuts" will be employed during the analysis' for the purpose of brevity. At the onset, all components will be treated as though they were ideal which simplifies the generation of the basic equations and relationships. As this section progresses, losses and non-ideal characteristics of the components will be added to the formulas. The timing summary will expound upon the equations for a precise analysis.

Another valid assumption is that the output filter section consisting of output inductor L_O and capacitor C_o has a time constant several orders of magnitude larger than any power conversion period. The filter inductance is large in comparison to that of the resonant inductor's value L_R and the magnetizing current ΔI_{Lo} as well as the inductor's DC resistance is negligible. In addition, both the input voltage V_{IN} and output voltage V_O are purely DC, and do not vary during a given conversion cycle. Last, the converter is operating in a closed loop configuration which regulates the output voltage V_O.

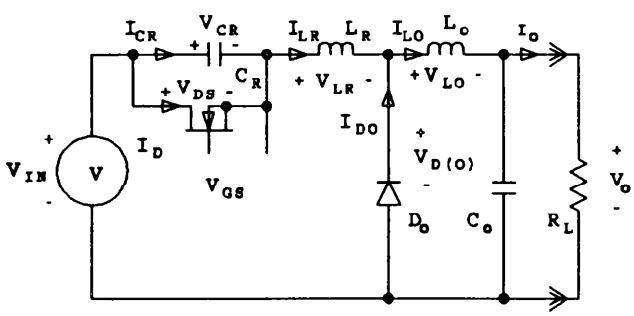


Fig. 4 - Zero Voltage Switched Buck Regulator

Initial Conditions: Time interval < t_0

Before analyzing the individual time intervals, the initial conditions of the circuit must be defined. The analysis will begin with switch Q_1 on, conducting a drain current I_D equal to the output current I_o, and $V_{DS} = V_{CR} = 0$ (ideal). In series with the switch Q_1 is the resonant inductor L_R and the output inductor L_O which also conduct the output current I_O. It has been established that the output inductance L_O is large in comparison to the resonant inductor L_R and all components are ideal. Therefore, the voltage across the output inductor V_{Lo} equals the input to output voltage differential; $V_{Lo} = V_{IN} - V_o$. The output filter section catch diode D_o is not conducting and sees a reverse voltage equal to the input voltage; $V_{Do} = V_1$, observing the polarity shown in Figure 4.

Table I - INITIAL CONDITIONS

COMP.	STATUS	CIRCUIT VALUES
Q_1	ON	$V_{DS}=V_{CR}=0$; $I_D=I_{LR}=I_{LO}=I_O$
D_O	OFF	$V_{DO}=V_{IN}$; $I_{DO}=0$
L_R		$I_{LR}=I_O$; $V_{LR}=0$
L_O		$V_{LO}=V_{IN}-V_O$; $I_{LO}=0$

Capacitor Charging State: $t_0 - t_1$

The conversion period is initiated at time t_0 when switch Q_1 is turned OFF. Since the current through resonant inductor L_R and output inductor L_O cannot change instantaneously, and no drain current flows in Q_1 while

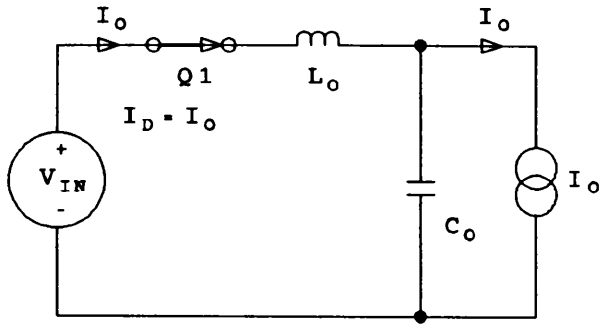


Fig. 5 - Simplified Model

$$V_{CR}(t) = \frac{I_O t}{C_R} \quad ; \quad t_{01} = \frac{C_R V_{IN}}{I_O}$$

$$I_{CR} = I_O \qquad for\ t_0 < t < t_1$$

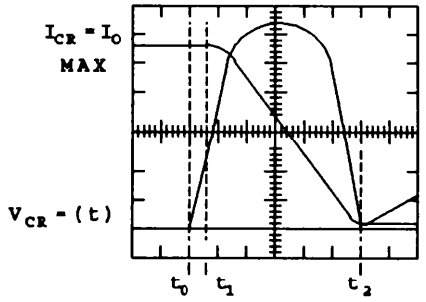


Fig. 6 - Resonant Capacitor Waveforms

it is off, the current is diverted around the switch through the resonant capacitor C_R. The constant output current will linearly increase the voltage across the resonant capacitor until it reaches the input voltage ($V_{CR} = V_{IN}$). *Since* the current is not changing, neither is the voltage across resonant inductor L_R.

At time t_0 the switch current I_D "instantly" drops from I_O to zero. Simultaneously, the resonant capacitor current I_{CR} snaps from zero to I,, while the resonant inductor current I_{LR} and output inductor current I_{LO} are constant and also equal to I_O during interval t_{01}. Voltage across output inductor L_O and output catch diode D_O linearly decreases during this interval due to the linearly increasing voltage across resonant capacitor C_R. At time t_1, V_{CR} equals V_{IN}, and D_O starts to conduct.

Table II - CAPACITOR CHARGING: $t_0 - t_1$

COMP.	STATUS	CIRCUIT VALUES
Q_1	OFF	$I_D = 0$; $V_{DS(t)} = V_{CR(t)}$
C_R	Charging	$I_{CR} = 0$; $V_{CR(t)}$ RISES LINEARLY $V_{CR(t0)} = 0$; $V_{CR(t1)} = V_{IN}$
L_R		$I_{LR(t)} = I_O$; $V_{LR} = 0$
D_O	OFF	$V_{DO(t0)} = V_{IN}$; $V_{DO(t1)} = 0$; DECREASES LINEARLY
L_O		$V_{LO(t0)} = V_{IN} - V_O$; $V_{LO(t1)} = -V_O$ DECREASES LINEARLY ; $I_{LO} = I_O$

Resonant State: $t_1 - t_2$

The resonant portion of the conversion cycle begins at t_1 when the voltage across resonant capacitor V_{CR} equals the input voltage V_{IN}, and the output catch diode begins conducting. At t_1, current through the resonant components I_{CR} and I_{LR} equals the output current I_O.

The stimulus for this series resonant L-C circuit is output current I_O flowing through the resonant inductor prior to time t_1. The ensuing resonant tank current follows a cosine function beginning at time t_1, and ending at time t_2. At the natural resonant frequency ω_R, each of the *L-C* tank components exhibit an impedance equal to the tank impedance, Z_R. Therefore, the peak voltage across C_R and switch Q_1 are a function of Z_R and I_O.

The instantaneous voltage across C_R and Q_1 can be evaluated over the resonant time interval using the following relationships:

$$V_{CR(t)} = V_{CR(t1)} + \frac{I_O}{\omega_R C_R} \sin\left[\omega_R (t - t_1)\right]_{t_1}^{t_2}$$

$$Z_R = 1/\omega_R C_R \quad ; \quad V_{CR(t1)} = V_{IN}$$

$$\therefore \quad V_{CR(t)} = V_{IN} + I_O Z_R \sin\left[\omega_R (t - t_1)\right]_{t_1}^{t_2}$$

Of greater importance is the ability to solve the equations for the precise off-time of the switch. This off-time will vary with line and load changes and the control circuit must respond in order to facilitate true zero ***voltage*** switching. While some allowance does exist for a fixed off time technique, the degree of lati-

tude is insufficient to accommodate typical input and output variations, The exact time is obtained by solving the resonant capacitor voltage equations for the condition when zero voltage is attained.

$$Let\ V_{CR(t)} = 0\ ;\ I_O Z_R\ SIN(\omega_R(t-t_1)) = -V_{IN}$$

The equation can be further simplified by extracting the half cycle (180 degrees) of conduction which is a constant for a given resonant frequency, and equal to π/ω_R.

$$t_{12} = \frac{\pi}{\omega_R} + \frac{1}{\omega_R} \arcsin \left[\frac{V_{IN}}{I_O Z_R} \right]_{t_1}^{t_2}$$

The resonant component current ($I_{CR} = I_{LR}$) is a cosine function between time t_1 and t_2, described as:

$$I_{CR(t)} = I_O \cos\left[\omega_R(t-t_1)\right]_{t_1}^{t_2}$$

The absolute maximum duration for this interval occurs when 270 degrees ($3\pi/2\omega_R$) of resonant operation is required to intersect the zero voltage axis. This corresponds to the limit of resonance as minimum load and maximum line voltage are approached.

Contributions of line and load influences on the resonant time interval t_{12} can be analyzed individually as shown in Figs. 7 and 8.

Prior to time t_1, the catch diode D_O was not conducting. Its voltage, V_{DO}, was linearly decreasing from V_{IN} at time t_0 to zero at t_1 while input source V_{IN} was supplying full output current, I_O. At time t_1, however, this situation changes as the resonant capacitor initiates resonance, diverting the resonant inductor current away from the output filter section. Instantly, the output diode voltage, V_{DO}, changes polarity as it begins to conduct, supplementing the decreasing resonant inductor current with diode current I', extracted from stored energy in output inductor L_O. The diode current waveshape follows a cosine function during this interval, equalling I_O minus $I_{CR}(t)$.

Also occurring at time t_1, the output filter inductor L_O releases the stored energy required

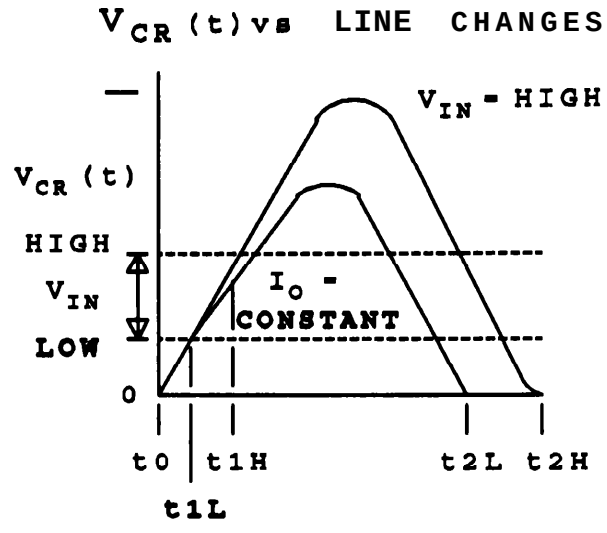


Fig. 7 -- Resonant Capacitor Voltage vs. Line

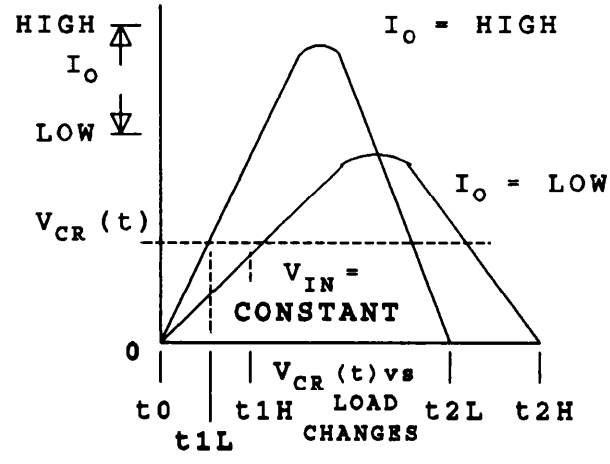


Fig. 8 -- Resonant Capacitor Voltage vs. Load

to maintain a constant output current I_O. Its reverse voltage is clamped to the output voltage V_O minus the diode voltage drop V_{DO} by the convention followed by Figure 4.

Table III - RESONANT INTERVAL: $t_1 \cdot t_2$

COMP.	STATUS	CIRCUIT VALUES
Q_1	OFF	$V_{DS(t)} = V_{CR(t)}$
C_R	Resonant	$V_{CR(t)} = V_{IN} + (I_O Z_R \sin(\omega_R(t-t_1)))$ $I_{CR(t)} = I_O \cos(\omega_R(t-t_1))$
L_R	Resonant	$V_{LR(t)} = [I_O Z_R \sin(\omega_R(t-t_1))$ $I_{LR(t)} = I_{CR(t)}$
D_O	ON	$I_{DO(t)} = I_O - I_{LR(t)}$

Inductor Charging State: t_2 - t_3

To facilitate zero voltage switching, switch Q_1 is activated once the voltage V_{DS} across Q_1 and resonant capacitor V_{CR} has reached zero, occurring at time t_2. During this inductor charging interval t_{23}, resonant inductor current I_{LR} is linearly returned from its negative peak of minus I_O to its positive level of plus I_O.

The output catch diode D_O conducts during the t_{23} interval. It continues to freewheel the full output current I_O, clamping one end of the resonant inductor to ground through D_O. There is a constant voltage, $V_{IN} - V_{DO}$, across the resonant inductor. As a result, I_{LR} rises linearly, I_{DO} decreases linearly. Energy stored in output inductor L_O continues to be delivered to the load during this time period.

A noteworthy peculiarity during this time-span can be seen in the switch dram current waveform. At time t_2, when the switch is turned on, current is actually returning from the resonant tank to the input source, V_{IN}. This indicates the requirement for a reverse polarity diode across the switch to accommodate the bi-directional current. An interesting result is that the switch can be turned on at any time during the first half of the t_{23} interval without affecting normal operation. A separate time interval could be used to identify this region if desired.

$$\frac{dI_R}{dt} = \frac{V_{IN}}{L_R} \; ; \; dt = dI_R L_R / V_{IN}$$

$$\therefore \; t_{23} = \frac{L_R \Delta I_R}{V_{IN}}$$

$$\text{where } \Delta I_R = -I_O \text{ to } +I_O = 2I_O$$

$$t_{23} = \frac{2L_R I_O}{V_{IN}} \quad \text{and varies with } V_{IN} \text{ and } V_O$$

Power Transfer State: t_3 - t_4

Once the resonant inductor current I_{LR} has reached I_O at time t_3, the zero voltage switched converter resembles a conventional square wave power processor. During the remainder of the conversion period, most of the pertinent waveforms approach DC conditions.

Table IV - INDUCTOR CHARGING: t_2 - t_3

COMP.	STATUS	CIRCUIT VALUES
Q_1	ON	$I_{D(t)} = -I_O + ((V_{IN} + V_{DO})/L_R)t$
C_R		$V_{CR} = 0$
L_R	Charging	$V_{LR} = V_{IN} + V_{DO}$ $I_{LR(t)} = -I_O + (V_{LR}/L_R)(t-t2)$
D_O	ON	$I_{DO(t)} = I_O - I_{LR(t)}$
L_O		$I_{LO} = I_O$; $V_{LO} = -(V_O + V_{DO})$

Assuming ideal components, with Q_1 closed, the input source supplies output current , and the output filter inductor voltage V_{LO} equals $V_{IN} - V_O$. The switch current and resonant inductor current are both equal to I_O, and their respective voltage drops are zero ($V_{DS} = V_{LR} = 0$). Catch diode voltage V_{DO} equals V_{IN}, and $I_{DO} = 0$.

In closed loop operation where the output voltage is in regulation, the control circuit essentially varies the on-time of the switch during the t_{34} interval. Variable frequency operation is actually the result of modulating the on-time as dictated by line and load conditions. Increasing the time duration, or lowering the conversion frequency has the same effect as widening the duty cycle in a traditional square wave converter. For example, if the output voltage were to drop in response to an increased load, the conversion frequency would decrease in order to raise the effective ON period. Conversely, at light loads where little energy is drawn from the output capacitor, the control circuit would adjust to minimize the t_{34} duration by increasing the conversion frequency. In summary, the conversion frequency is inversely proportional to the power delivered to the load.

$$V_O = \frac{V_{IN} t_{34}}{t_{01} + t_{12} + t_{23} + t_{34}} = \frac{V_{IN} t_{34}}{t_{03} + t_{34}}$$

$$t_{34} = \frac{V_O t_{03}}{V_{IN} - V_O}$$

Table V - POWER TRANSFER: t_3-t_4

COMP.	STATUS	CIRCUIT VALUES
Q_1	ON	$V_{DS}=I_O R_{DS(ON)}$; $I_D=I_O$
C_R		$V_{CR}=0$
L_R		$I_{LR}=I_O$; $V_{LR}=0$
D_O	OFF	$V_{DO}=V_{IN}$
L_O	Charging	$V_{LO}=V_{IN}-V_O$; $I_{LO}=I_O$

V_{IN} = 18 V
V_O = 5 V
I_O = 5 A

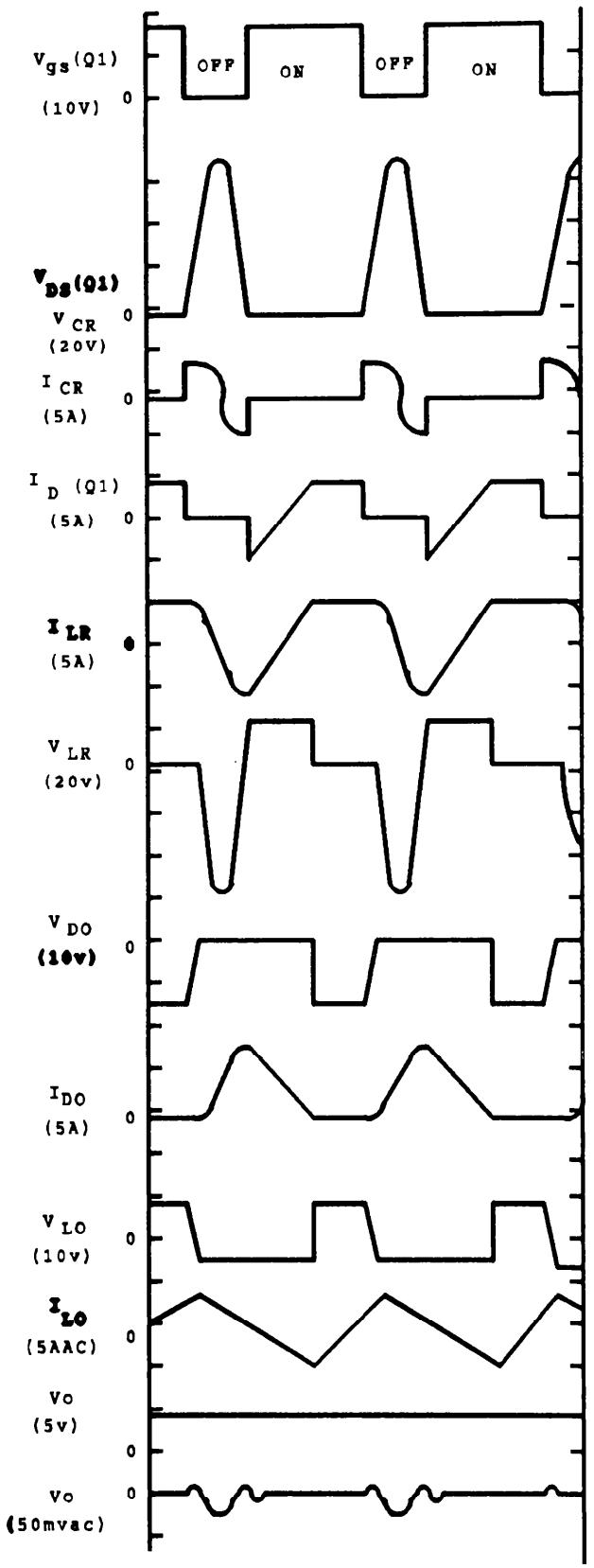


Fig. 9 -- ZVS Buck Regulator Waveforms

ZVS Converter Limitations:

In a ZVS converter operating under ideal conditions, the on-time of the switch $(t_{23}+t_{34})$ approaches zero, and the converter will operate at maximum frequency and deliver zero output voltage. In a practical design , however, the switch on-time cannot go to zero for several reasons.

First of all, the resonant tank components are selected based on the maximum input voltage V_{INmax} and minimum output current I_{Omin} for the circuit to remain resonant over all operating conditions of line and load. If the circuit is to remain zero voltage switched, then the resonant tank current cannot be allowed to go to zero. It can, however, reach I_{Omin}.

There is a finite switch on-time associated with the inductor charging interval t_{23} where the resonant inductor current linearly increases from $-I_O$ to $+I_O$. As the on-time in the power transfer interval t_{34} approaches zero, so will the converter output voltage. Therefore, the minimum on-time and the maximum conversion frequency can be calculated based upon the limitation of I_{Omin} and zero output voltage.

The limits of the four zero voltage switched time intervals will be analyzed when I_O *goes* to I_O minimum. Each solution will be retained in terms of the resonant tank frequency ω_R for generalization.

$$C_R = \frac{1}{Z_R \omega_R} = \frac{I_{O\min}}{V_{INmax}\omega_R}$$

$$\therefore t_{01\max} = \frac{C_R V_{INmax}}{I_{O\min}} = 1/\omega_R$$

$$t_{12\max} = \frac{3\pi}{2\omega_R} = \frac{1.5\pi}{\omega_R}$$

$$L_R = \frac{Z_R}{\omega_R} = \frac{V_{INmax}}{I_{O\min}\omega_R}$$

$$\therefore t_{23} = \frac{2L_R I_{O\min}}{V_{INmax}} = \frac{2}{\omega_R}$$

$$t_{34\min} = 0$$

Both the minimum on-time and maximum off-time have been described in terms of the resonant tank frequency , ω_R. Taking this one step further will result in the maximum conversion frequency $f_{CONVmax}$, also as a function of the resonant tank frequency.

Minimum On-Time:

$$t_{23\min} = \frac{2}{\omega_R} = \frac{1}{\pi f_R} = \frac{0.318}{f_R}$$

Maximum Off-Time:

$$t_{01}+t_{12\min} = \frac{1+1.5\pi}{\omega_R} = \frac{0.909}{f_R}$$

The maximum conversion frequency corresponds to the minimum conversion period, $T_{CONVmin}$, which is the sum of the minimum on-time and maximum off-time:

$T_{CONVmin}$:

$$t_{01}+t_{12\min}+t_{23} = \frac{0.909+0.308}{f_R} = \frac{1.227}{f_R}$$

The maximum conversion frequency, $f_{CONVmax} = 1/T_{CONVmin}$, equals

$$F_{CONV\max} = \frac{1}{T_{CONV(\min)}} = \frac{f_R}{1.227}$$

The ratio of the maximum conversion frequency to that of the resonant tank frequency can be expressed as a topology coefficient, K_T. For this zero voltage switched Buck regulator and its derivatives, K_{Tmax} equals:

$$K_{T\max} = \frac{F_{CONVmax}}{f_R} = \frac{f_R/1.227}{f_R} = 0.815$$

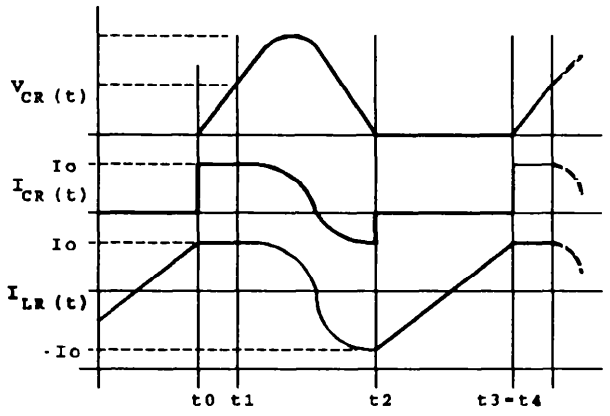


Fig. IO -- Waveforms at $F_{CONV} = K_T \cdot f_R$

In a realistic application, the output voltage of the power supply is held in regulation at V_O which stipulates that the on-time in the power processing state, t_{34}, cannot go to zero as in the example above. The volt-second product requirements of the output must be satisfied during this period, just as in any square wave converter design. Analogous to minimum duty cycle, the minimum on-time for a given design will be a function of V_{IN}, V_O and the resonant tank frequency, ω_R.

Although small, a specific amount of energy is transferred from the input to the output during the capacitor charging interval t_{01}. The voltage into the output filter section linearly decreases from V_{IN} at time t_0 to zero at t_1, equal to an average value of $V_{IN}/2$. In addition, a constant current equal to the output current I_O was being supplied from the input source. The average energy transferred during this interval is defined as:

$$W_{IN} = \frac{1}{2} V_{IN} I_O t_{01} = \frac{V_{IN} I_O}{2} \frac{C_R V_{IN}}{I_O} = \frac{V_{IN}^2 C_R}{2}$$

The equation can be reorganized in terms of C_R and ω_R as:

$$W_{IN} = \frac{V_{IN}^2 I_{O\min}}{2\omega_R V_{IN\max}}$$

This minimum energy can be equated to minimum output watts by dividing it by its conversion period where t_{34} equals zero. **Topology** coefficient K-r will be incorporated to define the ratio of the maximum conversion frequency (minimum conversion period) to that of the resonant tank frequency, ω_R.

$$W_{IN} = P_O T_{CONV} \quad , \quad Where \ T_{CONV} = \frac{7.71}{\omega_R}$$

$$W_{IN} = P_{O\min} \frac{7.71}{\omega_R} = \frac{V_{IN}^2 I_{O\min}}{2\omega_R V_{IN\max}}$$

$$P_{O\min} = V_O I_{O\min} = \frac{V_{IN}^2 I_{O\min}}{2(7.71) V_{IN\max}}$$

This demonstrates that a zero power output is **unobtainable** in reality. The same is true for the ability to obtain zero output voltage.
The equation can be rewritten as:

$$V_{O\min} = \frac{V_{IN}^2}{2(7.71) V_{IN\max}} = \frac{0.065\, V_{IN}^2}{V_{IN\max}}$$

Solving for the highest minimum output voltage, the worst case for occurs when I_O equals I_{Omin} and V_{IN} is at its maximum, V_{INmax}.

$$V_{O\min} = 0.065\, V_{IN\max} \ ; \quad \approx 6.5\%\ V_{IN\max}$$

$$P_{O\min} = 0.065\, V_{IN\max} I_{O\min} \ ; \quad \approx 6.5\%\ P_{IN\min}$$

Under normal circumstances the circuit will be operating far above this minimum requirement. In most applications, the amount of power transferred during the capacitor charging interval t_{01} can be neglected as it represents less than seven percent (7%) of the **minimum** input power. This corresponds to less than one percent of the total input power assuming a **10:1** load range.

ZVS Effective Duty Cycles:

A valid assumption is that a negligible amount of power is delivered to the load during the capacitor charging interval t_{01}. **Also,** no power is transferred during the resonant period from t_{12}. Although the switch is on during period t_{23}, it is only recharging the

resonant and output inductors to maintain the minimum output current, I_{Omin}. In summary, NO output power is derived from V_{IN} during interval t_{03}.

The power required to support V_O at its current of I_O is obtained from the input source during the power transfer period t_{34}. Therefore, an effective "duty cycle" can be used to describe the power transfer interval t_{34} to that of the entire switching period, t_{04}, or T_{CONV}.

ZVS - Effective Duty Cycle Calculations:

$$\text{"Duty Cycle"} = \frac{V_O}{V_{IN}} = \frac{t_{34}}{t_{04}}$$

$$\text{"Duty Cycle"} = \frac{t_{34}}{t_{01}+t_{12}+t_{23}+t_{34}}$$

And can be analyzed over line and load ranges using previous equations for each interval.

Accommodating Losses in the Design Equations:

Equations for zero voltage switching using ideal components and circuit parameters have been generated, primarily to understand each of the intervals in addition to computer modeling purposes. The next logical progression is to modify the equations to accommodate voltage drops across the components due to series impedance, like $R_{DS(on)}$, and the catch diode forward voltage drop. These two represent the most significant loss contributions in the buck regulator model. Later, the same equations will be adapted for the buck derived topologies which incorporate a transformer in the power stage.

The procedure to modify the equations is straightforward. Wherever V_{IN} appears in the equations while the switch is on it will be replaced by $V_{IN}-V_{DS(on)}$, the latter being a function of the load current I_O. The equations can be further adjusted to accept changes of $R_{DS(on)}$ and V_F, etc. with the device junction temperatures. Resonant component initial tolerances, and temperature variations likewise could optionally be evaluated.

A computer program to calculate the numerous time intervals and conversion frequencies as a function of line and load can simplify the design process, if not prove to be indispensable. Listed in the Appendix of this section is a BASIC language program which can be used to initiate the design procedure.

To summarize: When the switch is on, replace V_{IN} with $(V_{IN}-V_{DS(on)}) = (V_{IN}-I_O \cdot R_{DS(on)})$. When the free-wheeling diode is on, replace V_O with (V_O+V_F).

$$t_{01} = \frac{C_R(V_{IN}-I_O R_{DS(on)})}{I_O}$$

$$t_{12} = \frac{\pi}{\omega_R} + \frac{1}{\omega_R}\arcsin\left[\frac{V_{IN}-I_O R_{DS(on)}}{I_O Z_R}\right]_{t1}^{t2}$$

$$t_{23} = \frac{2L_R I_O}{V_{IN}-I_O R_{DS(on)}}$$

$$t_{34} = \frac{(V_O+V_F)(t_{01}+t_{12}+t_{23})}{(V_{IN}-I_O R_{DS(on)})-(V_O+V_F)}$$

$$Z_R = \frac{V_{INmax}-R_{DS(on)} I_{O\min}}{I_{O\min}}$$

Transformer Coupled Circuit Equations:

The general design equations for the Buck topology also apply for its derivates; namely the forward, half-bridge, full-bridge and push-pull converters. Listed below are the modifications and circuit specifics to apply the previous equations to transformer coupled circuits.

General Transformer Coupled Circuits. Maintaining the resonant tank components on the primary side of the transformer isolation boundary is probably the most common and simplest of configurations. The design procedure begins by transforming the output voltage and current to the primary side through the turns ratio, N. The prime (') designator will be used to signify the translated variables as seen by the primary side circuitry.

$$N = \frac{\textit{Primary Turns}}{\textit{Secondary Turns}}$$

$I_O' = I_O/\mathrm{N}$; $V_O' = V_O \cdot \mathrm{N}$; and $Z_O' = Z_O \cdot \mathrm{N}^2$

To satisfy the condition for resonance, $I_R < I_O'$

$$I_R \le I_O' = I_O/N \; ; \quad Z_R \le \frac{V_{INmax}}{I_{O\,min}'} = \frac{V_{INmax}N}{I_O}$$

The resonant tank component equations now become:

$$L_R = \frac{Z_R}{\omega_R} = \frac{V_{INmax}N}{I_{Omin}\omega_R}$$

Note: the calculated resonant inductance value does not include any series inductance, typical of the transformer leakage and wiring inductances.

$$C_R = \frac{1}{Z_R\omega_R} = \frac{I_{Omin}}{NV_{INmax}\omega_R}$$

Note: the calculated resonant capacitor value does not include any parallel capacitance, typical of a MOSFET output capacitance, C_{OSS}, in shunt. Multi-transistor variations of the buck topology should accommodate all switch capacitances in the analysis.

Timing Equations (including N):

$$t_{01} = \frac{C_R V_{IN} N}{I_O}$$

$$t_{12} = \frac{\pi}{\omega_R} + \frac{1}{\omega_R}\arcsin\left[\frac{V_{IN}N}{I_O Z_R}\right]_{t1}^{t2}$$

$$t_{23} = \frac{2L_R I_O}{V_{IN}N}$$

$$t_{34} = \frac{NV_O(t_{01}+t_{12}+t_{23})}{V_{IN}-NV_O}$$

$$T_{CONV} = t_{01}+t_{12}+t_{23}+t_{34}$$

Determining Transformer Turns Ratio (N): The transformer turns ratio is derived from the equations used to define the power transfer interval t_{34} in addition to the maximum off-time, t_{03}. While this may first seem like an iterative process, it simplifies to the volt-second product relationship described. The general equations are listed below.

The turns ratio N is derived by substituting $\mathrm{N} \cdot V_O$ for the output voltage V_O in the power transfer interval t_{34} equation. Solving for N results in the relationship:

$$NV_O/V_{IN} = t_{34}/(t_{01}+t_{12}+t_{23}+t_{34})$$

$$N = \frac{V_{IN\,min}\,t_{34}}{V_O\,t_{04}}$$

The transformer magnetizing and leakage inductance is part of the resonant inductance. This requires adjustment of the resonant inductor value, or both the resonant tank impedance Z_R and frequency ω_R will be off-target. One

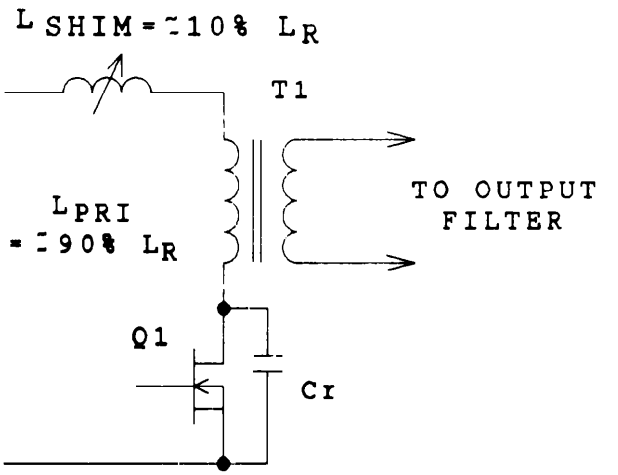


Fig. 11 -- Transformer Inductance "Shim "

option is to design the transformer inductance to be exactly the required resonant inductance, thus eliminating one component. For precision applications, the transformer inductance should be made slightly smaller than required, and "shimmed" up with a small inductor.

Expanding ZVS to Other Topologies

ZVS Forward Converter - Single Ended: The single ended forward converter can easily be configured for zero voltage switching with the addition of a resonant capacitor across the switch. Like the buck regulator, there is a high voltage excursion in the off state due to resonance, the amplitude of which varies with line and load. The transformer can be designed so that its magnetizing and leakage inductance equals the required resonant inductance. This simplifies transformer reset and eliminates one component. A general circuit diagram is shown in Fig. 12 below. The associated waveforms for when L_{PRI} equals L_R are shown in Fig. 13.

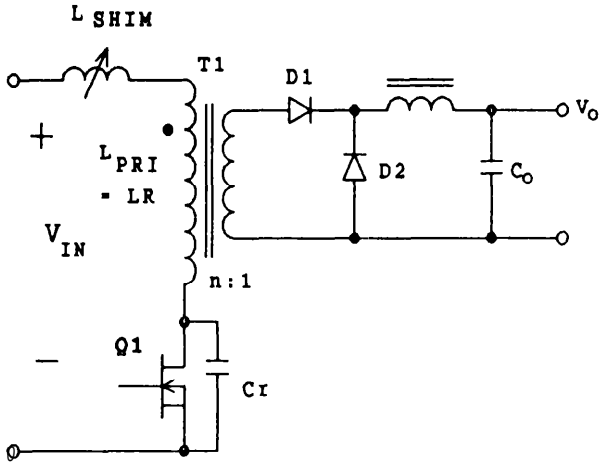
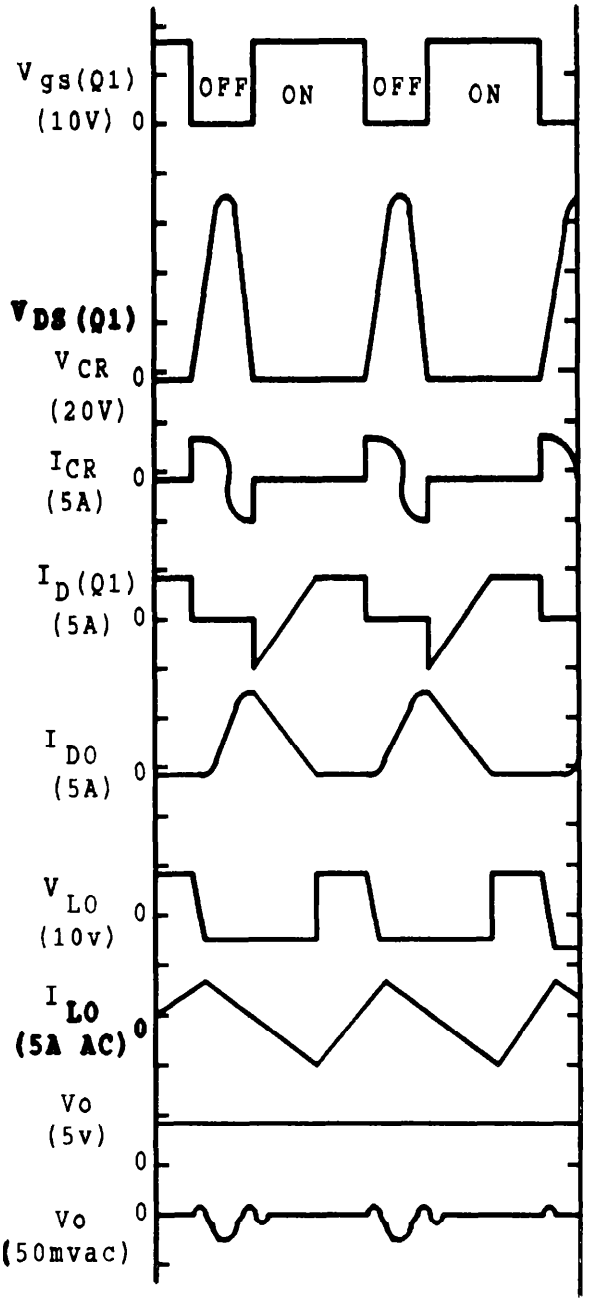


Fig. 12 -- ZVS Forward Converter



ZVS Clamped Configurations -- Half and Full Bridge Topologies: Zero voltage switching can be extended to multiple switch topologies for higher power levels, specifically the half and full bridge configurations. While the basic operation of each time interval remains similar, there is a difference in the resonant t_{12} interval.

While single switch converters have high off-state voltage, the bridge circuits clamp the switch peak voltages to the DC input rails, reducing the switch voltage stress. This alters the duration of the off segment of the resonant interval, since the opposite switch(es) must be activated long before the resonant cycle is completed. In fact, the opposite switch(es) should be turned on immediately after their voltage is clamped to the rails, where their drain to source voltage equals zero. If not, the resonant tank will continue to ring and return the switch voltage to its starting point, the opposite rail. Additionally, this off period varies with line and load changes.

Examples of this are demonstrated in Figs. 14 and 15. To guarantee true zero voltage switching, it is recommended that the necessary sense circuitry be incorporated.

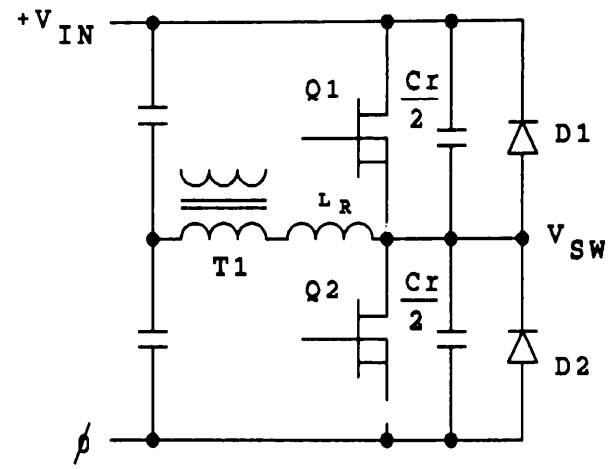


Fig. 14 -- Clamped ZVS Configuration

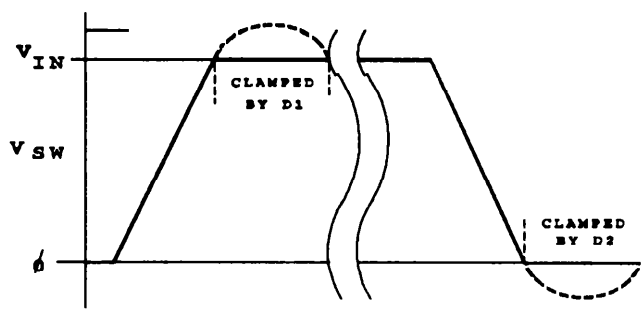


Fig. 15 -- Clamped ZVS Waveforms

ZVS Half Bridge: The same turns ratio, N, relationship applies to the half bridge topology when V_{IN} in the previous equations is considered to be one-half of the bulk rail-to-rail voltage. V_{IN} is the voltage across the transformer primary when either switch is on.

Refer to the circuit and waveforms of Figs. 14 and 15. C_R, the resonant capacitor becomes the parallel combination of the two resonant capacitors, the ones across each switch. Although the resonant inductor value is unaffected, all series leakage and wiring inductance must be taken into account.

The off state voltages of the switches will try to exceed the input bulk voltage during the resonant stages. **Automatic** clamping to the input bulk rails occurs by the MOSFET body diode, which can be externally shunted with a higher performance variety. Unlike the forward converter which requires a core reset equal to the applied volt second product, the bidirectional switching of the **half** (and full) bridge topology facilitate automatic core reset during consecutive switching cycles [ll,l2].

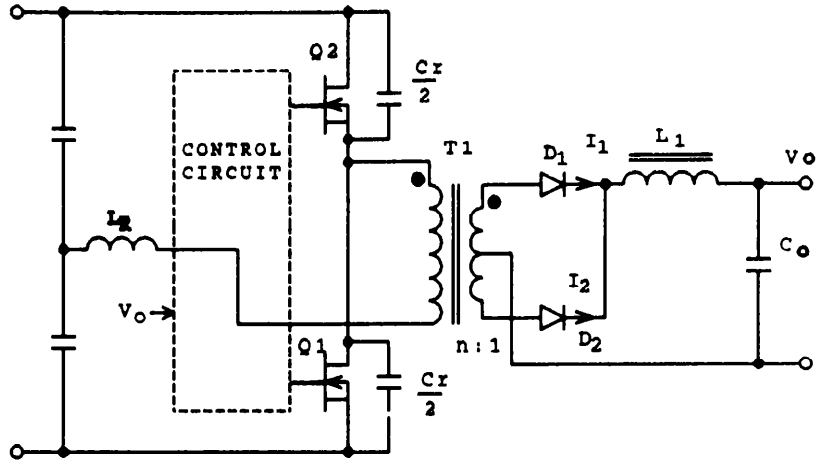


Fig. 16 -- ZVS Half Bridge Circuit

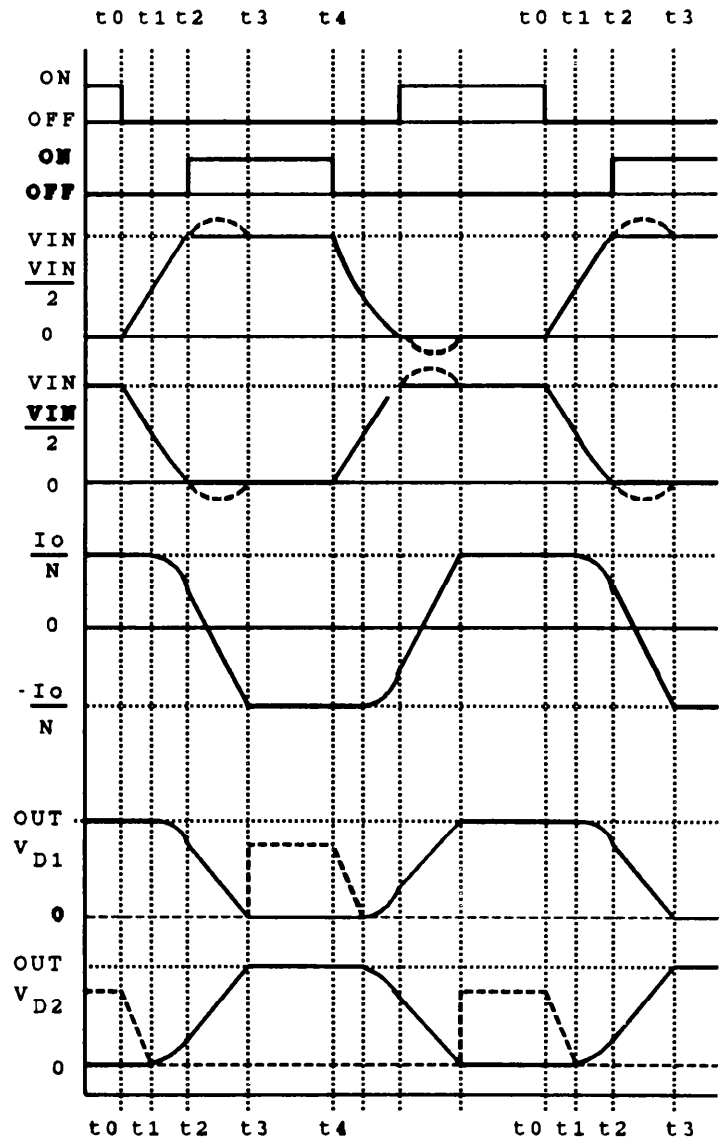


Fig. 17 -- ZVS Half Bridge Wavefoms

ZVS Full Bridge: The equations represented for the forward topology apply equally well for one conversion cycle of the full bridge topology, including the transformer turns ratio. Since the resonant capacitors located at each switch are "in-circuit" at all times, the values should be adjusted accordingly. As with the half bridge converter, the resonant capacitors' voltage will exceed the bulk rails, and clamping via the FET body diodes or external diodes to the rails is common [13].

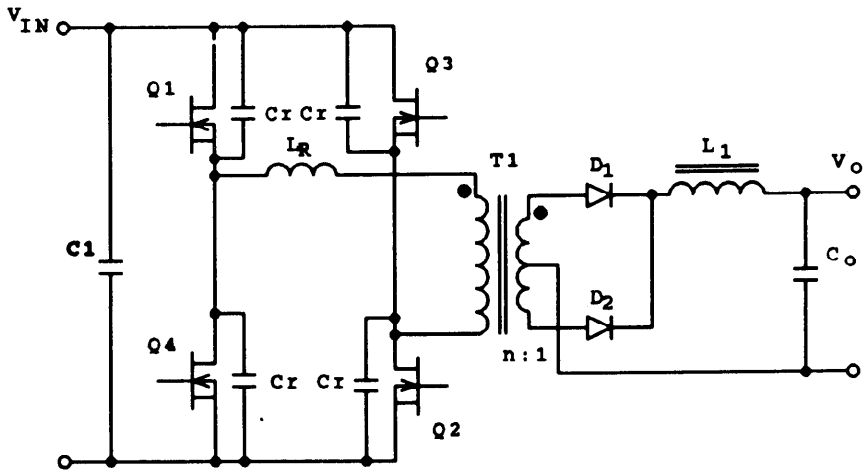


Fig. 18 -- ZVS Full Bridge Circuit

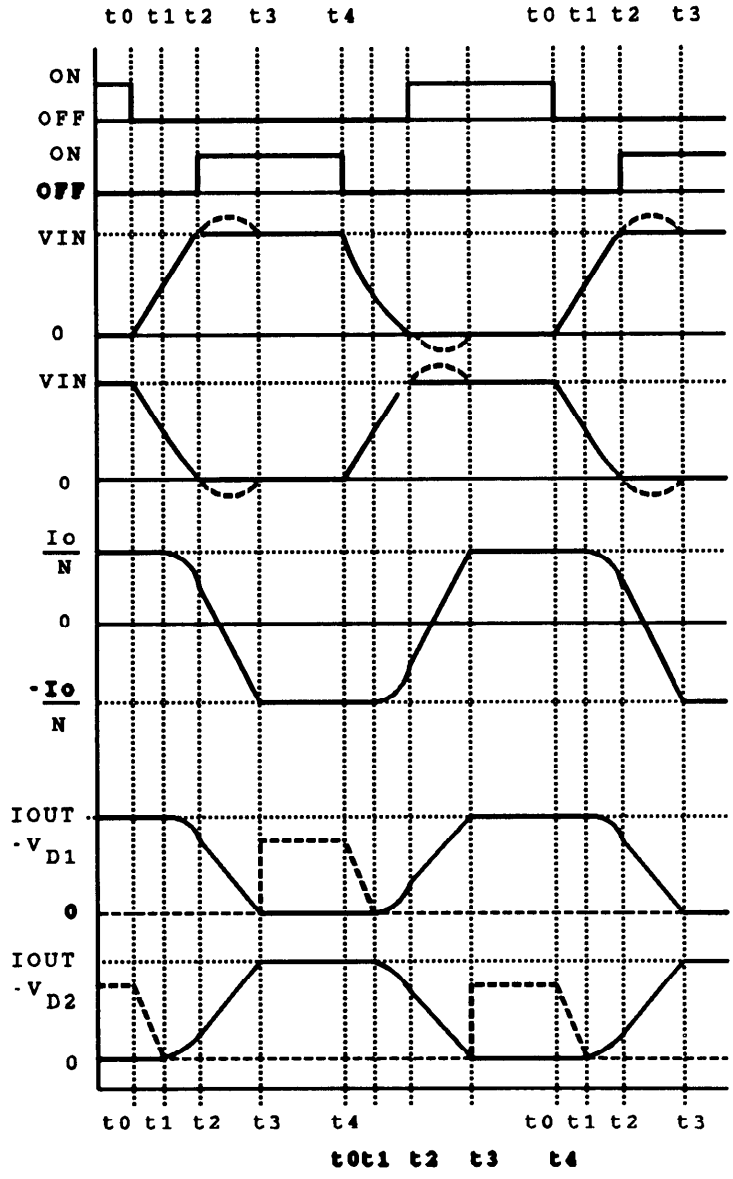


Fig. 19 -- ZVS Full Bridge Wavefoms

ZVS Design Procedure

Buck Derived Topologies -- Continuous output Current:

1. List all input/output specs and ranges.

   V_{IN} min & max ; *Vo* ; I_O min & max

2. Estimate the maximum switch voltages. For unclamped applications (buck and forward):

   $V_{DSmax} = V_{INmax}(1 + (I_{Omax}/I_{Omin})$

   Note: Increase I_{Omin} *if* V_{DSmax} is too high if possible).

   For clamped applications (bridges): $V_{DSmax} = V_{INmax}$

3. Select a resonant tank frequency, ω_R (HINT: $\omega_R = 2\pi f_R$).

4. Calculate the resonant tank impedance and component values.

5. Calculate each of the interval durations (t_{01} thru t_{34}) and their ranges as a function of all line and load combinations.
   (See Appendix for a sample computer program written in BASIC)

   Additionally, summarize the results to establish the range of conversion frequencies, peak voltages and currents, etc.

6. **Analyze the results.** Determine if the frequency range is suitable for the application. If not, a recommendation is to limit the load range by raising I_{Omin} and start the design procedure again. Verify also that the design is feasible with existing technology and components.

7. Finalize the circuit specifics and details.

- ☐ Derive the transformer turns ratio. (non-buck applications)
- ☐ Design the output filter section based upon the lowest conversion frequency and output ripple **current,I_O(ac).**
- ☐ Select applicable components; diode, MOSFET etc.

8. Breadboard the circuit **carefully** using RF techniques wherever possible. Remember -- parasitic inductances and capacitances prefer to resonate upon stimulation, and quite often, **unfavorably.**

9. Debug and modify the circuit as required to accommodate component parasitics, layout concerns or packaging considerations.

Avoiding Parasitics

Ringing of the catch diode junction capacitance with circuit inductance (and package leads) will significantly degrade the circuit performance. Probably the most common solution to this everyday occurrance in square wave converters is to shunt the diode with an R-C snubber. Although somewhat dissipative, a compromise can be established between snubber losses and parasitic overshoot caused by the ringing. Unsnubbed examples of various applicable diodes are shown in Fig. 20 below.

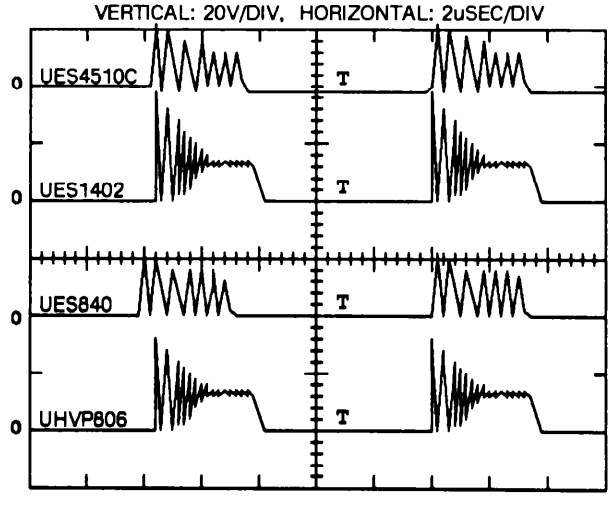


Fig. 20 -- Catch Diode Ringing

Multiresonant ZVS Conversion

Another technique to avoid the parasitic resonance involving the catch diode capacitance is to shunt it with a capacitor much larger than the junction capacitance. Labelled C_D, this element introduces favorable switching characteristics for both the switch and catch diode. The general circuit diagram and associated waveforms are shown below, but will not be explored further in this presentation [14,15].

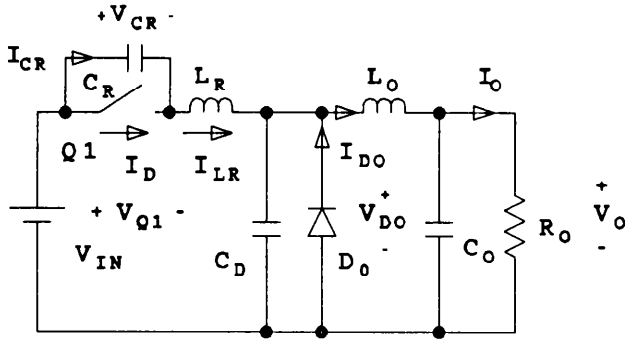


Fig. 21 -- Multiresonant ZVS Circuit

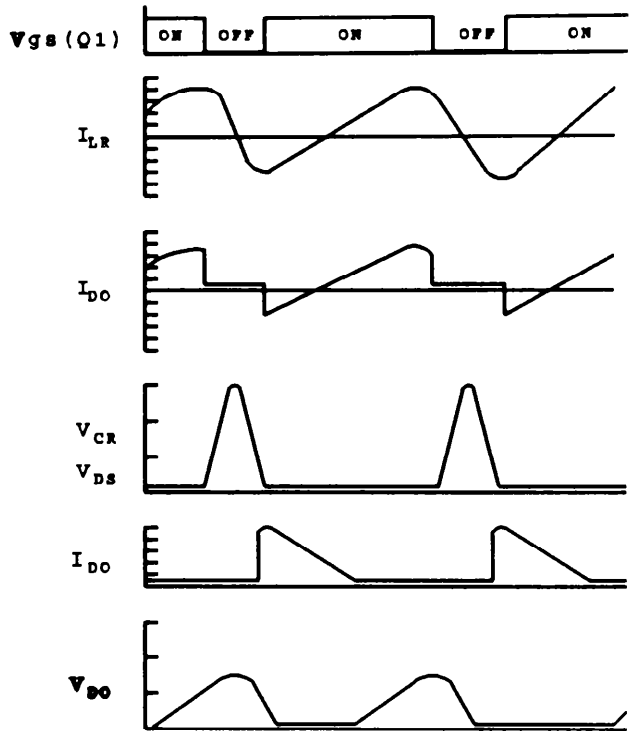


Fig. 22 -- Multiresonant Waveforms

Current Mode Controlled ZVS Conversion

Variable frequency power converters can also benefit from the use of current mode control. Two loops are used to determine the precise ON time of the power switch -- an "outer" voltage feedback loop, and an "inner" current sensing loop. The advantage to this approach is making the power stage operate as a voltage controlled current source. This eliminates the two pole output inductor characteristics in addition to providing enhanced dynamic transient response.

Principles of operation. Two control ICs are utilized in this design example. The UC3843A PWM performs the current mode control by providing an output pulse width determined by the two control loop inputs. This pulse width, or repetition rate is used to set the conversion period of the UC3864 ZVS resonant controller. Rather than utilize its voltage controlled oscillator to generate the conversion period, it is determined by the UC3843A output pulse width.

Zero voltage switching is performed by the UC3864 one-shot timer and zero crossing detection circuitry. When the resonant capacitor voltage crosses zero, the UC3864 output goes high. This turns ON the power switch and recycles the UC3843A to initiate the next current mode controlled period. The UC3864 fault circuitry functions, but its error amplifier and VCO are not used.

ZVS Forward Converter -- Design Example

1. List circuit specifications:

V_{IN} = 18 to 26 V
V_O = 5.0 V ; I_O = 2.5 to 10 A

2. Estimate the maximum voltage across the switch:

$V_{DSmax} = V_{INmax}(1 + (I_{Omax}/I_{Omin}))$
=26•(1+(10/2.5)) = 26•5 = 130 V

3. Select a resonant tank frequency, ω_R.

A resonant tank period frequency of 500KHz will be used. It was selected as a compromise between high frequency operation and low parasitic effects of the components and layout.

f_R = 500KHz ; $\omega_R = 3.14 \cdot 10^6$ radians/sec

4. Calculate the resonant tank impedance and component values.

Resonant tank impedance, $Z_R > V_{INmax}/I_{Omin}$

To accommodate the voltage drop across the MOSFET, calculate $V_{DS(on)min}$, which equals $R_{DS(on)}I_{Omin}$ = 0.8 · 2.5 = 2V

$Z_R = (V_{INmax} - V_{DSmin})/I_{Omin}$

$Z_R = (26-2)/2.5 = 10\ \Omega$

$C_R = 1/(Z_R\omega_R) = 1/(10 \cdot 3.14 \cdot 10^6) = 32nF$

$L_R = Z_R/\omega_R = 10/3.34 \cdot 10^6 = 3.18\mu H$

5. Calculate each of the interval durations (t_{01} thru t_{34}) and ranges as they vary with line and load changes.

The zero voltage switched buck converter "gain" in kiloHertz per volt of V_{IN} and kHz per amp of I_O can be evaluated over the specified ranges. A summary of these follows:

Table VI - Interval Durations vs. Line & Load

	V_{IN}=18 I_O=2.5	V_{IN}=18 I_O=10	V_{IN}=26 I_O=2.5	V_{IN}=26 I_O=10
t_{10}	0.217	0.055	0.314	0.078
t_{12}	1.29	1.06	1.49	1.08
t_{23}	0.93	3.72	0.64	2.58
t_{34}	1.39	6.68	0.78	1.78
T_{CONV}	3.83	11.51	3.23	5.52
f_{CONV}	261kHz	87kHz	310kHz	181kHz
Transistor Switch Durations:				
t_{ON}	2.32	10.4	1.42	4.36
t_{OFF}	1.51	1.11	1.80	1.16

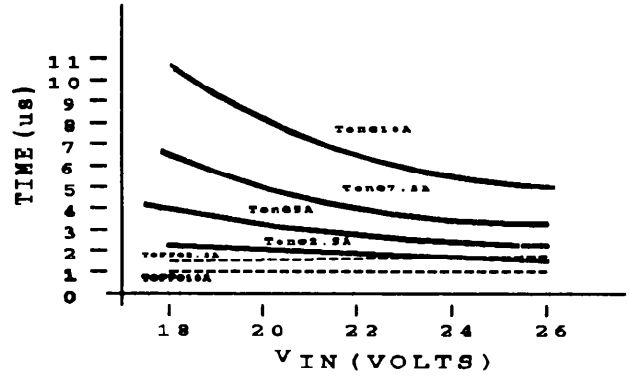


Fig. 23 - Switch Times vs. Line & Load

df_{CONV}/dV_{IN} vs I_O

I_O =	2.5A	5A	7.5A	10A	avg
df/dV =	6.1	11.2	11.9	11.7	10.2

Highest "gain" (11.9 kHz/V) occurs near full load.

df_{CONV}/dI_O vs V_{IN}

V_{IN} =	18	20	22	24	26	avg
df/dV =	23.3	22.1	20.5	18.8	17.3	20.4

Highest "gain" (23.3 kHz/A) occurs at V_{INmin}.

It may be necessary to use the highest gain values to design the control loop compensation for stability over all operating conditions. While this may not optimize the loop transient response for all operating loads, it will guarantee stability over the extremes of line and load.

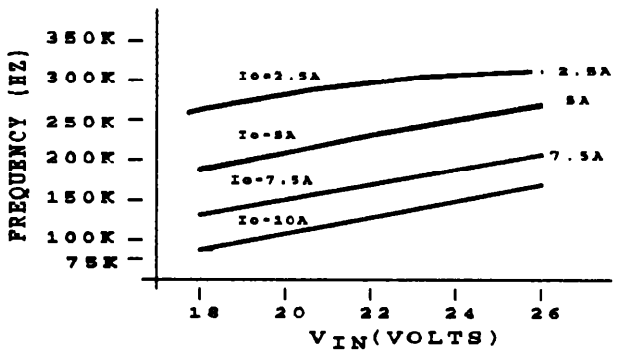


Fig. 24 - Conversion Freq. vs. Line & Load

6. Analyze the results.

The resonant component values, range of conversion frequencies, peak voltage and current ratings seem well within the practical limits of existing components and technology.

7. Finalize the circuit specifics and details based on the information obtained above.

A. Output Filter Section: Select L_O and C_O for operation at the lowest conversion frequency and designed ripple current.

B. Heatsink Requirements: An estimate of the worst case power dissipation of the power switch and output catch diode can be made over line and load ranges.

C. Control Circuit: The UC3861-64 series of controllers will be examined and programmed per the design requirements.

Programming the Control Circuit

One-shot= Accommodating Off-time Variations. The switch off-time varies with line and load by ≈ ± 35% in this design example using ideal components. Accounting for initial tolerances and temperature effects results in an much wider excursion. For all practical purposes, a true fixed off-time technique will ***not*** work.

Incorporated into the UC3861 family of ZVS controllers is the ability to modulate this off-

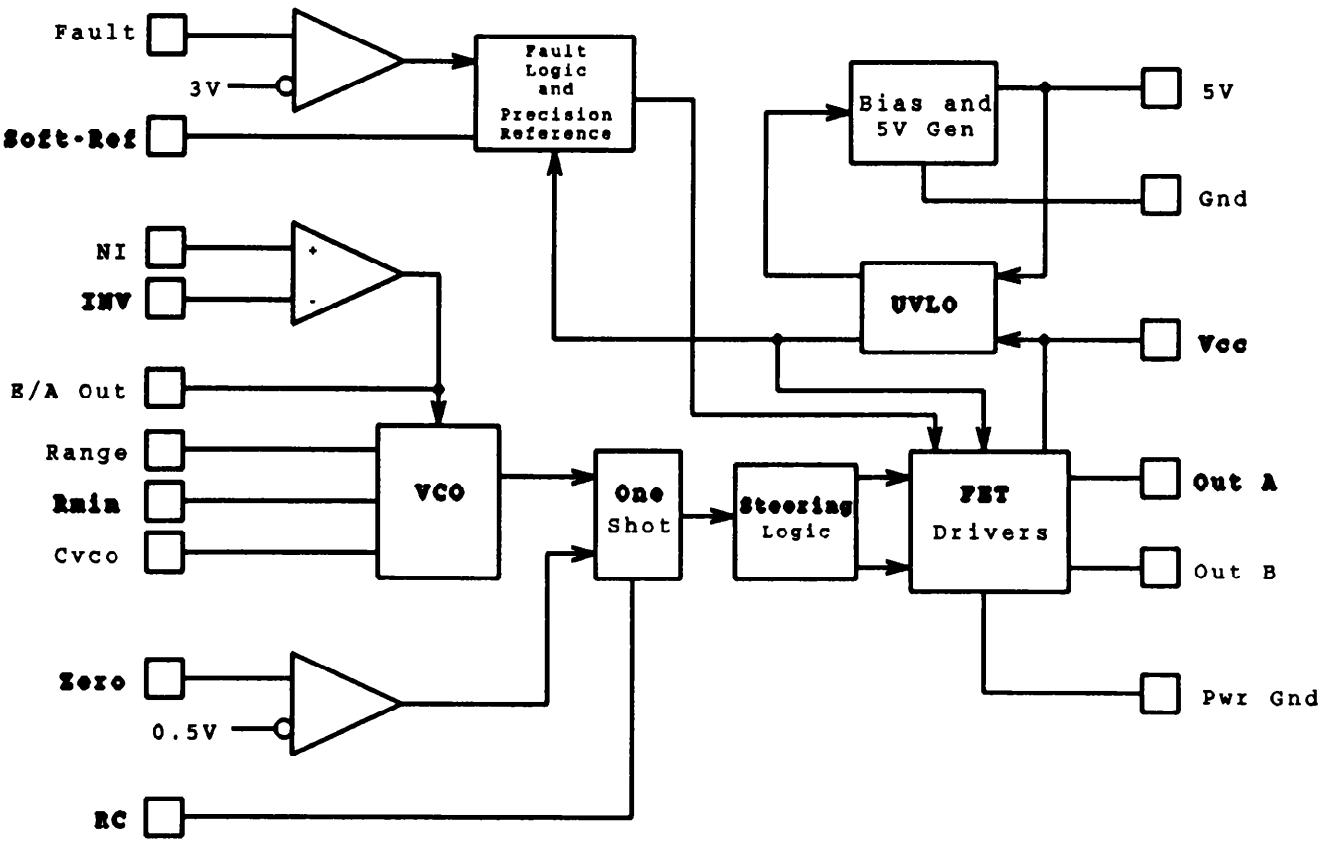


Fig. 25 -- The UC3861-64 ZVS Controllers -- Block Diagram

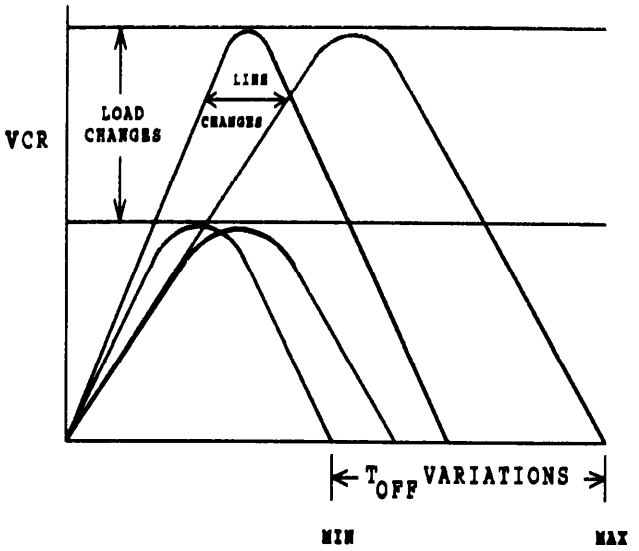


Fig. 26 -- C_R Volts & Off-time vs. Line & Load

time. Initially, the one-shot is programmed for the maximum off-time, and modulated via the ZERO detection circuitry. The switch drain-source voltage is sensed and scaled to initiate turn-on when the precision 0.5V threshold is crossed. This offset was selected to accommodate propogation delays between the instant the threshold is sensed and the instant that the switch is actually turned on. Although brief, these delays can become significant in high frequency applications, and if left unaccounted, can cause NONZERO switching transitions.

Referring to Fig. 26, in this design, the off-time varies between 1.11 and 1.80 microseconds, using ideal components and neglecting temperature effects on the resonant components. Since the ZERO detect logic will facilitate "true" zero voltage switching, the off-time can be set for a much greater period. The one-shot has a 3:1 range capability and will be programmed for 2.2 uS (max), controllable down to 0.75 uS. Programming of the one-shot requires a single R-C time constant, and is straightforward using the design information and equations from the data sheet. Implementation of this feature is shown in the control circuit schematic.

Programming the VCO. The calculated range of conversion frequencies spans 87 to 310 kHz. These values will be used for this "first cut" draft of the control circuit programming. Due to the numerous circuit specifics omitted from the computer program for simplicity, the actual range of conversion frequencies will probably be somewhat wider than planned. Later, the actual timing component values can be adjusted to accommodate these differences.

First, a minimum f_C of 75 kHz has been selected and programmed according to the following equation:

$$F_{VCOmin} = 3.6/(R_{min}C_{VCO})$$

The **maximum** f_C of 350 kHZ is programmed by:

$$F_{VCOmax} = 3.6/(R_{min} \parallel R_{range}) \cdot C_{VCO}$$

Numerous values of R_{min} and C_{VCO} will satisfy the equations. The procedure can be simplified by letting R_{min} equal 100K.

$$C_{VCO}\ (\mu F) = 0.036/f_{min}\ (kHz)$$

$$R_{RANGE}\ (k\Omega) = 100/(f_{CONVmax}/f_{CONVmin} - 1)$$

where $R_{min} = 100K$, $C_{VCO} = 470pF$, $R_{RANGE} = 27K$

The VCO gain in frequency per volt from the error amplifier output is approximated by:

$$dF/dV = 1/(R_{RANGE}C_{VCO}) = 78.2\ kHz/V$$

with an approximate 3.6 volt delta from the error amplifier.

VOLTAGE **CONTROLLED OSCILLATOR**

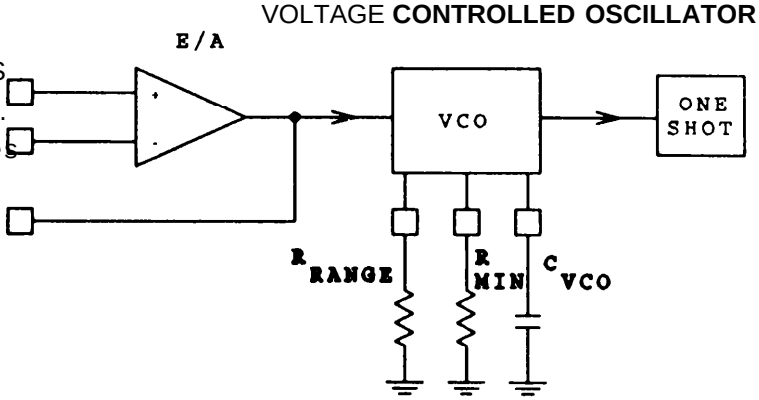


Fig. 27 -- E/A - VCO Block Diagram

Fault Protection - Soft Start & Restart Delay One of the unique features of the UC 3861 family of resonant mode controllers can be found in its fault management circuitry. A single pin connection interfaces with the soft start, restart delay and programmable fault mode protection circuits. In most applications, one capacitor to ground will provide full protection upon power-up and during overload conditions. Users can reprogram the timing relationships or add control features (latch off following fault, etc) with a single resistor.

Selected for this application is a 1 uF soft-restart capacitor value, resulting in a soft-start duration of 10 ms and a restart delay of approximately 200 ms. The preprogrammed ratio of 19:l (restart delay to soft start) will be utilized, however the relevant equations and relationships have also been provided for other applications. Primary current will be utilized as the fault trip mechanism, indicative of an overload or short circuit current condition. A current transformer is incorporated to maximize efficiency when interfacing to the three volt fault threshold.

Optional Programming of T_{SS} and T_{RD} :

Soft Start: $T_{SS} = C_{SR} \bullet$ 10K

Restart Delay: $T_{RD} = C_{SR} \bullet$ 19OK

Timing Ratio: $T_{RD}:T_{SS}$ = 19:l

Gate Drive: Another unique feature of the UC 3861-64 family of devices is the optimal utilization of the silicon devoted to output totem pole drivers. Each controller uses two pins for the A and B outputs which are internally configured to operate in either unison or in an alternating configuration. Typical performance for these 1 Amp peak totem pole outputs shows 30 ns rise and fall times into **1nF.**

Loop Compensation -- General Information. The ZVS technique is similar to that of conventional voltage mode square wave conversion which utilizes a single voltage feedback loop. Unlike the dual loop system of current mode control, the ZVS output filter section exhibits

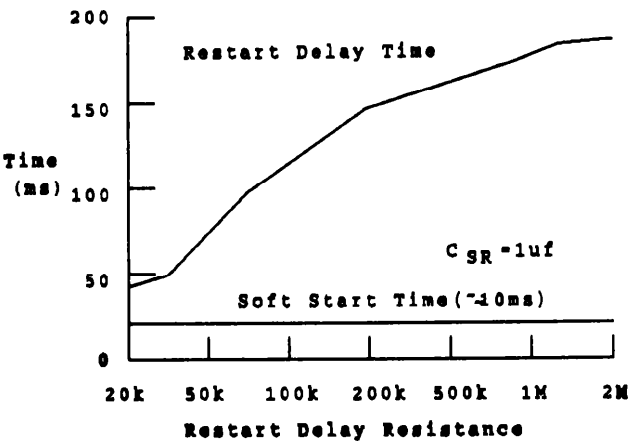


Fig. 28 -- Programming T_{SS} and T_{RD}

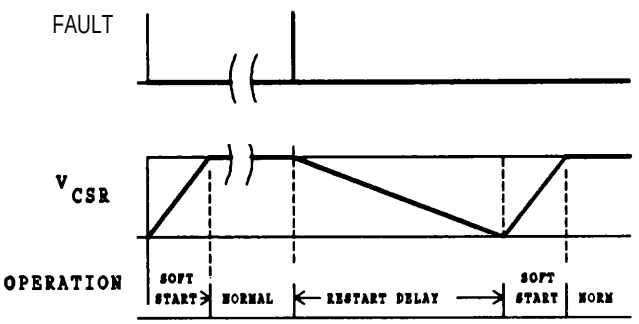


Fig. 29 -- Fault Operational Waveforms

a two pole-zero pair and is compensated accordingly. Generally, the overall loop is designed to cross zero dB at a frequency below one-tenth that of the switching frequency. In this variable frequency converter, the lowest conversion frequency will apply, corresponding to approximately 85 KHz, for a zero crossing of 8.5 KHz. Compensation should be optimized for the highest low frequency gain in addition to ample phase margin at crossover. Typical examples utilize two zeros in the error amplifier compensation at a frequency equal to that of the output filter's two pole break. An additional high frequency pole is placed in the loop to combat the zero due to the output capacitance ESR, assuming adequate error amplifier gain-bandwidth.

A noteworthy alternative is the use of a two loop approach which is similar to current mode control, eliminating one of the output poles. One technique known as Multi-Loop Control for Quasi-Resonant Converters [18] has been

developed. Another, called Average Current Mode Control is also a suitable candidate,

$$\omega_{P1} = \frac{1}{R_{FP}C_F} \quad ; \quad \omega_{Z1} = \frac{1}{(R_{FP} \| R_{FZ})C_F}$$

$$\omega_{Z2} = \frac{1}{(R_{IP}+R_{IZ})C_I} \quad ; \quad \omega_{P2} = \frac{1}{R_{IP}C_I}$$

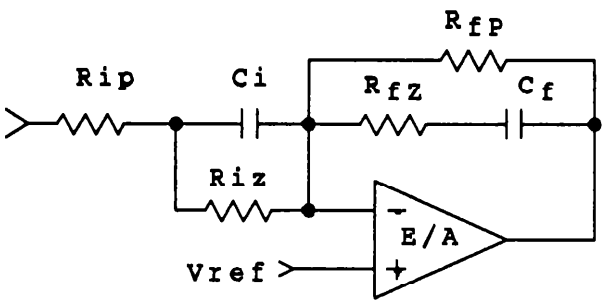


Fig. 30 - Error Amplifier Compensation

Summary

The zero voltage switched quasi-resonant technique is applicable to most power conversion designs, but is most advantageous to those operating from a high voltage input. In these applications, losses associated with discharging of the MOSFET output capacitance can be significant at high switching frequencies, impairing efficiency. Zero voltage switching avoids this penalty by negating the drain-to-source, "off-state" voltage via the resonant tank.

A high peak voltage stress occurs across the switch during resonance in the buck regulator and single switch forward converters. Limiting this excursion demands limiting the useful load range of the converter as well, an unacceptable solution in certain applications. For these situations, the zero voltage switched multi-resonant approach [14,15] could prove more beneficial than the quasi-resonant ZVS variety.

Significant improvements in efficiency can be obtained in high voltage, half and full bridge ZVS applications when compared to their square wave design complements. Clamping of

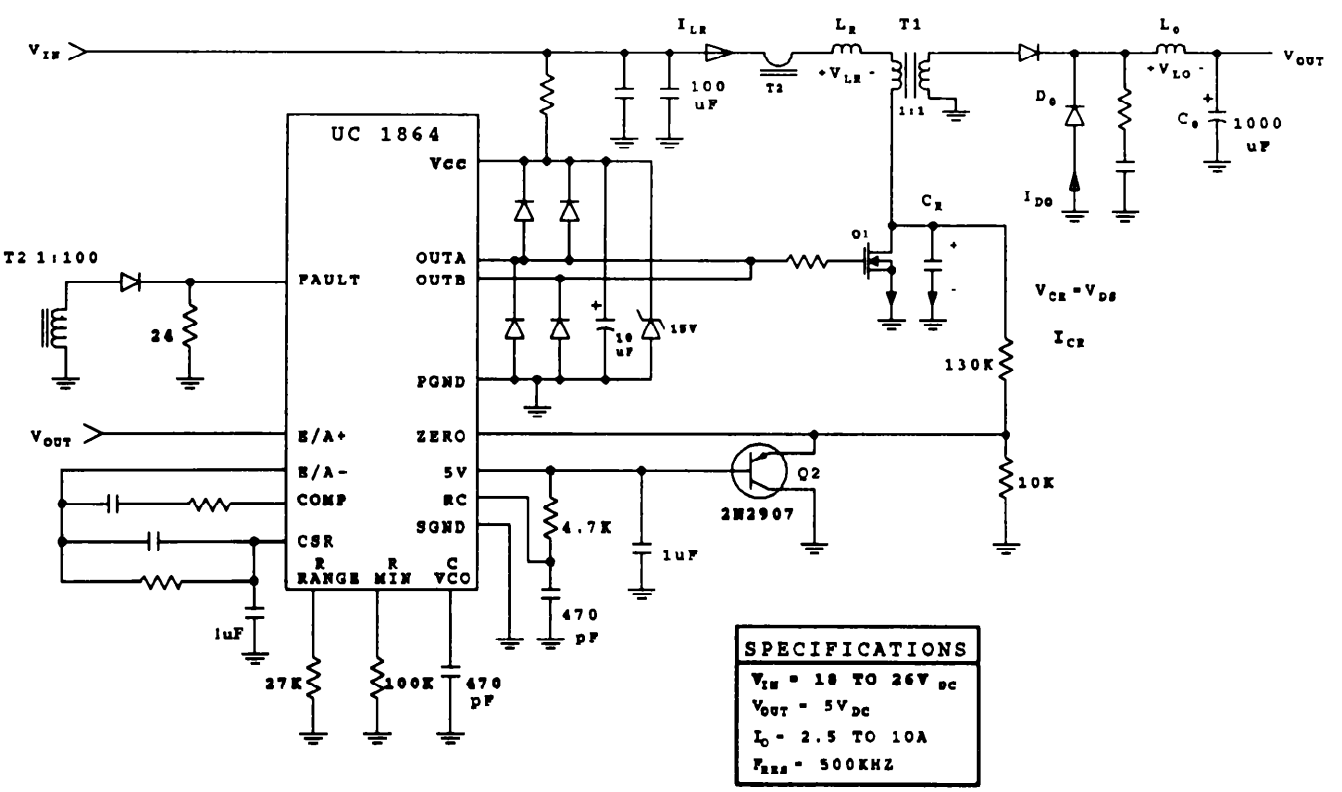


Fig. 31 - Zero Voltage Switched Forward Converter

the peak resonant voltage to the input rails avoids the high voltage overshoot concerns of the single switch converters, while transformer reset is accomplished by the bidirectional switching. Additionally, the series transformer primary and circuit inductances can beneficial, additives in the formation of the total resonant inductor value. This not only reduces size, but incorporates the detrimental parasitic generally snubbed in square wave designs, further enhancing efficiency.

A new series of control ICs has been developed specifically for the zero voltage switching techniques with a list of features to facilitate lossless switching transitions with complete fault protection. The multitude of functions and ease of programmability greatly simplify the interface to this new generation of power conversion techniques; those developed in response to the demands for increased power density and efficiency.

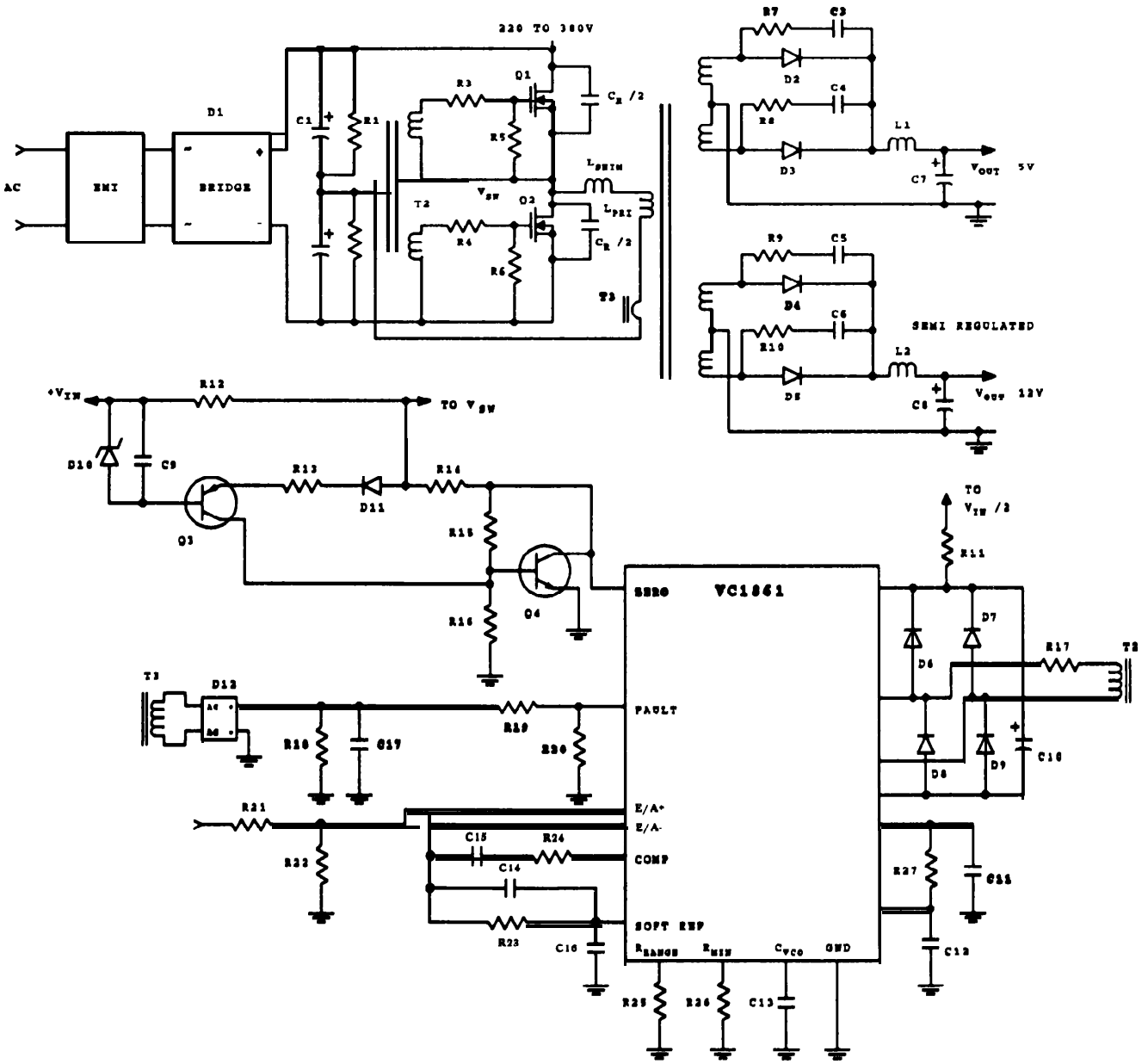


Fig. 32 -- Zero Voltage Switched Half-Bridge Converter

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```
10 ' Zero Voltage Switching Calculations and Equations
20 ' Using the Continuous Current Buck Topology
30 ' in a Typical DC/DC Converter Power Supply Application
40 '
50 PRINTER$ = "lptl:": ' Printer at parallel port #l **********
60 '
70 ' Summary of Variables and Abbreviations
80 '
90 ' Cr = Resonant Capacitor
100 ' Lr = Resonant Inductor
110 ' Zr = Resonant Tank Impedance
120 ' Fres = Resonant Tank Frequency (Hz)
130 '
140 ' VImin = Minimum DC Input Voltage
150 ' VImax = Maximum DC Input Voltage
160 ' Vdson = Mosfet On Voltage = Io*Rds
170 ' Rds = Mosfet On Resistance
180 ' Vdsmax = Peak MOSFET Off State Voltage
190 ' Vo = DC Output Voltage
200 ' Vdo = Output Diode Voltage Drop
210 ' Iomax = Maximum Output Current
220 ' Iomin = Minimum Output Current
230 '
240 ' Start with parameters for low voltage dc/dc buck regulator
250 '
260 ' ****Define 5 Vi and 5 Io data points ranging from min to max*****
270 ' (Suggestion: With broad ranges, use logarithmic spread)
280 DATA 18,20,22,24,27 : 'Vi data
290 DATA 2.5,4,6,8,10 : 'Io data
300 FRES = 500000!
310 VO = 5!
320 VDO = .8
330 RDS = .8
340 SAFT = .95
350 '
360 FOR J = 1 TO 5: READ VI(J): NEXT
370 FOR K = 1 TO 5: READ IO(K): NEXT
380 CLS
390 PRINT "For output to screen, enter 'S' or 'S'."
400 INPUT "Otherwise output will be sent to printer : ", K$
410 IF K$ = "S" OR K$ = "s" THEN K$ = "scrn:" ELSE K$ = PRINTER$
420 OPEN K$ FOR OUTPUT AS #1: CLS
430 PRINT #1, "================================================="
440 PRINT #1, "Zero Voltage Switching Times (uSec) vs. Vi, Io"
450 PRINT #1,"============================================================"
460 '
```

```
470 ' '========HERE GOES========
480 '
490 VIMAX = VI(5): IOMIN = IO(1): IOMAX = IO(5)
500 ZR = (VIMAX - (RDS * IOMIN)) / (IOMIN * SAFT)
510 WR = 6.28 * FRES
520 CR = 1 / (ZR * WR)
530 LR = ZR / WR
540 '
550 FOR J = 1 TO 5: VI = VI(J)
560    PRINT #l, USING "                    Input Voltage = ###.## V"; VI
570    FOR K = 1 TO 5: IO = IO(K)
580       RSIN = (VI / (IO * ZR)):     VDSON = RDS * IO
590 '
600       D(0, K) = IO * .00000l:    ' Compensate for later mult. by 10^6
610       D(l, K) = (CR * VI) / IO: 'dtO1
620       D(2, K) = (3.14 / WR) + (1 / WR) * ATN(RSIN / (1 - RSIN ^ 2)): ‘dt12
630       D(3, K) = (2 * LR * IO) / VI: 'dt23
640       D(6, K) = D(1, K) + D(2, K) + D(3, K): ' dt03
650       D(4, K) = ((VO + VDO) * D(6, K)) / ((VI - VDSON) - (VO + VDO)): 'dt34
660       D(5, K) = D(1 K) + D(2, K) + D(3, K) + D(4, K): 'Tconv
670 NEXT K
680 '
690 PAR$(0) = “Io (A) ="
700  PAR$(l) = “dt01 ="
710  PAR$(2) = “dt12 ="
720  PAR$(3) = "dt23 ="
730  PAR$(4) = "dt34 ="
740 PAR$(5) = "Tconv ="
750  PAR$(6) = "dt03 ="
760 '
770    FOR P = 0 TO 6
780       PRINT #1, PAR$(P);
790       FOR K = 1 TO 5
800          PRINT #l, USING " ####.###"; D(P, K) * l000000!;
810       NEXT K: PRINT #l,
820    NEXT P
830 PRINT #l,
840 NEXT J
850 '
860 PRINT #l, "Additional Information:”
870 PRINT #l, “Zr(Ohms) =“; INT(l000! * ZR) / 1000
880 PRINT #l, “wR(KRads)=“; INT(WR / 1000)
890 PRINT #l. "Cr(nF)    =“; INT((l000 * CR) / 10 ^ -9) / 1000
900 PRINT #l, “Lr(uH)    ="; INT((1000 * LR) / 10 ^ -6) / 1000
910 PRINT #l, “Vdsmax    ="; VIMAX * (1 + IOMAX / IOMIN)
920 END
```

Input Voltage = 18.00 V

Io (A) =	2.500	4.000	6.000	8.000	10.000
dt01 =	0.218	0.136	0.091	0.068	0.054
dt12 =	1.290	1.153	1.096	1.070	1.056
dt23 =	0.931	1.490	2.235	2.980	3.725
dt34 =	1.387	1.791	2.682	4.118	6.677
Tconv =	3.825	4.571	6.103	8.236	11.511
dt03 =	2.439	2.780	3.421	4.118	4.835

Input Voltage = 20.00 V

Io (A) =	2.500	4.000	6.000	8.000	10.000
dt01 =	0.242	0.151	0.101	0.076	0.061
dt12 =	1.339	1.175	1.108	1.079	1.062
dt23 =	0.838	1.341	2.011	2.682	3.352
dt34 =	1.150	1.406	1.987	2.852	4.186
Tconv =	3.569	4.074	5.207	6.688	8.661
dt03 =	2.419	2.667	3.220	3.836	4.475

Input Voltage = 22.00 V

Io (A) =	2.500	4.000	6.000	8.000	10.000
dt01 =	0.266	0.166	0.111	0.083	0.067
dt12 =	1.390	1.198	1.120	1.087	1.069
dt23 =	0.762	1.219	1.829	2.438	3.048
dt34 =	0.988	1.153	1.557	2.136	2.958
Tconv =	3.406	3.737	4.616	5.744	7.141
dt03 =	2.418	2.584	3.060	3.608	4.183

Input Voltage = 24.00 V

Io (A) =	2.500	4.000	6.000	8.000	10.000
dt01 =	0.290	0.182	0.121	0.091	0.073
dt12 =	1.442	1.223	1.133	1.096	1.075
dt23 =	0.698	1.117	1.676	2.235	2.794
dt34 =	0.870	0.975	1.268	1.682	2.241
Tconv =	3.301	3.498	4.199	5.103	6.183
dt03 =	2.431	2.522	2.930	3.421	3.941

Input Voltage = 27.00 V

Io (A) =	2.500	4.000	6.000	8.000	10.000
dt01 =	0.327	0.204	0.136	0.102	0.082
dt12 =	0.516	1.264	1.153	1.109	1.085
dt23 =	0.621	0.993	1.490	1.987	2.483
dt34 =	0.442	0.793	0.983	1.253	1.604
Tconv =	1.906	3.254	3.763	4.451	5.254
dt03 =	1.464	2.461	2.780	3.198	3.650

Additional Information:
Zr(Ohms) = 10.526
wR(KRads)= 3140
Cr(nF) = 30.254
Lr(uH) = 3.352
Vdsmax = 135

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