SLA5081

N-channel
General purpose

External dimensions Ⓐ ··· SLA (15-pin)

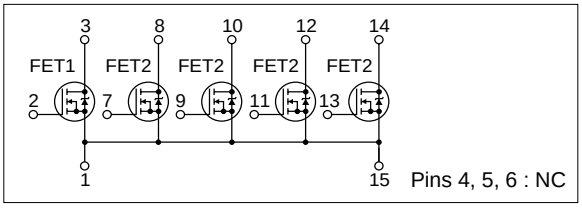
Absolute maximum ratings

(Ta=25°C)

Symbol	Ratings		Unit
	FET 1	FET 2	
V_{DSS}	150		V
V_{GSS}	+20, –10		V
I_D	±7		A
$I_{D\ (pulse)}$*1	±15		A
E_{AS}*2	100		mJ
P_T	5 (T_a=25°C, with all circuits operating, without heatsink)		W
	47 (T_c=25°C, with all circuits operating, with infinite heatsink)		W
$\theta_{j\text{-}a}$	25 (Junction-Air, T_a=25°C, with all circuits operating)		°C/W
$\theta_{j\text{-}c}$	2.66 (Junction-Case, T_c=25°C, with all circuits operating)		°C/W
V_{ISO}	1000 (Between fin and lead pin, AC)		Vrms
Tch	150		°C
Tstg	–40 to +150		°C

*1 : PW≤100μs, duty≤1%
*2 : V_{DD}=25V, L=3.4mH, I_D=7A, unclamped, R_G=50Ω, see Fig. E on page 15.

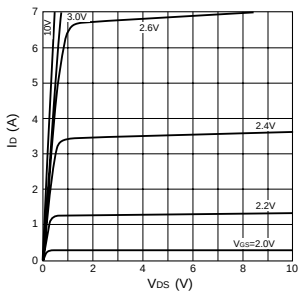
■Equivalent circuit diagram



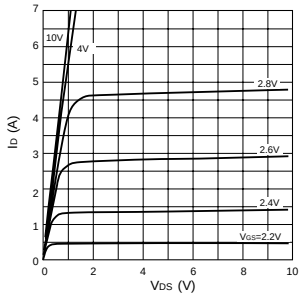
Characteristic curves

I_D-V_{DS} Characteristics (Typical)

FET 1

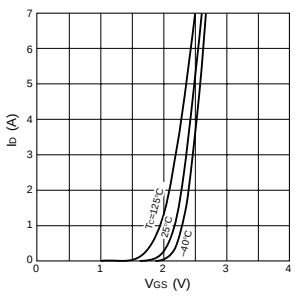


FET 2

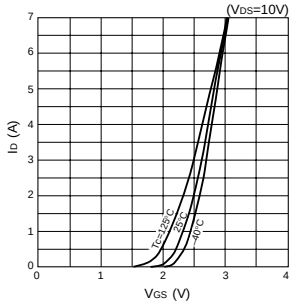


I_D-V_{GS} Characteristics (Typical)

FET 1

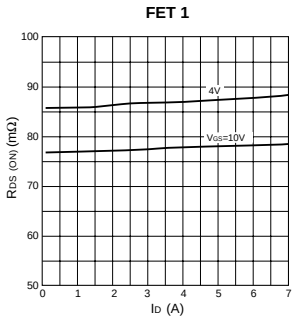


FET 2

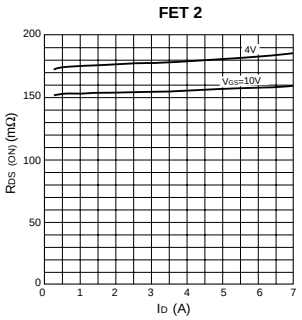


$R_{DS(ON)}$-I_D Characteristics (Typical)

FET 1

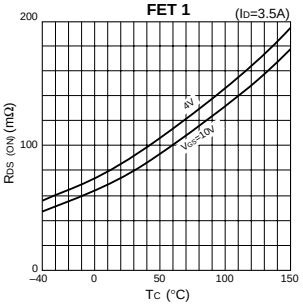


FET 2

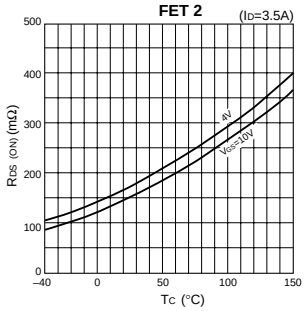


$R_{DS(ON)}$-T_C Characteristics (Typical)

FET 1 (I_D=3.5A)



FET 2 (I_D=3.5A)



Electrical characteristics

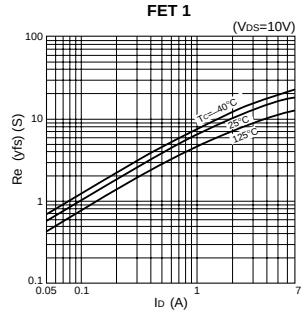
(Ta=25°C)

Symbol	FET 1					FET 2				
	Specification			Unit	Conditions	Specification			Unit	Conditions
	min	typ	max			min	typ	max		
$V_{(BR)DSS}$	150			V	I_D=100μA, V_{GS}=0V	150			V	I_D=100μA, V_{GS}=0V
I_{GSS}			±100	nA	V_{GS}=20V, –10V			±100	nA	V_{GS}=20V, –10V
I_{DSS}			100	μA	V_{DS}=150V, V_{GS}=0V			100	μA	V_{DS}=150V, V_{GS}=0V
V_{TH}	1.0		2.0	V	V_{DS}=10V, I_D=250μA	1.0		2.0	V	V_{DS}=10V, I_D=250μA
$Re_{(yfs)}$	7	12		S	V_{DS}=10V, I_D=3.5A	4	9		S	V_{DS}=10V, I_D=3.5A
$R_{DS(ON)}$		80	105	mΩ	V_{GS}=10V, I_D=3.5A		150	200	mΩ	V_{GS}=10V, I_D=3.5A
		85	115	mΩ	V_{GS}=4V, I_D=3.5A		170	230	mΩ	V_{GS}=4V, I_D=3.5A
Ciss		1600		pF	V_{DS}=10V,		870		pF	V_{DS}=10V
Coss		380		pF	f=1.0MHz,		320		pF	f=1.0MHz
Crss		90		pF	V_{GS}=0V		210		pF	V_{GS}=0V
td (on)		35		ns	I_D=3.5A,		25		ns	I_D=3.5A
tr		70		ns	V_{DD}≒70V,		55		ns	V_{DD}≒70V
td (off)		125		ns	R_L=20Ω,		80		ns	R_L=20Ω
tf		90		ns	V_{GS}=5V, see Fig.3 on page 16.		50		ns	V_{GS}=5V, see Fig.3 on page 16.
V_{SD}		1.0	1.5	V	I_{SD}=7A, V_{GS}=0V		1.0	1.5	V	I_{SD}=7A, V_{GS}=0V
trr		320		ns	I_F=±100mA		500		ns	I_F=±100mA

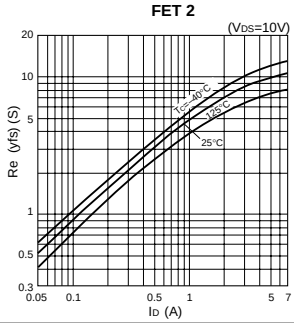
Characteristic curves

$Re_{(yfs)}$-I_D Characteristics (Typical)

FET 1

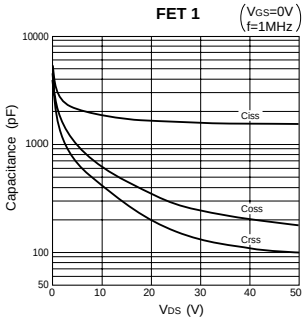


FET 2

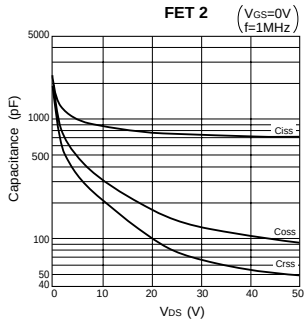


Capacitance-V_{DS} Characteristics (Typical)

FET 1

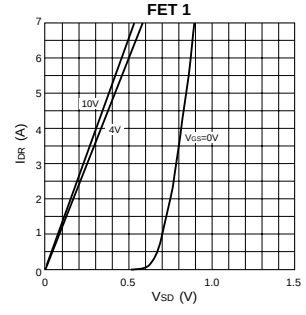


FET 2

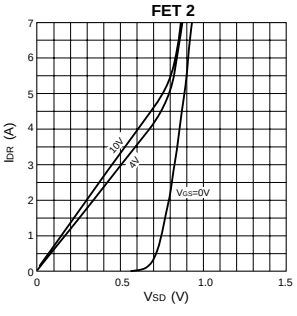


I_{DR}-V_{SD} Characteristics (Typical)

FET 1

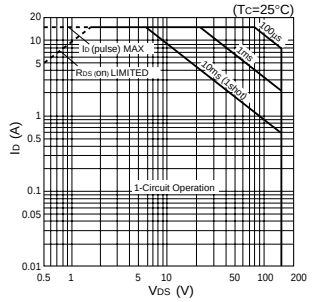


FET 2

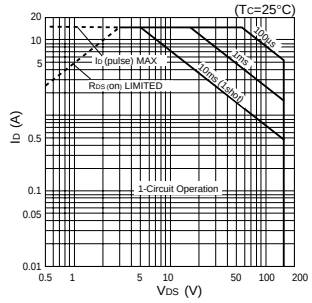


Safe Operating Area (SOA)

FET 1



FET 2



P_T-T_a Characteristics

