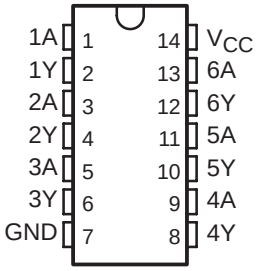
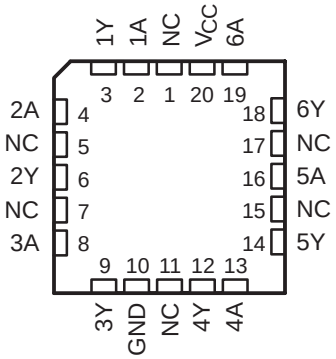
- **2-V to 5.5-V V_{CC} Operation**
- **Max t_{pd} of 6.5 ns at 5 V**
- **Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) >2.3 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Outputs Are Disabled During Power Up and Power Down With Inputs Tied to GND**
- **Support Mixed-Mode Voltage Operation on All Ports**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

SN54LV06A . . . J OR W PACKAGE
SN74LV06A . . . D, DB, DGV, NS, OR PW PACKAGE
(TOP VIEW)



SN54LV06A . . . FK PACKAGE
(TOP VIEW)



NC − No internal connection

description/ordering information

These hex inverter buffers/drivers are designed for 2-V to 5.5-V V_{CC} operation.

The ’LV06A devices perform the Boolean function $Y = \overline{A}$ in positive logic.

The open-drain outputs require pullup resistors to perform correctly and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions.

These devices are fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SOIC − D	Tube of 50	SN74LV06AD	LV06A
		Reel of 2500	SN74LV06ADR	
	SOP − NS	Reel of 2000	SN74LV06ANSR	74LV06A
	SSOP − DB	Reel of 2000	SN74LV06ADBR	LV06A
	TSSOP − PW	Tube of 90	SN74LV06APW	LV06A
		Reel of 2000	SN74LV06APWR	
		Reel of 250	SN74LV06APWT	
	TVSOP − DGV	Reel of 2000	SN74LV06ADGVR	LV06A
−55°C to 125°C	CDIP − J	Tube of 25	SNJ54LV06AJ	SNJ54LV06AJ
	CFP − W	Tube of 150	SNJ54LV06AW	SNJ54LV06AW
	LCCC - FK	Tube of 55	SNJ54LV06AFK	SNJ54LV06AFK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

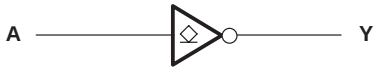
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FUNCTION TABLE
(each buffer/driver)

INPUT A	OUTPUT Y
H	L
L	H

logic diagram, each inverter (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . −0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . −0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O
(see Note 1) . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} (V_I < 0) . . . . . −20 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . −50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . −35 mA
Continuous current through V_{CC} or GND . . . . . ±50 mA
Package thermal impedance, θ_{JA} (see Note 3): D package . . . . . 86°C/W
DB package . . . . . 96°C/W
DGV package . . . . . 127°C/W
NS package . . . . . 76°C/W
PW package . . . . . 113°C/W
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

			SN54LV06A		SN74LV06A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 2.3 V to 2.7 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
		V_{CC} = 3 V to 3.6 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
		V_{CC} = 4.5 V to 5.5 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 2.3 V to 2.7 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
		V_{CC} = 3 V to 3.6 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
		V_{CC} = 4.5 V to 5.5 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	5.5	0	5.5	V
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	μA
		V_{CC} = 2.3 V to 2.7 V		2		2	mA
		V_{CC} = 3 V to 3.6 V		8		8	
		V_{CC} = 4.5 V to 5.5 V		16		16	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 2.3 V to 2.7 V		200		200	ns/V
		V_{CC} = 3 V to 3.6 V		100		100	
		V_{CC} = 4.5 V to 5.5 V		20		20	
T_A	Operating free-air temperature		−55	125	−40	85	°C

PRODUCT PREVIEW

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	SN54LV06A			SN74LV06A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OL}	I_{OL} = 50 μA		2 V to 5.5 V			0.1			0.1	V
	I_{OL} = 2 mA		2.3 V			0.4			0.4	
	I_{OL} = 8 mA		3 V			0.44			0.44	
	I_{OL} = 16 mA		4.5 V			0.55			0.55	
I_I	V_I = 5.5 V or GND		0 to 5.5 V			±1			±1	μA
I_{OH}	$V_I = V_{IL}$,	$V_{OH} = V_{CC}$	5.5 V			±2.5			±2.5	μA
I_{CC}	$V_I = V_{CC}$ or GND,	I_O = 0	5.5 V			20			20	μA
I_{off}	V_I or V_O = 0 to 5.5 V		0			5			5	μA
C_i	$V_I = V_{CC}$ or GND		3.3 V		1.6			1.6		pF

PRODUCT PREVIEW

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switching characteristics over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54LV06A		SN74LV06A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	C_L = 15 pF		5.4*	10.4*	1*	13*	1	13	ns
t_{PHL}					7.2*	10.4*	1*	13*	1	13	
t_{PLH}	A	Y	C_L = 50 pF		9.7	15.2	1	18	1	18	ns
t_{PHL}					9.3	15.2	1	18	1	18	

PRODUCT PREVIEW

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54LV06A		SN74LV06A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	C_L = 15 pF		4.1*	7.1*	1*	8.5*	1	8.5	ns
t_{PHL}					4.9*	7.1*	1*	8.5*	1	8.5	
t_{PLH}	A	Y	C_L = 50 pF		7.1	10.6	1	12	1	12	ns
t_{PHL}					6.4	10.6	1	12	1	12	

PRODUCT PREVIEW

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54LV06A		SN74LV06A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	C_L = 15 pF		3*	5.5*	1*	6.5*	1	6.5	ns
t_{PHL}					3.3*	5.5*	1*	6.5*	1	6.5	
t_{PLH}	A	Y	C_L = 50 pF		4.8	7.5	1	8.5	1	8.5	ns
t_{PHL}					4.4	7.5	1	8.5	1	8.5	

PRODUCT PREVIEW

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics, V_{CC} = 3.3 V, C_L = 50 pF, T_A = 25°C (see Note 5)

PARAMETER		SN74LV06A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.5	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		−0.1	−0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		3.3		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

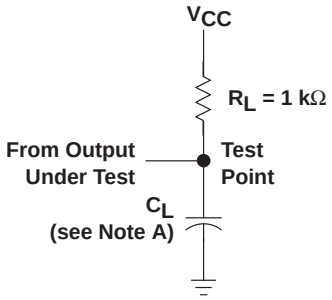
NOTE 5: Characteristics are for surface-mount packages only.

operating characteristics, T_A = 25°C

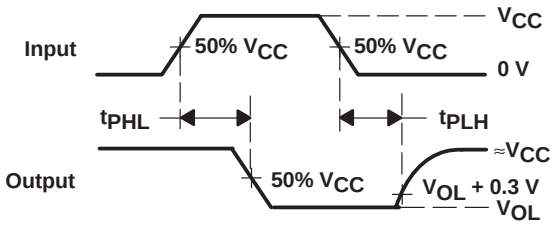
PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 10 MHz	3.3 V	2.6	pF
			5 V	4.7	

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PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR
OPEN-DRAIN OUTPUTS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
C. The outputs are measured one at a time, with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
SN74LV06AD	ACTIVE	SOIC	D	14	50	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74LV06ADBR	ACTIVE	SSOP	DB	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74LV06ADBRE4	ACTIVE	SSOP	DB	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74LV06ADE4	ACTIVE	SOIC	D	14	50	TBD	Call TI	Call TI
SN74LV06ADGVR	ACTIVE	TVSOP	DGV	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74LV06ADGVRE4	ACTIVE	TVSOP	DGV	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74LV06ADR	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74LV06ADRE4	ACTIVE	SOIC	D	14	2500	TBD	Call TI	Call TI
SN74LV06ANSR	ACTIVE	SO	NS	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74LV06ANSRE4	ACTIVE	SO	NS	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74LV06APW	ACTIVE	TSSOP	PW	14	90	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74LV06APWE4	ACTIVE	TSSOP	PW	14	90	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74LV06APWR	ACTIVE	TSSOP	PW	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74LV06APWRE4	ACTIVE	TSSOP	PW	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74LV06APWT	ACTIVE	TSSOP	PW	14	250	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74LV06APWTE4	ACTIVE	TSSOP	PW	14	250	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

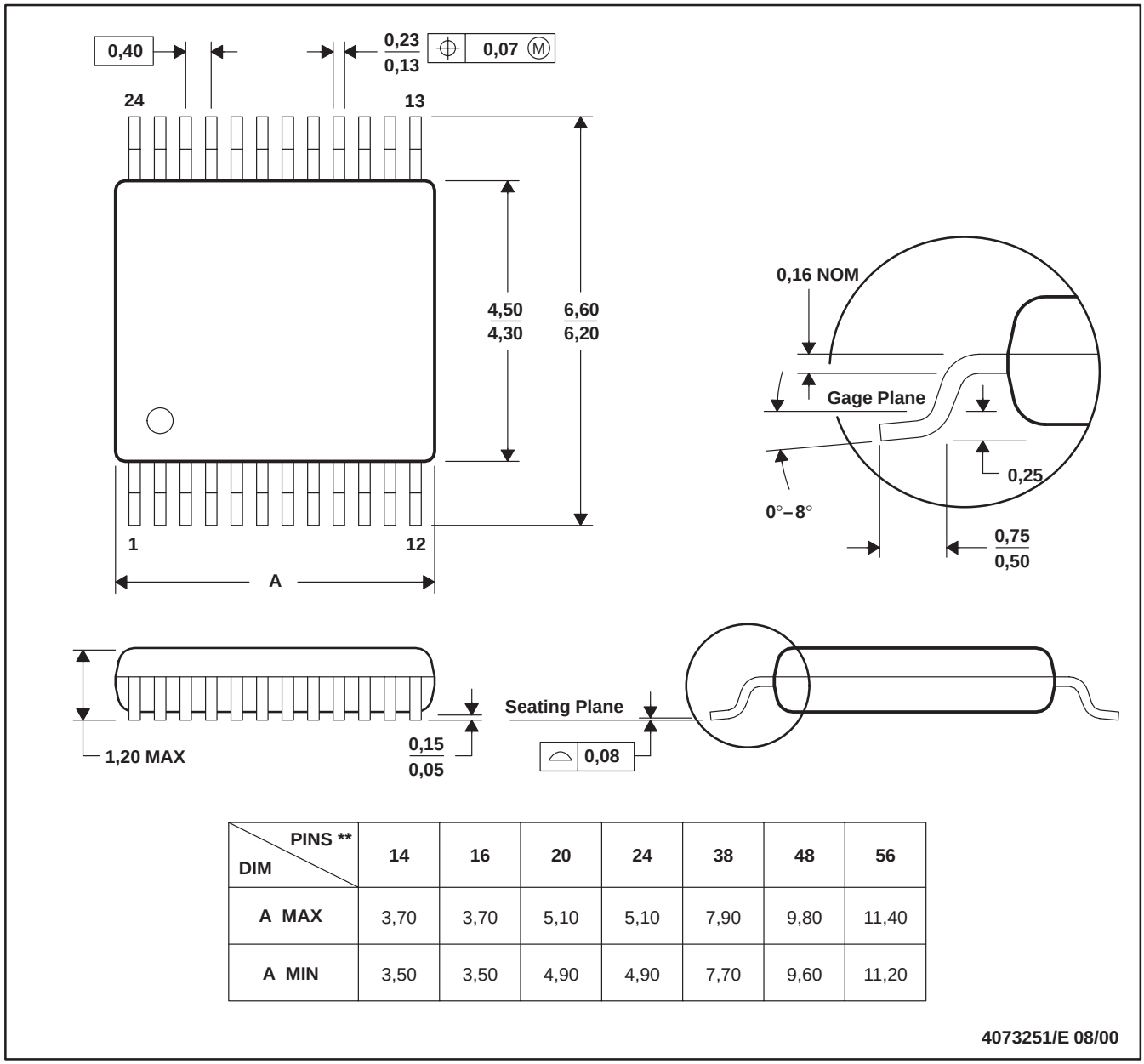
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DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN

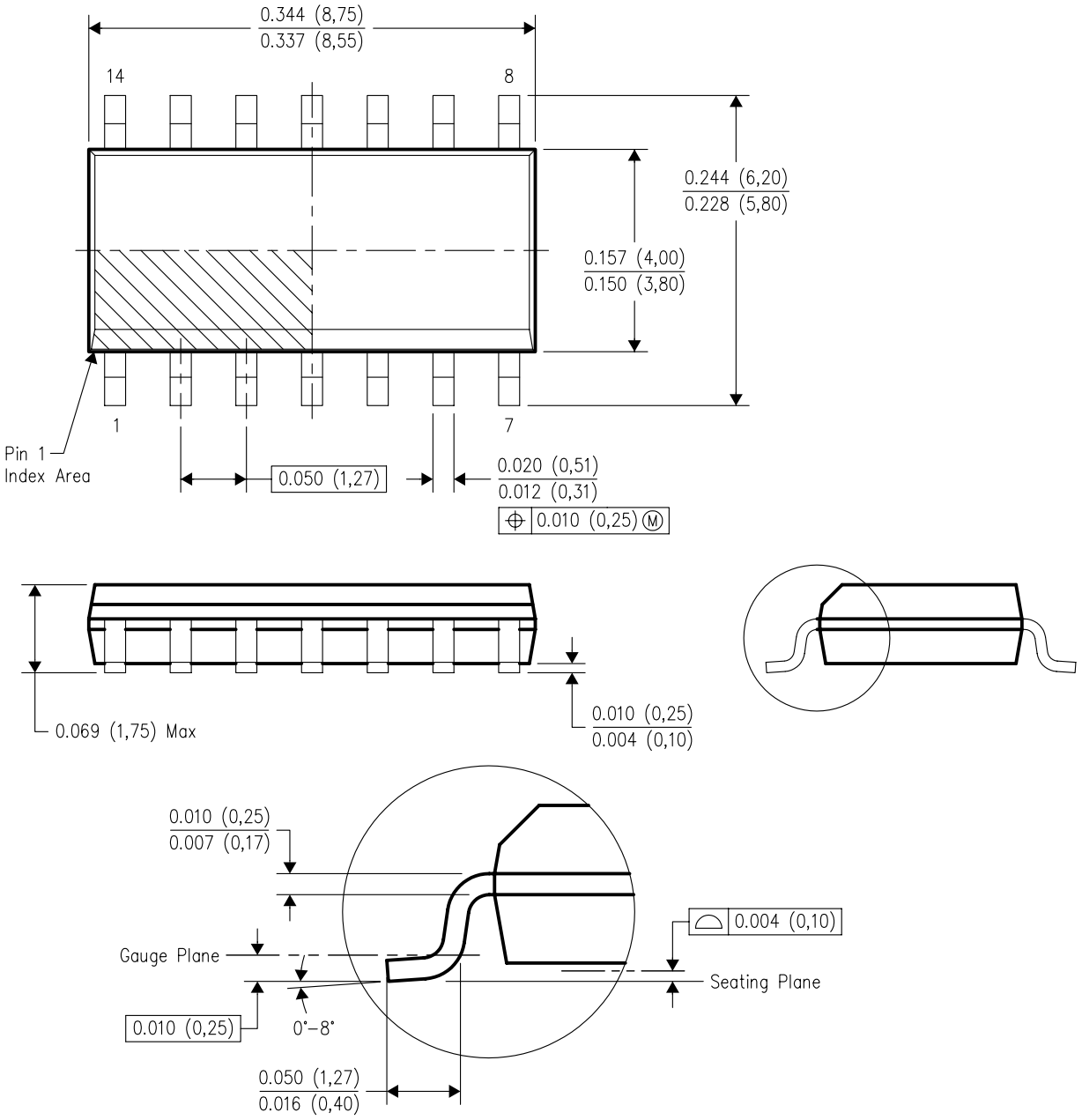


DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

D (R–PDSO–G14) PLASTIC SMALL–OUTLINE PACKAGE

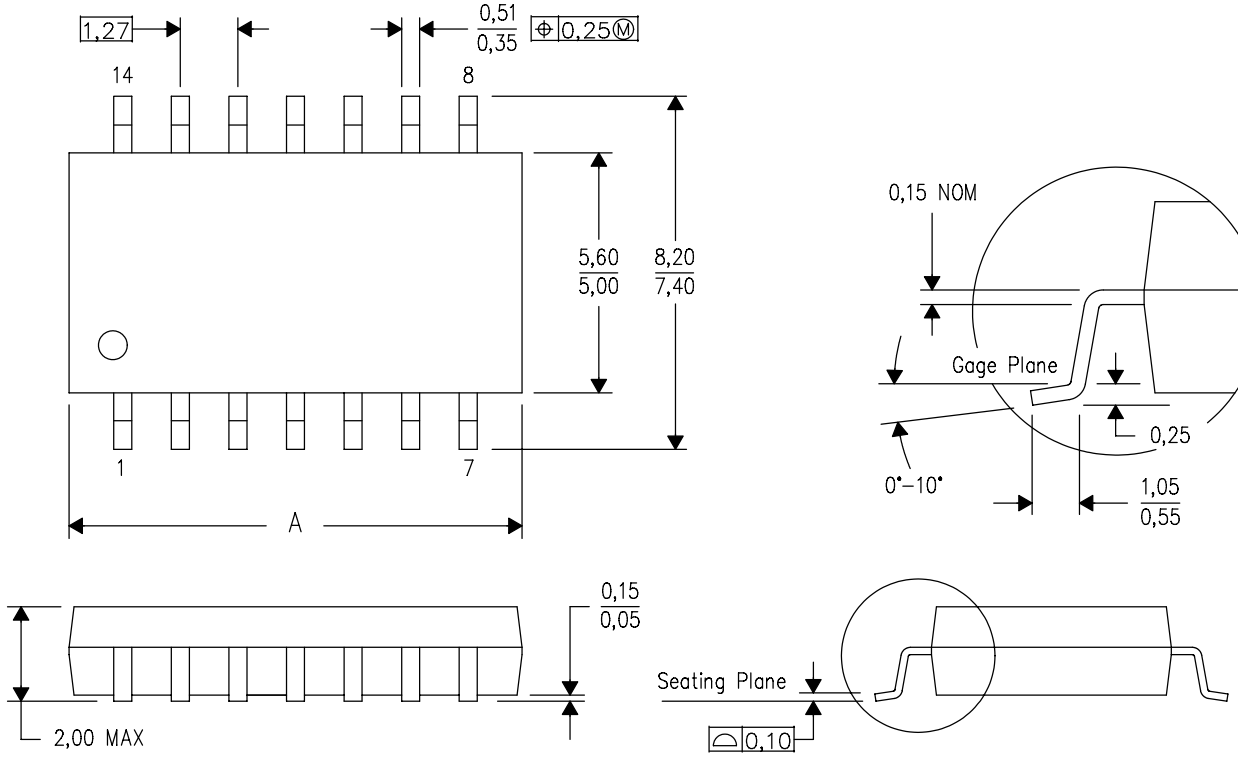


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–012 variation AB.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

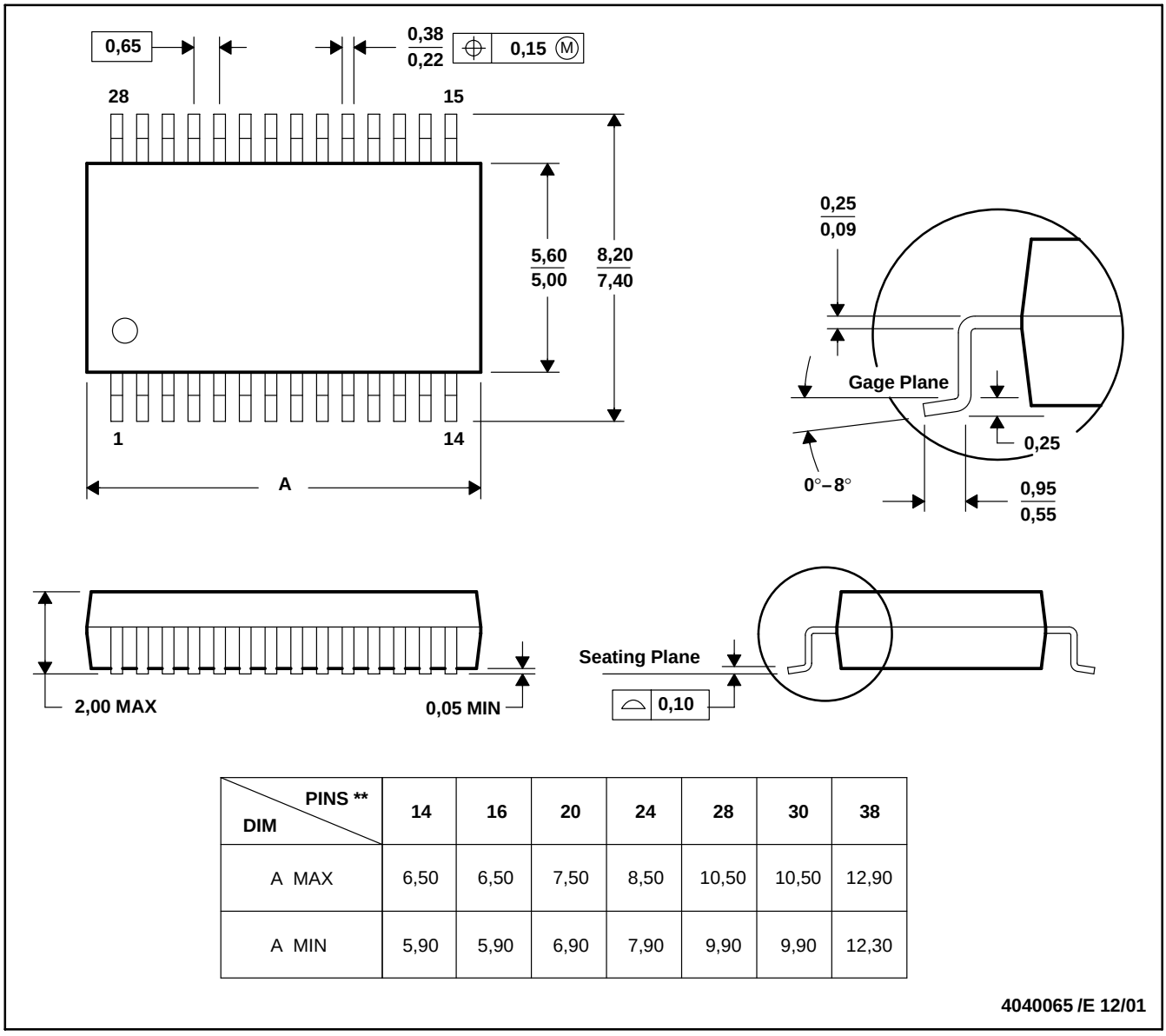
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



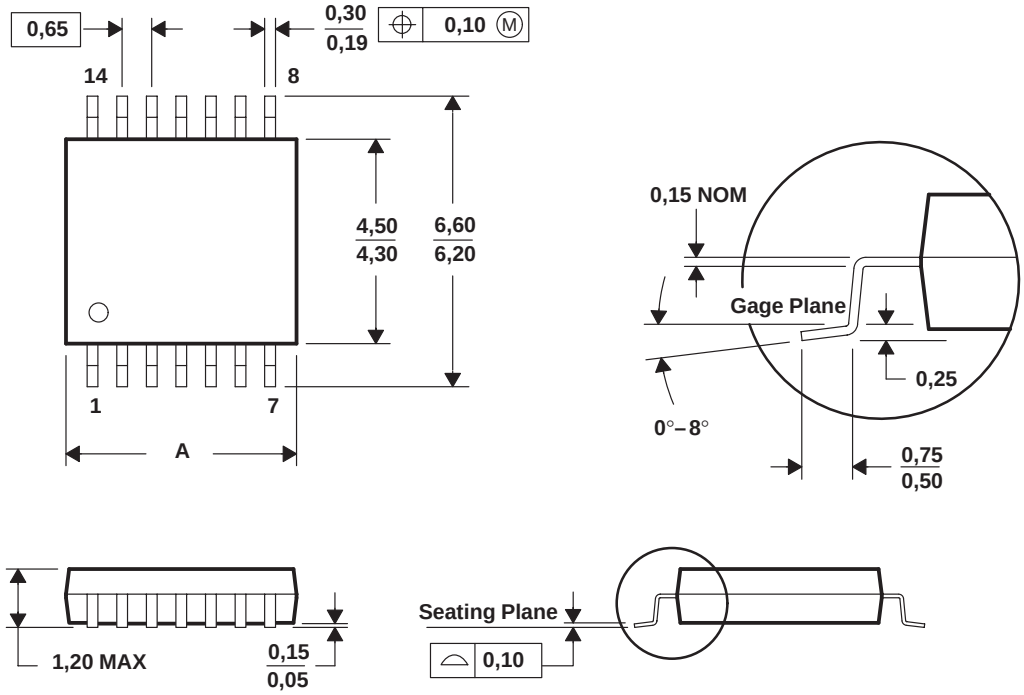
DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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