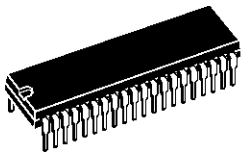
SGS-THOMSON MICROELECTRONICS

M3488

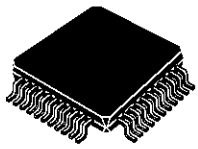
256 x 256 DIGITAL SWITCHING MATRIX

PRELIMINARY DATA

- 256 INPUT AND 256 OUTPUT CHANNEL CMOS DIGITAL SWITCHING MATRIX COMPATIBLE WITH M088
- BUILDING BLOCK DESIGNED FOR LARGE CAPACITY ELECTRONIC EXCHANGES, SUBSYSTEMS AND PABX
- NO EXTRA PIN NEEDED FOR NOT-BLOCKING SINGLE STAGE AND HIGHER CAPACITY SYNTHESIS BLOCKS (512 or 1024 channels)
- EUROPEAN TELEPHONE STANDARD COMPATIBLE (32 serial channels per frame)
- PCM INPUTS AND OUTPUTS MUTUALLY COMPATIBLE
- ACTUAL INPUT-OUTPUT CHANNEL CONNECTIONS STORED AND MODIFIED VIA AN ON CHIP 8-BIT PARALLEL MICROPROCESSOR INTERFACE
- TYPICAL BIT RATE : 2Mbit/s
- TYPICAL SYNCHRONIZATION RATE : 8KHz (time frame is 125µs)
- 5V P0WER SUPPLY
- CMOS & TTL INPUT/OUTPUT LEVELS COMPATIBLE
- HIGH DENSITY ADVANCED 1.2µm HCMOS3 PROCESS



DIP40



PQFP44

ORDERING NUMBERS:

M3488B1 M3488Q1

Main instructions controlled by the microprocessor interface

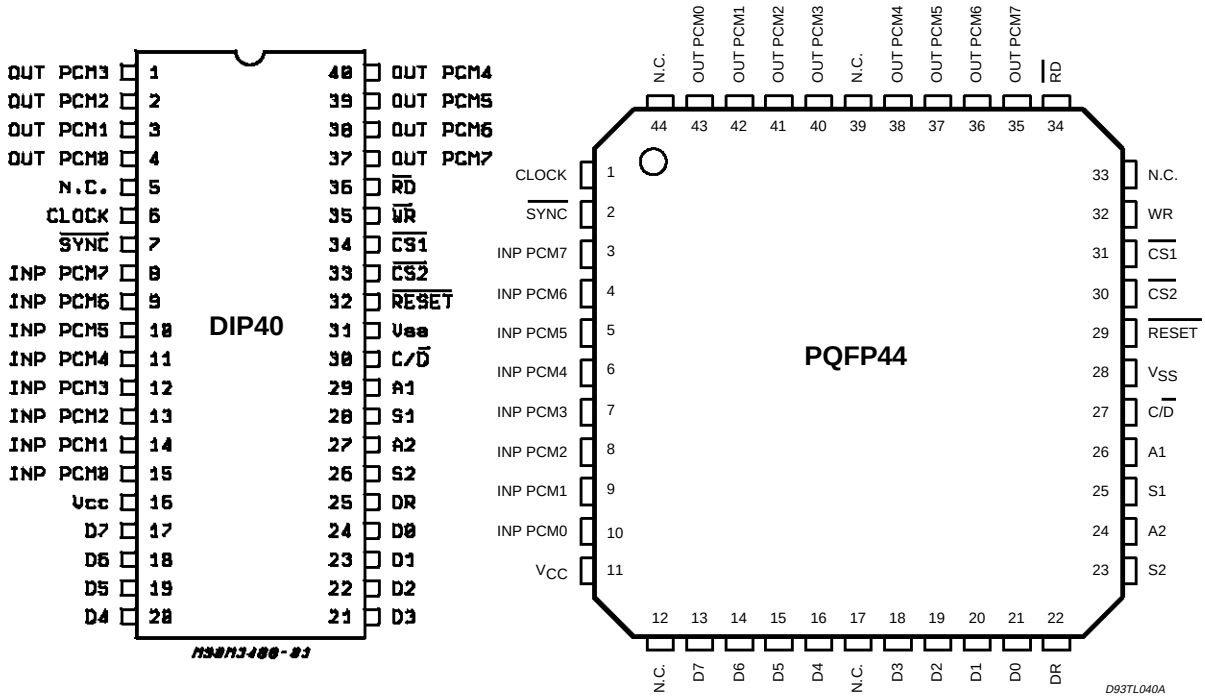
- CHANNEL CONNECTION/DISCONNECTION
- OUTPUT CHANNEL DISCONNECTION
- INSERTION OF A BYTE ON A PCM OUTPUT CHANNEL/DISCONNECTION
- TRANSFER TO THE MICROPROCESSOR OF A SINGLE PCM OUTPUT CHANNEL SAMPLE
- TRANSFER TO THE MICROPROCESSOR OF A SINGLE OUTPUT CHANNEL CONTROL WORD
- TRANSFER TO THE MICROPROCESSOR OF A SELECTED 0 CHANNEL PCM INPUT DATA

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Test Conditions	Unit
V_{CC}	Supply Voltage	-0.3 to 7	V
V_I	Input Voltage	-0.3 to V_{CC}+0.3	V
V_O	Off State Output Voltage	-0.3 to V_{CC}+0.3	V
I_O	Current at Digital Outputs	30	mA
P_{tot}	Total Package Power Dissipation	1.5	W
T_{stg}	Storage Temperature Range	-65 to 150	°C
T_{op}	Operating Temperature Range	0 to 70	°C

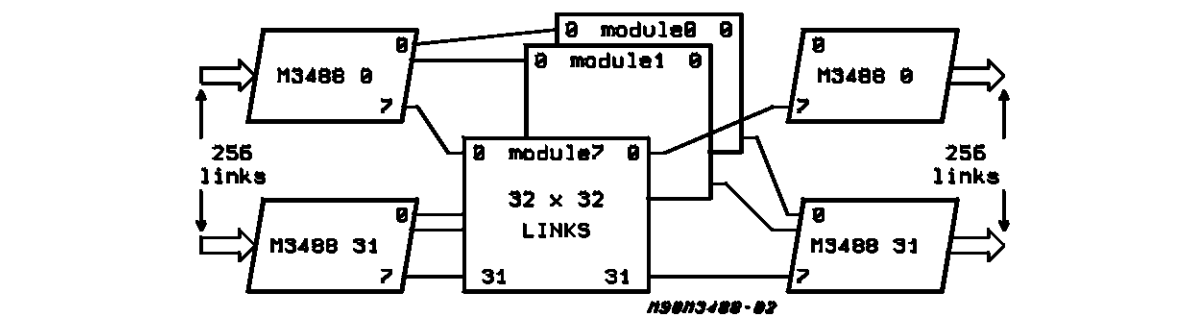
Stresses above those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operating conditions of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONNECTIONS (Top views)

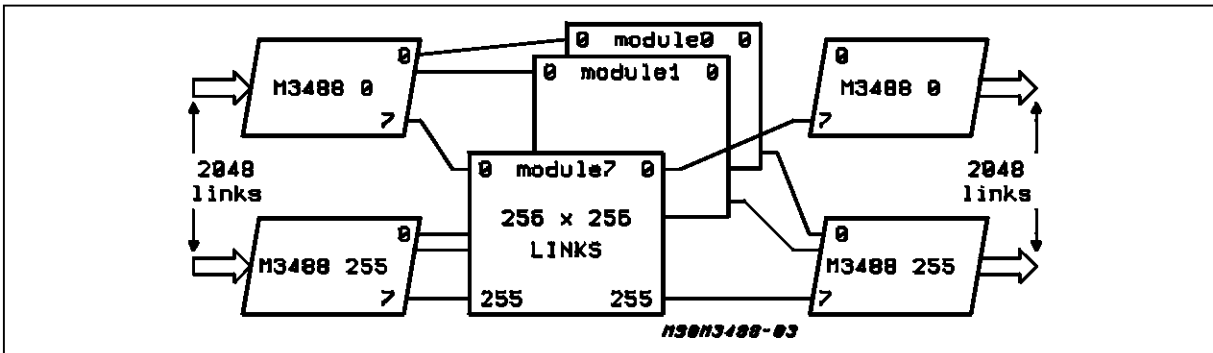


EXCHANGE NETWORKS APPLICATIONS

256 PCM links network (160 or 192 DSM) : the 32 x 32 link module shown on the next page.

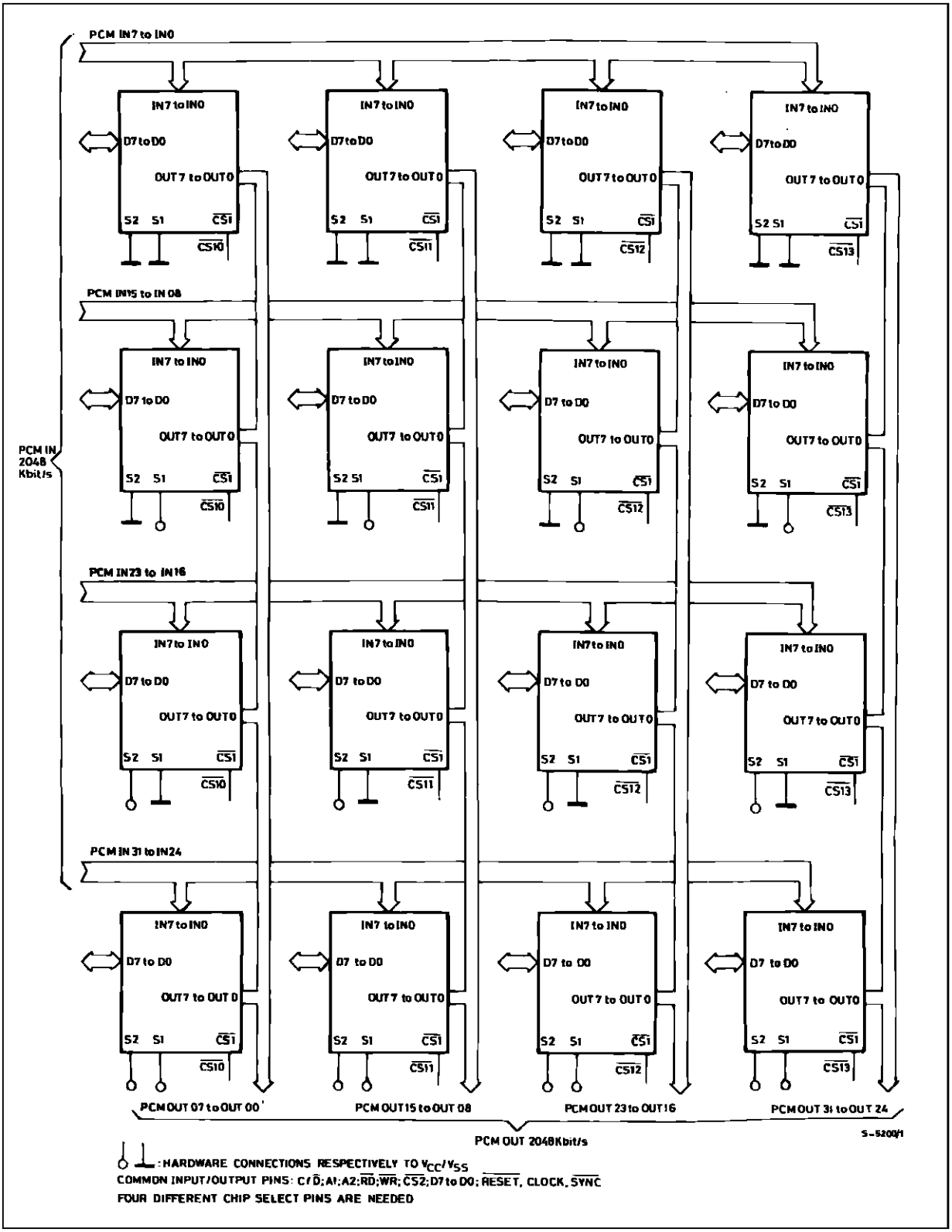


2048 PCM links network (1792 or 2048 DSM) : the 256 x 256 link network is shown above.

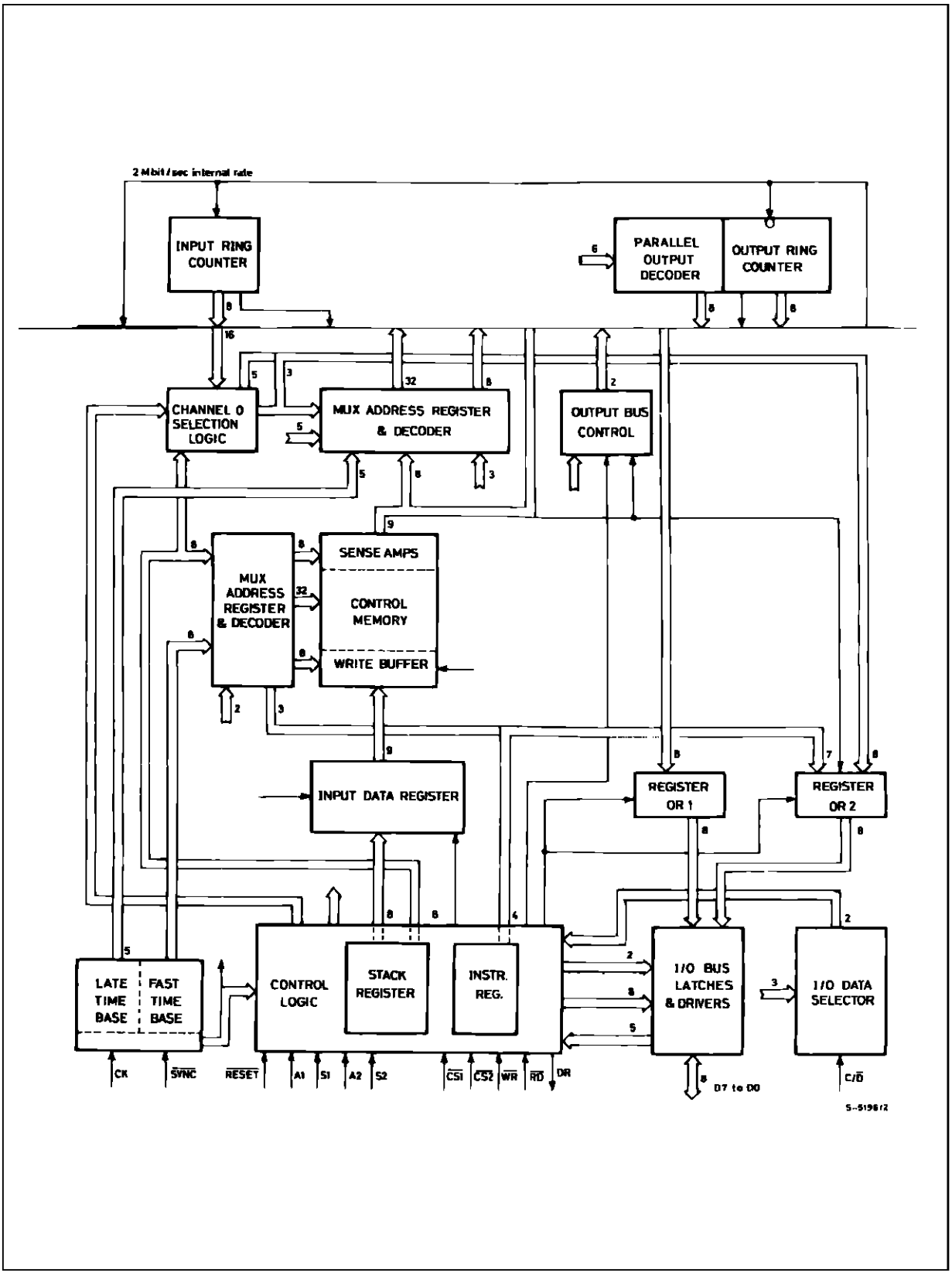


EXCHANGE NETWORKS APPLICATIONS (continued)

Single Stage/Sixteen Devices Configuration (32 by 32 links or 1024 channels).



BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.75 to 5.25	V
V_i	Input Voltage	0 to 5.25	V
V_O	Off State Input Voltage	0 to 5.25	V
CLOCK Freq.	Input Clock Frequency	4.096	MHz
SYNC Freq.	Input Synchronization Frequency	8	KHz
T_{op}	Operating Temperature	0 to 70	°C

CAPACITANCES (measurement freq. = 1MHz; T_{op} = 0 to 70°C; unused pins tied to V_{SS})

Symbol	Parameter	Pins (*)	Min.	Typ.	Max.	Unit
C_I	Input Capacitance	6 to 15; 26 to 30; 32 to 36			5	pF
$C_{I/O}$	I/O Capacitance	20 to 24			15	pF
C_O	Output Capacitance	1 to 4; 17 to 19; 25; 37 to 40			10	pF

D.C. ELECTRICAL CHARACTERISTICS (T_{amb} = 0 to 70°C, V_{CC} = 5V ±5%)
All D.C. characteristics are valid 250µs after V_{CC} and clock have been applied.

Symbol	Parameter	Pins (*)	Test Condition	Min.	Typ.	Max.	Unit
V_{ILC}	Clock Input Low Level	6		-0.3		0.8	V
V_{IHC}	Clock Input High Level	6		2.4		V_{CC}	V
V_{IL}	Input Low Level	7 to 15 20 to 24 26 to 30 32 to 36		-0.3		0.8	V
V_{IH}	Input High Level	7 to 15 20 to 24 26 to 30 32 to 36		2		V_{CC}	V
V_{OH}	Output High Voltage (Level)	17 to 25	I_{OH} = 5mA	2.4			V
I_{OH}	Output High Current		V_{OH} = 2.4V	5			mA
V_{OL}	Output Low Voltage (Level)	1 to 4 37 to 40 17 to 25	I_{OL} = 5mA			0.4	V
I_{OL}	Output Low Current		V_{OL} = 0.4V	5			mA
I_{IL}	Input Leakage Current	6 to 15 26 to 30 32 to 36	V_{IN} = 0 to V_{CC}			5	µA
I_{DL}	Data Bus Leakage Current	17 to 24	V_{IN} = 0 to V_{CC} V_{CC} applied; Pins 35 and 36 tied to V_{CC}, after Device Initialization			±5	µA
I_{CC}	Supply Current	16	Clock Freq. = 4.096MHz		15	30	mA

(*) The pin number is referred to the DIP40 version.

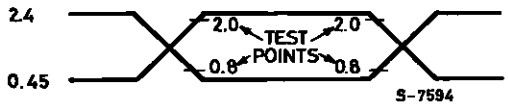
A.C. ELECTRICAL CHARACTERISTICS (T_{amb} = 0 to 70°C, V_{CC} = 5V ±5%)
All A.C. characteristics are valid 250µs after V_{CC} and clock have been applied. C_L is the max. capacitive load.

Signal	Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
CK (clock)	t_{CK}	Clock Period		230	244		ns
	t_{WL}	Clock Low Level Width		100			ns
	t_{WH}	Clock High Level Width		100			ns
	t_R	Rise Time				25	ns
	t_F	Fall Time				25	ns
SYNC (frame pulse)	t_{SL}	Low Level Setup Time		60			ns
	t_{HL}	Low Level Hold Time		30			ns
	t_{SH}	High Level Setup Time		80			ns
	t_{WH}	High Level Width		t_{CK}			ns
PCM Input Busses	t_S	Setup Time		5			ns
	t_H	Hold Time		+40			ns
PCM Output Busses Open Drain	$t_{PD\ min}$	Propagation time referred to CK low level	C_L = 150pF	45	110		ns
	$t_{PD\ max}$	Propagation time referred to CK high level	R_L = 1K		110	140	ns
RESET	t_{SL}	Low Level Setup Time		60			ns
	t_{HL}	Low Level Hold Time		30			ns
	t_{SH}	High Level Setup Time		80			ns
	t_{WH}	High level Width		t_{CK}			ns
$\overline{WR}$, $\overline{RD}$	t_{WL}	Low Lvel Width		100			ns
	t_{WH}	High Level Width		t_{CK}			ns
	t_{REP}	Repetition Interval between Active Pulses		see formula			ns
	t_{SH}	High Level Setup Time to Active Read Strobe	t_{REP} 40 + 2 t_{CK} + $t_{WL(CK)}$ + + $t_{R(CK)}$	0			ns
	t_{HH}	High Level Hold Time from Active Write Strobe		15			ns
	t_R	Rise Time				60	ns
	t_F	Fall Time				60	ns

A.C. ELECTRICAL CHARACTERISTICS (continued)

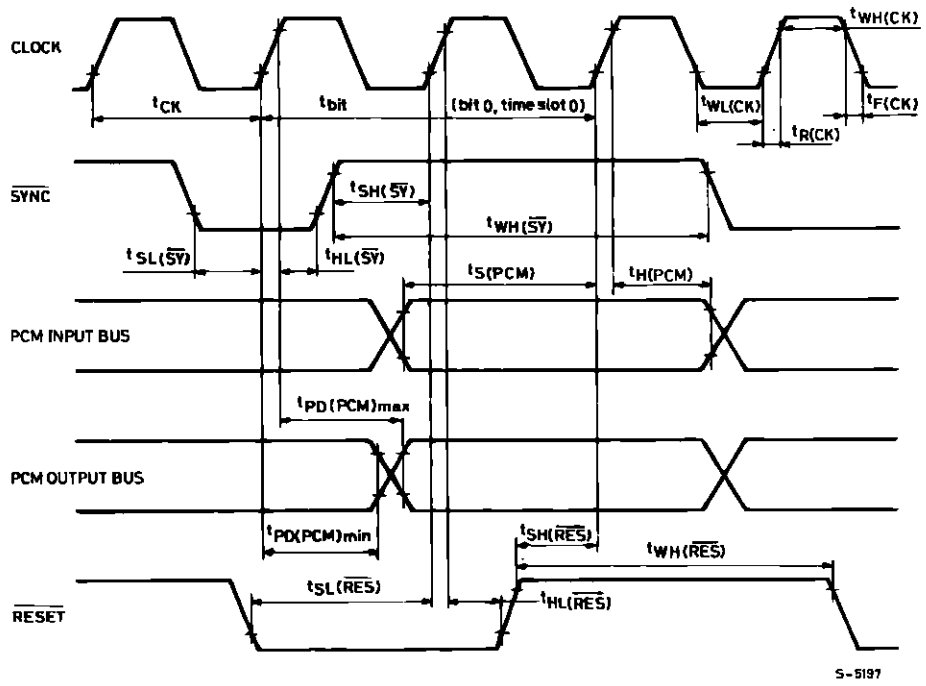
Signal	Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
CS1, $\overline{CS2}$	$t_{SL(\overline{CS}\text{-}\overline{WR})}$	Low level setup time to WR falling edge	Active Case	0			ns
	$t_{HL(\overline{CS}\text{-}\overline{WR})}$	Low Level hold time from WR rising edge	Active Case	0			ns
	$t_{\overline{SH}(\overline{CS}\text{-}WR)}$	High Level setup time to WR falling edge	Inactive Case	0			ns
	$t_{\overline{HH}(\overline{CS}\text{-}WR)}$	High level hold time from WR rising edge	Inactive Case	0			ns
	$t_{\overline{SL}(\overline{CS}\text{-}RD)}$	Low level setup time to RD falling edge	Active Case	0			ns
	$t_{\overline{HL}(\overline{CS}\text{-}RD)}$	Low level hold time from RD rising edge	Active Case	0			ns
	$t_{\overline{SH}(\overline{CS}\text{-}RD)}$	High level setup time RD falling edge	Inactive Case	0			ns
	$t_{\overline{HH}(\overline{CS}\text{-}RD)}$	High level hold time from RD	Inactive Case	0			ns
C/$\overline{D}$	$t_{\overline{S}(C/\overline{D}\text{-}WR)}$	Setup time to write strobe end		130			ns
	$t_{\overline{H}(C/\overline{D}\text{-}WR)}$	Hold time from write strobe end		15			ns
	$t_{\overline{S}(C/\overline{D})\text{-}RD)}$	Setup time to read strobe start		20			ns
	$t_{\overline{H}(C/\overline{D}\text{-}RD)}$	Hold time from read strobe end		20			ns
A1, S1, A2, S2 (match inputs)	$t_{S(match\text{-}\overline{WR})}$	Setup time to write strobe end		130			ns
	$t_{H(match\text{-}\overline{WR})}$	Hold time from strobe end		15			ns
	$t_{S(match\text{-}\overline{RD})}$	Setup time to read strobe start		20			ns
	$t_{H(match\text{-}\overline{RD})}$	Hold time from read strobe end		20			ns
DR (data ready)	t_W	Low state width	Instructions 5 and 6			$2.t_{CK}$	ns
	t_{PD}	DR output delay from write strobe end (active command)	Instruction 5, C_L = 150pF	$4.t_{CK}$		$7.t_{CK}$	ns
D0 to D7 (interface bus)	$t_{S(\overline{BUS}\text{-}WR)}$	Input setup time to write strobe end		130			ns
	$t_{H(\overline{BUS}\text{-}WR)}$	Input hold time from write strobe end		15			ns
	$t_{PD(BUS)}$	Propagation time from (active) falling Edge of read strobe	C_L = 200pF			120	ns
	$t_{HZ(BUS)}$	Propagation time from (active) rising Edge of read strobe to high impedance state	C_L = 200pF			80	ns

A.C. TESTING, OUTPUT WAVEFORM

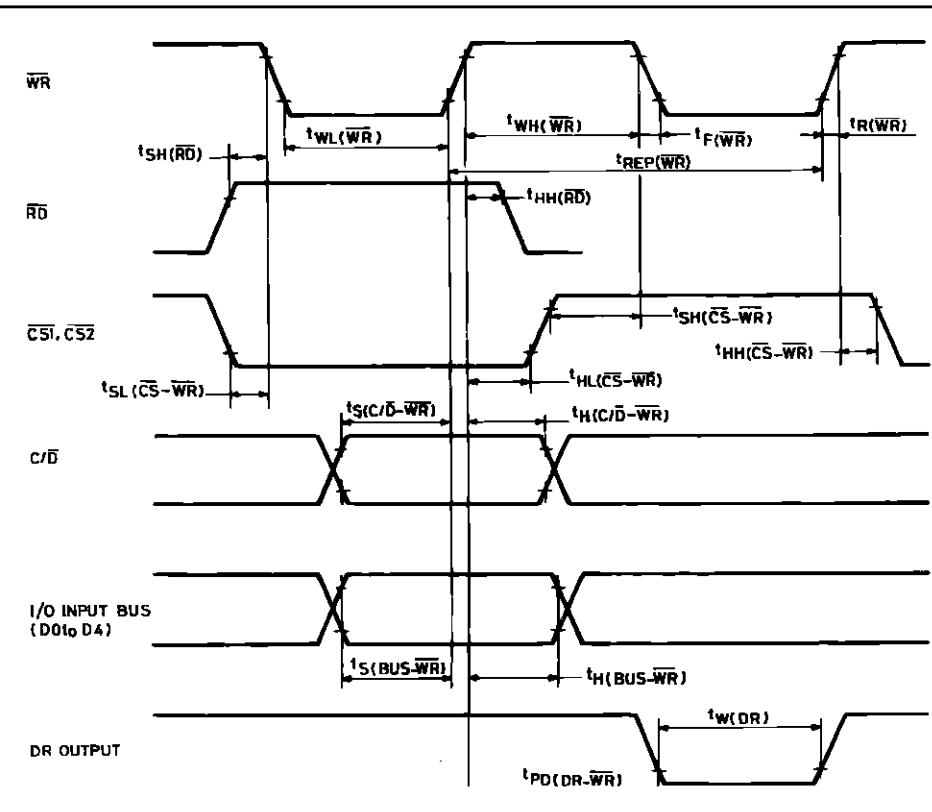


A.C. testing inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0", timing measurement are made at 2.0V for a logic "1"and 0.8V for a logic "0".

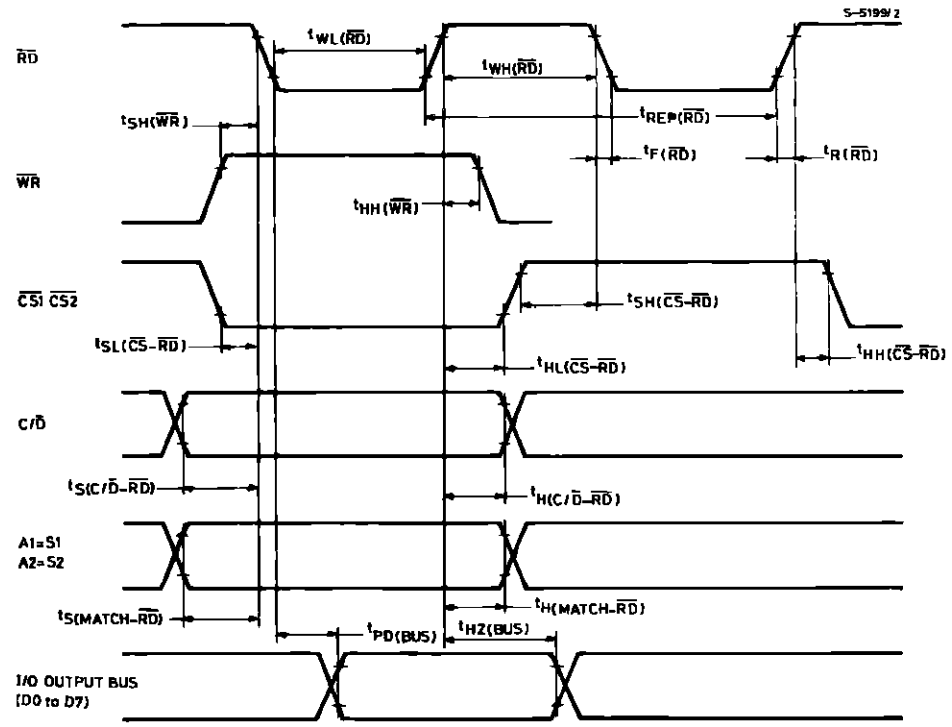
PCM TIMING, $\overline{\text{RESET}}$, $\overline{\text{SYNC}}$



WRITE OPERATION TIMING



READ OPERATION TIMING



GENERAL DESCRIPTION

The M3488 is intended for large telephone switching systems, mainly central exchanges, digital line concentrators and private branch exchanges where a distributed microcomputer control approach is extensively used. It consists of a speech memory (SM), a control memory (CM), a serial/parallel and a parallel/serial converter, an internal parallel bus, an interface (8 data lines, 11 control signals) and dedicated control logic.

By means of repeated clock division two timebases are generated. These are preset from an external synchronization signal to two specific count numbers so that sequential scanning of the bases give synchronous addresses to the memories and I/O channel controls. Different preset count numbers are needed because of processing delays and data path direction. The timebase for the input channels is delayed and the timebase for output channels is advanced with respect to the actual time.

Each serial PCM input channel is converted to parallel data and stored in the speech memory at the beginning of any new time slot (according to first timebase) in the location determined by input pin number and time slot number. The control memory CM maintains the correspondences between input and output channels. More exactly, for any output pin/output channel combination the control memory gives either the full address of the speech memory location involved in the PCM transfer or an 8-bit word to be supplied to the parallel/serial output converter. A 9^{th} bit at each CM location defines the data source for output links, low for SM, high for CM.

The late timebase is used to scan the output channels and to determine the pins to be serviced within each channel ; enough idle cycles are left to the microprocessor for asynchronous instruction processing.

Two 8-bit registers OR1 and OR2 supply feedback data for control or diagnostic purposes ; OR1 comes from internal bus i.e. from memories, OR2 gives an opcode copy and additional data to the microcomputer. A four byte-five bit stack register and an instruction register, under microcomputer control, store input data available at the interface.

Dedicated logic, under control of the microprocessor interface, extracts the 0 channel content of any selected PCM input bus, using spare cycles of SM.

PINS FUNCTION

Symbol	Name	Pin Assignement	
		DIP40	PQFP44
D7 to D0	Data bus	17 to 24	13 to 21
C/$\overline{D}$	Input control	30	27
A1, S1, A2, S2	Address select or match	26 to 29	23 to 26
$\overline{CS1}$, $\overline{CS2}$	Chip select	33, 34	30, 31
$\overline{WR}$	Data transfer enable	35	32
$\overline{RD}$	Read enable	36	34
DR	Data ready	25	22
$\overline{RESET}$	$\overline{RESET}$ control	32	29
CLOCK	Input master clock	6	1
$\overline{SYNC}$	Input synchronization	7	2
IN PCM 7 to 0	PCM input bus	8 to 15	3 to 10
OUT PCM 7 to 0	PCM output bus	37 to 40 and 1 to 4	35 to 38 and 40 to 43

PIN DESCRIPTION

D7 to D0

Data bus pins. The bidirectional bus is used to transfer data and instructions to/from the microprocessor. D0 is the least significant digit. The output bus is 8 bits wide ; input is only 5 bits wide. (D4 to D0)

The bus is tristate and cannot be used while $\overline{\text{RESET}}$ is held low.

The meaning of input data, such as bus or channel numbers, and of expected output data is specified in detail by the instruction description. (Pagg. 12-14)

C/$\overline{\text{D}}$ (pin 30)

Input control pin, select pin. In a write operation C/$\overline{\text{D}}$ = 0 qualifies any bus content as data, while C/$\overline{\text{D}}$ = 1 qualifies it as an opcode. In a read operation OR1 is selected by C/$\overline{\text{D}}$ = 0, OR2 by C/$\overline{\text{D}}$ = 1.

A1, S1, A2, S2

Address select or match pins. In a multi-chip configuration (e.g. a single stage matrix expansion), using the same $\overline{\text{CS}}$ pins, the match condition (A1 = S1 and A2 = S2) leaves the command instruction as defined; on the contrary the mismatch condition modifies the execution as follows : instructions 1 and 3 are reversed to channel disconnection, instruction 5 is unaffected, instructions 2-4-6 are cancelled (not executed).

Bus reading takes place only on match condition, instruction flow is in any case affected.

Each pins couple is commutative : in a multichip configuration pins S1 and S2 give a hard-wired address selection for individual matrixes, while in single configuration S1 and A1 or S2 and A2 are normally tied together.

$\overline{\text{CS1}}$, $\overline{\text{CS2}}$

Commutative chip select pins. They enable the device to perform valid read/write operations (active low). Two pins allow row/column selection with different types of microprocessors ; normally one is tied to ground.

$\overline{\text{WR}}$

Pin $\overline{\text{WR}}$, when $\overline{\text{CS1}}$ and $\overline{\text{CS2}}$ are low, enables data transfer from microprocessor to the device. Data or opcode and controls are latched on $\overline{\text{WR}}$ rising edge. Because of internal clock resynchronization one single additional requirement is recommended in order to produce a simultaneous instruction execution in a multichip configuration : $\overline{\text{WR}}$ rising edge has to be 20 to 20 + $t_{WL(CK)}$ nsec late relative to clock falling edge.

$\overline{\text{RD}}$

When CS1 and CS2 are low and match condition exists, a low level on $\overline{\text{RD}}$ enables a register OR1 or OR2 read operation, through the bidirectional bus.

In addition, the rising edge of $\overline{\text{RD}}$ latches C/$\overline{\text{D}}$ and the match condition pins in order to direct the internal flow of operations. Because of internal clock resynchronization, one single additional requirement is recommended in order to produce a simultaneous instruction flow in a multichip configuration: the RD rising edge has to be 20 to 20 + $t_{WL(CK)}$ nsec late relative to clock falling edge.

DR

Data ready. Normally high, DR output pin goes low to tell the microprocessor that :

a) the instruction code was found to be invalid ;

b) executing instruction 5 an active output channel was found in the whole matrix array, that is a CM word not all "ones" was found in a configuration of devices sharing the same CS pins ;

c) executing instruction 6 "0 channel extraction" took place and OR2 was loaded with total number of messages inserted on 0 time slot.

DR is active low about two clock cycles in case **b** and **c** ; in case a it is left low until a valid instruction code is supplied.

$\overline{\text{RESET}}$

$\overline{\text{RESET}}$ control pin is normally used at the very beginning to initialize the device or the network. Any logical status is reset and CM is set to all "ones" after $\overline{\text{RESET}}$ going low.

The internal initialization routine takes one time frame whatever the $\overline{\text{RESET}}$ width on low level (minimum one cycle roughly), but it is repeated an integer number of time frames as long as $\overline{\text{RESET}}$ is found low during 0 time slot.

Initialization pulls the interface bus immediately to a high impedance state. After the CM has been set to all "ones" the PCM output channels are also set to high impedance state.

CLOCK

Input master clock. Typical frequency is 4.096MHz. First division gives an internal clock controlling the input and output channels bit rate.

$\overline{\text{SYNC}}$

Input synchronization signal is active low. Typical frequency is 8kHz.

Internal time bases are forced by synchronism to an assigned count number in order to restore channels and bit sequential addressing to a known state. Count difference between the bases is 32, corresponding to two time slots, that is the minimum PCM propagation time, or latency time.

INP PCM 7 to INP PCM 0

PCM input busses or pins ; they accept a standard 2Mbit/s rate. Bit 1 (sign bit) is the first of the serial sequence ; in a parallel conversion it is left adjusted as the most significant digit.

OUT PCM 7 to OUT PCM 0

PCM output busses or pins ; bit rate and organization are the same as input pins.

Output buffers are open drain CMOS .

The device drives the output channels theoretically one bit time before they can be exploited as logical input channels (bit and slot compatibility is preserved): this feature allows inputs and outputs to be tied together cancelling any analog delay of digital outputs up to

$t_{DEL\ max} = t_{bit} - t_{\overline{PD(PCM)max}} + t_{\underline{PD(PCM)min}}$

MIXED $\overline{RD}$ and $\overline{WR}$ OPERATIONS

In principle $\overline{RD}$ and $\overline{WR}$ operations are allowed in any order within specification constraints.

In practive, only one control pin is low at any given time when CS1 and CS2 are enabled.

If by mistake or hardware failure both $\overline{RD}$ and $\overline{WR}$ pins are low, the interface bus is internally pushed to tristate condition as long as $\overline{WR}$ is held low and input registers are protected.

Registers OR1 and OR2 can be read in any order with a single $\overline{RD}$ strobe using C/$\overline{D}$ as multiplexing control ; never the less this procedure is not recommended because the device is directed for instruction flow only according to data latched by $\overline{RD}$ rising edge.

Multiple $\overline{RD}$ operations of the same kind are allowed without affecting the instruction flow : only "new" OR1 or OR2 read operations step the flow.

Input and output registers are held for sure in the previous state for the first 3 cycles following an opcode or an OR2 read.

FUNCTIONAL DESCRIPTION OF SPECIFIC MICROPROCESSOR OPERATIONS

The device, under microprocessor control, performs the following instructions :

1 CHANNEL CONNECTION

2 CHANNEL DISCONNECTION

3 LOADING OF A BYTE ON A PCM OUTPUT CHANNEL

4 TRANSFER OF A SINGLE PCM OUTPUT CHANNEL SAMPLE

5 TRANSFER OF A SINGLE OUTPUT CHANNEL CONTROL WORD

6 TRANSFER OF A SELECTED 0 CHANNEL PCM INPUT DATA ACCORDING TO AN 8-BIT MASK PREVIOUSLY STORED IN THE "EXPECTED MESSAGES" REGISTER

The instruction flow is as follows.

Any input protocol is started by the microprocessor interface loading the internal stack register with 2 bytes (4 bytes for instructions 1 and 3) qualified as data bytes by C/$\overline{D}$ = 0 and a specific opcode qualified by C/$\overline{D}$ = 1 (match condition is normally needed).

After the code is loaded in the instruction register it is immediately checked to see whether it is acceptable and if not it is rejected. If accepted the instruction is also processed as regards match condition and is appended for execution during the memories' spare cycles.

Four cases are possible :

a) the code is not valid ; execution cannot take place, the DR output pin is reset to indicate the error ; all registers are saved ;

b) the code is valid for types 2, 4 and 6 but it is unmatched ; execution cannot take place, DR is not affected.

c) the code is valid for types 1 and 3 and it is unmatched ; the instruction is interpreted as a channel disconnection.

d) the code is valid and is either matched or of type 5 ; the instruction is processed as received.

Validation control takes only two cycles out of a total execution time of 4 to 7 cycles ; the last operation is updating of the content of registers OR1 and OR2, according to the following instruction tables.

During a very long internal operation (device initialization after RESET going high or execution of instruction 6) a new set of data bytes with a valid opcode is accepted while a wrong code is rejected. At the end of the current routine execution takes place in the same way as described before.

At the end of an instruction it is normally recommended to read one or both registers. To exploit instruction 6, however, it is mandatory to read register OR2. This is because instruction 6, used between other short instructions of type 1 to 5, must have priority and can be enabled only after the short instructions have been completed. Instruction 6 normally has a long process and a special flow which is described below.

First a not-all-zero mask is stored in the "expected messages" register and in another "background" register. This operation starts the second phase of instruction 6 which is called "channel 0 extraction" and is repeated at the beginning of any new time frame. At the beginning of the time frame a new copy of activated channels to be extracted is made from the "background register" and put in the "expected messages" register. In addition the latter register is modified to indicate the exact number of messages that have arrived. The term messages covers any input 0 channel data with starting sequence different from the label 01. So using this label the number of expected messages can be reduced to correspond to the number of effective messages. If and only if the residual number is different from zero will the device start the extraction protocol at the end of the current routine.

The procedure is as follows: the DR output is pulsed low as a two cycle interrupt request and OR2 is loaded with the total number of active channels to be extracted.

The transfer of OR2 content to the microprocessor continues the extraction which consists of repeated steps of OR1 and OR2 loading, indicating respectively the message and the incoming bus number. Reading the registers in the order OR1, OR2 must be continued until completion or until the time frame runs out.

With a new time frame a new extraction process begins, resuming the copy operation from the background register.

During extraction the active channels are scanned from the highest to the lowest number (from 7 to 0). While extraction is being carried out the time interval requirements between active rising edges of RD are minimum 4 to 7 t_{CK} for sequence OR2 - OR1 and minimum 2 times t_{CK} for sequence OR1 - OR2. More details are given in the following tables.

INSTRUCTION TABLES

The most significant digits of OR2 A7, A6, A5 are a copy of the PCM selected output bus ; the least significant digits of OR2 are the opcode, C8 is the control bit. In any case parentheses () define actual register content.

INSTRUCTION 1: CHANNEL CONNECTION

Control Signals					Data Bus								Notes
Match	C/$\overline{D}$	$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	D7	D6	D5	D4	D3	D2	D1	D0	
X	0	0	0	1	X	X	X	X	X	Bi2	Bi1	Bi0	1st Data Byte: selected input bus.
X	0	0	0	1	X	X	X	Ci4	Ci3	Ci2	Ci1	Ci0	2nd Data Byte: selected input channel.
x	0	0	0	1	X	X	X	X	X	Bo2	Bo1	Bo0	3rd Data Byte: selected output bus.
X	0	0	0	1	X	X	X	Co4	Co3	Co2	Co1	Co0	4th Data Byte: selected output channel.
yes/no	1	0	0	1	X	X	X	X	0	0	0	1	Instruction Opcode
yes	0	0	1	0	C7 (1 (Bi2	C6 1 Bi1	C5 1 Bi0	C4 1 Ci4	C3 1 Ci3	C2 1 Ci2	C1 1 Ci1	C0 1) Ci0)	OR1: CM content copy, that is, for mismatch condition, for match condition
yes	1	0	1	0	A7 (Bo2 (Bo2	A6 Bo1 Bo1	A5 Bo0 Bo0	C8 1 0	0 0 0	0 0 0	0 0 0	1 1) 1)	OR2: that is, for mismatch condition for match condition

INSTRUCTION2: OUTPUT CHANNEL DISCONNECTION

Control Signals					Data Bus								Notes
Match	C/$\overline{D}$	$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	D7	D6	D5	D4	D3	D2	D1	D0	
X	0	0	0	1	X	X	X	X	X	Bo2	Bo1	Bo0	1st Data Byte: selected output bus.
X	0	0	0	1	X	X	X	Co4	Co3	Co2	Co1	Co0	2nd Data Byte: selected output channel.
Yes	1	0	0	1	X	X	X	X	0	0	1	0	Instruction Opcode
Yes	0	0	1	0	1	1	1	1	1	1	1	1	OR1: CM Content Copy (output channel is inactive)
Yes	1	0	1	0	A7 (Bo2	A6 Bo1	A5 Bo0	1 1	0 0	1 1	1 1	1 1)	OR2: that is.

INSTRUCTION3: LOADING ON A PCM OUTPUT CHANNEL FROM A MICROPROCESSOR BYTE

Control Signals					Data Bus								Notes
Match	C/$\overline{D}$	$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	D7	D6	D5	D4	D3	D2	D1	D0	
X	0	0	0	1	X	X	X	X	X	Ci7	Ci6	Ci5	1st Data Byte: most significant digits to be inserted.
X	0	0	0	1	X	X	X	Ci4	Ci3	Ci2	Ci1	Ci0	2nd Data Byte: least significant digits to be inserted.
X	0	0	0	1	X	X	X	X	X	Bo2	Bo1	Bo0	3rd Data Byte: selected output bus.
X	0	0	0	1	X	X	X	Co4	Co3	Co2	Co1	Co0	4th Data Byte: selected output channel..
Yes/no	1	0	0	1	X	X	X	X	0	1	0	0	Instruction Opcode
Yes	0	0	1	0	C7 (1 (Ci7	C6 1 Ci6	C5 1 Ci5	C4 1 Ci4	C3 1 Ci3	C2 1 Ci2	C1 1 Ci1	C0 1) Ci0)	OR1: CM content copy, that is, for mismatch condition, for match condition
Yes	1	0	1	0	A7 (Bo2	A6 Bo1	A5 Bo0	1 1	0 0	1 1	1 1	1 1)	OR2: that is.

INSTRUCTION4: TRANSFER OF A SINGLE PCM SAMPLE

Control Signals					Data Bus								Notes
Match	C/$\overline{D}$	$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	D7	D6	D5	D4	D3	D2	D1	D0	
X	0	0	0	1	X	X	X	X	X	Bo2	Bo1	Bo0	1st Data Byte: selected output bus.
X	0	0	0	1	X	X	X	Co4	Co3	Co2	Co1	Co0	2nd Data Byte: selected output channel.
Yes	1	0	0	1	X	X	X	X	1	0	1	1	Instruction Opcode
Yes	0	0	1	0	C7 S7	C6 S6	C5 S5	C4 S4	C3 S3	C2 S2	C1 S1	C0 S0	OR1: CM Content Copy if C8 = 1; or SM Content Sample if C8 = 0
Yes	1	0	1	0	A7 (Bo2	A6 Bo1	A5 Bo0	1 1	0 0	1 1	1 1	1 1)	OR2: that is.

Notes : S7...S0 is a parallel copy of a PCM data, S7 is the most significant digit and the first of the sequence.

INSTRUCTION5: TRANSFER OF AN OUTPUT CHANNEL CONTROL WORD

Control Signals					Data Bus								Notes
Match	C/D	CS	WR	RD	D7	D6	D5	D4	D3	D2	D1	D0	
X	0	0	0	1	X	X	X	X	X	Bo2	Bo1	Bo0	1st Data Byte: selected output bus.
X	0	0	0	1	X	X	X	Co4	Co3	Co2	Co1	Co0	2nd Data Byte: selected output channel.
Yes	1	0	0	1	X	X	X	X	1	0	0	0	Instruction Opcode
Yes	0	0	1	0	C7	C6	C5	C4	C3	C2	C1	C0	OR1: CM selected CM word copy.
Yes	1	0	1	0	A7 (Bo2	A6 Bo1	A5 Bo0	C8 C8	1 1	0 0	0 0	0 0)	OR2: that is.

INSTRUCTION6: CHANNEL 0 SELECTION MASK STORE/DATA TRANSFER

Control Signals					Data Bus								Notes
Match	C/D	CS	WR	RD	D7	D6	D5	D4	D3	D2	D1	D0	
X	0	0	0	1	X	X	X	X	X	Mi7	Mi6	Mi5	1st Data Byte: most sign. digits of selection mask.
X	0	0	0	1	X	X	X	Mi4	Mi3	Mi2	Mi1	Mi0	2nd Data Byte: least sign. digits of selection mask.
Yes	1	0	0	1	X	X	X	X	1	1	1	0	Instruction Opcode
Mask store control													
Yes	0	0	1	0	(previous content)								OR1: register is not affected.
Yes	1	0	1	0	N2	N1	N0	Tn	1	1	1	0	OR2: see below.
First Data Transfer (after DR going low)													
Yes	0	0	1	0	(previous content)								OR1: register is not affected.
Yes	1	0	1	0	N2	N1	N0	Tn	1	1	1	0	OR2: see below.
Repeated Data Transfer (after first OR2 transfer)													
Yes	0	0	1	0	S7	S6	S5	S4	S3	S2	S1	S0	OR1: expected message stored in SM.
Yes	1	0	1	0	P2	P1	P0	Fn	1	1	1	0	OR2: see below.

Notes : 1. About mask bits Mi0 to Mi7 a logic "0" level means disabling condition, a logic "1" level means enabling condition.
2. A null mask or a RESET pulse clear the mask and the deep background mask registers and disable channel 0 extraction function.
3. Reading of OR2 is optional after mask store or redefinition, because function is activated only by not-null mask writing.
4. After mask store (N2 N1 N0) is the sum of activated channels, after DR is the sum of active channels ; Tn = 1/0 means activation/suppression of the function after store while after DR only Tn = 1 can appear to tell a not-null configuration to be extracted.
5. Reading of OR2 is imperative after DR in order to step the data transfer ; reading of OR1 is also needed to scan in descending order the priority register. Relevant messages only are considered, that means only messages with a MSD label different from 0 1.
6. (P2 P1 P0) is the PCM bus on which the message copied in OR1 was found ; Fn is a continuation bit telling respectively on level 1/0 for any more/no more extraction step to be performed.

M3488 WITH LESS PCM LINKS THAN 32 CHANNELS

It is also possible to use M3488 when the PCM frames are made up of a number of channels other than 32.

Suppose that the PCM frames are made up of N-Channels, which will be numbered from 0 to (N-1).

Each PCM frame will thus be made up of a number of bits multiplied by 8 ; this exactly equal to (N · 8).

Also, in this case, it is necessary to respect the timing relationship between the different signals shown on the data sheet ; in particular, a relation-ship is always carefully made between the rising edge of SYNC and the first clock (CK) bit contained in the slot time for bit 0 of channel 0.

In order to use M3488 with these frames, it is sufficient, using the data bytes sent by the microprocessor, to modify the numbering of a few channels.

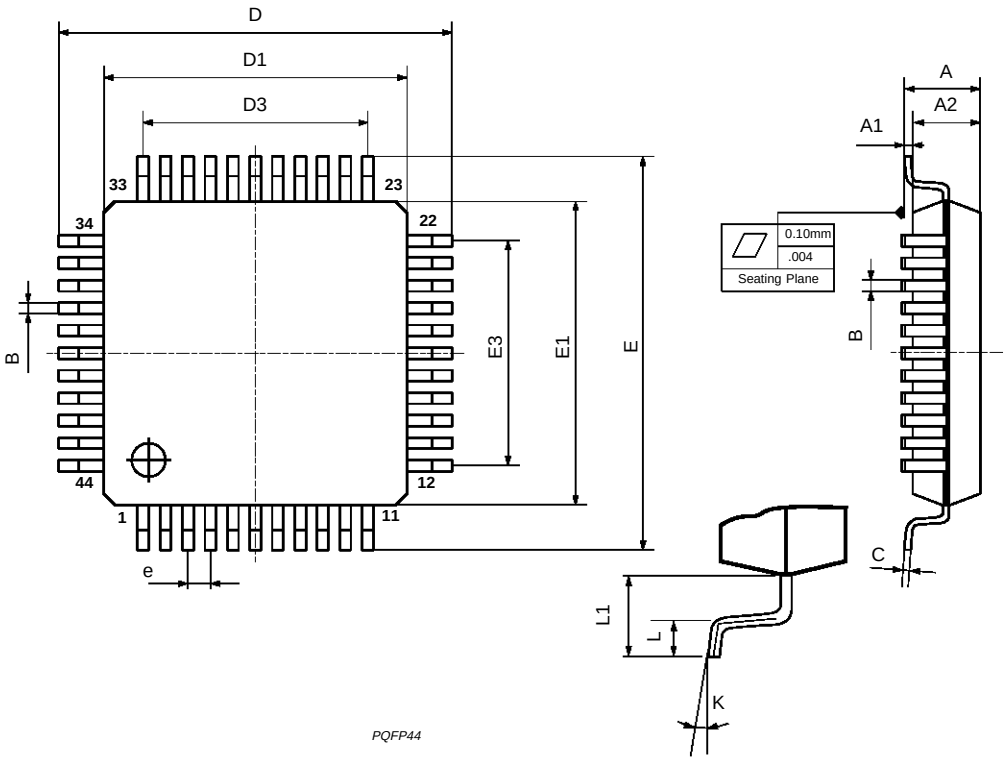
In particular :

a) in all instructions in which reference is made to the input channel (N-1), the number 31 should be substituted for the number (N-1) ;

b) in all instructions in which reference is made to the output channel 0, the number N should be substituted for the number 0.

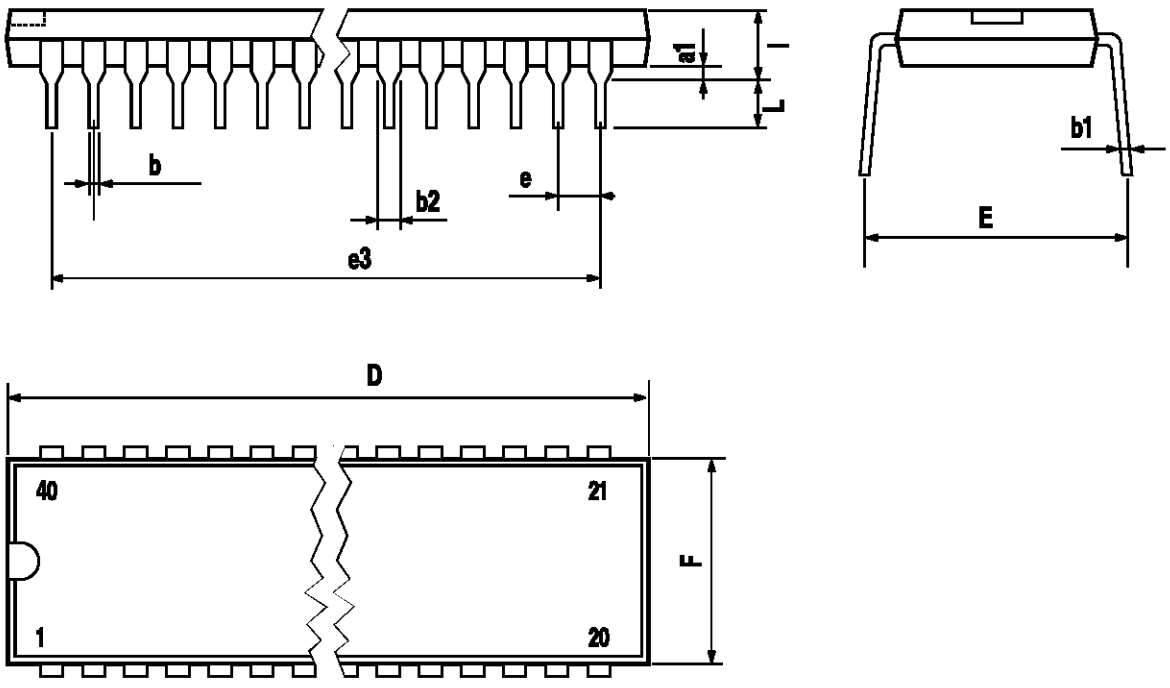
PQFP44 (10 x 10) PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.45			0.096
A1	0.25			0.010		
A2	1.95	2.00	2.10	0.077	0.079	0.083
B	0.30		0.45	0.012		0.018
c	0.13		0.23	0.005		0.009
D	12.95	13.20	13.45	0.51	0.52	0.53
D1	9.90	10.00	10.10	0.390	0.394	0.398
D3		8.00			0.315	
e		0.80			0.031	
E	12.95	13.20	13.45	0.510	0.520	0.530
E1	9.90	10.00	10.10	0.390	0.394	0.398
E3		8.00			0.315	
L	0.65	0.80	0.95	0.026	0.031	0.037
L1		1.60			0.063	
K	0°(min.), 7°(max.)					



DIP40 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN	TYP	MAX	MIN	TYP	MAX
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
D			52.58			2.070
E	15.2		16.68	0.598		0.657
e		2.54			0.100	
e3		48.26			1.900	
F			14.1			0.555
I		4.445			0.175	
L		3.3			0.130	



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