1 KEY TOUCH PAD DETECTOR IC

GENERAL DESCRIPTION

The TTP224N-FO8 TonTouch™ IC is capacitive sensing design specifically for touch pad controls. The device built in regulator for touch sensor. Stable sensing method can cover diversity conditions. Human interfaces control panel links through non-conductive dielectric material. The main application is focused at replacing of the mechanical switch or button. The ASSP can independently handle the 1 touch pad with 1 direct CMOS output pin and 1 open drain output pin that has diode protective circuit.

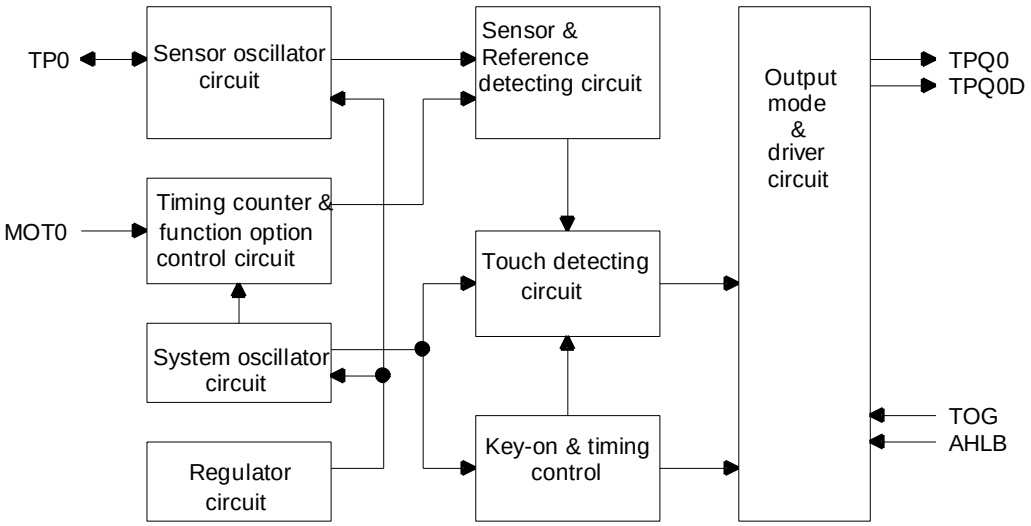
FEATURES

- Operating voltage 2.4V~5.5V
- Built-in regulator
- Operating current, @VDD=3V no load
  At low power mode typical 2uA, At fast mode typical 6.5uA
- @VDD=3V operating voltage :
  The response time about 60mS at fast mode,160mS at low power mode
- Sensitivity can adjust by the capacitance(0~50pF) outside
- Provides direct mode or toggle mode、active high or active low by pad option (TOG/AHLB pin).
- Provides one output pin TPQ0D that has no diode protection, active low
- Have the maximum on time 16sec/infinite by pad option(MOT0 pin)
- After power-on have about 0.5sec stable-time, during the time do not touch the key pad, and the function is disabled
- Auto calibration for life, and the re-calibration period is about 4.0sec, when key has not be touched.

APPLICATION

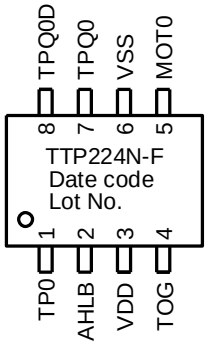
- Wide consumer products
- Button key replacement

BLOCK DIAGRAM



PACKAGE LIST

TTP224N-FO8 package type is SOP-8 ,package configuration is below



PIN DESCRIPTION

Pin No.	Pin Name	Type	Pad Description
1	TP0	I/O	Touch pad input pin
2	AHLB	I-PL	Output active high or low option, default:0
3	VDD	P	Positive power supply
4	TOG	I-PL	Output type option, default:0
5	MOT0	I-PH	Key maximum on time option, default:1
6	VSS	P	Negative power supply, ground
7	TPQ0	O	Direct output for TP0 touch input pin
8	TPQ0D	OD	Open Drain output(have no Diode protective circuit), active low for TP0 touch input pin

Note : Pin Type

I ＝＞CMOS input only
I-PH ＝＞CMOS input and pull-high resister
I-PL ＝＞CMOS input and pull-low resister
O ＝＞CMOS push-pull output
I/O ＝＞CMOS I/O
P ＝＞Power / Ground
OD ＝＞Open drain output, have no Diode protective circuit

ELECTRICAL CHARACTERISTICS

• Absolute Maximum Ratings

Parameter	Symbol	Conditions	RATING	Unit
Operating Temperature	Top	—	-40℃ ~ +85℃	℃
Storage Temperature	T_{STG}	—	-50℃ ~ +125℃	℃
Supply Voltage	VDD	Ta=25°C	VSS-0.3 ~VSS+6.0	V
Input Voltage	V_{IN}	Ta=25°C	VSS -0.3 to VDD+0.3	V
Human Body Mode	ESD	—	5	KV
Note: VSS symbolizes for system ground				

• DC/AC Characteristics：(Test condition at room temperature=25℃)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Operating Voltage	**VDD**	Regulator enable	2.4	-	5.5	**V**
Internal Regulator Output	**VREG**	Regulator enable	2.2	2.3	2.4	**V**
Operating Current (no load, regulator enable)	**I_{op1}**	VDD=3V,At low power mode		2		**uA**
		VDD=3V,At fast mode		6.5		**uA**
Input Ports	**V_{IL}**	Input Low Voltage	0	-	0.2	**VDD**
Input Ports	**V_{IH}**	Input High Voltage	0.8	-	1.0	**VDD**
Output Port Sink Current	**I_{OL}**	VDD=3V, V_{OL}=0.6V	-	8	-	**mA**
Output Port Source Current	**I_{OH}**	VDD=3V, V_{OH}=2.4V	-	-4	-	**mA**
Input Pin Pull-high Resistor	**R_{PH}**	VDD=3V,		30K		**ohm**
Input Pin Pull-low Resistor	**R_{PL}**	VDD=3V,		25K		**ohm**
Output Response Time	**T_R**	VDD=3V, At fast mode		100		**mS**
		VDD=3V, At low power mode		200		**mS**
Output Response Time	**T_R**	VDD=3V, At fast mode		60		**mS**
		VDD=3V, At low power mode		160		**mS**

FUNCTION DESCRIPTION

1. Sensitivity adjustment

The total loading of electrode size and capacitance of connecting line on PCB can affect the sensitivity. So the sensitivity adjustment must according to the practical application on PCB. The TTP224N-FO8 offers some methods for adjusting the sensitivity outside.

1-1 by the electrode size

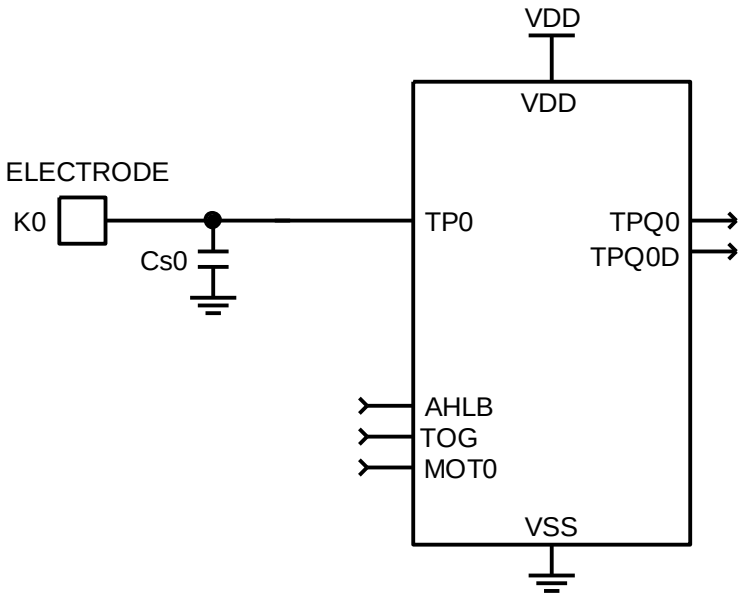
Under other conditions are fixed. Using a larger electrode size can increase sensitivity. Otherwise it can decrease sensitivity. But the electrode size must use in the effective scope.

1-2 by the panel thickness

Under other conditions are fixed. Using a thinner panel can increase sensitivity. Otherwise it can decrease sensitivity. But the panel thickness must be below the maximum value.

1-3 by the value of Cs0 (please see the down figure)

Under other conditions are fixed. Add the capacitors Cs0 can fine tune the sensitivity for single key, that lets all key's sensitivity identical. When do not use any capacitor to VSS, the sensitivity is most sensitive. When adding the values of Cs0 will reduce sensitivity in the useful range ($0 \leqq Cs0 \leqq 50pF$).

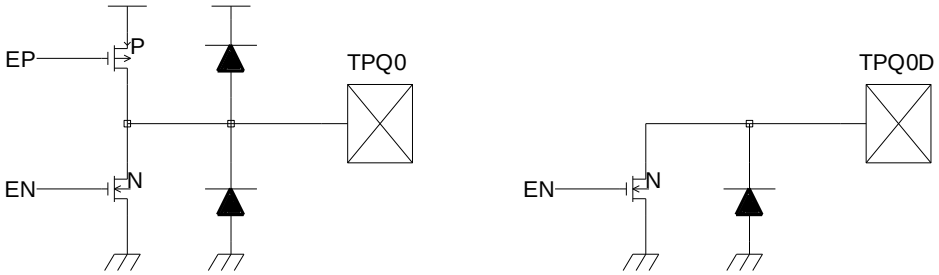


2. Output mode(By TOG, AHLB pad option)

The TTP224N-FO8 outputs(TPQ0) has direct mode active high or low by AHLB pad option, has toggle mode by TOG pad option. Another TPQ0D is open drain active low output pin has no diode protective circuit.

TOG	AHLB	Pad TPQ0 option features	Remark
0	0	Direct mode, CMOS active high output	Default
0	1	Direct mode, CMOS active low output	
1	0	Toggle mode, COMS output, Power on state=0	
1	1	Toggle mode, COMS output, Power on state=1	

TOG	Pad TPQ0D option features	Remark
0	Direct mode, Open drain active low output, Power on state high-Z	Default
1	Toggle mode, Open drain active low output, Power on state high-Z	



3. Maximum key on duration time (By MOT0 pad option)

If some objects cover in the sense pad, and causing the change quantity enough to be detected. To prevent this, the TTP224N-FO8 sets a timer to monitor the detection. The timer is the maximum on duration time. When the detection is over the timer, the system will return to the power-on initial state, and the output becomes inactive until the next detection.

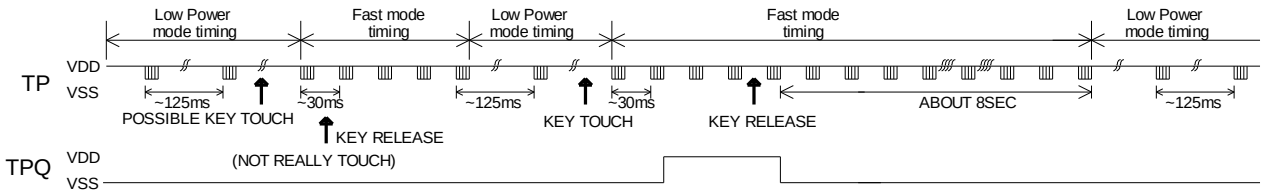
MOT0	Option features	Remark
0	Maximum on time 16sec	
1	Infinite(Disable maximum on time)	Default

4. Low power mode

The TTP224N-FO8 is Low Power mode. It will be saving power. When detecting key touch, it will switch to Fast mode. Until the key touch is released and will keep a time about 8sec. Then it returns to Low Power mode.

The states and timing please see below figure.

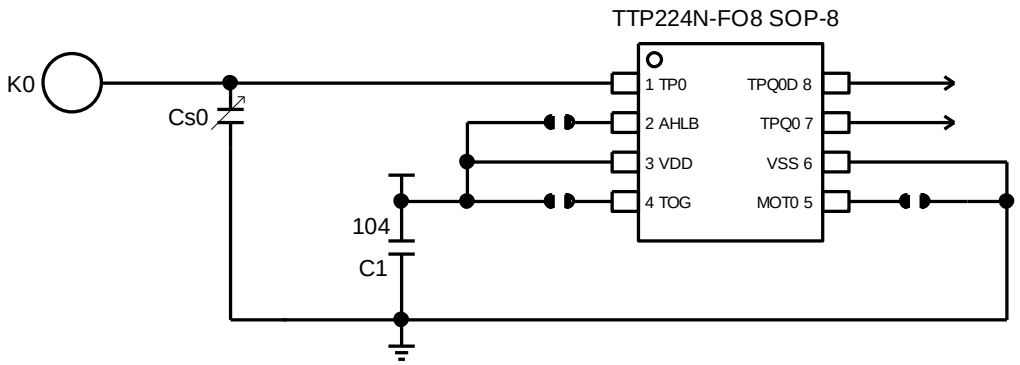
TTP224N-FO8 timing diagram :



Low Power Mode

APPLICATION CIRCUIT

TTP224N-FO8 APPLICATION



Option table:

Output mode:

TOG	AHLB	Pad TPQ0 option features
open	open	Direct mode, CMOS active high output
open	VDD	Direct mode, CMOS active low output
VDD	open	Toggle mode, COMS output, Power on state=0
VDD	VDD	Toggle mode, COMS output, Power on state=1

TOG	Pad TPQ0D (has no diode protection) option features
open	Direct mode, Open drain active low output, Power on state high-Z
VDD	Toggle mode, Open drain active low output, Power on state high-Z

Maximum key on duration time:

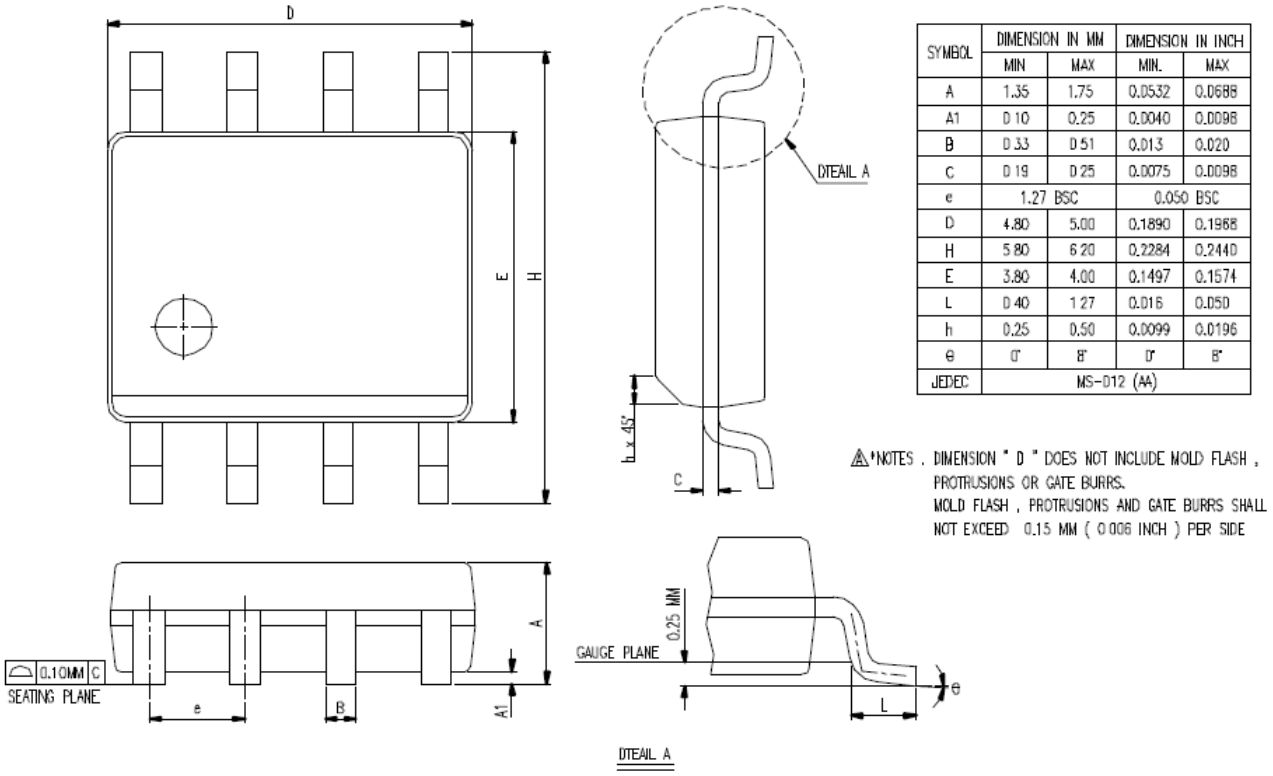
MOT0	Option features
open	Infinite(Disable maximum on time)
VSS	Maximum on time 16sec

PS：1. On PCB, the length of lines from touch pad to IC pin shorter is better.
And the lines do not parallel and cross with other lines.

2. The material of panel covering on the PCB can not include the metal or the electric element. The paints on the surfaces are the same.
3. The C1 capacitor must be used between VDD and VSS; and should be routed with very short tracks to the device's VDD and VSS pins.
4. The capacitance Cs0 can be used to adjust the sensitivity. The value of Cs0 use smaller, then the sensitivity will be better. The sensitivity adjustment must according to the practical application on PCB. The range of Cs0 value are 0~50pF.
5. The sensitivity adjustment capacitors (Cs0) must use smaller temperature coefficient and more stable capacitors. Such are X7R, NPO for example. So for touch application, recommend to use NPO capacitor, for reducing that the temperature varies to affect sensitivity.

Package Type: SOP-8

Package Outline Dimension



SYMBOL	DIMENSION IN MM		DIMENSION IN INCH	
	MIN	MAX	MIN.	MAX
A	1.35	1.75	0.0532	0.0688
A1	0.10	0.25	0.0040	0.0098
B	0.33	0.51	0.013	0.020
C	0.19	0.25	0.0075	0.0098
e	1.27 BSC		0.050 BSC	
D	4.80	5.00	0.1890	0.1968
H	5.80	6.20	0.2284	0.2440
E	3.80	4.00	0.1497	0.1574
L	0.40	1.27	0.016	0.050
h	0.25	0.50	0.0099	0.0196
θ	0°	8°	0°	8°
JEDEC	MS-012 (AA)			

⚠ *NOTES : DIMENSION " D " DOES NOT INCLUDE MOLD FLASH , PROTRUSIONS OR GATE BURRS.
MOLD FLASH , PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.15 MM (0.006 INCH) PER SIDE

ORDER INFORMATION

a. Package form: TTP224N-FO8
b. Chip form: TCP224N
c. Wafer base: TDP224-02

REVISE HISTORY

1. 2009/06/30
   - Original version：V1.0
2. 2009/08/25 ➔ V2.0
   Add the TTP224N-FO8
3. 2010/06/08 ➔ V3.0
   Add the TTP224L-FO8
4. 2014/06/05 ➔V3.1
   Remove TTP224-FO8 and TTP224L-FO8 function