



P-Channel JFETs

J174	SST174
J175	SST175
J176	SST176
J177	SST177

PRODUCT SUMMARY				
Part Number	$V_{GS(off)}$ (V)	$r_{DS(on)}$ Max (Ω)	$I_{D(off)}$ Typ (pA)	t_{ON} Typ (ns)
J/SST174	5 to 10	85	-10	25
J/SST175	3 to 6	125	-10	25
J/SST176	1 to 4	250	-10	25
J/SST177	0.8 to 2.25	300	-10	25

FEATURES

- Low On-Resistance: J174 <85 Ω
- Fast Switching— t_{ON} : 25 ns
- Low Leakage: -10 pA
- Low Capacitance: 5 pF
- Low Insertion Loss

BENEFITS

- Low Error Voltage
- High-Speed Analog Circuit Performance
- Negligible "Off-Error," Excellent Accuracy
- Good Frequency Response
- Eliminates Additional Buffering

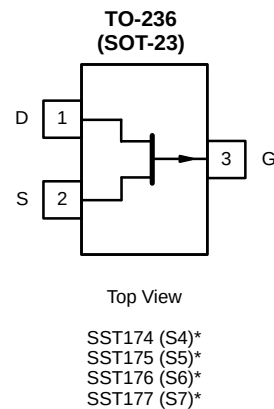
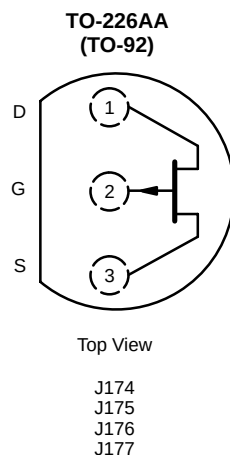
APPLICATIONS

- Analog Switches
- Choppers
- Sample-and-Hold
- Normally "On" Switches
- Current Limiters

DESCRIPTION

The J/SST174 series consists of p-channel analog switches designed to provide low on-resistance and fast switching. This series simplifies series-shunt switching applications when combined with the Siliconix J/SST111 series.

The TO-226AA (TO-92) plastic package provides a low-cost option, while the TO-236 (SOT-23) package provides surface-mount capability. Both the J and SST series are available in tape-and-reel for automated assembly (see Packaging Information).



*Marking Code for TO-236

For applications information see AN104.

ABSOLUTE MAXIMUM RATINGS

Gate-Drain Voltage 30 V
 Gate-Source Voltage 30 V
 Gate Current -50 mA
 Storage Temperature -55 to 150°C
 Operating Junction Temperature -55 to 150°C

Lead Temperature (l_{16} " from case for 10 sec.) 300°C
 Power Dissipation^a 350 mW

Notes

a. Derate 2.8 mW/°C above 25°C

SPECIFICATIONS FOR J/SST174 AND J/SST175 (T _A = 25° C UNLESS OTHERWISE NOTED)								
Parameter	Symbol	Test Conditions	Typ ^a	Limits				Unit
				J/SST174		J/SST175		
				Min	Max	Min	Max	
Static								
Gate-Source Breakdown Voltage	V _{(BR)GSS}	I _G = 1 μA , V _{DS} = 0 V	45	30		30		V
Gate-Source Cutoff Voltage	V _{GS(off)}	V _{DS} = -15 V, I _D = -10 nA		5	10	3	6	
Saturation Drain Current ^b	I _{DSS}	V _{DS} = -15 V, V _{GS} = 0 V		-20	-135	-7	-70	mA
Gate Reverse Current	I _{GSS}	V _{GS} = 20 V, V _{DS} = 0 V	0.01		1		1	nA
		T _A = 125° C	5					
Gate Operating Current	I _G	V _{DG} = -15 V, I _D = -1 mA	0.01					
Drain Cutoff Current	I _{D(off)}	V _{DS} = -15 V, V _{GS} = 10 V	-0.01		-1		-1	
		T _A = 125° C	-5					
Drain-Source On-Resistance	r _{DS(on)}	V _{GS} = 0 V, V _{DS} = -0.1 V			85		125	Ω
Gate-Source Forward Voltage	V _{GS(F)}	I _G = -1 mA , V _{DS} = 0 V	-0.7					V
Dynamic								
Common-Source Forward Transconductance	g _{fs}	V _{DS} = -15 V, I _D = -1 mA f = 1 kHz	4.5					mS
Common-Source Output Conductance	g _{os}		20					μS
Drain-Source On-Resistance	r _{ds(on)}	V _{GS} = 0 V, I _D = 0 mA , f = 1 kHz			85		125	Ω
Common-Source Input Capacitance	C _{iSS}	V _{DS} = 0 V, V _{GS} = 0 V, f = 1 MHz	20					pF
Common-Source Reverse Transfer Capacitance	C _{rSS}	V _{DS} = 0 V, V _{GS} = 10 V f = 1 MHz	5					
Equivalent Input Noise Voltage	ē _n	V _{DG} = -10 V, I _D = -1 mA f = 1 kHz	20					nV/ √Hz
Switching								
Turn-On Time	t _{d(on)}	V _{GS(L)} = 0 V, V _{GS(H)} = 10 V See Switching Circuit	10					ns
	t _r		15					
Turn-Off Time	t _{d(off)}		10					
	t _f		20					

Notes

a. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

b. Pulse test: PW ≤ 300 μs duty cycle ≤ 3%.

PSCIA

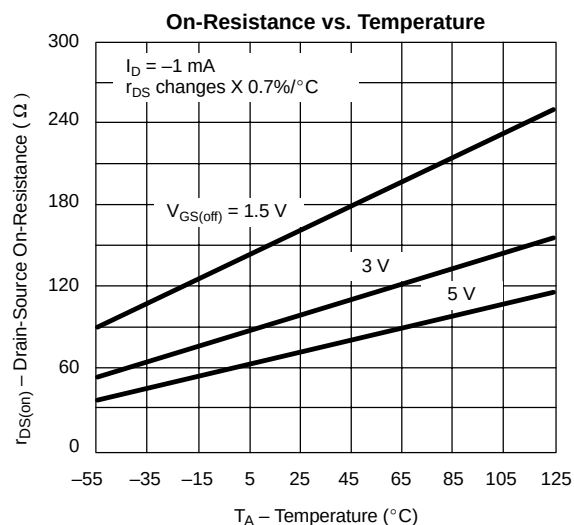
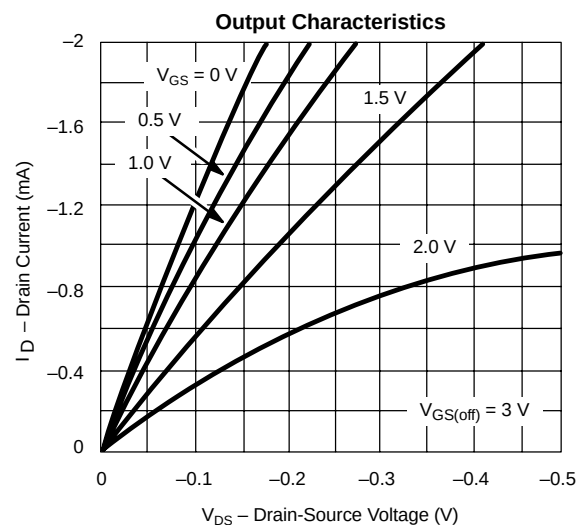
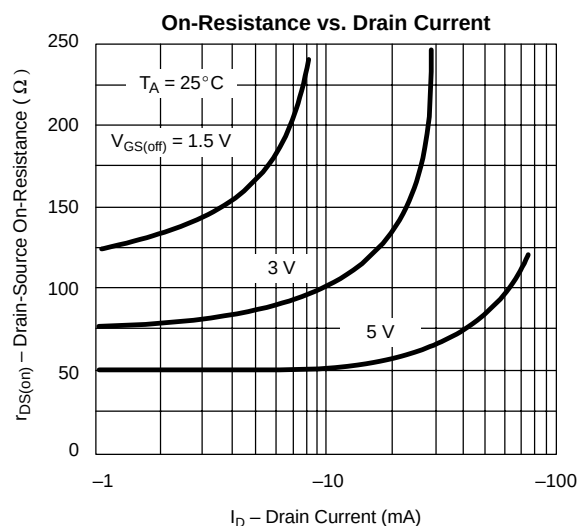
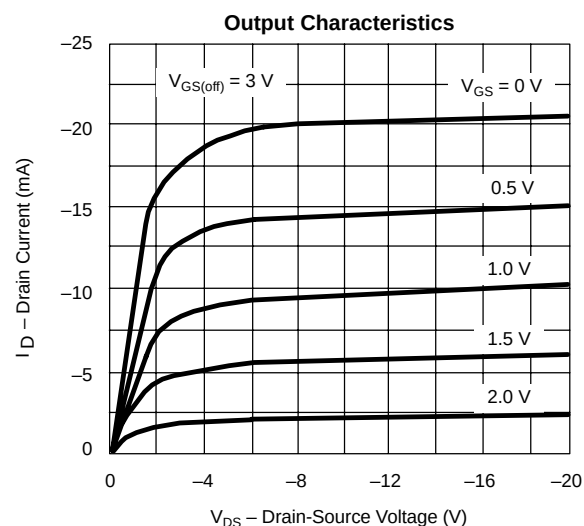
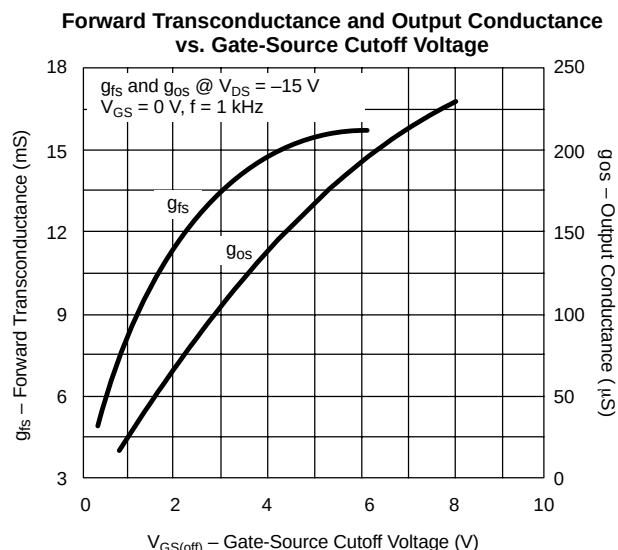
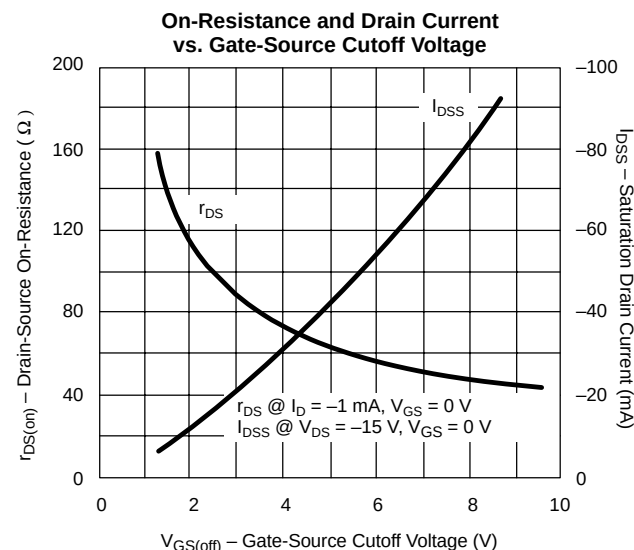
**SPECIFICATIONS FOR J/SST176 AND J/SST177 (T_A = 25 °C UNLESS OTHERWISE NOTED)**

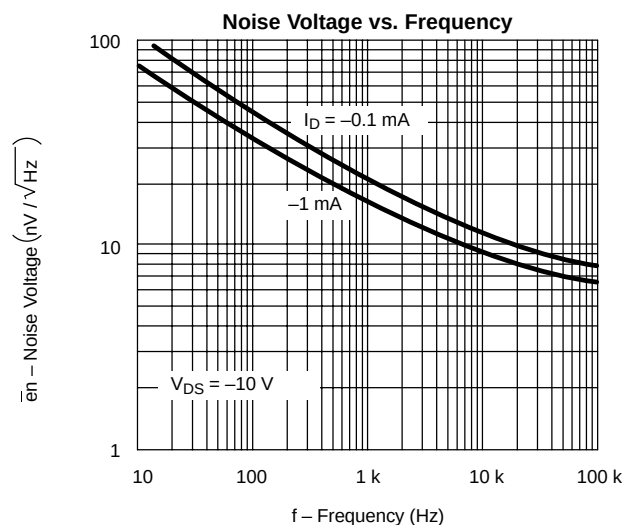
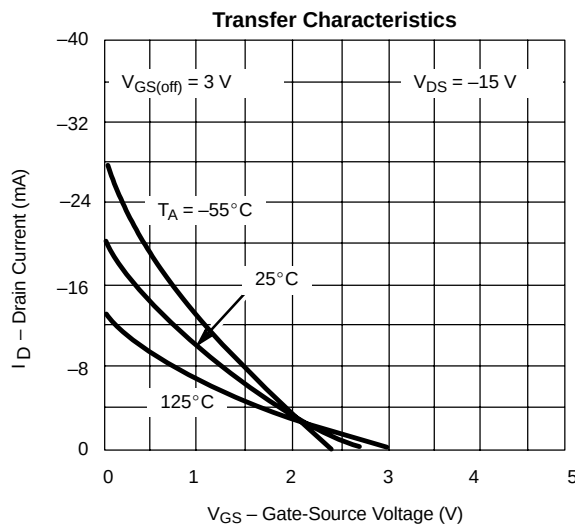
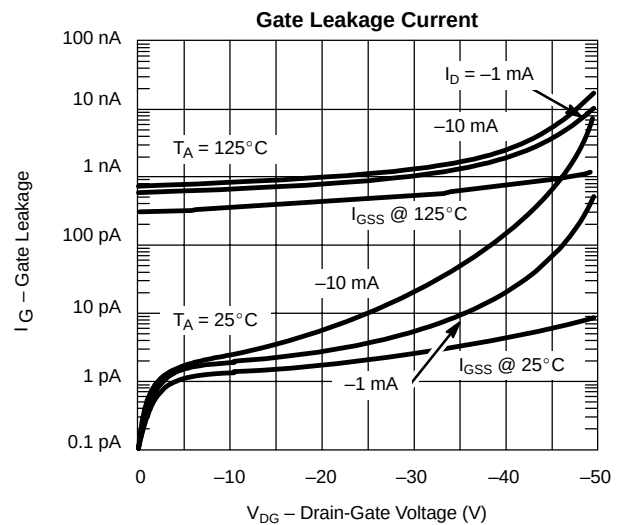
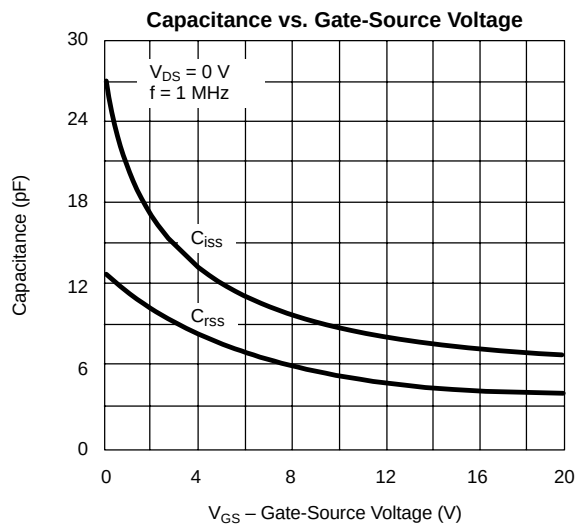
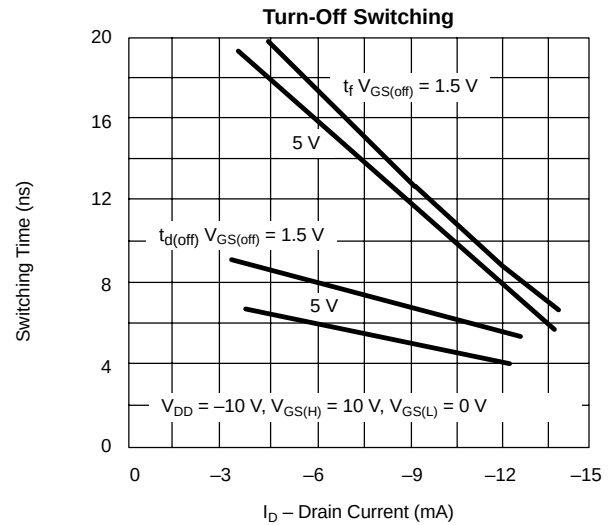
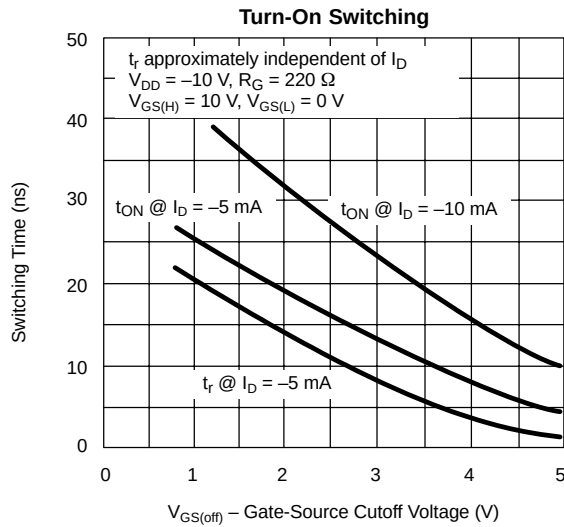
Parameter	Symbol	Test Conditions	Typ ^a	Limits				Unit
				J/SST176		J/SST177		
				Min	Max	Min	Max	
Static								
Gate-Source Breakdown Voltage	V _{(BR)GSS}	I _G = 1 μA , V _{DS} = 0 V	45	30		30		V
Gate-Source Cutoff Voltage	V _{GS(off)}	V _{DS} = −15 V, I _D = −10 nA		1	4	0.8	2.25	
Saturation Drain Current ^b	I _{DSS}	V _{DS} = −15 V, V _{GS} = 0 V		−2	−35	−1.5	−20	mA
Gate Reverse Current	I _{GSS}	V _{GS} = 20 V, V _{DS} = 0 V	0.01		1		1	nA
		T _A = 125°C	5					
Gate Operating Current	I _G	V _{DG} = −15 V, I _D = −1 mA	0.01					
Drain Cutoff Current	I _{D(off)}	V _{DS} = −15 V, V _{GS} = 10 V	−0.01		−1		−1	
		T _A = 125°C	−5					
Drain-Source On-Resistance	r _{DS(on)}	V _{GS} = 0 V, V _{DS} = −0.1 V			250		300	Ω
Gate-Source Forward Voltage	V _{GS(F)}	I _G = −1 mA , V _{DS} = 0 V	−0.7					V
Dynamic								
Common-Source Forward Transconductance	g _{fs}	V _{DS} = −15 V, I _D = −1 mA f = 1 kHz	4.5					mS
Common-Source Output Conductance	g _{os}		20					μS
Drain-Source On-Resistance	r _{ds(on)}	V _{GS} = 0 V, I _D = 0 mA , f = 1 kHz			250		300	Ω
Common-Source Input Capacitance	C _{iss}	V _{DS} = 0 V, V _{GS} = 0 V, f = 1 MHz	20					pF
Common-Source Reverse Transfer Capacitance	C _{rss}	V _{DS} = 0 V, V _{GS} = 10 V f = 1 MHz	5					
Equivalent Input Noise Voltage	e _n	V _{DG} = −10 V, I _D = −1 mA f = 1 kHz	20					nV/ √Hz
Switching								
Turn-On Time	t _{d(on)}	V _{GS(L)} = 0 V, V _{GS(H)} = 10 V See Switching Circuit	10					ns
	t _r		15					
Turn-Off Time	t _{d(off)}		10					
	t _f		20					

Notes

- a. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
b. Pulse test: PW ≤ 300 μs duty cycle ≤ 3%.

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TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

**TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)**

SWITCHING TIME TEST CIRCUIT				
	174	175	176	177
V_{DD}	-10 V	-6 V	-6 V	-6 V
V_{GG}	20 V	12 V	8 V	5 V
R_L^*	560 Ω	750 Ω	1800 Ω	5600 Ω
R_G^*	100 Ω	220 Ω	390 Ω	390 Ω
$I_{D(on)}$	-15 mA	-7 mA	-3 mA	-1 mA

*Non-inductive

INPUT PULSE

Rise Time < 1 ns
 Fall Time < 1 ns
 Pulse Width 100 ns
 PRF 1 MHz

SAMPLING SCOPE

Rise Time 0.4 ns
 Input Resistance 10 M Ω
 Input Capacitance 1.5 pF

See Typical Characteristics curves for changes.

