LM74500-Q1 Reverse Polarity Protection Controller

1 Features

- AEC-Q100 qualified with the following results
  - Device temperature grade 1: –40°C to +125°C ambient operating temperature range
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C4B
- 3.2-V to 65-V input range (3.9-V start up)
- –65-V input reverse voltage rating
- Charge pump for external N-Channel MOSFET
- Enable pin feature
- 1-µA shutdown current (EN=Low)
- 80-µA typical operating quiescent current (EN=High)
- Meets automotive ISO7637 pulse 1 transient requirements with additional TVS Diode
- Available in 8-pin SOT-23 package 2.90 mm × 1.60 mm

2 Applications

- Body electronics and lighting
- Automotive infotainment systems - digital cluster, head unit
- Automotive USB Hubs
- Industrial factory automation - PLC

3 Description

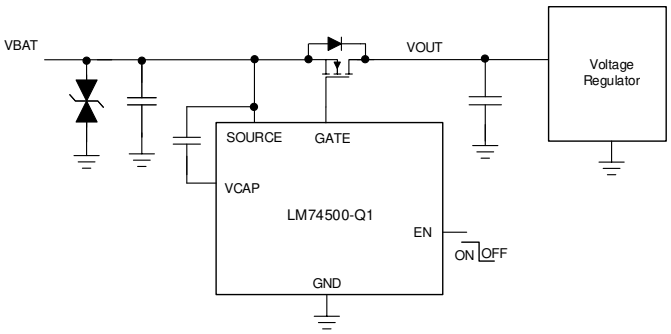
The LM74500-Q1 is an automotive AEC Q100 qualified controller which operates in conjunction with an external N-channel MOSFET as a low loss reverse polarity protection solution. The wide supply input range of 3.2 V to 65 V allows control of many popular DC bus voltages such as 12-V, 24-V and 48-V automotive battery systems. The 3.2-V input voltage support is particularly well suited for severe cold crank requirements in automotive systems. The device can withstand and protect the loads from negative supply voltages down to –65 V. The LM74500-Q1 does not have reverse current blocking and is suitable for input reverse poalrity protection of loads that can potentially deliver energy back to the input supply such as automotive body control module motor loads.

The LM74500-Q1 controller provides a charge pump gate drive for an external N-channel MOSFET. The high voltage rating of LM74500-Q1 helps to simplify the system designs for automotive ISO7637 protection. With the enable pin low, the controller is off and draws approximately 1 µA of current thus offering low system current when put into sleep mode.

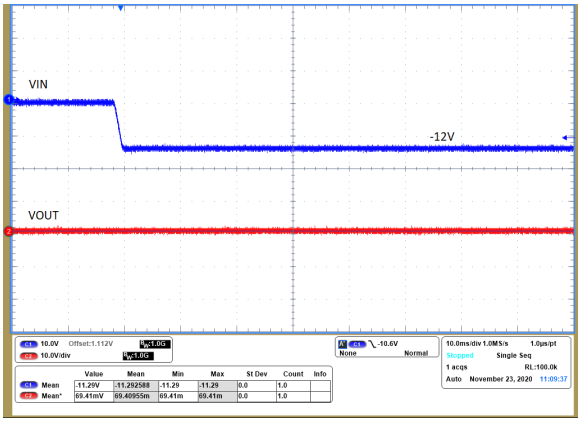
Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM74500-Q1	SOT-23 (8)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



LM74500-Q1 Typical Application Schematic



LM74500-Q1 Startup with –12-V Supply

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features....1
2 Applications....1
3 Description....1
4 Revision History....2
5 Pin Configuration and Functions....3
6 Specifications....4
6.1 Absolute Maximum Ratings....4
6.2 ESD Ratings....4
6.3 Recommended Operating Conditions....4
6.4 Thermal Information....4
6.5 Electrical Characteristics....5
6.6 Switching Characteristics....6
7 Typical Characteristics....7
8 Detailed Description....9
8.1 Overview....9
8.2 Functional Block Diagram....9
8.3 Feature Description....9
8.4 Device Functional Modes....11
9 Application and Implementation....12
9.1 Reverse Battery Protection for Automotive Body Control Module Applications....12
9.2 Reverse Polarity Protection....14
9.3 Application Information....16
10 Power Supply Recommendations....20
11 Layout....20
11.1 Layout Guidelines....20
11.2 Layout Example....20
12 Device and Documentation Support....21
12.1 Receiving Notification of Documentation Updates....21
12.2 Support Resources....21
12.3 Trademarks....21
12.4 Electrostatic Discharge Caution....21
12.5 Glossary....21
13 Mechanical, Packaging, and Orderable Information....22

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2020	*	Initial release.

Copyright © 2020 Texas Instruments Incorporated

5 Pin Configuration and Functions

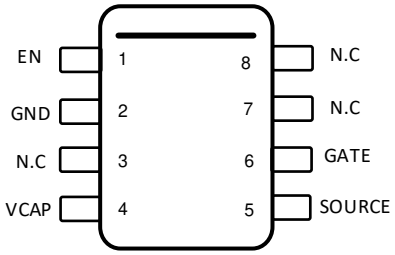


Figure 5-1. DDF Package 8-Pin SOT-23 LM74500-Q1 Top View

Table 5-1. LM74500-Q1 Pin Functions

PIN		I/O(1)	DESCRIPTION
NO.	NAME		
1	EN	I	Enable pin. Can be connected to SOURCE for always ON operation
2	GND	G	Ground pin
3	N.C	-	No connection
4	VCAP	O	Charge pump output. Connect to external charge pump capacitor
5	SOURCE	I	Input supply pin to the controller. Connect to the source of the external N-channel MOSFET
6	GATE	O	Gate drive output. Connect to gate of the external N-channel MOSFET
7	N.C	-	No connection
8	N.C	-	No connection

(1) I = Input, O = Output, G = GND

Copyright © 2020 Texas Instruments Incorporated

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input Pins	SOURCE to GND	–65	65	V
	EN to GND, $V_{(SOURCE)}$ > 0 V	–0.3	65	V
	EN to GND, $V_{(SOURCE)}$ ≤ 0 V	$V_{(SOURCE)}$	(65 + $V_{(SOURCE)}$)	V
Output Pins	GATE to SOURCE	–0.3	15	V
	VCAP to SOURCE	–0.3	15	V
Operating junction temperature(2)		–40	150	°C
Storage temperature, T_{stg}		–40	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (EN, VCAP, SOURCE, NC)	±750	
			Other pins	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	NOM	MAX	UNIT
Input Pins	SOURCE to GND	–60		60	V
	EN to GND	–60		60	
External capacitance	SOURCE	22			nF
	VCAP to SOURCE	0.1			µF
External MOSFET max V_{GS} rating	GATE to SOURCE	15			V
T_J	Operating junction temperature range(2)	–40		150	°C

(1) Recommended Operating Conditions are conditions under which the device is intended to be functional. For specifications and test conditions, see *electrical characteristics*

(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

6.4 Thermal Information

THERMAL METRIC(1)		LM74500-Q1 DDF (SOT) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	133.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	72.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	4.6	°C/W

Copyright © 2020 Texas Instruments Incorporated

6.4 Thermal Information (continued)

THERMAL METRIC(1)		LM74500-Q1 DDF (SOT) 8 PINS	UNIT
Ψ_{JB}	Junction-to-board characterization parameter	54.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

6.5 Electrical Characteristics

T_J = –40°C to +125°C; typical values at T_J = 25°C, $V_{(SOURCE)}$ = 12 V, $C_{(VCAP)}$ = 0.1 µF, $V_{(EN)}$ = 3.3 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{SOURCE} SUPPLY VOLTAGE						
$V_{(SOURCE)}$	Operating input voltage		4		60	V
$V_{(SOURCE\ POR)}$	VSOURCE POR Rising threshold				3.9	V
	VSOURCE POR Falling threshold		2.2	2.8	3.1	V
$V_{(SOURCE\ POR(Hys))}$	VSOURCE POR Hysteresis		0.44		0.67	V
$I_{(SHDN)}$	Shutdown Supply Current	$V_{(EN)}$ = 0 V		0.9	1.5	µA
$I_{(Q)}$	Operating Quiescent Current			80	130	µA
ENABLE INPUT						
$V_{(EN_IL)}$	Enable input low threshold		0.5	0.9	1.22	V
$V_{(EN_IH)}$	Enable input high threshold		1.06	2	2.6	
$V_{(EN_Hys)}$	Enable Hysteresis		0.52		1.35	V
$I_{(EN)}$	Enable sink current	$V_{(EN)}$ = 12 V		3	5	µA
GATE DRIVE						
$I_{(GATE)}$	Peak source current	$V_{(GATE)} – V_{(SOURCE)}$ = 5 V	3	11		mA
	Peak sink current	EN= High to Low $V_{(GATE)} – V_{(SOURCE)}$ = 5 V		2370		mA
RDS_{ON}	discharge switch RDS_{ON}	EN = High to Low $V_{(GATE)} – V_{(SOURCE)}$ = 100 mV	0.4		2	Ω
CHARGE PUMP						
$I_{(VCAP)}$	Charge Pump source current (Charge pump on)	$V_{(VCAP)} – V_{(SOURCE)}$ = 7 V	162	300	600	µA
	Charge Pump sink current (Charge pump off)	$V_{(VCAP)} – V_{(SOURCE)}$ = 14 V		5	10	µA
$V_{(VCAP)} – V_{(SOURCE)}$	Charge pump voltage at $V_{(SOURCE)}$ = 3.2 V	$I_{(VCAP)} \le$ 30 µA	8			V
$V_{(VCAP)} – V_{(SOURCE)}$	Charge pump turn on voltage		10.3	11.6	13	V
$V_{(VCAP)} – V_{(SOURCE)}$	Charge pump turn off voltage		11	12.4	13.9	V
$V_{(VCAP)} – V_{(SOURCE)}$	Charge Pump Enable comparator Hysteresis		0.4	0.8	1.2	V
$V_{(VCAP\ UVLO)}$	$V_{(VCAP)} – V_{(SOURCE)}$ UV release at rising edge		5.7	6.5	7.5	V
$V_{(VCAP\ UVLO)}$	$V_{(VCAP)} – V_{(SOURCE)}$ UV threshold at falling edge		5.05	5.4	6.2	V

Copyright © 2020 Texas Instruments Incorporated

6.6 Switching Characteristics

T_J = –40°C to +125°C; typical values at T_J = 25°C, $V_{(SOURCE)}$ = 12 V, C_{IN} = $C_{(VCAP)}$ = C_{OUT} = 0.1 µF, $V_{(EN)}$ = 3.3 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EN_{TDLY}	Enable (low to high) to Gate Turn On delay	$V_{(VCAP)}$ > $V_{(VCAP\ UVLOR)}$		75	110	µs

Copyright © 2020 Texas Instruments Incorporated

7 Typical Characteristics

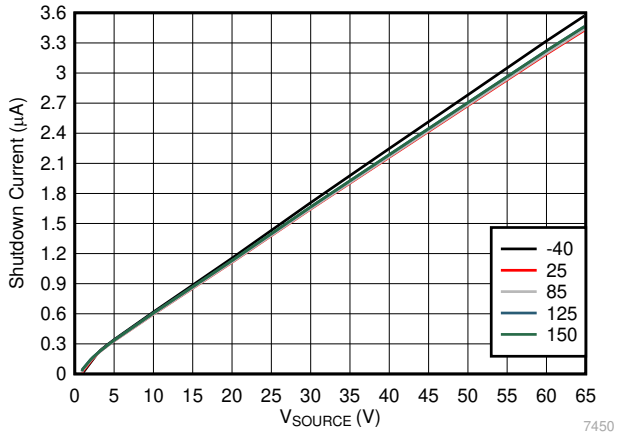


Figure 7-1. Shutdown Supply Current vs Supply Voltage

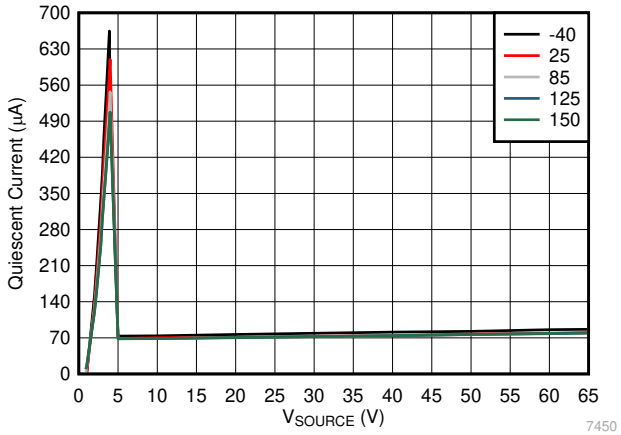


Figure 7-2. Operating Quiescent Current vs Supply Voltage

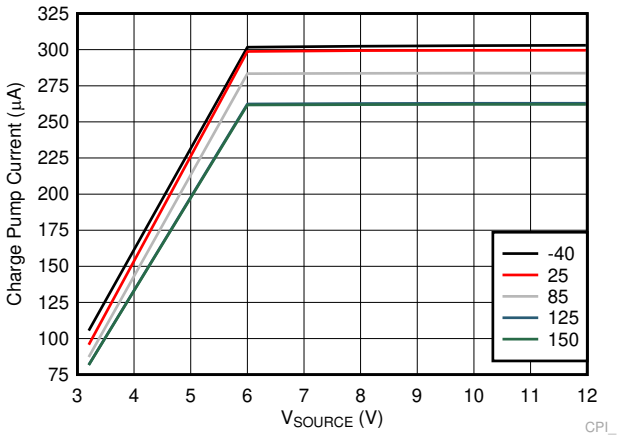


Figure 7-3. Charge Pump Current vs Supply Voltage at V_{CAP} = 6 V

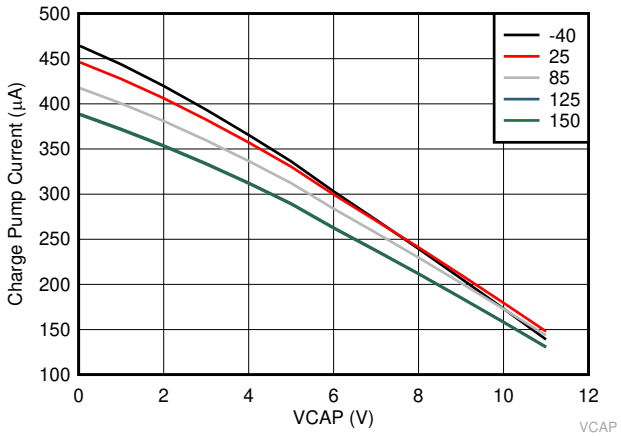


Figure 7-4. Charge Pump V-I Characteristics at V_{SOURCE} > = 12 V

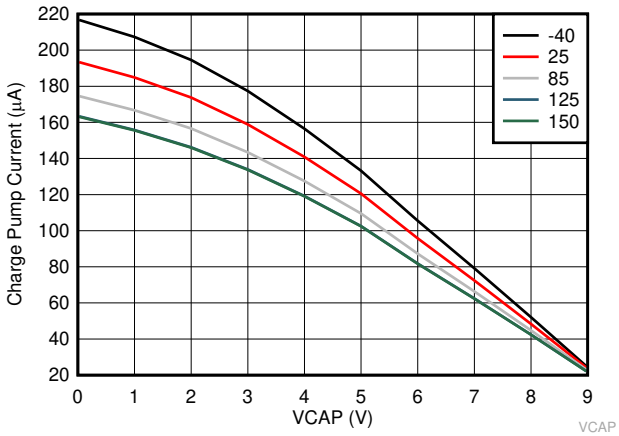


Figure 7-5. Charge Pump V-I Characteristics at V_{SOURCE} = 3.2 V

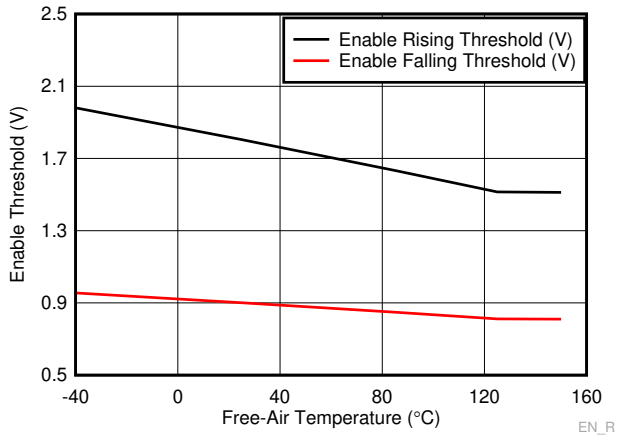


Figure 7-6. Enable Rising and Falling threshold vs Temperature

Copyright © 2020 Texas Instruments Incorporated

7 Typical Characteristics (continued)

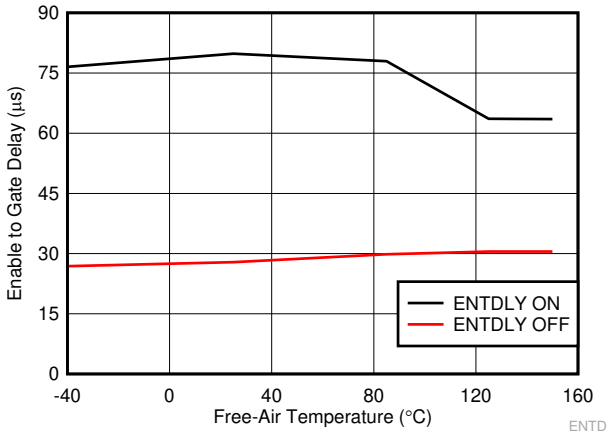


Figure 7-7. Enable to Gate Delay vs Temperature

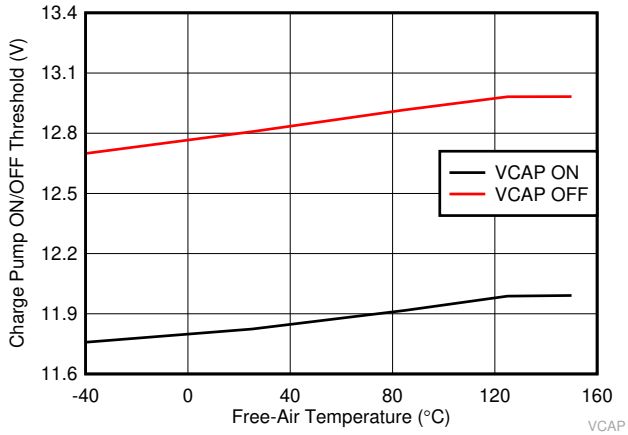


Figure 7-8. Charge Pump ON/OFF Threshold vs Temperature

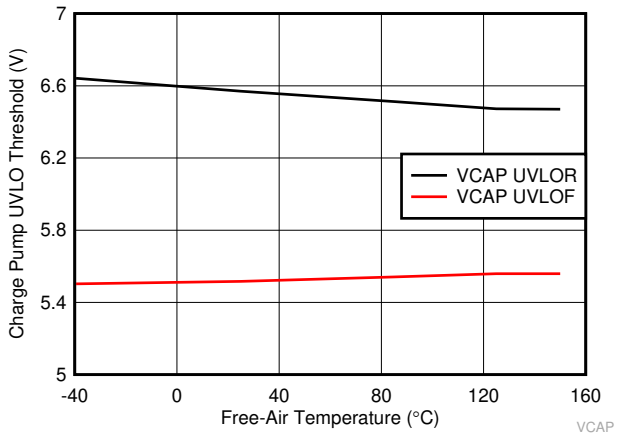


Figure 7-9. Charge Pump UVLO Threshold vs Temperature

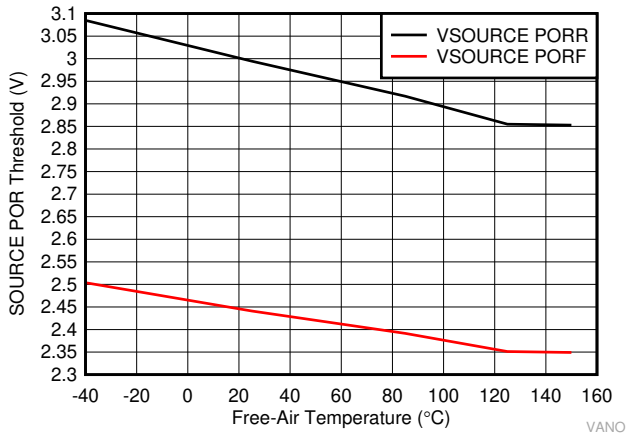


Figure 7-10. V_{SOURCE} POR Threshold vs Temperature

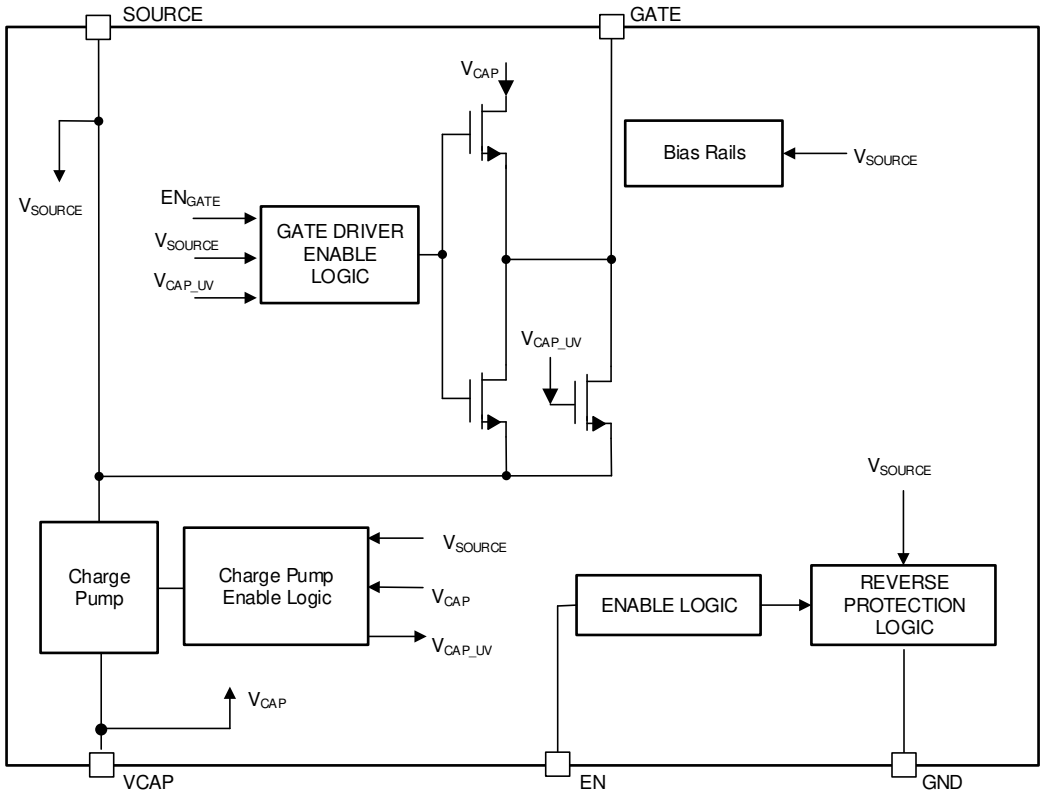
Copyright © 2020 Texas Instruments Incorporated

8 Detailed Description

8.1 Overview

The LM74500-Q1 controller has all the features necessary to implement an efficient and fast reverse polarity protection circuit. This easy to use reverse polarity protection controller is paired with an external N-channel MOSFET to replace other reverse polarity schemes such as a P-channel MOSFET. An internal charge pump is used to drive the external N-Channel MOSFET to a maximum gate drive voltage of approximately 15 V. An enable pin, EN is available to place the LM74500-Q1 in shutdown mode disabling the N-Channel MOSFET and minimizing the quiescent current.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Input Voltage

The SOURCE pin is used to power the LM74500-Q1's internal circuitry, typically drawing 80 µA when enabled and 1 µA when disabled. If the SOURCE pin voltage is greater than the POR Rising threshold, then LM74500-Q1 operates in either shutdown mode or conduction mode in accordance with the EN pin voltage. The voltage from SOURCE to GND is designed to vary from 65 V to –65 V, allowing the LM74500-Q1 to withstand negative voltage transients.

8.3.2 Charge Pump

The charge pump supplies the voltage necessary to drive the external N-channel MOSFET. An external charge pump capacitor is placed between VCAP and SOURCE pin to provide energy to turn on the external MOSFET. In order for the charge pump to supply current to the external capacitor the EN pin voltage must be above the

Copyright © 2020 Texas Instruments Incorporated

specified input high threshold, $V_{(EN_IH)}$. When enabled the charge pump sources a charging current of 300 µA typically. If EN pins is pulled low, then the charge pump remains disabled. To ensure that the external MOSFET can be driven above its specified threshold voltage, the VCAP to SOURCE voltage must be above the undervoltage lockout threshold, typically 6.5 V, before the internal gate driver is enabled. Use Equation 1 to calculate the initial gate driver enable delay.

$$T_{(DRV_EN)} = 75\mu s + C_{(VCAP)} x \frac{V_{(VCAP_UVLOR)}}{300\mu A} \quad (1)$$

where

- $C_{(VCAP)}$ is the charge pump capacitance connected across SOURCE and VCAP pins
- $V_{(VCAP_UVLOR)}$ = 6.5 V (typical)

To remove any chatter on the gate drive approximately 800 mV of hysteresis is added to the VCAP undervoltage lockout. The charge pump remains enabled until the VCAP to SOURCE voltage reaches 12.4 V, typically, at which point the charge pump is disabled decreasing the current draw on the SOURCE pin. The charge pump remains disabled until the VCAP to SOURCE voltage is below to 11.6 V typically at which point the charge pump is enabled. The voltage between VCAP and SOURCE continue to charge and discharge between 11.6 V and 12.4 V as shown in Figure 8-1. By enabling and disabling the charge pump, the operating quiescent current of the LM74500-Q1 is reduced. When the charge pump is disabled it sinks 5-µA typical.

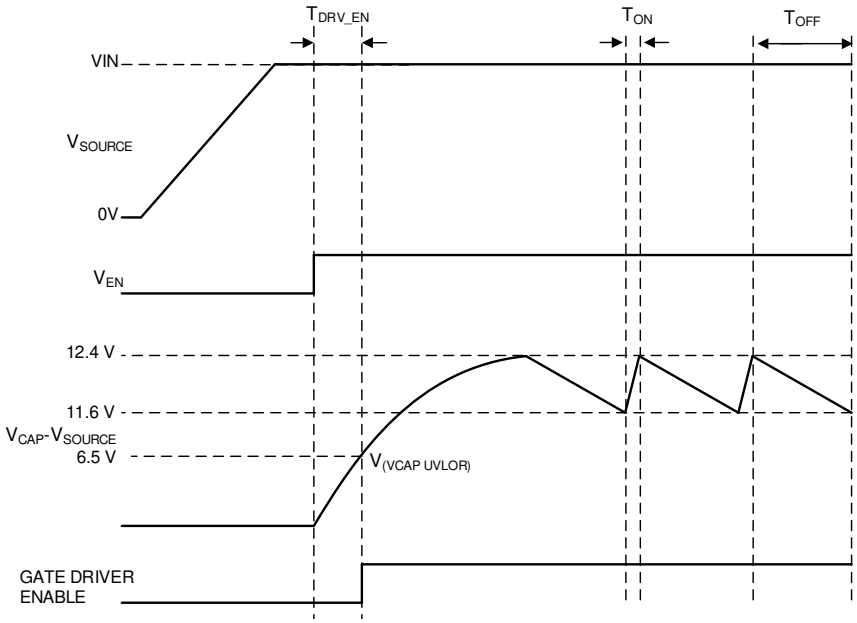


Figure 8-1. Charge Pump Operation

8.3.3 Gate Driver

The gate driver is used to control the external N-Channel MOSFET by setting the appropriate GATE to SOURCE voltage .

Before the gate driver is enabled following three conditions must be achieved:

- The EN pin voltage must be greater than the specified input high voltage.
- The VCAP to SOURCE voltage must be greater than the undervoltage lockout voltage.
- The SOURCE voltage must be greater than V_{SOURCE} POR Rising threshold.

Copyright © 2020 Texas Instruments Incorporated

If the above conditions are not achieved, then the GATE pin is internally connected to the SOURCE pin, assuring that the external MOSFET is disabled. Once these conditions are achieved the gate driver operates in the conduction mode enhancing the external MOSFET completely.

8.3.4 Enable

The LM74500-Q1 has an enable pin, EN. The enable pin allows for the gate driver to be either enabled or disabled by an external signal. If the EN pin voltage is greater than the rising threshold, the gate driver and charge pump operates as described in *Gate Driver* and *Charge Pump* sections. If the enable pin voltage is less than the input low threshold, the charge pump and gate driver are disabled placing the LM74500-Q1 in shutdown mode. The EN pin can withstand a voltage as large as 65 V and as low as –65 V. This allows for the EN pin to be connected directly to the SOURCE pin if enable functionality is not needed. In conditions where EN is left floating, the internal sink current of 3 uA pulls EN pin low and disables the device.

8.4 Device Functional Modes

8.4.1 Shutdown Mode

The LM74500-Q1 enters shutdown mode when the EN pin voltage is below the specified input low threshold $V_{(EN_IL)}$. Both the gate driver and the charge pump are disabled in shutdown mode. During shutdown mode the LM74500-Q1 enters low I_Q operation with the SOURCE pin only sinking 1 µA. When the LM74500-Q1 is in shutdown mode, forward current flow through the external MOSFET is not interrupted but is conducted through the MOSFET's body diode.

8.4.2 Conduction Mode

For the LM74500-Q1 to operate in conduction mode the gate driver must be enabled as described in the *Gate Driver* section. If these conditions are achieved the GATE pin is internally connected to the VCAP pin resulting in the GATE to SOURCE voltage being approximately the same as the VCAP to SOURCE voltage. By connecting VCAP to GATE the external MOSFET's $R_{DS(ON)}$ is minimized reducing the power loss of the external MOSFET when forward currents are large.

Copyright © 2020 Texas Instruments Incorporated

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Reverse Battery Protection for Automotive Body Control Module Applications

Reverse-battery protection activates when battery terminals are incorrectly connected during jump start, vehicle maintenance or service because a connection error can damage the components in ECUs if they are not rated to handle reverse polarity. An N-channel MOSFET (N-FET) based reverse polarity protection solutions are becoming obivious choice over discrete reverse-battery protection solutions like Schottky diodes and P-channel field-effect transistors (P-FETs) due to their better power and thermal efficiency and the comparitively smaller space they consume on a printed circuit board. Based on the application needs, reverse polarity protection solutions can be divided into two main categories

- Applications which need both input reverse polarity protection and reverse current blocking
- Applications which need only input reverse polarity protection and does not need reverse current blocking

Figure 9-1 provides an overview of these two reverse polarity protection solution categories. Typically for applications where output loads are DC/DC converters, voltage regulator followed by MCU/processors (Logic paths), input reverse polarity protection and reverse current blocking feature is required. For reverse polarity protection solution of the logic path ideal diode controllers such as LM74700-Q1 is a suitable device.

Copyright © 2020 Texas Instruments Incorporated

For the applications such as Body Control Module (BCM) load driving paths, input reverse polarity protection is required but reverse current blocking is not a must have feature. For reverse polarity protection solution of the BCM load driving paths, reverse polarity potection controllers such as LM74500-Q1 is a suitable device.

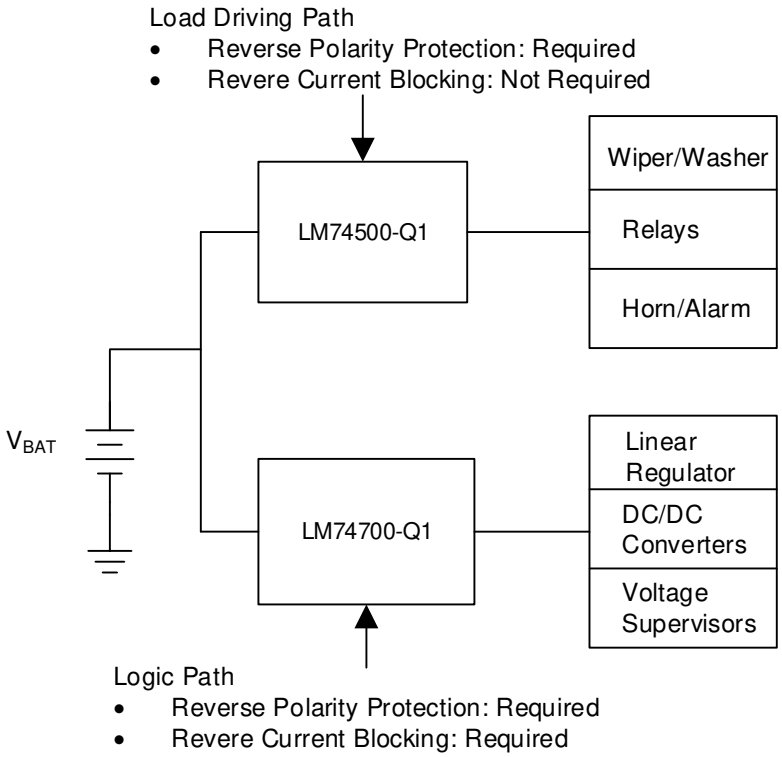


Figure 9-1. Typical Block Diagram for Automotive BCM Reverse Battery Protection Solution

For certain applications such as body control module load driving paths where output loads are inductive in nature such as wiper motor, door control module, it is required that reverse polarity protection device should provide protection against incorrect input polarity. However, it should not block reverse current from loads back to the battery. This is mainly required to avoid voltage overshoot which is caused when inductive loads are turned off. If reverse polarity protection device blocks the reverse current then there could be voltage overshoot caused due to inductive kick back or motor regenrative action and can damage parallel loads connected on the output of reverse polarity protection device. For certain specific loads such as wiper motor, a voltage overshoot is seen due to transformer effect when wiper motor speed is changed from fast speed to slow speed. LM74500-Q1 is designed to provide protection against input reverse polarity for such applications where reverse current

Copyright © 2020 Texas Instruments Incorporated

blocking is not reuiqred. Figure 9-2 shows typical application circuit of reverse polarity protection of body control module load driving paths.

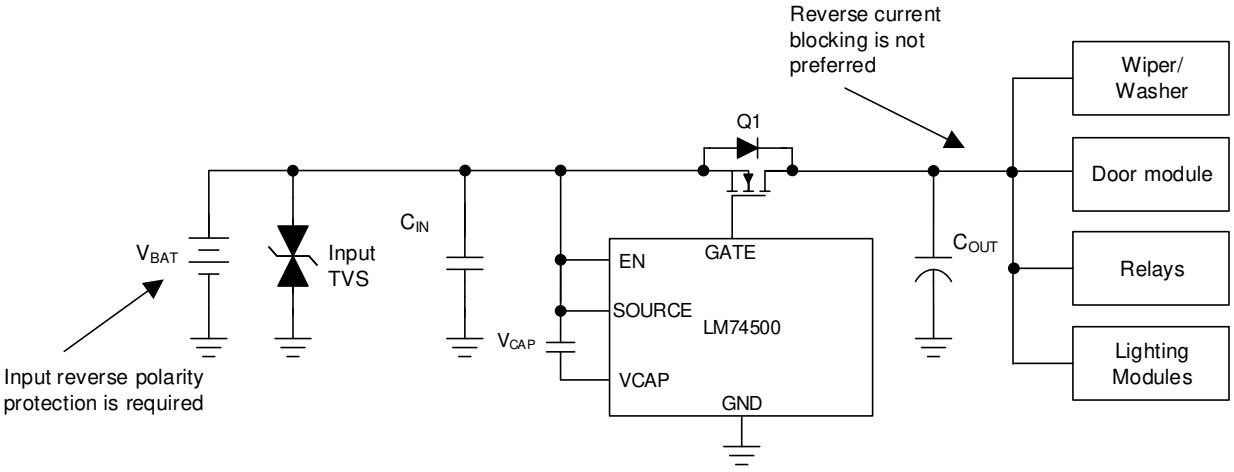


Figure 9-2. Typical Block Diagram of Reverse Battery Protection for Body Control Module Load Driving Path

9.2 Reverse Polarity Protection

P-FET based reverse polarity protection is a very commonly used scheme in industrial and automotive applications to achieve low insertion loss protection solution. A low loss reverse polarity protection solution can be realised using LM74500-Q1 with an external N-FET to replace P-FET based solution. LM74500-Q1 based reverse polarity protection solution offers better cold crank performance (low V_{IN} operation) and smaller solution size compared to P-FET based solution. Figure 9-3 compares the performance benefits of LM74500-Q1 +N-FET over traditional P-FET based reverse polarity protection solution. As shown in Figure 9-3, for a given power level LM74500-Q1+N-FET solution can be three times smaller than a similar power rated P-FET solution. Also as P-FET is self biased by simply pulling it's gate pin low and thus P-FET shows poorer cold crank performance (low V_{IN} operation) compared to LM74500-Q1. During severe cold crank where battery voltage falls below 4 V, P-FET series resistance increase drastically as shown in Figure 9-3. This leads to higher voltage drop across the P-FET. Also with higher gate to source threshold (V_T) this can sometimes lead to system reset due to turning off of

Copyright © 2020 Texas Instruments Incorporated

the P-FET. On the other side LM74500-Q1 has excellent severe cold crank performance. LM74500-Q1 keeps external FET completely enhanced even when input voltage falls to 3.2 V during severe cold crank operation.

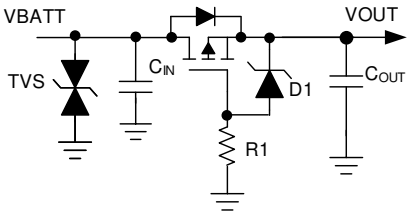
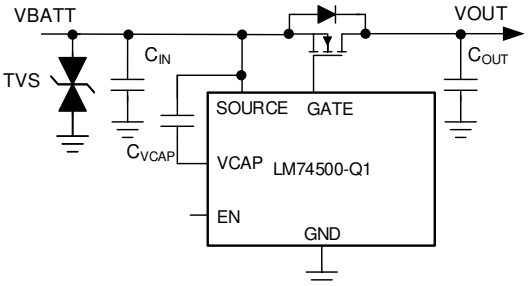
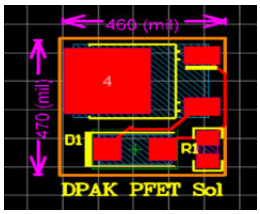
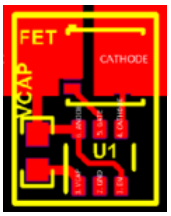
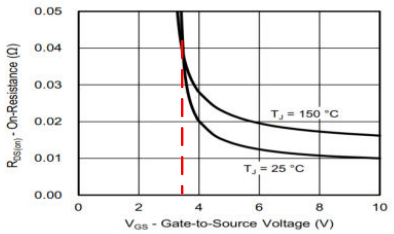
Parameter	P-FET	LM74500-Q1 + N-FET
Typical Application Diagram		
Solution Size (Load current >6A)	12mm x 11.7mm ($140mm^2$) 	7mm x 5.3mm ($37.1mm^2$) 
Low V_{IN} / Cold-Crank Performance		Better cold crank performance compared to PFET based solution. External N-FET remains fully enhanced even if input voltage falls to 3.2V.

Figure 9-3. Performance Comparison of P-FET and LM74500-Q1 Based Reverse Polarity Protection Solution

Copyright © 2020 Texas Instruments Incorporated

9.3 Application Information

The LM74500-Q1 is used with N-Channel MOSFET controller in a typical reverse polarity protection application. The schematic for the 12-V battery protection application is shown in Figure 9-4 where the LM74500-Q1 is used to drive the MOSFET Q1 in series with a battery. The TVS is not required for the LM74500-Q1 to operate, but they are used to clamp the positive and negative voltage surges. The output capacitor C_{OUT} is recommended to protect the immediate output voltage collapse as a result of line disturbance.

9.3.1 Typical Application

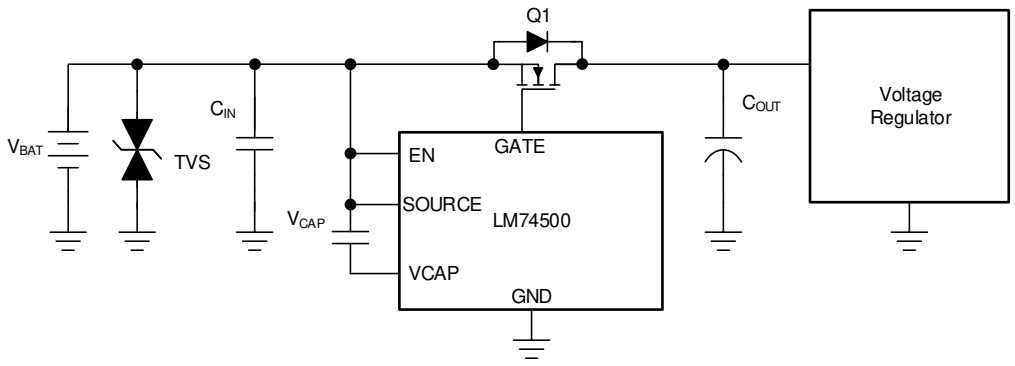


Figure 9-4. Typical Application Circuit

9.3.1.1 Design Requirements

A design example, with system design parameters listed in Table 9-1 is presented.

Table 9-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	12-V Battery, 12-V Nominal with 3.2-V Cold Crank and 35-V Load Dump
Output voltage	3.2 V during Cold Crank to 35-V Load Dump
Output current range	3-A Nominal, 5-A Maximum
Output capacitance	220-µF Typical Output Capacitance
Automotive EMC Compliance	ISO 7637-2 and ISO 16750-2

9.3.1.2 Detailed Design Procedure

9.3.1.2.1 Design Considerations

- Input operating voltage range, including cold crank and load dump conditions
- Nominal load current and maximum load current

9.3.1.2.2 MOSFET Selection

The important MOSFET electrical parameters are the maximum continuous drain current I_D, the maximum drain-to-source voltage $V_{DS(MAX)}$, the maximum source current through body diode and the drain-to-source On resistance R_{DSON}.

The maximum continuous drain current, I_D, rating must exceed the maximum continuous load current. The maximum drain-to-source voltage, $V_{DS(MAX)}$, must be high enough to withstand the highest differential voltage seen in the application. This would include any anticipated fault conditions. It is recommended to use MOSFETs with voltage rating up to 60-V maximum with the LM74500-Q1 because SOURCE pin maximum voltage rating is 65-V. The maximum V_{GS} LM74500-Q1 can drive is 13 V, so a MOSFET with 15-V minimum V_{GS} rating should be selected. If a MOSFET with V_{GS} rating < 15 V is selected, a zener diode can be used to clamp V_{GS} to safe level.

Copyright © 2020 Texas Instruments Incorporated

During startup, inrush current flows through the body diode to charge the bulk hold-up capacitors at the output. The maximum source current through the body diode must be higher than the inrush current that can be seen in the application.

To reduce the MOSFET conduction losses, lowest possible $R_{DS(ON)}$ is preferred.

Based on the design requirements, preferred MOSFET ratings are:

- 60-V $V_{DS(MAX)}$ and ±20-V $V_{GS(MAX)}$

DMT6007LFG MOSFET from Diodes Inc. is selected to meet this 12-V reverse battery protection design requirements and it is rated at:

- 60-V $V_{DS(MAX)}$ and ±20-V $V_{GS(MAX)}$
- $R_{DS(ON)}$ 6.5-mΩ typical and 8.5-mΩ maximum rated at 4.5-V V_{GS} to ensure lower power dissipationa cross the FET

Thermal resistance of the MOSFET should be considered against the expected maximum power dissipation in the MOSFET to ensure that the junction temperature (T_J) is well controlled.

9.3.1.2.3 Charge Pump VCAP, Input and Output Capacitance

Minimum required capacitance for charge pump VCAP and input/output capacitance are:

- VCAP: Minimum 0.1 µF is required; recommended value of VCAP (µF) ≥ 10 x $C_{ISS(MOSFET)}$ (µF)
- C_{IN}: Typical input capacitor of 0.1 µF
- C_{OUT}: Typical output capacitor 220 µF

9.3.1.3 Selection of TVS Diodes for 12-V Battery Protection Applications

TVS diodes are used in automotive systems for protection against transients. In the 12-V battery protection application circuit shown in Figure 9-5, a bi-directional TVS diode is used to protect from positive and negative transient voltages that occur during normal operation of the car and these transient voltage levels and pulses are specified in ISO 7637-2 and ISO 16750-2 standards.

The two important specifications of the TVS are breakdown voltage and clamping voltage. Breakdown voltage is the voltage at which the TVS diode goes into avalanche similar to a zener diode and is specified at a low current value typical 1 mA and the breakdown voltage should be higher than worst case steady state voltages seen in the system. The breakdown voltage of the TVS+ should be higher than 24-V jump start voltage and 35-V suppressed load dump voltage and less than the maximum input voltage rating of LM74500-Q1 (65 V). The breakdown voltage of TVS- should be higher than maximum reverse battery voltage –16 V, so that the TVS- is not damaged due to long time exposure to reverse connected battery.

Clamping voltage is the voltage the TVS diode clamps in high current pulse situations and this voltage is much higher than the breakdown voltage. TVS diodes are meant to clamp transient pulses and should not interfere with steady state operation. In the case of an ISO 7637-2 pulse 1, the input voltage goes up to –150 V with a generator impedance of 10 Ω. This translates to 15 A flowing through the TVS - and the voltage across the TVS would be close to its clamping voltage.

Copyright © 2020 Texas Instruments Incorporated

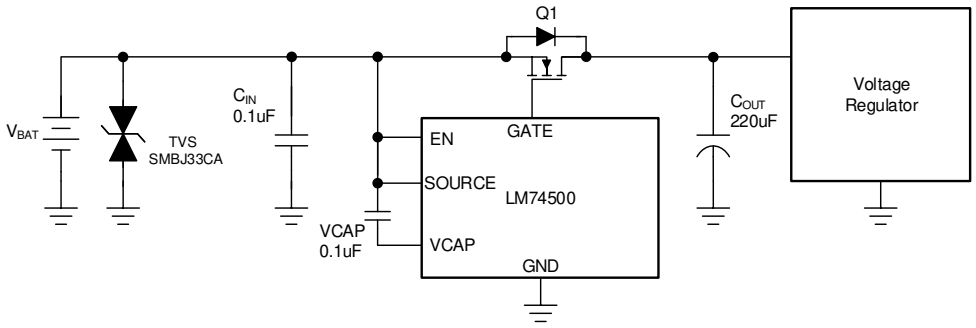


Figure 9-5. Typical 12-V Battery Protection with Single Bi-Directional TVS

The next criterion is that the absolute minimum rating of source voltage of the LM74500-Q1 (–65 V) and the maximum V_{DS} rating MOSFET are not exceeded. In the design example, 60-V rated MOSFET is chosen.

SMBJ series of TVS' are rated up to 600-W peak pulse power levels. This is sufficient for ISO 7637-2 pulses and suppressed load dump (ISO-16750-2 pulse B).

9.3.1.4 Selection of TVS Diodes and MOSFET for 24-V Battery Protection Applications

Typical 24-V battery protection application circuit shown in Figure 9-6 uses two uni-directional TVS diodes to protect from positive and negative transient voltages.

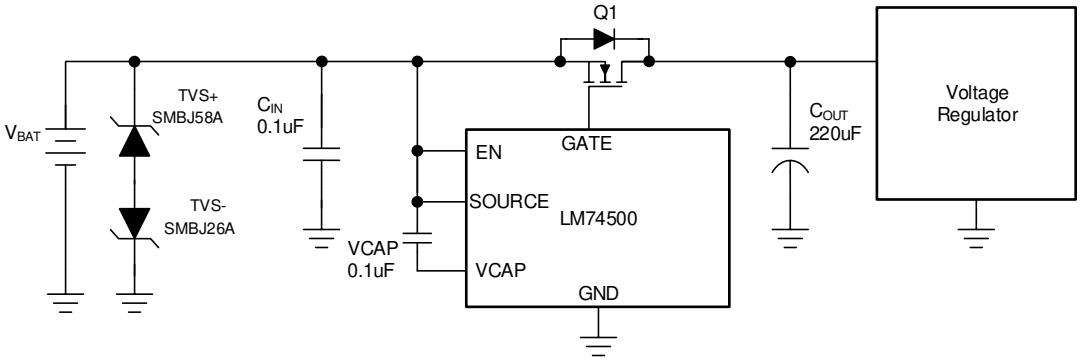


Figure 9-6. Typical 24-V Battery Protection with Two Uni-Directional TVS

The breakdown voltage of the TVS+ should be higher than 48-V jump start voltage, less than the absolute maximum ratings of source and enable pin of LM74500-Q1 (65 V) and should withstand 65-V suppressed load dump. The breakdown voltage of TVS- should be lower than maximum reverse battery voltage –32 V, so that the TVS- is not damaged due to long time exposure to reverse connected battery.

During ISO 7637-2 pulse 1, the input voltage goes up to –600 V with a generator impedance of 50 Ω. Single bi-directional TVS cannot be used for 24-V battery protection because breakdown voltage for TVS+ ≥ 48V, maximum negative clamping voltage is ≤ –65 V . Two uni-directional TVS connected back-back needs to be used at the input. For positive side TVS+, SMBJ58A with the breakdown voltage of 64.4 V (minimum), 67.8 (typical) is recommended. For the negative side TVS-, SMBJ26A with breakdown voltage close to 32 V (to withstand maximum reverse battery voltage –32 V) and maximum clamping voltage of 42 V is recommended.

For 24-V battery protection, a 75-V rated MOSFET is recommended to be used along with SMBJ26A and SMBJ58A connected back-back at the input.

Copyright © 2020 Texas Instruments Incorporated

9.3.1.5 Application Curves

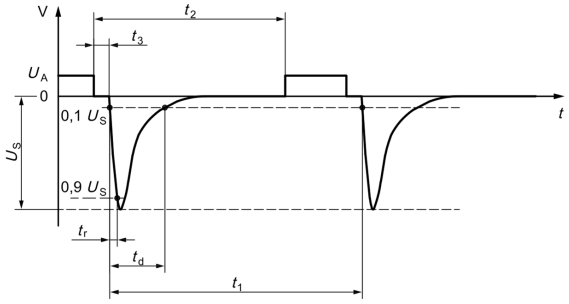
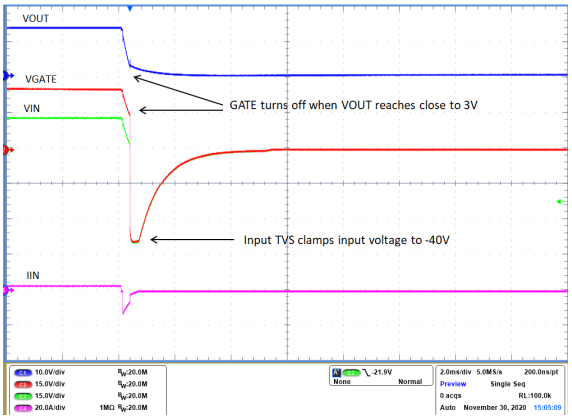
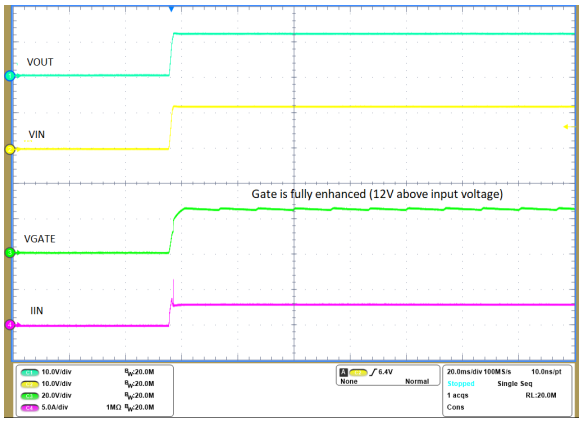


Figure 9-7. ISO 7637-2 Pulse 1



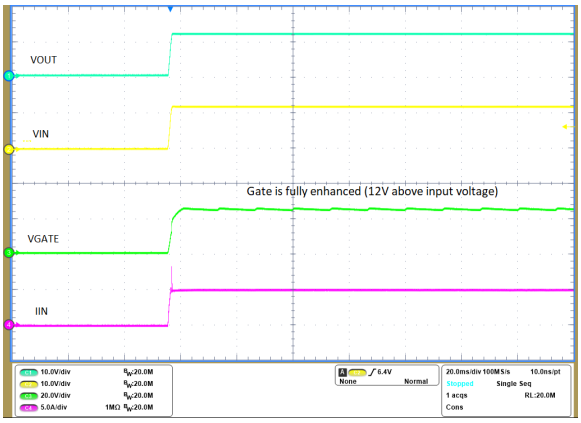
Time (2 ms/DIV)

Figure 9-8. Response to ISO 7637-2 Pulse 1



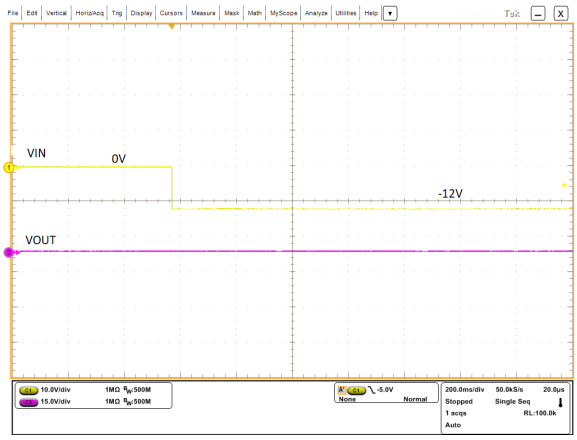
Time (20 ms/DIV)

Figure 9-9. Startup with 3-A Load



Time (20ms/DIV)

Figure 9-10. Startup with 5-A Load



Time (200 ms/DIV)

Figure 9-11. Startup with Input Reverse Voltage (–12 V)

10 Power Supply Recommendations

The LM74500-Q1 reverse polarity protection controller is designed for the supply voltage range of 3.2 V ≤ V_{SOURCE} ≤ 65 V. If the input supply is located more than a few inches from the device, an input ceramic bypass capacitor higher than 22 nF is recommended. To prevent LM74500-Q1 and surrounding components from damage under the conditions of a direct output short circuit, it is necessary to use a power supply having over load and short circuit protection.

11 Layout

11.1 Layout Guidelines

- Connect SOURCE and GATE pins of LM74500-Q1 close to the MOSFET's SOURCE and GATE pins.
- The high current path of for this solution is through the MOSFET, therefore it is important to use thick traces for source and drain of the MOSFET to minimize resistive losses.
- The charge pump capacitor across VCAP and SOURCE pins must be kept away from the MOSFET to lower the thermal effects on the capacitance value.
- The Gate pin of the LM74500-Q1 must be connected to the MOSFET gate with short trace. Avoid excessively thin and long running trace to the Gate Drive.

11.2 Layout Example

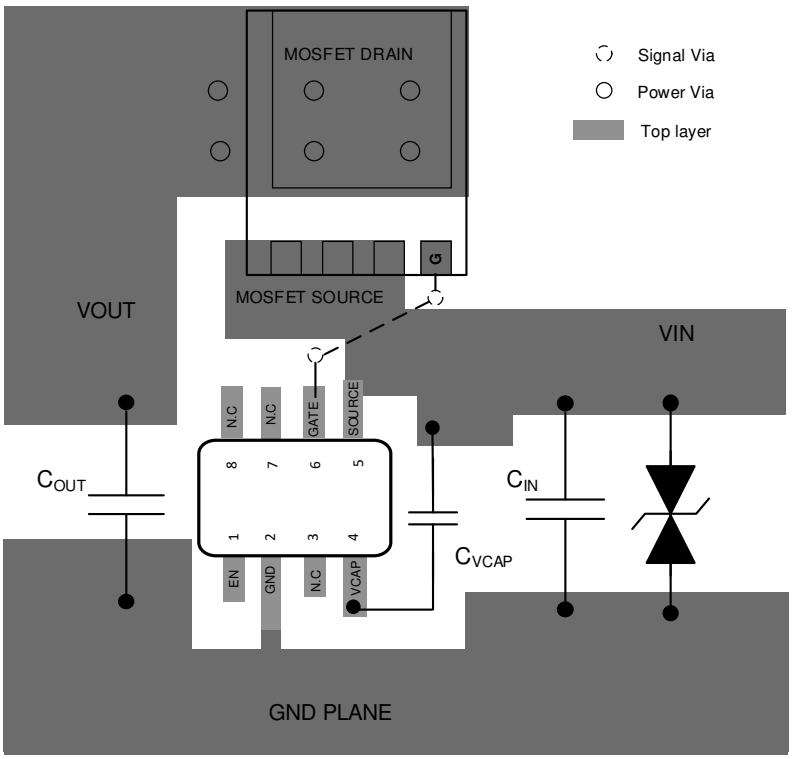


Figure 11-1. Layout Example

Copyright © 2020 Texas Instruments Incorporated

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

Copyright © 2020 Texas Instruments Incorporated

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Copyright © 2020 Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM74500QDDFRQ1	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	745F	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

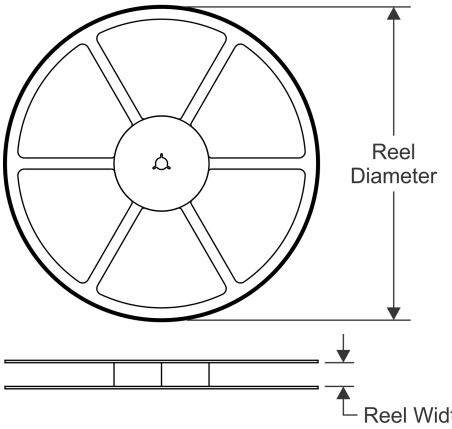
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

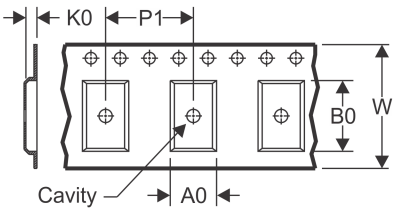
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

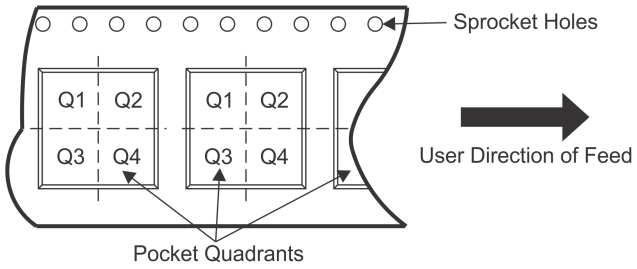


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

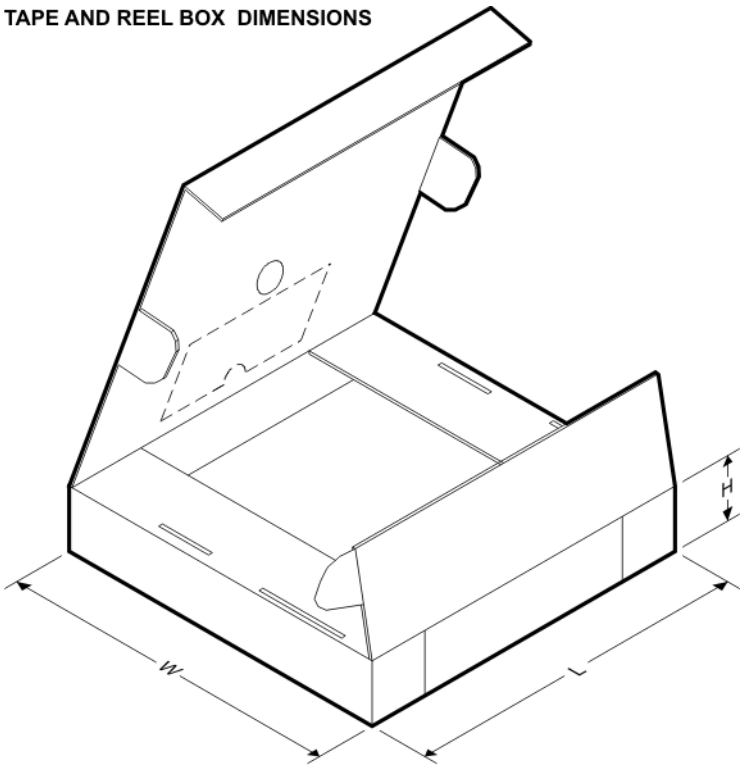
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM74500QDDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

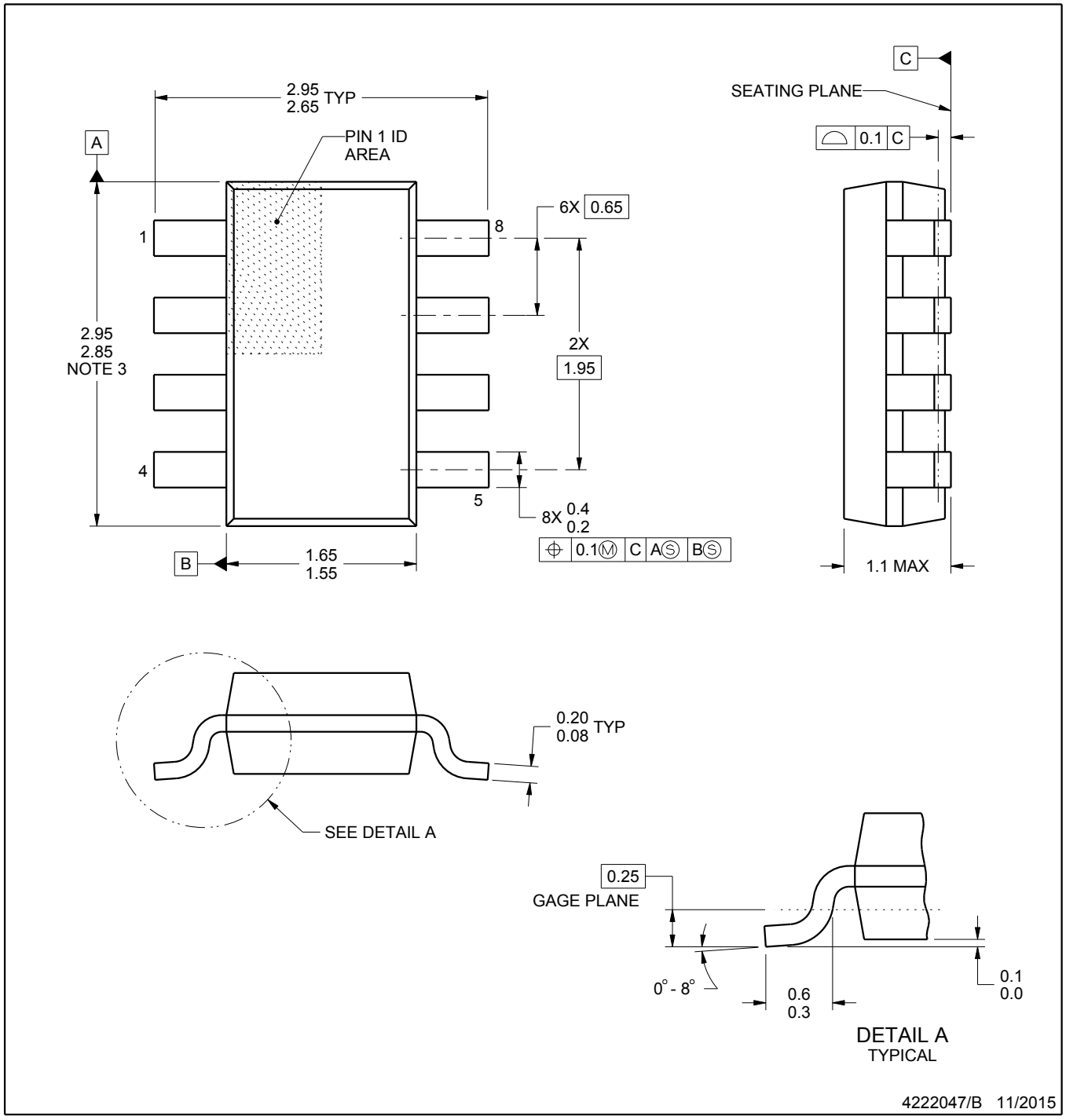
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM74500QDDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DDF0008A

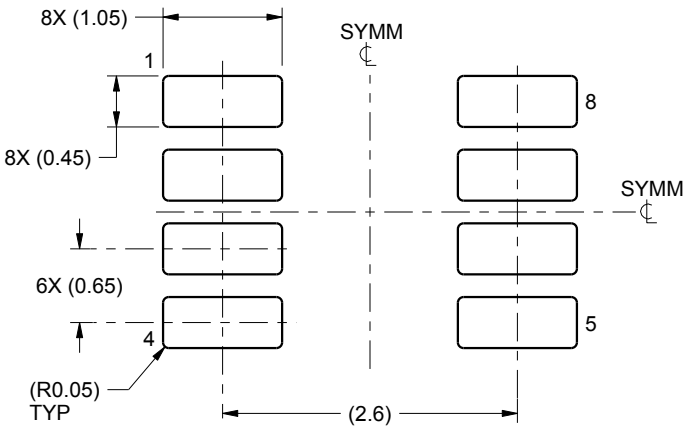
SOT-23 - 1.1 mm max height

PLASTIC SMALL OUTLINE

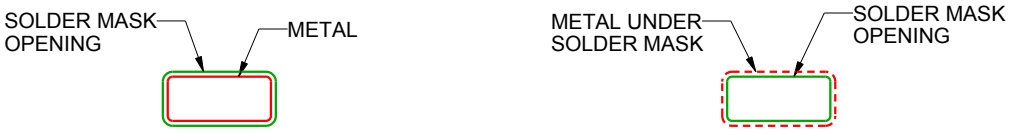


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
SCALE:15X



NON SOLDER MASK
DEFINED

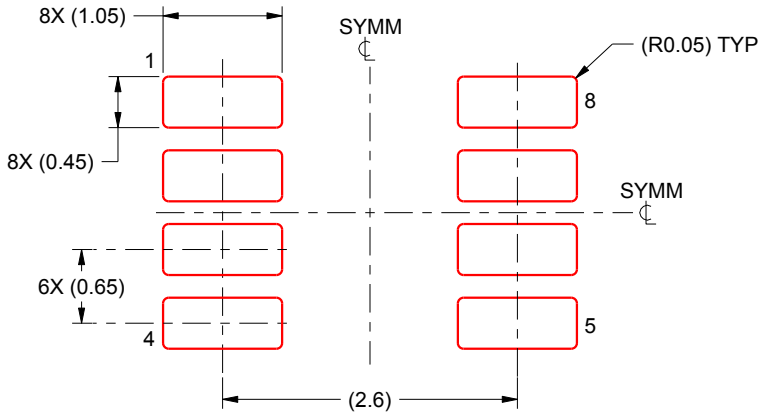
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4222047/B 11/2015

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/B 11/2015

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (https:www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2021, Texas Instruments Incorporated