# *Dual Full-Bridge PWM Motor Driver*

## Last Time Buy

This part is in production but has been determined to be LAST TIME BUY. This classification indicates that the product is obsolete and notice has been given. Sale of this device is currently restricted to existing customer applications. The device should not be purchased for new design applications because of obsolescence in the near future. Samples are no longer available.

Date of status change: May 3, 2010

Deadline for receipt of LAST TIME BUY orders: October 29, 2010

**Recommended Substitutions:**

*For existing customer transition, and for new customers or new applications, contact Allegro Sales.*

NOTE: For detailed information on purchasing options, contact your local Allegro field applications engineer or sales representative.

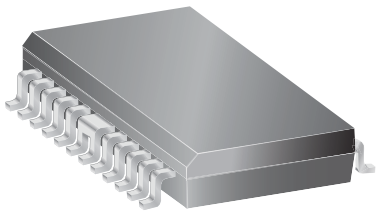
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# *Dual Full-Bridge PWM Motor Driver*

## Features and Benefits

- 750 mA continuous output current
- 45 V output sustaining voltage
- Internal clamp diodes
- Internal PWM current control
- Low output saturation voltage
- Internal thermal shutdown circuitry
- Half- or quarter-step operation of bipolar stepper motors

## Package: 24-pin SOIC with exposed thermal tabs (suffix LB)



*Not to scale*

## Description

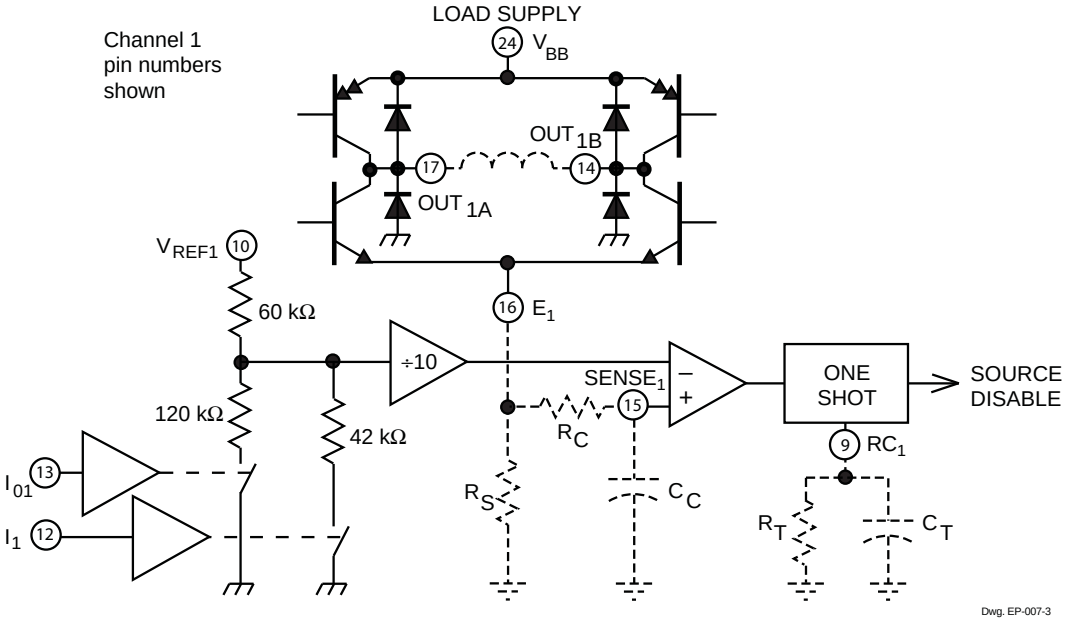
The A2919 motor driver is designed to drive both windings of a bipolar stepper motor or bidirectionally control two DC motors. Both bridges are capable of sustaining 45 V and include internal pulse width modulation (PWM) control of the output current to 750 mA. The outputs have been optimized for a low output-saturation voltage drop (less than 1.8 V total source plus sink at 500 mA).

For PWM current control, the maximum output current is determined by the user's selection of a reference voltage and sensing resistor. Two logic-level inputs select output current limits of 0%, 41%, 67%, or 100% of the maximum level. A PHASE input to each bridge determines load current direction.

The bridges include both ground clamp and flyback diodes for protection against inductive transients. Internally generated delays prevent crossover currents when switching current direction. Special power-up sequencing is not required. Thermal protection circuitry disables the outputs if the chip temperature exceeds safe operating limits.

*Continued on the next page…*

## PWM Control Circuitry



### Description (continued)

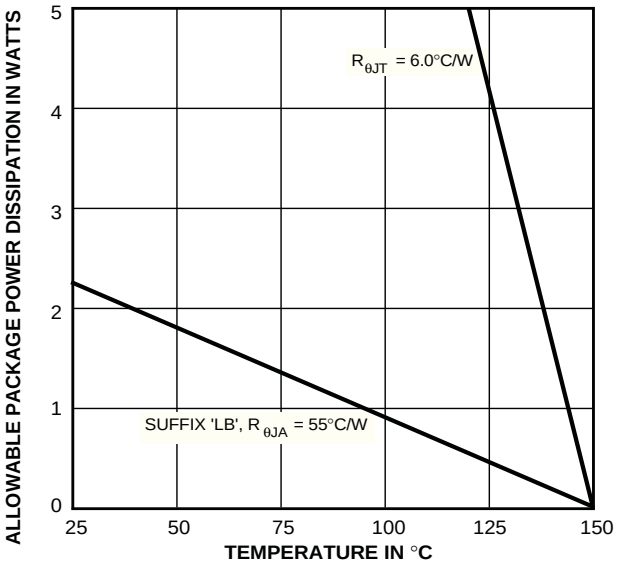
The A2919 is supplied in a 24-pin surface-mountable SOICW with heat sinkable tabs for improved power dissipation capabilities . This batwing construction provides for maximum package power dissipation in the smallest possible construction. The A2919 is available for operation from -20°C to 85°C, and are also available on special order for operation to +125°C.

### Selection Guide

| Part Number | Packing | Package |
|---|---|---|
| A2919SLBTR-T | 1000 pieces per reel | 24-pin SOICW with exposed thermal tabs |

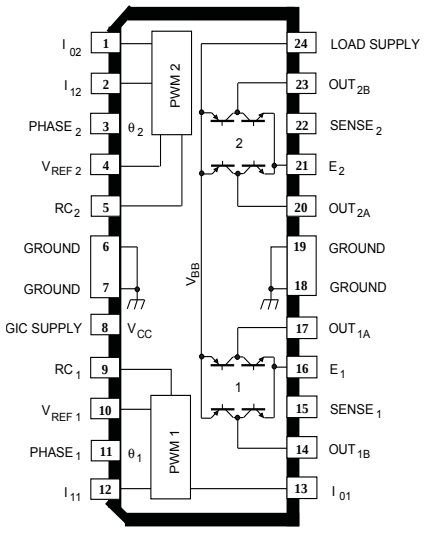
### Absolute Maximum Ratings

| Characteristic | Symbol | Notes | | Rating | Units |
|---|---|---|---|---|---|
| Logic Supply Voltage | $V_{CC}$ | | | 7.0 | V |
| Logic Input Voltage Range | $V_{IN}$ | | | –0.3 to $V_{CC}$+0.3 | V |
| Motor Supply Voltage | $V_{BB}$ | | | 45 | V |
| Output Emitter Voltage | $V_E$ | | | 1.5 | V |
| Output Current | $I_{OUT}$ | Output current rating may be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified peak current rating or a junction temperature of +150°C. | Peak, $t_w \le 20$ µs | ±1.0 | A |
| | | | Continuous | ±750 | mA |
| Package Power Dissipation | $P_D$ | See graph | | – | – |
| Operating Ambient Temperature | $T_A$ | Range S | | –20 to 85 | ºC |
| Maximum Junction Temperature | $T_J$(max) | | | 150 | ºC |
| Storage Temperature | $T_{stg}$ | | | –55 to 150 | ºC |




Dwg. GP-049A

### Pin-out Diagram




Dwg. PP-047

**ELECTRICAL CHARACTERISTICS at $T_A$ = +25°C, $T_J \leq$ 150°C, $V_{BB}$ = 45 V, $V_{CC}$ = 4.75 V to 5.25 V, $V_{REF}$ = 5.0 V (unless otherwise noted).**

| Characteristic | Symbol | Test Conditions | Limits | | | |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | Units |
| **Output Drivers ($OUT_A$ or $OUT_B$)** | | | | | | |
| Motor Supply Range | $V_{BB}$ | Operating | 10 | — | 45 | V |
| Output Leakage Current | $I_{CEX}$ | $V_{OUT}$ = $V_{BB}$ | — | < 1.0 | 50 | µA |
| | | $V_{OUT}$ = 0 | — | <-1.0 | -50 | µA |
| Output Sustaining Voltage | $V_{CE(sus)}$ | $I_{OUT}$ = ±750 mA, L = 3.0 mH | 45 + $V_F$ | — | — | V |
| Output Saturation Voltage | $V_{CE(SAT)}$ | Sink Driver, $I_{OUT}$ = +500 mA | — | 0.4 | 0.6 | V |
| | | Sink Driver, $I_{OUT}$ = +750 mA | — | 1.0 | 1.2 | V |
| | | Source Driver, $I_{OUT}$ = -500 mA | — | 1.0 | 1.2 | V |
| | | Source Driver, $I_{OUT}$ = -750 mA | — | 1.3 | 1.5 | V |
| Clamp Diode Leakage Current | $I_R$ | $V_R$ = 45 V | — | < 1.0 | 50 | µA |
| Clamp Diode Forward Voltage | $V_F$ | $I_F$ = 750 mA | — | 1.6 | 2.0 | V |
| Driver Supply Current | $I_{BB(ON)}$ | Both Bridges ON, No Load | — | 20 | 25 | mA |
| | $I_{BB(OFF)}$ | Both Bridges OFF | — | 5.0 | 10 | mA |
| **Control Logic** | | | | | | |
| Input Voltage | $V_{IN(1)}$ | All inputs | 2.4 | — | — | V |
| | $V_{IN(0)}$ | All inputs | — | — | 0.8 | V |
| Input Current | $I_{IN(1)}$ | $V_{IN}$ = 2.4 V | — | <1.0 | 20 | µA |
| | | $V_{IN}$ = 0.8 V | — | - 3.0 | -200 | µA |
| Reference Voltage Range | $V_{REF}$ | | 1.0 | — | 7.5 | V |
| Current Limit Threshold (at trip point) | $V_{REF}/V_{SENSE}$ | $I_0$ = $I_1$ = 0.8 V, $V_{REF}$ = 1.0 V to 7.5 V | 9.5 | 10 | 10.5 | — |
| | | $I_0$ = 2.4 V, $I_1$ = 0.8 V, $V_{REF}$ = 1.5 V to 7.5 V | 13.5 | 15 | 16.5 | — |
| | | $I_0$ = 0.8 V, $I_1$ = 2.4 V, $V_{REF}$ = 1.5 V to 7.5 V | 20.7 | 24.4 | 28.0 | — |
| Thermal Shutdown Temperature | $T_J$ | | — | 170 | — | °C |
| Total Logic Supply Current | $I_{CC(ON)}$ | $I_0$ = $I_1$ = 0.8 V, No Load | — | 40 | 50 | mA |
| | $I_{CC(OFF)}$ | $I_0$ = $I_1$ = 2.4 V, No Load | — | 10 | 12 | mA |
| Total Reference Current | $I_{REF1}$ + $I_{REF2}$ | $V_{REF1}$ = $V_{REF2}$ = 7.5 V, $I_0$ = $I_1$ = 2.4 V | 140 | 185 | 250 | µA |
| Fixed Off-Time | $t_{off}$ | $R_T$ = 56 kΩ, $C_T$ = 820 pF | — | 46 | — | µs |

## APPLICATIONS INFORMATION

### PWM CURRENT CONTROL

The A2919 dual bridges are designed to drive both windings of a bipolar stepper motor. Output current is sensed and controlled independently in each bridge by an external sense resistor ($R_S$), internal comparator, and monostable multivibrator.

When the bridge is turned ON, current increases in the motor winding and flows through the external sense resistor until the sense voltage ($V_S$) reaches the level set at the comparator input:

$$I_{TRIP} = V_{REF}/10\ R_S$$

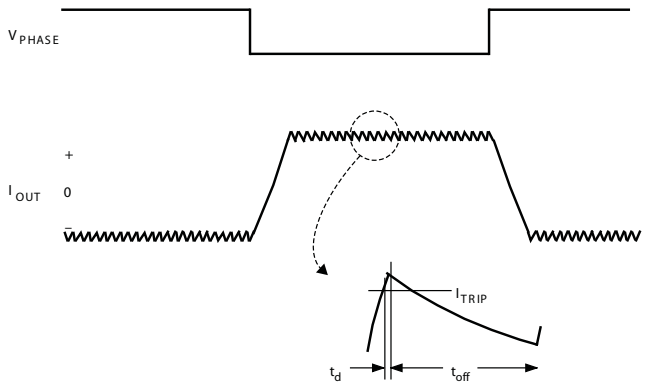
The comparator then triggers the monostable, which turns off the source driver of the bridge. The actual load current peak will be slightly higher than the trip point (especially for low-inductance loads) because of the internal logic and switching delays. This delay ($t_d$) is typically 2 µs. After turn-off, the motor current decays, circulating through the ground-clamp diode and sink transistor. The source driver off-time (and therefore the magnitude of the current decrease) is determined by the monostable external RC timing components, where $t_{off} = R_T C_T$ within the range of 20 kΩ to 100 kΩ and 100 pF to 1000 pF.

The fixed off-time should be short enough to keep the current chopping above the audible range (< 46 µs) and long enough to properly regulate the current. Because only slow-decay current control is available, short off times (< 10 µs) require additional efforts to ensure proper current regulation. Factors that can negatively affect the ability to properly regulate the current when using short off times include: higher motor-supply voltage, light load, and longer than necessary blank time.

When the source driver is re-enabled, the winding current (the sense voltage) is again allowed to rise to the comparator's threshold. This cycle repeats itself, maintaining the average motor winding current at the desired level.

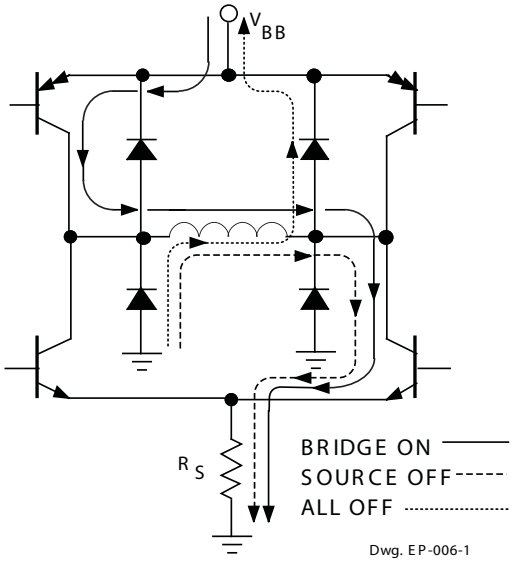
Loads with high distributed capacitances may cause current spikes capable of tripping the comparator, resulting in erroneous current control. An external $R_C C_C$ time delay should be used to delay the action of the comparator. Depending on load type, many applications will not require these external components (SENSE connected to E).

**PWM OUTPUT CURRENT WAVE FORM**




Dwg. WM-003-1A

**LOAD CURRENT PATHS**




Dwg. EP-006-1

## LOGIC CONTROL OF OUTPUT CURRENT

Two logic level inputs ($l_0$ and $I_1$) allow digital selection of the motor winding current at 100%, 67%, 41%, or 0% of the maximum level per the table. The 0% output current condition turns off all drivers in the bridge and can be used as an output enable function.

### CURRENT-CONTROL TRUTH TABLE

| $I_0$ | $I_1$ | Output Current |
|---|---|---|
| L | L | $V_{REF}/10\ R_S$ = 100% $I_{TRIP}$ |
| H | L | $V_{REF}/15\ R_S$ = 67% $I_{TRIP}$ |
| L | H | $V_{REF}/24.4\ R_S$ = 41% $I_{TRIP}$ |
| H | H | 0 |

These logic level inputs greatly enhance the implementation of µP-controlled drive formats.

During half-step operations, $l_0$ and $l_1$ allow the µP to control the motor at a constant torque between all positions in an eight-step sequence. This is accomplished by digitally selecting 100% drive current when only one phase is on and 67% drive current when two phases are on. Logic highs on both $l_0$ and $l_1$ turn off all drivers to allow rapid current decay.

During quarter-step operation, $I_0$ and $I_1$ allow the µP to control the motor position in a sixteen-step sequence. This is accomplished by digitally selecting drive current as shown in the table (for one quadrant of operation). Logic highs on both $I_0$ and $I_1$ turn off all drivers to allow rapid current decay.

The logic control inputs can also be used to select a reduced current level (and reduced power dissipation) for 'hold' conditions and/or increased current (and available torque) for start-up conditions.

### QUARTER-STEPPING CURRENT CONTROL

| Phase 1 Current Level | Phase 2 Current Level |
|---|---|
| 100% | 0% |
| 100% | 41% |
| 67% | 67% |
| 41% | 100% |
| 0% | 100% |

## GENERAL

The PHASE input to each bridge determines the direction motor winding current flows. An internally generated deadtime (approximately 2 µs) prevents crossover currents that can occur when switching the PHASE input.

All four drivers in the bridge output can be turned off between steps ($l_0 = l_1$ ž 2.4 V) resulting in a fast current decay through the internal output clamp and flyback diodes. The fast current decay is desirable in half-step and high-speed applications. The PHASE, $l_0$, and $I_1$ inputs float high.

Varying the reference voltage ($V_{REF}$) provides continuous control of the peak load current for micro-stepping applications.

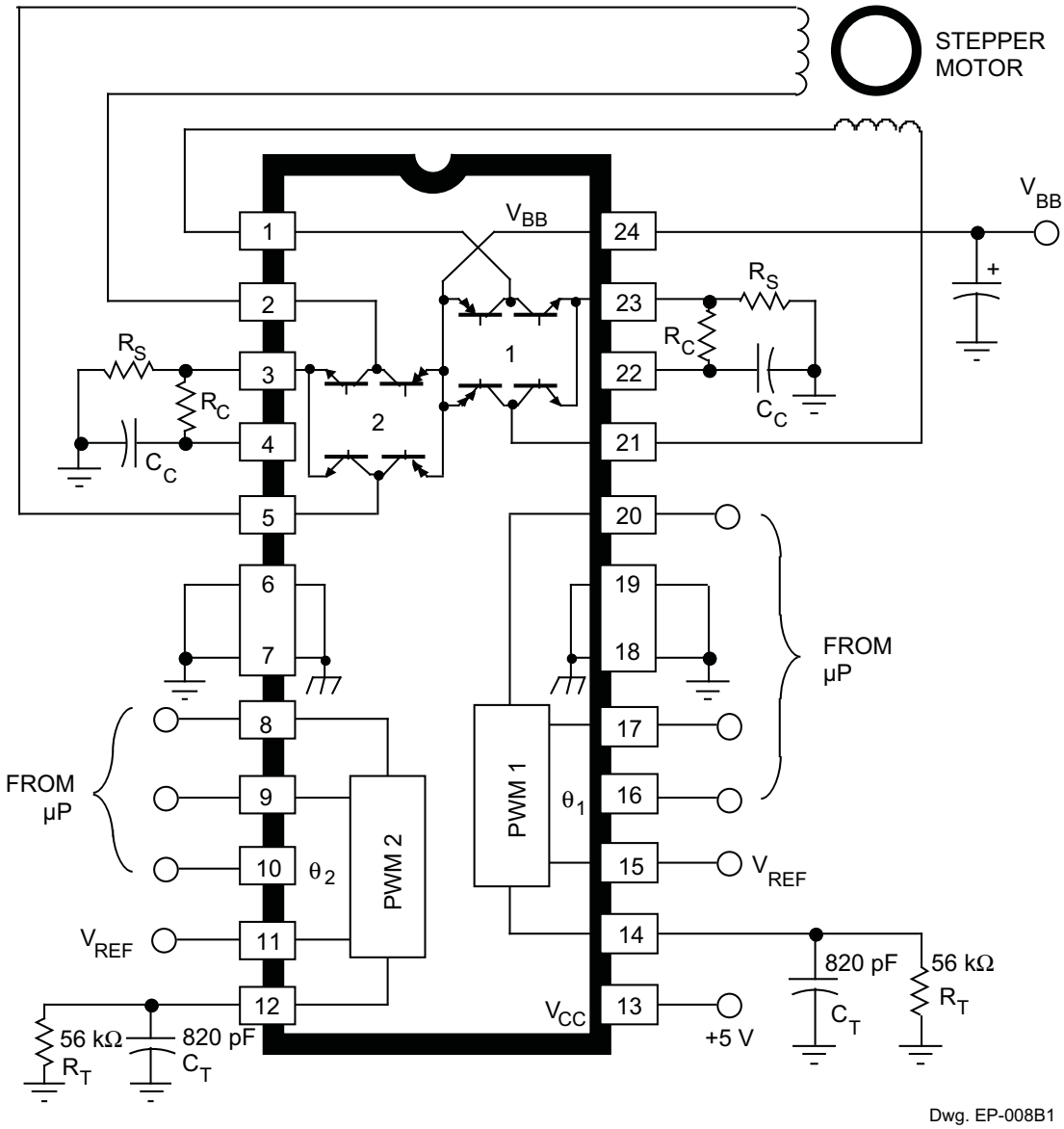
Thermal protection circuitry turns off all drivers when the junction temperature reaches +170°C. It is only intended to protect the device from failures due to excessive junction temperature and should not imply that output short circuits are permitted. The output drivers are re-enabled when the junction temperature cools to +145°C.

The A2919 output drivers are optimized for low output saturation voltages—less than 1.8 V total (source plus sink) at 500 mA. Under normal operating conditions, when combined with the excellent thermal properties of the batwing package design, this allows continuous operation of both bridges simultaneously at 500 mA.

### TRUTH TABLE

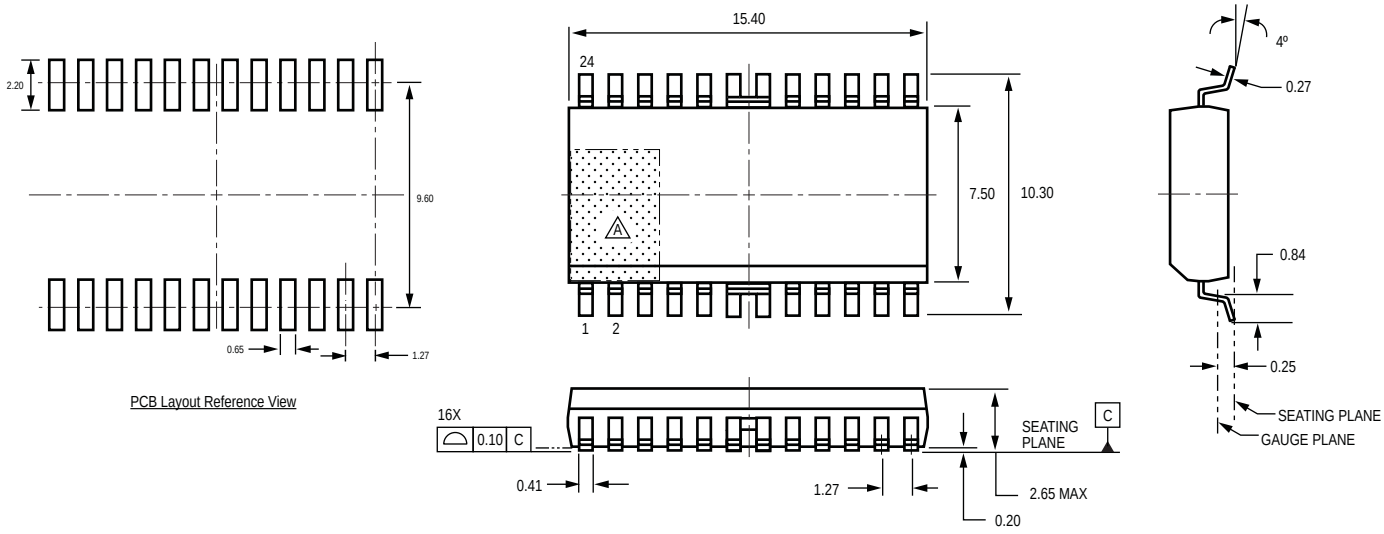
| PHASE | $OUT_A$ | $OUT_B$ |
|---|---|---|
| H | H | L |
| L | L | H |

## TYPICAL APPLICATION




Dwg. EP-008B1

## LB Package, 24-pin SOIC




All dimensions nominal, not for tooling use
Dimensions in millimeters
Pins 6 and 7, and 18 and 19 internally fused
(Reference JEDEC MS-013 AD)
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Reference pad layout (reference IPC SOIC127P1030X265-24M)
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

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