




Description

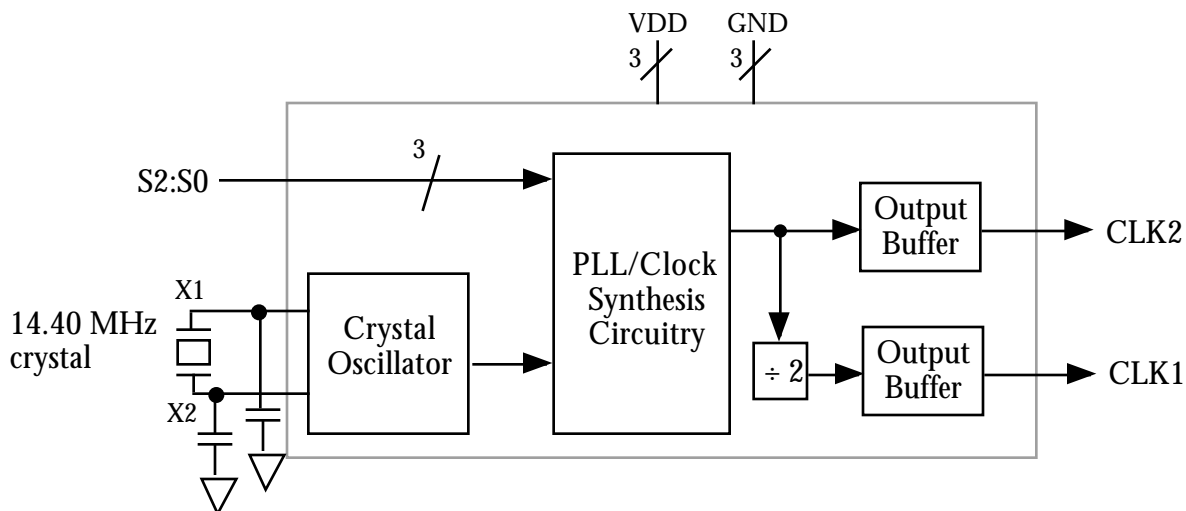
The MK2731-04 is a low cost, low jitter, high performance clock synthesizer designed to replace expensive discrete clock oscillators in MPEG audio applications. Using ICS/MicroClock's patented analog/digital Phase-Locked Loop (PLL) techniques, the device uses an inexpensive 14.4 MHz crystal input to produce all of the popular audio sampling frequencies.

ICS manufactures the largest variety of Set-Top Box and multimedia clock synthesizers for all applications. Consult ICS to eliminate VCXOs, crystals and oscillators from your board.

Features

- Packaged in 16 pin narrow SOIC 
- Replaces multiple oscillators
- 3.3V or 5V operation
- Uses an inexpensive 14.4 MHz crystal
- Supports 32 kHz, 44.1 kHz, 48 kHz, and 96 kHz audio sampling rates
- Has 256x, 384x, and 512x sampling rates - compatible with every popular audio DAC
- Zero ppm synthesis error
- 25 mA output drive capability at TTL levels
- Advanced, low power, sub-micron CMOS process

Block Diagram



**Pin Assignment**

MK2731-04

X2	□ 1	16	□ DC
X1	□ 2	15	□ DC
VDD	□ 3	14	□ S0
VDD	□ 4	13	□ S1
GND	□ 5	12	□ DC
GND	□ 6	11	□ CLK2
GND	□ 7	10	□ VDD
S2	□ 8	9	□ CLK1

16 pin narrow (150 mil) SOIC

Output Clocks Select Table (MHz)

S2	S1	S0	CLK1	CLK2
Pin 8	Pin 13	Pin 14	Pin 9	Pin 11
0	0	0	16.9344	33.8688
0	0	1	11.2896	22.5792
0	1	0	8.192	16.384
0	1	1	18.432	36.864
1	0	0	11.2896	22.5792
1	0	1	12.288	24.576
1	1	0	Test	Test
1	1	1	Test	Test

Key: 0 = connect directly to GND
1 = connect directly to VDD**Pin Descriptions**

Number	Name	Type	Description
1	X2	XO	Crystal connection. Connect to a parallel mode 14.4 MHz crystal.
2	X1	XI	Crystal connection. Connect to a parallel mode 14.4 MHz crystal.
3, 4, 10	VDD	P	Connect to +3.3V or +5V. Must be same at all VDDs.
5, 6, 7	GND	P	Connect to ground.
8	S2	I	Frequency select pin 2. Determines clock outputs per table above.
9	CLK1	O	Clock output 1 set by status of S0-S2. See table above. This output is CLK2/2
11	CLK2	O	Clock output 2 set by status of S0-S2. See table above.
12, 15, 16	DC	-	Don't Connect. Do not connect anything to these pins.
13	S1	I	Frequency select pin 1. Determines clock outputs per table above.
14	S0	I	Frequency select pin 0. Determines clock outputs per table above.

Key: I = Input with internal pull-up resistor; O = output; P = power supply connection; XI, XO = crystal connections

External Components

The MK2731-04 requires a minimum number of external components for proper operation. Decoupling capacitors of 0.01μF should be connected between VDD and GND on pins 3 and 5, and VDD and GND on pins 10 and 6, as close to the MK2731-04 as possible. Other VDDs can be connected to pin 10. A series termination resistor of 33 Ω may be used for each clock output. Any unused clock outputs should be left unconnected (DC, floating). The input crystal must be connected as close to the chip as possible. The input crystal should be fundamental mode, parallel resonant. For accurate outputs, the crystal should be tuned with two identical capacitors to ground, as shown on the block diagram. The value of these two crystal caps should be equal to $(C_L - 6) * 2$, where C_L is the crystal load (or correlation) capacitance.

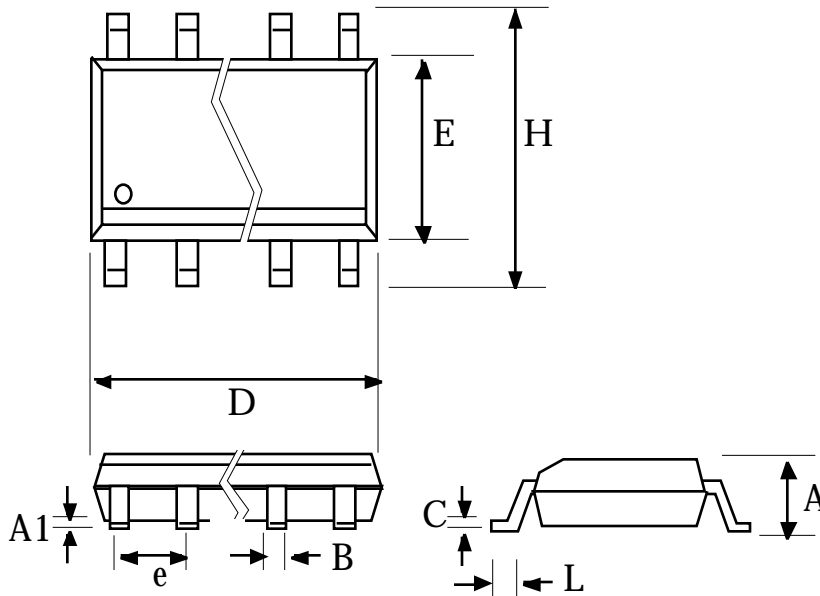
**Electrical Specifications**

Parameter	Conditions	Minimum	Typical	Maximum	Units
ABSOLUTE MAXIMUM RATINGS (note 1)					
Supply voltage, VDD	Referenced to GND			7	V
Inputs and Clock Outputs	Referenced to GND	-0.5		VDD+0.5	V
Ambient Operating Temperature		0		70	°C
Soldering Temperature	Max of 10 seconds			260	°C
Storage temperature		-65		150	°C
DC CHARACTERISTICS (VDD = 3.3V unless noted)					
Operating Voltage, VDD		3.00	5.0	5.50	V
Input High Voltage, VIH, X1 pin only		(VDD/2)+1	VDD/2		V
Input Low Voltage, VIL, X1 pin only			VDD/2	(VDD/2)-1	V
Input High Voltage, VIH		2			V
Input Low Voltage, VIL				0.8	V
Output High Voltage, VOH	IOH=-12mA	2.4			V
Output Low Voltage, VOL	IOL=12mA			0.4	V
Output High Voltage, VOH, CMOS level	IOH=-4mA	VDD-0.4			V
Operating Supply Current, IDD	No Load		10		mA
Short Circuit Current	Each output		±50		mA
Input Capacitance	S0, S1, S2		7		pF
Frequency synthesis error	Both clocks			0	ppm
AC CHARACTERISTICS (VDD = 3.3V unless noted)					
Input Crystal Frequency			14.40		MHz
Output Clock Rise Time	0.8 to 2.0V			1.5	ns
Output Clock Fall Time	2.0 to 0.8V			1.5	ns
Output Clock Duty Cycle	At VDD/2	40		60	%
Maximum Absolute Jitter, short term	11.288MHz, VDD=5V		±65		ps
	11.288MHz, VDD=3.3V		±85		ps

Note: 1. Stresses beyond those listed under Absolute Maximum Ratings could cause permanent damage to the device. Prolonged exposure to levels above the operating limits but below the Absolute Maximums may affect device reliability.

**Package Outline and Package Dimensions**

(For current dimensional specifications, see JEDEC Publication No. 95.)

**16 pin narrow SOIC**

Symbol	SOIC	
	Min	Max
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	9.80	10.00
E	3.80	4.00
H	5.80	6.20
e	1.27 BSC	
h	0.25	0.50
L	0.40	1.27

All dimensions in mm.

Ordering Information

Part/Order Number	Marking	Shipping packaging	Package	Temperature
MK2731-04S	MK2731-04S	tubes	16 pin SOIC	0-70 °C
MK2731-04STR	MK2731-04S	tape and reel	16 pin SOIC	0-70 °C

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