DUAL N-CHANNEL AND DUAL P-CHANNEL MATCHED MOSFET PAIR

GENERAL DESCRIPTION

The ALD1103 is a monolithic dual N-channel and dual P-channel matched transistor pair intended for a broad range of analog applications. These enhancement-mode transistors are manufactured with Advanced Linear Devices' enhanced ACMOS silicon gate CMOS process. It consists of an ALD1101 N-channel MOSFET pair and an ALD1102 P-channel MOSFET pair in one package.

The ALD1103 offers high input impedance and negative current temperature coefficient. The transistor pair is matched for minimum offset voltage and differential thermal response, and it is designed for precision signal switching and amplifying applications in +2V to +12V systems where low input bias current, low input capacitance and fast switching speed are desired. Since these are MOSFET devices, they feature very large (almost infinite) current gain in a low frequency, or near DC, operating environment. When used in pairs, a dual CMOS analog switch can be constructed. In addition, the ALD1103 is intended as a building block for differential amplifier input stages, transmission gates, and multiplexer applications.

The ALD1103 is suitable for use in precision applications which require very high current gain, beta, such as current mirrors and current sources. The high input impedance and the high DC current gain of the Field Effect Transistors result in extremely low current loss through the control gate. The DC current gain is limited by the gate input leakage current, which is specified at 50pA at room temperature. For example, DC beta of the device at a drain current of 5mA at 25°C is = 5mA/50pA = 100,000,000.

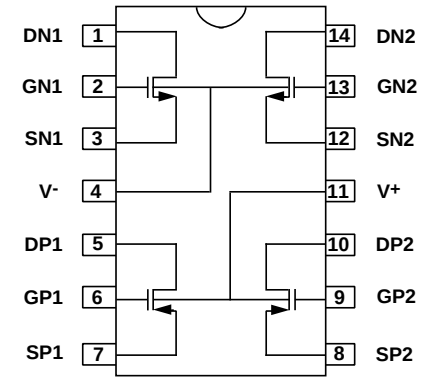
FEATURES

- Thermal tracking between N-channel and P-channel pairs
- Low threshold voltage of 0.7V for both N-channel & P-channel MOSFETS
- Low input capacitance
- Low Vos -- 10mV
- High input impedance -- $10^{13}\Omega$ typical
- Low input and output leakage currents
- Negative current (I_{DS}) temperature coefficient
- Enhancement mode (normally off)
- DC current gain 10^9
- Matched N-channel and matched P-channel in one package

APPLICATIONS

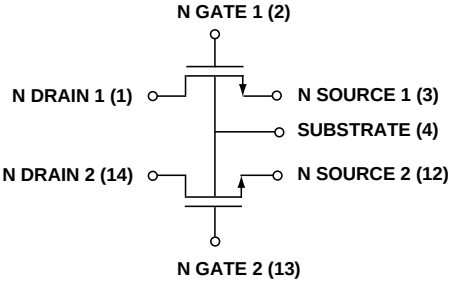
- Precision current mirrors
- Complementary push-pull linear drives
- Analog switches
- Choppers
- Differential amplifier input stage
- Voltage comparator
- Data converters
- Sample and Hold
- Analog inverter
- Precision matched current sources

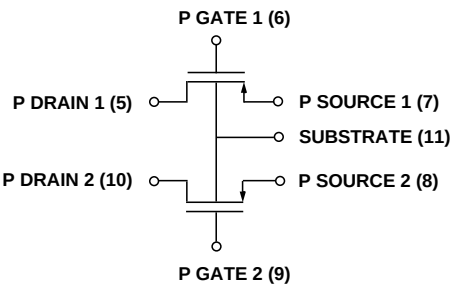
PIN CONFIGURATION



DB, PB, SB PACKAGE

BLOCK DIAGRAM





ORDERING INFORMATION

Operating Temperature Range*		
-55°C to +125°C	0°C to +70°C	0°C to +70°C
14-Pin CERDIP Package	14-Pin Plastic Dip Package	14-Pin SOIC Package
ALD1103 DB	ALD1103 PB	ALD1103 SB

* Contact factory for industrial temperature range.

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ABSOLUTE MAXIMUM RATINGS

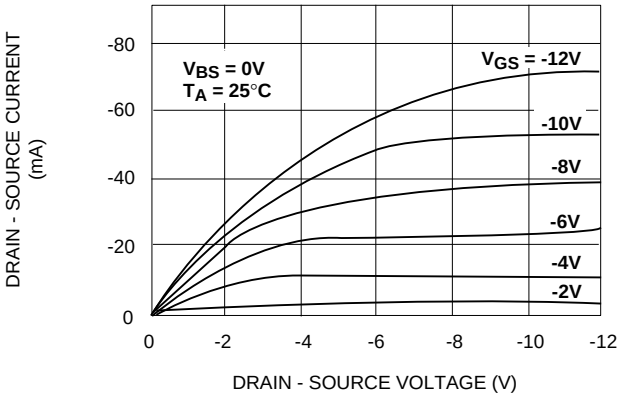
Drain-source voltage, V_{DS} — 13.2V
Gate-source voltage, V_{GS} — 13.2V
Power dissipation — 500 mW
Operating temperature range PB, SB package — 0°C to +70°C
DB package — -55°C to +125°C
Storage temperature range — -65°C to +150°C
Lead temperature, 10 seconds — +260°C

OPERATING ELECTRICAL CHARACTERISTICS
T_A = 25°C unless otherwise specified

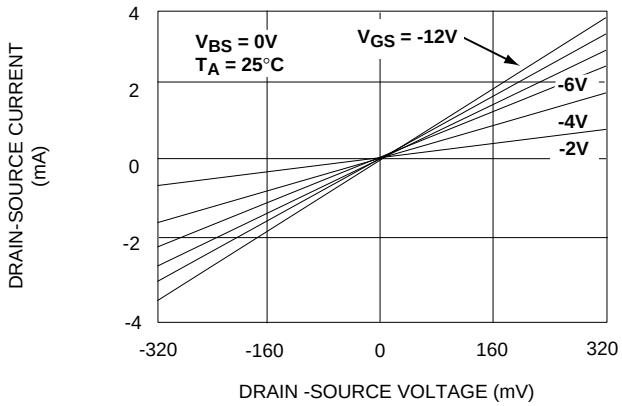
		N - Channel					P - Channel				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Gate Threshold Voltage	V_T	0.4	0.7	1.0	V	I_{DS} = 10µA V_{GS} = V_{DS}	-0.4	-0.7	-1.2	V	I_{DS} = -10µA V_{GS} = V_{DS}
Offset Voltage V_{GS1} - V_{GS2}	V_{OS}			10	mV	I_{DS} = 100µA V_{GS} = V_{DS}			10	mV	I_{DS} = -100µA V_{GS} = V_{DS}
Gate Threshold Temperature Drift	TC_{VT}		-1.2		mV/°C			-1.3		mV/°C	
On Drain Current	$I_{DS\ (ON)}$	25	40		mA	V_{GS} = V_{DS} = 5V	-8	-16		mA	V_{GS} = V_{DS} = -5V
Trans-. conductance	G_{fs}	5	10		mmho	V_{DS} = 5V I_{DS}= 10mA	2	4		mmho	V_{DS} = -5V I_{DS}= -10mA
Mismatch	ΔG_{fs}		0.5		%			0.5		%	
Output Conductance	G_{OS}		200		µmho	V_{DS} = 5V I_{DS} = 10mA		500		µmho	V_{DS} = -5V I_{DS} = -10mA
Drain Source ON Resistance	$R_{DS(ON)}$		50	75	Ω	V_{DS} = 0.1V V_{GS} = 5V		180	270	Ω	V_{DS} = -0.1V V_{GS} = -5V
Drain Source ON Resistance Mismatch	$\Delta R_{DS(ON)}$		0.5		%	V_{DS} = 0.1V V_{GS} = 5V		0.5		%	V_{DS} = -0.1V V_{GS} = -5V
Drain Source Breakdown Voltage	BV_{DSS}	12			V	I_{DS} = 10µA V_{GS} =0V	-12			V	I_{DS} = -10µA V_{GS} =0V
Off Drain Current	$I_{DS(OFF)}$		0.1	4 4	nA µA	V_{DS} =12V I_{GS} = 0V T_A = 125°C		0.1	4 4	nA µA	V_{DS} = -12V V_{GS} = 0V T_A = 125°C
Gate Leakage Current	I_{GSS}		1	50 10	pA nA	V_{DS} = 0V V_{GS} =12V T_A = 125°C		1	50 10	pA nA	V_{DS} = 0V V_{GS} =-12V T_A = 125°C
Input Capacitance	C_{ISS}		6	10	pF			6	10	pF	

P- CHANNEL TYPICAL PERFORMANCE CHARACTERISTICS

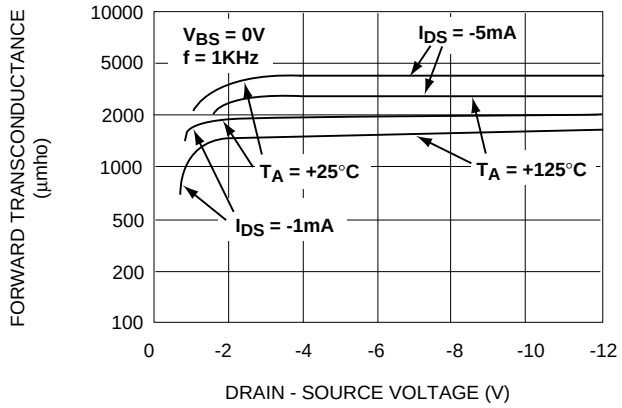
OUTPUT CHARACTERISTICS



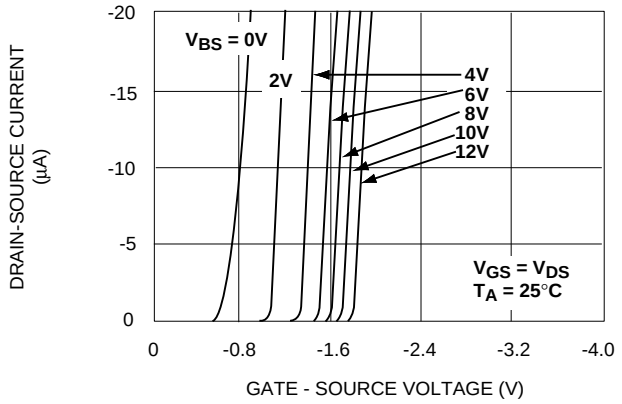
LOW VOLTAGE OUTPUT CHARACTERISTICS



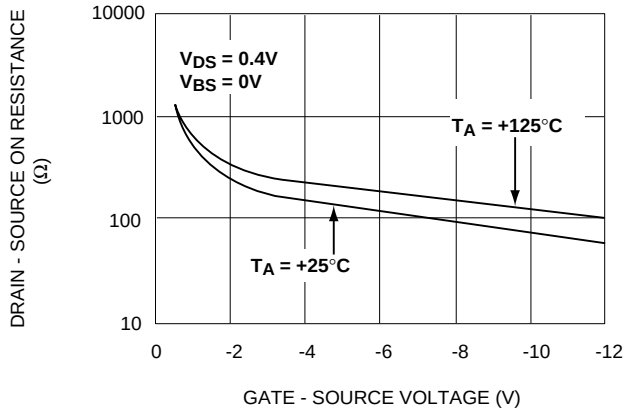
FORWARD TRANSCONDUCTANCE vs. DRAIN - SOURCE VOLTAGE



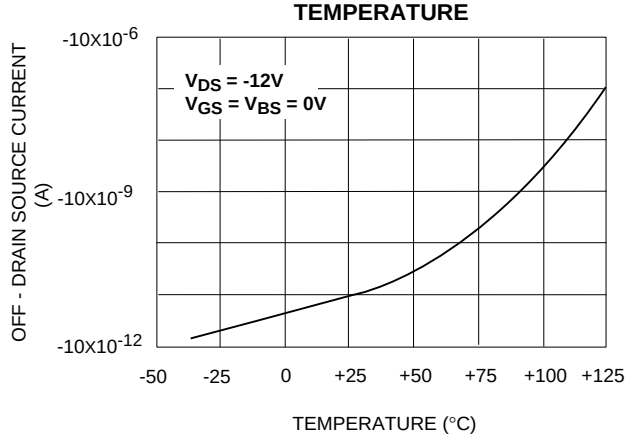
TRANSFER CHARACTERISTIC WITH SUBSTRATE BIAS



$R_{DS\ (ON)}$ vs. GATE - SOURCE VOLTAGE

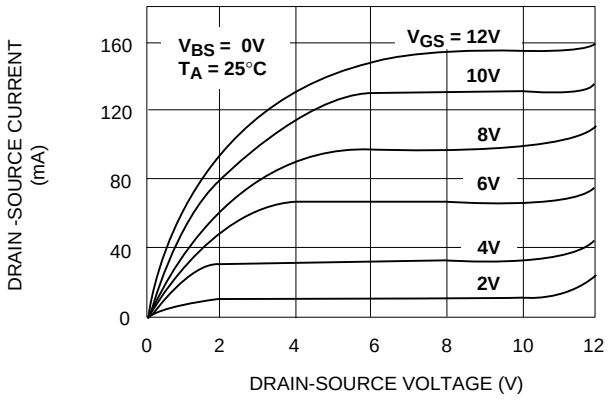


OFF DRAIN - CURRENT vs. TEMPERATURE

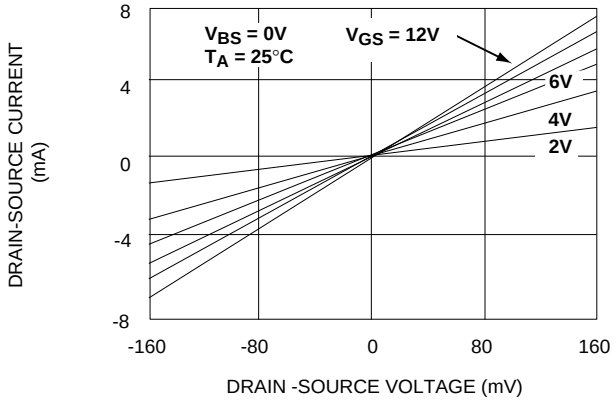


N- CHANNEL TYPICAL PERFORMANCE CHARACTERISTICS

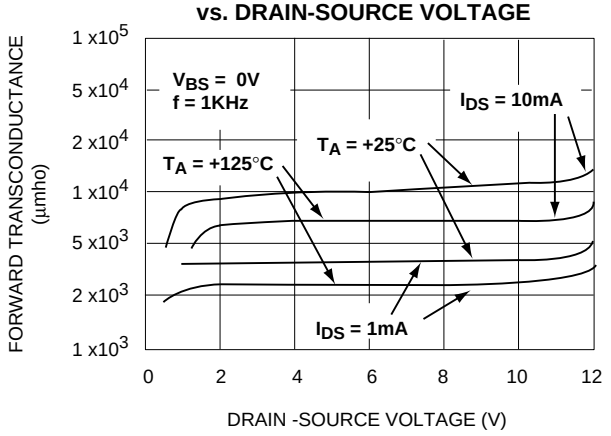
OUTPUT CHARACTERISTICS



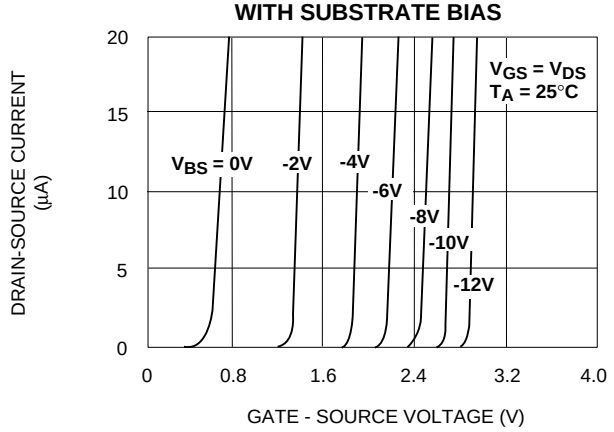
LOW VOLTAGE OUTPUT CHARACTERISTICS



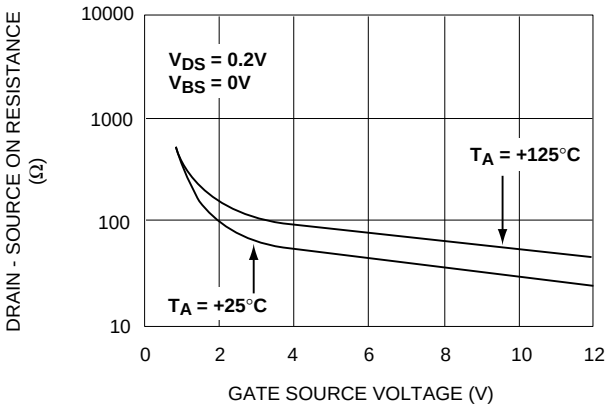
FORWARD TRANSCONDUCTANCE vs. DRAIN-SOURCE VOLTAGE



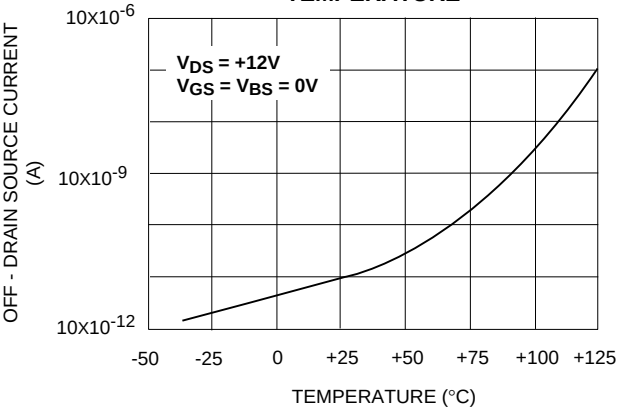
TRANSFER CHARACTERISTIC WITH SUBSTRATE BIAS



$R_{DS\ (ON)}$ vs. GATE - SOURCE VOLTAGE

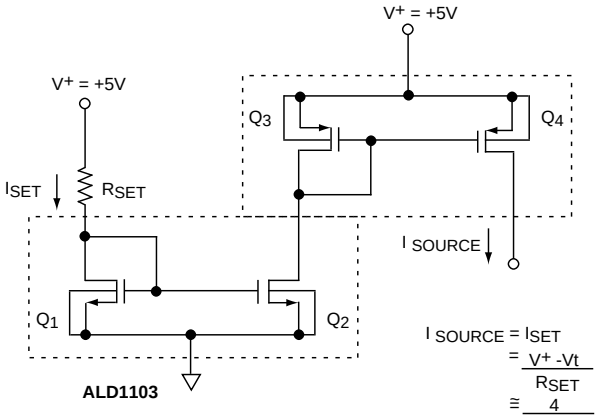


OFF DRAIN - CURRENT vs. TEMPERATURE



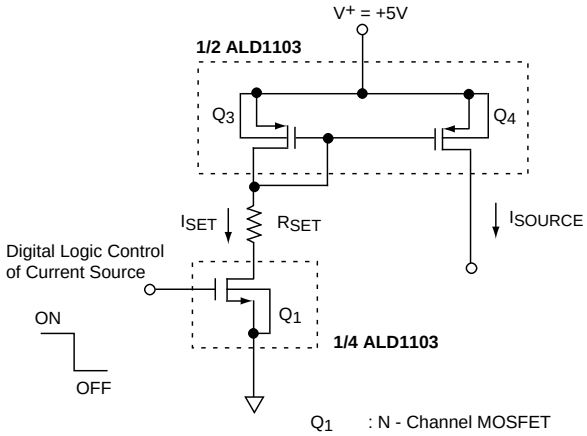
TYPICAL APPLICATIONS

CURRENT SOURCE MIRROR



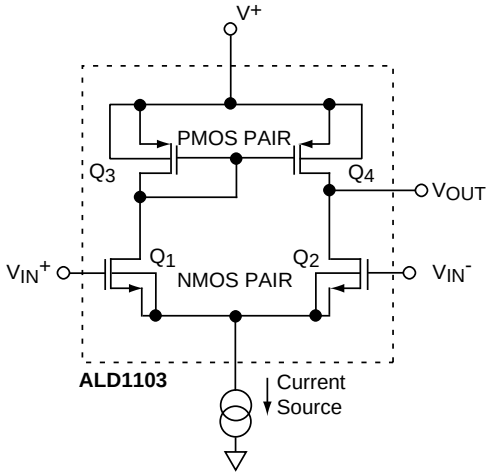
Q1, Q2: N - Channel MOSFET
Q3, Q4: P - Channel MOSFET

CURRENT SOURCE WITH GATE CONTROL



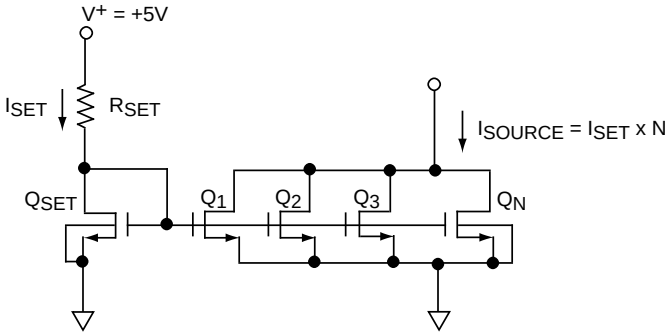
Q1 : N - Channel MOSFET
Q3,Q4 : P - Channel MOSFET

DIFFERENTIAL AMPLIFIER



Q1, Q2: N - Channel MOSFET
Q3, Q4: P - Channel MOSFET

CURRENT SOURCE MULTIPLICATION

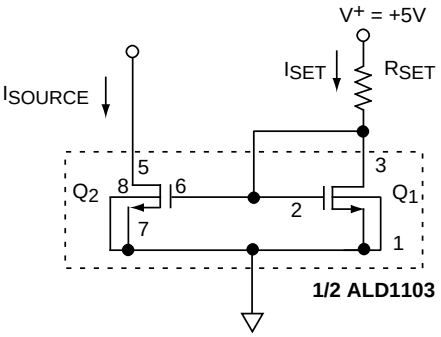


QSET, Q1..QN: ALD 1101 or ALD 1103
N - Channel MOSFET

TYPICAL APPLICATIONS

BASIC CURRENT SOURCES

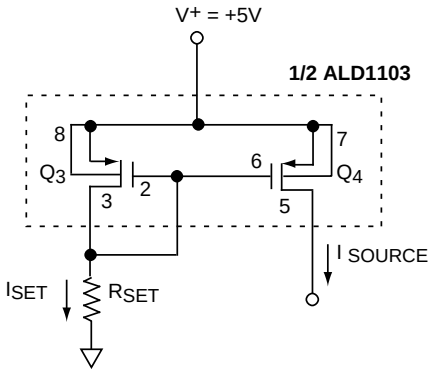
N- CHANNEL CURRENT SOURCE



$$I_{SOURCE} = I_{SET} = \frac{V^+ - Vt}{R_{SET}} \cong \frac{V^+ - 1.0}{R_{SET}} \cong \frac{4}{R_{SET}}$$

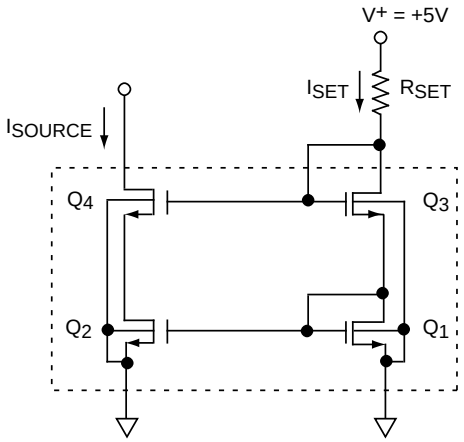
Q_1, Q_2 : N - Channel MOSFET

P- CHANNEL CURRENT SOURCE

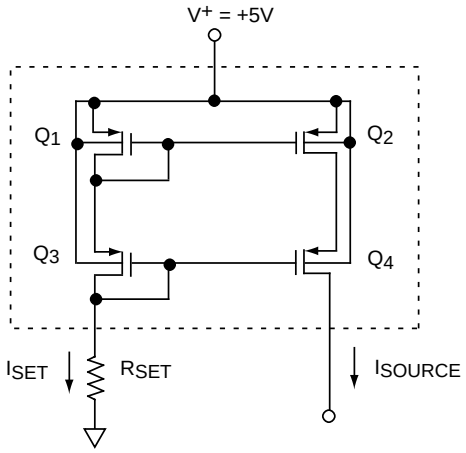


Q_3, Q_4: P - Channel MOSFET

CASCODE CURRENT SOURCES



Q_1, Q_2, Q_3, Q_4: N - Channel MOSFET
(ALD1101 or ALD1103)



$$I_{SOURCE} = I_{SET} = \frac{V^+ - 2Vt}{R_{SET}} \cong \frac{3}{R_{SET}}$$

Q1, Q2, Q3, Q4: P - Channel MOSFET
(ALD1102 or ALD1103)