

# DATA SHEET

## **74ALS645A/74ALS645A-1** Octal transceiver (3-State)

Product specification  
IC05 Data Handbook

1991 Jun 03

# Octal transceiver (3-State)

# 74ALS645A/74ALS645A-1

## FEATURES

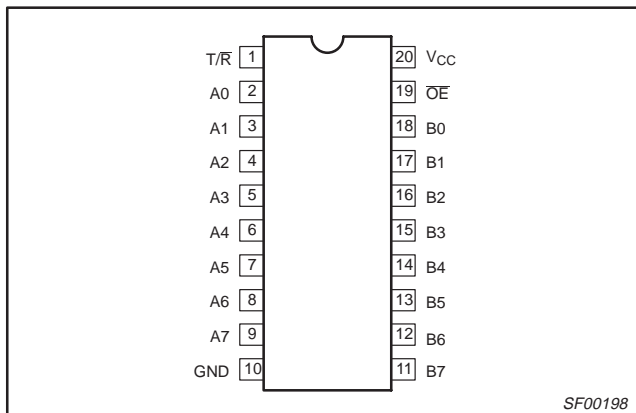
- Octal bidirectional bus interface
- 3-State buffer outputs sink 24mA and source 15mA
- Outputs are placed in high impedance state during power-off conditions
- The -1 version sinks 48mA  $I_{OL}$  within the +5%  $V_{CC}$  range

## DESCRIPTION

The 74ALS645A is an octal transceiver featuring non-inverting 3-State bus compatible outputs in both transmit and receive directions. The device features an output enable ( $\overline{OE}$ ) input for easy cascading and transmit/receive ( $R/\overline{T}$ ) input for direction control.

The 74ALS645A-1 is the same as the 74ALS645A except that both ports sink 48mA within the  $\pm 5\%$   $V_{CC}$  range.

## PIN CONFIGURATION



SF00198

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS645A	7.0ns	34mA
74ALS645A-1	7.0ns	34mA

## ORDERING INFORMATION

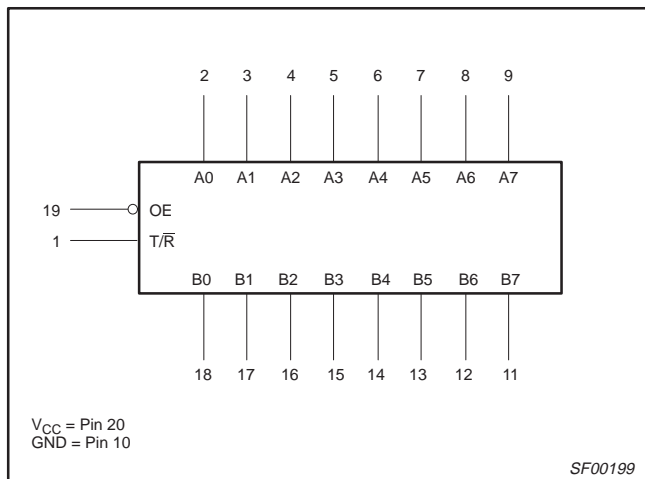
DESCRIPTION	ORDER CODE	DRAWING NUMBER
	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$ , $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$	
20-pin plastic DIP	74ALS645AN, 74ALS645A-1N	SOT146-1
20-pin plastic SOL	74ALS645AD, 74ALS645A-1D	SOT163-1

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74ALS (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0 – A7, B0 – B7	Data inputs	1.0/1.0	20 $\mu$ A/0.1mA
$\overline{OE}$	Output Enable input (active-Low)	1.0/1.0	20 $\mu$ A/0.1mA
T/R	Transmit/receive input	1.0/1.0	20 $\mu$ A/0.1mA
A0 – A7	A port outputs	750/240	15mA/24mA
B0 – B7	B port outputs	750/240	15mA/24mA
A0 – A7	A port outputs (-1 version)	750/480	15mA/48mA
B0 – B7	B port outputs (-1 version)	750/480	15mA/48mA

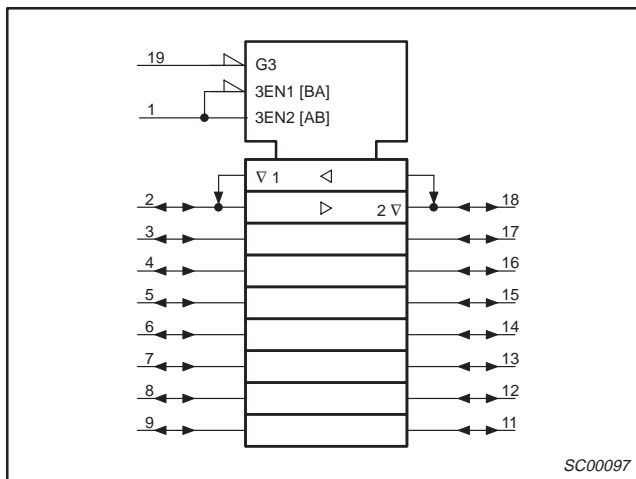
**NOTE:** One (1.0) ALS unit load is defined as: 20 $\mu$ A in the High state and 0.1mA in the Low state.

## LOGIC SYMBOL



SF00199

## IEC/IEEE SYMBOL

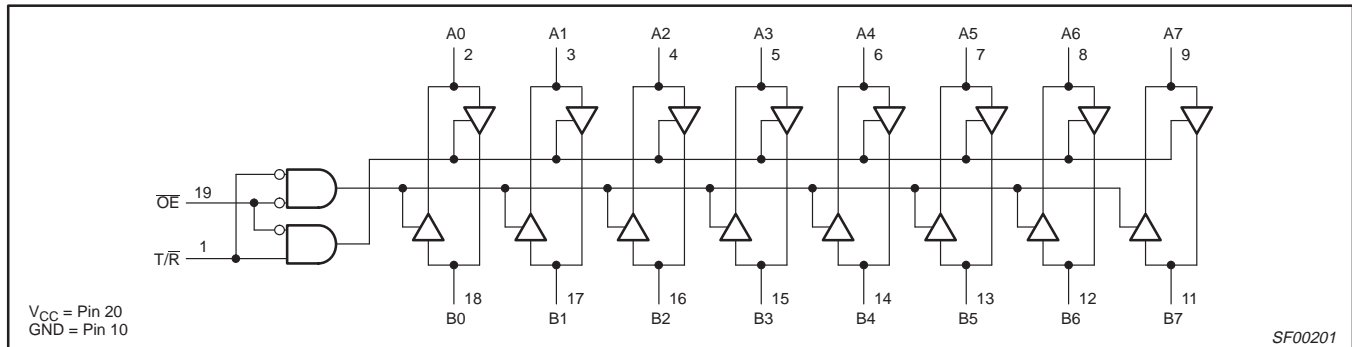


SC00097

# Octal transceiver (3-State)

# 74ALS645A/74ALS645A-1

## LOGIC DIAGRAM



## FUNCTION TABLE

INPUTS		OUTPUTS
$\overline{OE}$	T/R	
L	L	Bus B data to Bus A
L	H	Bus A data to Bus B
H	X	Z

H = High voltage level  
 L = Low voltage level  
 X = Don't care  
 Z = High impedance "off" state

## ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
$V_{CC}$	Supply voltage	-0.5 to +7.0	V
$V_{IN}$	Input voltage	-0.5 to +7.0	V
$I_{IN}$	Input current	-30 to +5	mA
$V_{OUT}$	Voltage applied to output in High output state	-0.5 to $V_{CC}$	V
$I_{OUT}$	Current applied to output in Low output state	All versions	48
		-1 version	96
$T_{amb}$	Operating free-air temperature range	0 to +70	°C
$T_{stg}$	Storage temperature range	-65 to +150	°C

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5.0	5.5	V
$V_{IH}$	High-level input voltage	2.0			V
$V_{IL}$	Low-level input voltage			0.8	V
$I_{IK}$	Input clamp current			-18	mA
$I_{OH}$	High-level output current			-15	mA
$I_{OL}$	Low-level output current	All versions		24	mA
		-1 version		48 <sup>1</sup>	mA
$T_{amb}$	Operating free-air temperature range	0		+70	°C

### NOTES:

1. The 48mA limit applies only under the condition of  $V_{CC} = 5.0V \pm 5\%$ .

## Octal transceiver (3-State)

## 74ALS645A/74ALS645A-1

**DC ELECTRICAL CHARACTERISTICS**

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS <sup>1</sup>		LIMITS			UNIT
					MIN	TYP <sup>2</sup>	MAX	
V <sub>OH</sub>	High-level output voltage		V <sub>CC</sub> ±10%, V <sub>IL</sub> = MAX, V <sub>IH</sub> = MIN	I <sub>OH</sub> = -0.4mA	V <sub>CC</sub> - 2	2.4	3.2	V
				I <sub>OH</sub> = -3mA				
			V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = MIN	I <sub>OH</sub> = -15mA	2.0		V	
V <sub>OL</sub>	Low-level output voltage	All versions	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = MIN	I <sub>OL</sub> = 12mA		0.25	0.40	V
				I <sub>OL</sub> = 24mA		0.35	0.50	V
		-1 version	V <sub>CC</sub> = 4.75V, V <sub>IL</sub> = MAX, V <sub>IH</sub> = MIN	I <sub>OL</sub> = 48mA		0.35	0.50	V
V <sub>IK</sub>	Input clamp voltage		V <sub>CC</sub> = MIN, I <sub>I</sub> = I <sub>IK</sub>			-0.73	-1.5	V
I <sub>I</sub>	Input current at maximum input voltage	$\overline{OE}$ or T/R	V <sub>CC</sub> = MAX, V <sub>I</sub> = 7.0V				0.1	mA
		A or B ports	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5V				0.1	mA
I <sub>IH</sub>	High-level input current <sup>3</sup>		V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7V				20	μA
I <sub>IL</sub>	Low-level input current <sup>3</sup>		V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4V				-0.1	mA
I <sub>O</sub>	Output current <sup>4</sup>		V <sub>CC</sub> = MAX, V <sub>O</sub> = 2.25V		-30		-112	mA
I <sub>CC</sub>	Supply current (total)	I <sub>CCH</sub>	V <sub>CC</sub> = MAX			28	45	mA
		I <sub>CCL</sub>				40	55	mA
		I <sub>CCZ</sub>				44	58	mA

**NOTES:**

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V<sub>CC</sub> = 5V, T<sub>amb</sub> = 25°C.
- For I/O ports, the parameter I<sub>IH</sub> and I<sub>IL</sub> include the off-state current.
- The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I<sub>OS</sub>.

**AC ELECTRICAL CHARACTERISTICS**

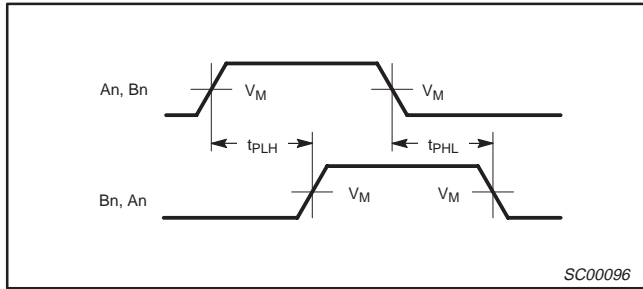
SYMBOL	PARAMETER		TEST CONDITION	LIMITS		UNIT
				T <sub>amb</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V ± 10% C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω		
				MIN	MAX	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay An to Bn, Bn to An		Waveform 1	2.0 2.0	10.0 10.0	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output enable time to High or Low level		Waveform 2 Waveform 3	3.0 3.0	20.0 20.0	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output disable time from High or Low level		Waveform 2 Waveform 3	2.0 4.0	10.0 15.0	ns

# Octal transceiver (3-State)

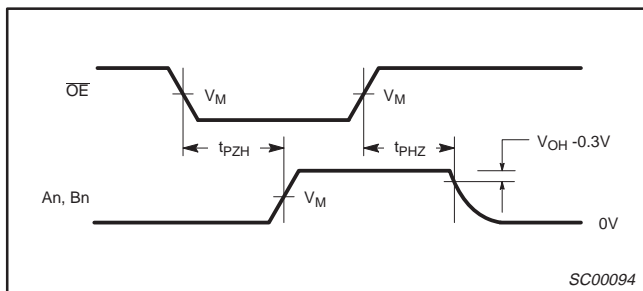
# 74ALS645A/74ALS645A-1

## AC WAVEFORMS

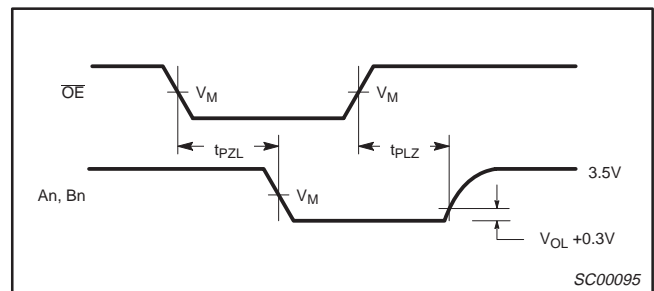
For all waveforms,  $V_M = 1.3V$ .



Waveform 1. Propagation Delay for Non-inverting Outputs



Waveform 2. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 3. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

## TEST CIRCUIT AND WAVEFORMS

**Test Circuit for 3-State Outputs**

SWITCH POSITION	
TEST	SWITCH
$t_{PLZ}, t_{PZL}$	closed
All other	open

**DEFINITIONS:**  
 $R_L$  = Load resistor; see AC electrical characteristics for value.  
 $C_L$  = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.  
 $R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.

**Input Pulse Definition**

Family	INPUT PULSE REQUIREMENTS					
	Amplitude	$V_M$	Rep.Rate	$t_w$	$t_{TLH}$	$t_{THL}$
74ALS	3.5V	1.3V	1MHz	500ns	2.0ns	2.0ns

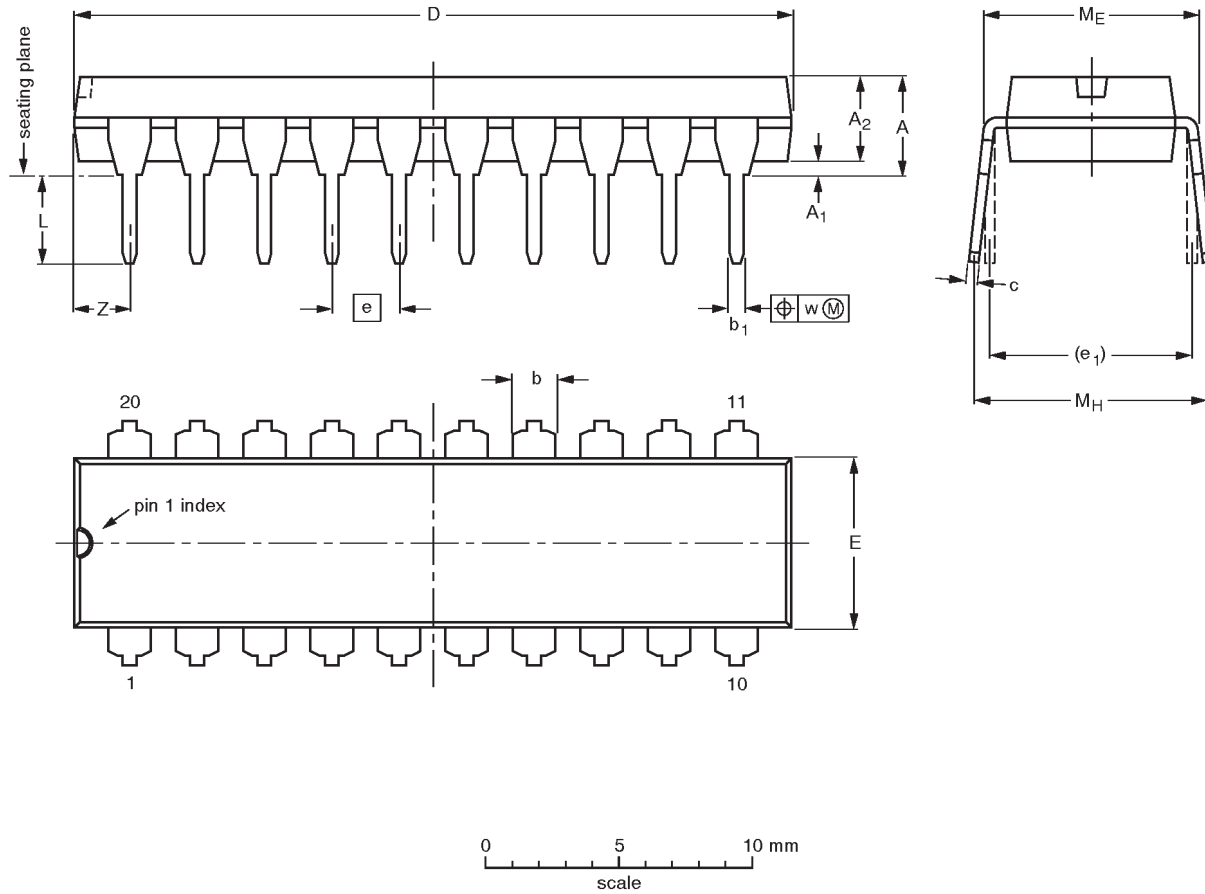
SC00072

# Octal transceiver (3-State)

# 74ALS645A/74ALS645A-1

DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1




**DIMENSIONS** (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			92-11-17 95-05-24

# Octal transceiver (3-State)

# 74ALS645A/74ALS645A-1

**SO20: plastic small outline package; 20 leads; body width 7.5 mm**

**SOT163-1**



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	$\theta$
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				92-11-17 95-01-24

## Octal transceiver (3–State)

74ALS645A/74ALS645A–1

## Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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print code

Date of release: 05-96

Document order number:

9397-750-03308

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