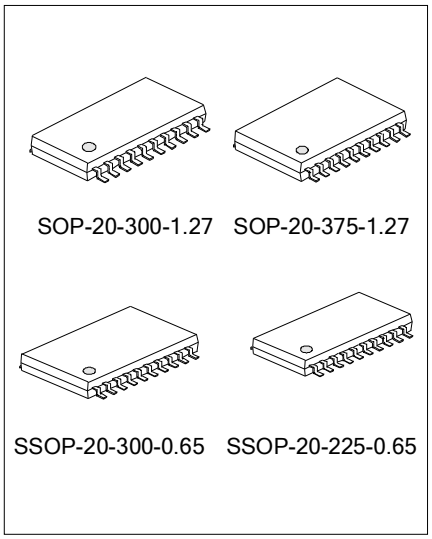
4-BIT MCU FOR REMOTE CONTROLLER(OTP TYPE)

DESCRIPTION

SC73P1601 is one of Silan's 4-bit CMOS single-chip micro-controllers for infrared remote control transmitters (IRCTs). It can be implemented in various IRCTs circuits by OTP program. And it is compatible with SC73C1602 on software and package.



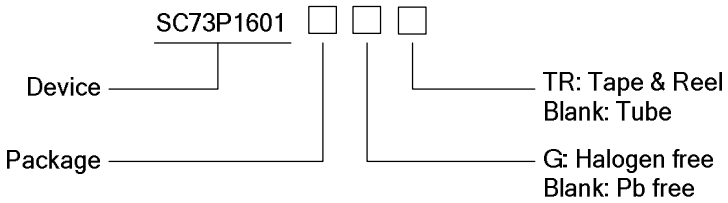
FEATURES

* Wide operating voltage (2.0~4.0V), and low static power consumption (<1μA)
* OTP: 1K x 9 bits
* RAM: 16 x 4bits
* Timer/counter: (10~15 bits)
* 8-bit timer, generates various carrier frequencies and outputs carrier duty
* 16 I/O pins, four 4-bit programmable I/O ports (except P50 and P53)
* Oscillator frequency (f_{osc}): f_{osc}=4MHz(TYP.)
* Operating frequency: $f_{main}=f_{osc}/8$
* Instruction cycle: 5/fmain
* Support low voltage detection

APPLICATIONS

* Infrared remote control device
* TV controller
* Video Cassette Recorder controller
* VTR, laser phonograph and acoustics remote controller

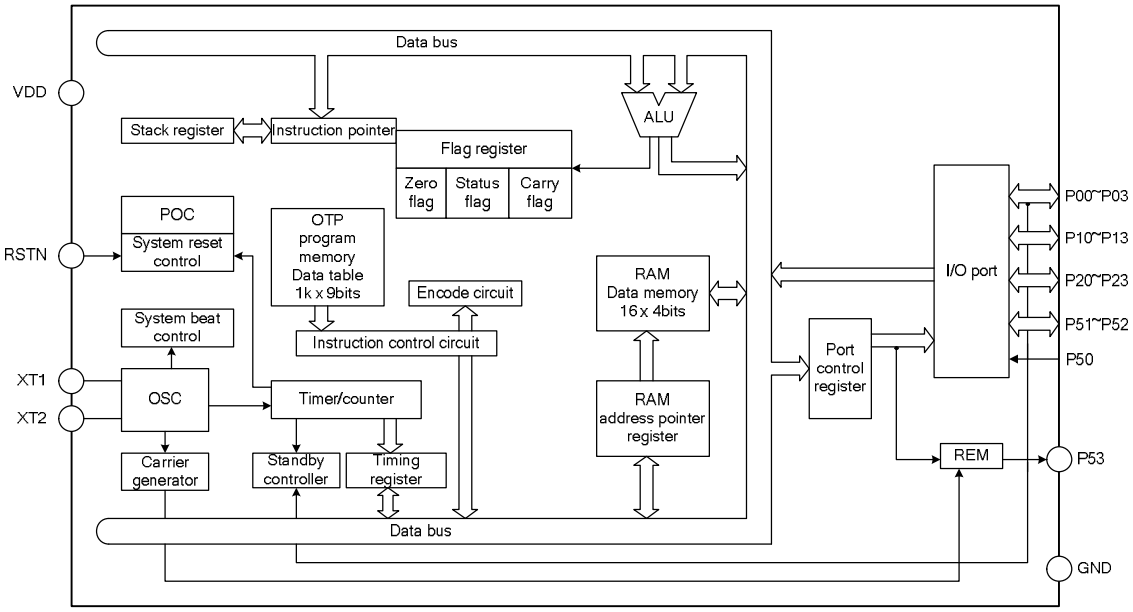
ORDERING FORMATION



Part No.	Package	Marking	Material	Package Type
SC73P1601M	SSOP-20-300-0.65	SC73P1601M	Pb free	Tube
SC73P1601MTR	SSOP-20-300-0.65	SC73P1601M	Pb free	Tape & Reel
SC73P1601MA	SOP-20-300-1.27	SC73P1601MA	Pb free	Tube
SC73P1601MATR	SOP-20-300-1.27	SC73P1601MA	Pb free	Tape & Reel
SC73P1601MC	SSOP-20-225-0.65	SC73P1601MC	Pb free	Tube
SC73P1601MCTR	SSOP-20-225-0.65	SC73P1601MC	Pb free	Tape & Reel
SC73P1601MD	SOP-20-375-1.27	SC73P1601MD	Pb free	Tube
SC73P1601MDTR	SOP-20-375-1.27	SC73P1601MD	Pb free	Tape & Reel
SC73P1601MG	SSOP-20-300-0.65	SC73P1601MG	Halogen free	Tube
SC73P1601MGTR	SSOP-20-300-0.65	SC73P1601MG	Halogen free	Tape & Reel

Part No.	Package	Marking	Material	Package Type
SC73P1601MAG	SOP-20-300-1.27	SC73P1601MAG	Halogen free	Tube
SC73P1601MAGTR	SOP-20-300-1.27	SC73P1601MAG	Halogen free	Tape & Reel
SC73P1601MCG	SSOP-20-225-0.65	SC73P1601MCG	Halogen free	Tube
SC73P1601MCGTR	SSOP-20-225-0.65	SC73P1601MCG	Halogen free	Tape & Reel
SC73P1601MDG	SOP-20-375-1.27	SC73P1601MDG	Halogen free	Tube
SC73P1601MDGTR	SOP-20-375-1.27	SC73P1601MDG	Halogen free	Tape & Reel

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Otherwise specified, T_{amb}=25°C)

Characteristics	Symbol	Rating	Unit
Supply Voltage	V_{DD}	-0.3 ~ +5.0	V
Input Voltage	V_{IN}	-0.3~V_{DD}+0.3	V
Output Current	I_{OUT} (P53)	-9	mA
Power Dissipation	P_D	500	mW
Storage Temperature	T_{stg}	-40~+125	°C
Operating Temperature	T_{opr}	-20~+75	°C

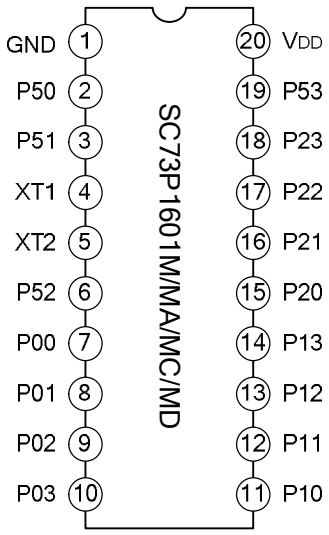
ELECTRICAL CHARACTERISTICS (T_{amb}=25°C, V_{DD}=3.0V)

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Power Supply	V_{DD}	In all the functions	2	--	4	V
Power Reset	V_{POC}	In all the functions	1.4		1.6	V
Operating Current	I_{DD}	In operating mode	--	--	1.0	mA
Oscillation Frequency	F_{OSC}	In operating mode	2M	4M	6M	Hz

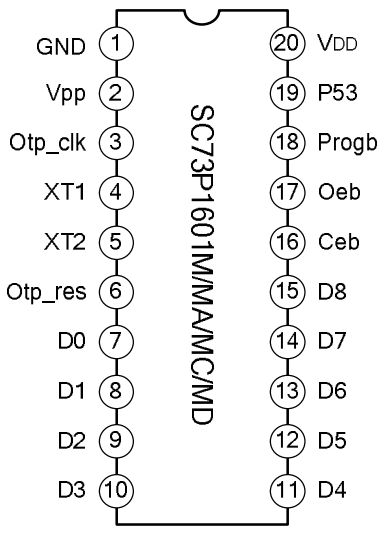
Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
Quiescent Current	I_{DS}	Oscillator stops		--	--	1	μA
Input Pull-Down Resistor	R	V_{DD}=3V	P50	50	60	70	KΩ
			P00-P03 P10-P13 P20-P23 P51-P52	60	75	90	KΩ
Input High Level Voltage	V_{IH}	--		0.7V_{DD}	--	V_{DD}	V
Input Low Level Voltage	V_{IL}	--		0	--	0.3V_{DD}	V
Output High Level Current	I_{OH}	V_{DD}=3V V_{OH}=2.7V	P53	--	-9.0	--	mA
			P00-P03 P10-P13 P20-P23 P51-P52	--	-0.8	--	
Output Low Level Current	I_{OL}	V_{DD}=3V V_{OL}=0.3V	P53	--	10.8	--	mA
			P00-P03 P10-P13 P20-P23 P51-P52	--	--	0.17	

PIN CONFIGURATIONS

1.Normal working mode



2.EPROM programming mode



PIN DESCRIPTIONS

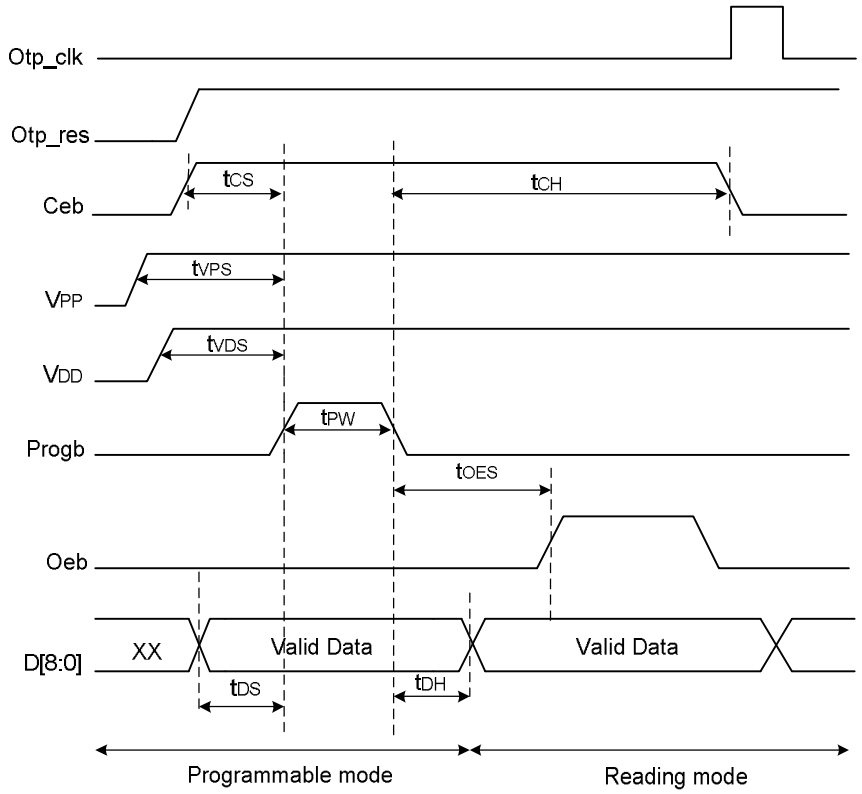
Normal mode

Symbol	Description
VDD	Power Supply (2.0V~4.0V)
GND	Ground
XT1	Oscillator output pin
XT2	Oscillator input pin
P00~P03	4-bit I/O pin. In input mode, it is used as the keyboard-scan input port (with internal pull-down resistor). In output mode, it is used as the keyboard-scan output port.
P10~P13	4-bit I/O pin. In input mode, it is used as the keyboard-scan input port (with internal pull-down resistor). In output mode, it is used as the keyboard-scan output port.
P20~P23	4-bit I/O pin. In input mode, it is used as the keyboard-scan input port (with internal pull-down resistor). In output mode, it is used as the keyboard-scan output port.
P50	1-bit input pin with pull-down resistor, used for keyboard-scan input.
P51	1-bit I/O pin. In input mode, it is used as the keyboard-scan input port (with internal pull-down resistor). In output mode, it is used as the keyboard-scan output port.
P52	1-bit I/O pin. In input mode, it is used as the keyboard-scan input port (with internal pull-down resistor). In output mode, it is used as the keyboard-scan output port,
P53	Outputs remote control signal with carrier or without carrier.

Programming mode:

Symbol	Description
D0-D8	9-bit data when EPROM write in/ verify
Otp_clk	Address increment clock when EPROM write in/ verify
Ceb	EPROM program enable, and high active
Oeb	EPROM output enable, and high active
Progb	EPROM program enable, and high active
VDD	Power supply of +6.5 V
GND	Ground
Vpp	In program mode, provide 12.5V to this pin
Otp_res	Clear eprom address pointer, and high active

Program time sequence:



Performance Characteristics	Symbol	Condition	Min.	Typ.	Max.	Unit
Setup time of “Oeb”	tOES		1	-	-	s
Setup time of “Ceb”	tCS		1	-	-	s
Setup time of “D[8:0]”	tDS		1	-	-	s
Hold time of “Ceb”	tCH		1	-	-	s
Hold time of “D[8:0]”	tDH		1	-	-	s
Setup time of “VPP”	tVPS		1	-	-	s
Setup time of “VDD”	tVDS		1	-	-	s
Pulse width of “Progb”	tPW		200	300	-	s

FUNCTION DESCRIPTION

SC73P1601 includes 4-bit MCU, outlay oscillator, system reset module. Next we will mainly introduce the functions.

1. PC

PC refers to the program address pointer, 10 bits. The maximum addressing space is 1K ROM .The program counter contains the address of the instruction that will be executed next. The PC value is cleared to 0 after reset. The PC is set to predefined value when one of the 3 following occasions occurs: 1) when the JUMP instruction is executed; 2) when a subroutine call is back; 3) when a program call is back. In the SC73P1601, all instructions are one-byte instructions, PC increments by 1 each time an instruction is executed.

2. MBR

Memory buffer register (MBR) is write-only, higher 4-bit of the program pointer. The EPROM of SC73P1601 can be divided into 8 blocks. Each block is 128 bytes. The 8 blocks can be addressed by the MBR. When the program starts executing a branch instruction, it must load the corresponding value to the MBR register, and then executes the command BSS label.

3. STACK

Stack register stores the previous value of program pointer during execution of subroutine calls, 11 bits. There is two-level hardware stack register, so two-level programs can be called. When the user tries to make more than two-level program call, an error will occur.

4. B, H, D

Referred to as the pointer to data table. BHD are separately 2 bits, 4 bits and 4 bits. The 1K EPROM space of SC73P1601 can be used as the data table which can be diplex with program space. When addressing the fixed data of EPROM, the registers act as the pointers to the data table (to form the EPROM address according to BHD order). In other cases, the H, D registers can be used as general purpose registers. Fixed data stored in the data table can be addressed by the transmit instructions. When executing the transmit-instructions, the program will look for the data from the correspond space of EPROM. The low 10 bits address of the EPROM are composed of two lower bits of B , four bits of H and four bits of D.

When the most significant bit is 1, P53 transmits the data with carrier; while the most significant bit is 0, P53 transmits the data without carrier. The second bit of B is of no real use, and it is set 0 by the software at program imitation.

5. PROM

Address	1k x 9bits
000H	
001H	
002H ⋮ 01FH	Subroutine call start address
020H ⋮ 3FFH	Normal program Area (can be duplex as data table)

6. CH0、CH1、CL0、CL1

CH0, CH1, CL0, CL1 are carrier high and low level control registers, which can control the high-low level of carrier is (CH＋1)/fosc and(CL＋1)/fosc.

7. LL, LH

LL register, 4 bits, LH register, bit. LL[3:0] is the address pointer of RAM, and is used as the general-purpose register at the same time.

LH register, 4 bits, used as the general-purpose register.

8. RAM

Data memory consists of 16x4 bits and is used to store temporary data and results after a program is executed. It can address the entire RAM areas by the pointer LL[3:0]. When reset, the contents of RAM are not defined. We recommend users to initialize it at the beginning of their software program.

9. ALU

The arithmetic and logic unit plays a leading role in performing various operations of 4-bit binaries. The operation of ALU will change the carry flag (CF) and the zero flag(ZF).

10. Acc

4-bit accumulator, which is in the ALU. It is mostly used to store data and results.

11. CF

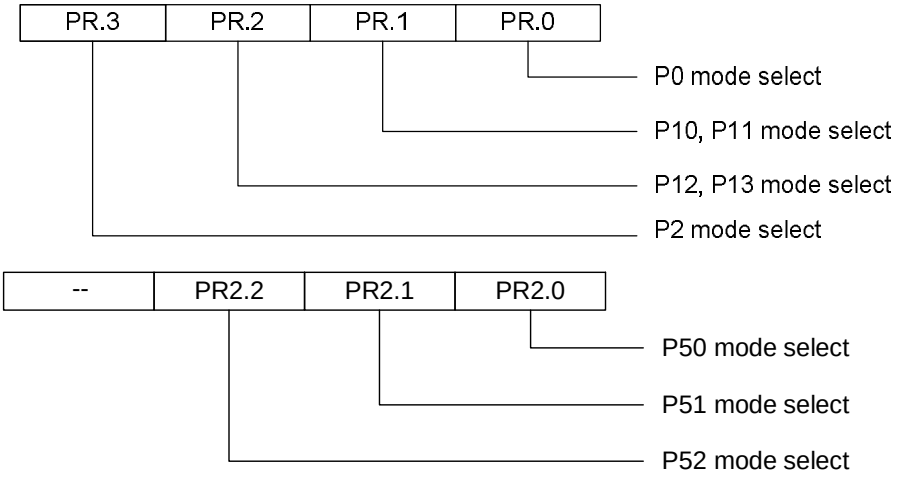
Carry flag.

12. SF

Status flag bit, the value of SF is 1 after reset.

13. PR (PR, PR2)

The port mode register, which specifies the input mode or output mode of the I/O port, is 4-bit write-only. When the value is 1, the corresponding port is set to output mode. PR=0, it is set to input mode. The execution of the HOLD instruction won't affect the I/O modes of operation. When reset, the initialization value is 0000B, and the port is in input mode.



14. PORT

SC73P1601 has 4 groups of I/O ports, totally 20 pins. Each group can operate in both input and output mode (except P50 and P53, P50 is only input port, P53 is only output port). Details are as follows:

P0 port: P00-P03, 4-bit input/output port. The PR determines the port operation mode. In input mode, it has an internal pull-down resistor and can be used for keyboard scan input. When the input level is high, it can release the HOLD mode. In output mode, it can be used for keyboard scan output.

P1 port: P10-P13, same as P0 port;

P2 port: P20-P23, same as P0 port;

P5 port: P50-P53

P50: only as input pin with pull-down resistor used for keyboard scan input. When input high level, the HOLD state is unlocked.

P51: the configuration same as P00;

P52: the configuration same as P00;

P53: large current output port, this pin is used to output infrared remote signal. If P53 is set to 1, this pin outputs modulated signal with carrier or high level signal. If it is set to 0, it outputs low level voltage.

15. Timer/counter

SC73P1601 has two internal timers:

One is a 17-bit timer. The clock source of the timer is main frequency (fmain) of the circuit. There are timing steps from 10 (which generates pulses with frequency fmain/210) to 15 (fmain/215). The timer can output pulse frequency ranging from fmain/210 to fmain/215, and can be used for timer after releasing the HOLD mode. It can also be used as a WDT. After the HOLD mode released and the timer reset instruction TMRST executed, the timer value is cleared.

The other timer is a carrier generator. Setting different length of high and low level time span respectively through programming, it generates various different duty and frequency carriers.

16. TR

Timer register, it selects the status of the timer mode, use the instruction LD TM, A to write the data. SC73P1601 uses the instruction LD A, TM or LD @LR, TM to read the status of timer; TM to read the timing value. For example:

3	2	1	0
IBNS	TIBS		

TR timer register

17. IBNS

The control bit of the read timer. When the value is 0, it reads TM3 (IT3), and IT2~IT0 become 0. When the value is 1, it reads 4-bit data TM3~TM0(IT3~IT0).

TM3: 2^{15}/fmain

TM2: 2^{14}/fmain

TM1: 2^{13}/fmain

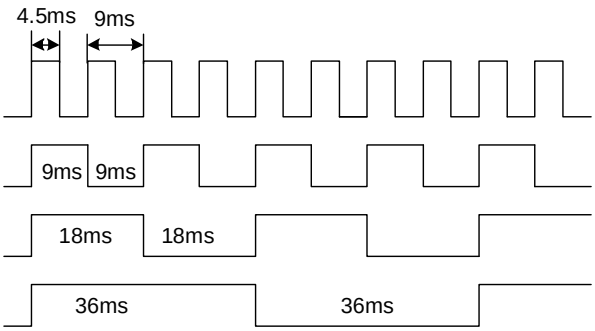
TM0: 2^{12}/fmain

Example: when the crystal oscillator select 455KHz, the corresponding time of port P50 is 2^{12}÷455≈9ms. This means the time from TM=1111B to 1101 is 9ms, and the time from TM=1111B to 1110 is 4.5ms.See the following program:

```
        LD      A#1000B
        LD      TM,A
      TMRST
        ......
        LD      L,#TEMP
        LD      @LL,#1110B
LOOP:   LD      A,TM
        XOR     A,@LL
        JMPS    LOOP
        END
```

In above program, the time from TMRST start to END is 4.5ms, that it from TM=1111B to 1110B is 4.5ms..

Time change :



The maximum adjustable time of the timer is 2^{16}/fmain. When the timer acts as a WDT and the timer is activated, it must execute the TMRST instruction and clear the timer in 2^{16}/fmain's time, otherwise, it will lead the WDT to overflow, and causes the MCU to reset.

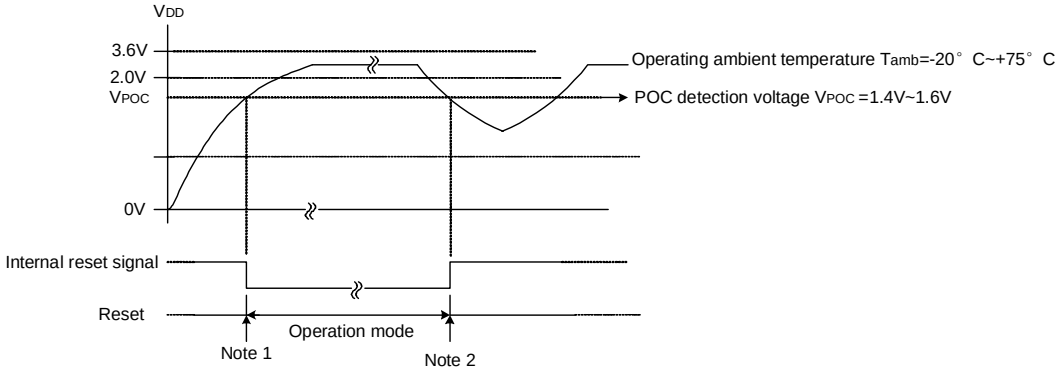
18. POC Circuit

The POC circuit monitors the power supply voltage and applies an internal reset to the micro-controller.

The POC circuit has the following functions:

- Generates an internal reset signal when V_{DD}< V_{POC}. (Note 1)
- Cancels an internal reset signal when V_{DD} > V_{POC}.

Here, V_{DD}: power supply voltage. V_{POC}: POC detection voltage.



Notes. 1. After the circuit is power on, there is a short oscillation stabilization wait time before the circuit is in operation mode. The oscillation stabilization wait time is about 2^{16}/fmain.

2. The POC circuit generates an internal reset signal when the power supply voltage has fallen to a certain value in working mode.

19. Instruction Cycle

Instructions and internal operations are executed in synchronization with the main clock. The minimum time of carrying out a complete instruction is called the instruction cycle. SC73P1601 has 1 and 2-cycle two kind of instructions.

An instruction cycle consists of 5 states (STCLK1 to STCLK5). Each state consists of 1 main clock. Therefore, the instruction cycle time is 5/fmain [s].

INSTRUCTION SETS

1. Transmit instruction

Instruction	Operation	CF	SF	Cycle
LD A, LL	A ← LL	---	1	2
LD A, B	A ← B	---	1	2
LD A, H	A ← H	---	1	2
LD A, D	A ← D	---	1	2
LD A, @LL	A ← RAM(LL)	---	1	1
LD A, #k	A ← k	---	1	1
LD CL1, A	CL1 ← A	---	1	2
LD CL0, A	CL0 ← A	---	1	2
LD CH1, A	CH1 ← A	---	1	2
LD CH0, A	CH0 ← A	---	1	2
LDH A, @BD	A ← ROM(BD)7-4	---	1	2
LDL A, @BD	A ← ROM(BD)3-0	---	1	2
LDS A, @BD	A ← ROM(BD)8	---	1	2
LDH @LL, @BD	RAM(LL) ← ROM(BD)7-4	---	1	2
LDL @LL, @BD	RAM(LL) ← ROM(BD)3-0	---	1	2
LDS @LL, @BD	RAM(LL) ← ROM(BD)8	---	1	2
LD LL, A	LL ← A	---	1	2
LD LL, #k	LL ← k	---	1	1
LD @LL, A	RAM(LL) ← A	---	1	1
LD @LL, #k	RAM(LL) ← k	---	1	1
LD D, A	D ← A	---	1	2
LD H, A	H ← A	---	1	2
LD B, A	B ← A	---	1	2
LD PR, A	PR ← A	---	1	2
LD PR2, A	PR2 ← A	---	1	2
LD TM, A	TM ← A	---	1	2
LD A, TM	A ← TM	---	1	2

1	LD A, LL	Load values in the LL register to the accumulator.
2	LD A, D	Load values in the D register to the accumulator.
3	LD A, H	Load values in the H register to the accumulator.
4	LD A, B	Load values in the B register to the accumulator.
5	LD A, @LL	Load the contents of RAM pointed at by the LL (LL & LH) register to accumulator.
6	LD A, #k	Load the 4 bit immediate K to accumulator.
7	LDL A, @BD	Load the lower 4 bit of ROM data pointed at by the BHD to accumulator.
8	LDH A, @BD	Load the higher 4 bit of ROM data pointed at by the BHD to accumulator.
9	LDS A, @BD	Load the highest 1 bit of ROM data pointed at by the BHD to accumulator
10	LDL @LL, @BD	Load the lower 4 bit of ROM data pointed at by the BHD to RAM pointed at by the LL register.

11	LDH @LL, @BD	Load the higher 4 bit of ROM data pointed at by the BHD to RAM pointed at by the LL register.
12	LDS @LL, @BD	Load the highest 1 bit of ROM data pointed at by the BHD to RAM pointed at by the LL register.
13	LD LL, A	Load the contents of the accumulator to the LL register.
14	LD LH, A	Load the contents of the accumulator to the LH register.
15	LD LL,#K	Load immediate K to the LL register.
16	LD @LL, A	Load the content of the accumulator to the RAM pointed at by the LL register.
17	LD @LL, #k	Load the immediate K to RAM pointed at by the LL register.
18	LD D, A	Load the content of the accumulator to the D register.
19	LD H, A	Load the content of the accumulator to the H register.
20	LD B, A	Load the content of the accumulator to the B register.
21	LD CL1, A	Load the content of the accumulator to the CL1 register.
22	LD CL0, A	Load the content of the accumulator to the CL0 register.
23	LD CH1, A	Load the content of the accumulator to the CH1 register.
24	LD CH0, A	Load the content of the accumulator to the CH0 register.
25	LD PR, A	Load the content of the accumulator to the port register(PR).
26	LD PR2, A	Load the content of the accumulator to the port register(PR2).
27	LD TM, A	Load the content of the accumulator to the timer register.
28	LD A, TM	Load the content of the timer register to the accumulator.

Execution the above transmit instructions will not affect the carry flag, and the status flag remains 1.

2. Input/output instructions

Instruction	Operation	CF	SF	Cycle
LD A, %p	A ← PORT(p)	---	/Z	2
LD @LL, %p	RAM(LL) ← PORT(p)	---	/Z	2
LD %p, A	PORT(p) ← A	---	1	2
LD %p, @LL	PORT(p) ← RAM(LL)	---	1	2

a.	LD A, %P	Move the value of port(P) to the accumulator
b.	LD @LL, %p	Move the value of port(P) to RAM pointed at by the LL register.
c.	LD %p, A	Move the contents of the accumulator to port (P).
d.	LD %p, @LL	Load the contents of RAM pointed at by the LL register to port(P).

The above four input/output instructions are used mostly for port operation, the two read instructions will affect the status flag SF.

3. Arithmetic and logical instructions

Instruction	Operation	CF	SF	Cycle
ADD A, @LL	A ← A+RAM(LL)	---	/C	1
ADDC A, @LL	A ← A+RAM(LL)+CF	C	/C	1
ADD A, #k	A ← A+k	---	/C	1
ADD LL, #k	LL ← LL+k	---	/C	2
SUBRC A, @LL	A ← RAM(LL)-A-/CF	C	C	1
INC @LL	RAM(LL) ← RAM(LL)+1	---	/C	1
DEC @LL	RAM(LL) ← RAM(LL)-1	---	C	1
INC LL	LL ← LL+1	---	/C	2
DEC LL	LL ← LL-1	---	C	2
INC D	D ← D+1	---	/C	2
INC H	H ← H+1	---	/C	2
INC B	B ←B+1	---	/C	2
DEC D	D ← D-1	---	C	2
DEC H	H ← H-1	---	C	2
DEC B	B ← B-1	---	C	2
AND A, @LL	A ← A&RAM(LL)	---	/Z	1
OR A, @LL	A ← A | RAM(LL)	---	/Z	1
XOR A, @LL	A ← A^RAM(LL)	---	/Z	1

1. ADD A, @LL — Add the contents of RAM pointed at by the LL to accumulator, store the sum in the ACC. This operation will affect SF, SF=/CF.
2. ADDC A, @LL — Add the contents of RAM pointed at by the LL register to accumulator with carry. Store the carry bit in the CF. This operation will affect SF, SF=/CF.
3. ADD A,#K — Add immediate K to accumulator. Store the sum in the ACC. This will affect SF, SF=/CF.
4. ADD L,#K — Add immediate K to the LL register. Store the sum in the LL. This will affect SF, SF=/CF.
5. SUBRC A, @LL — Subtract instruction with borrow(the complement of carry). Subtract the contents of the accumulator from the contents of RAM pointed at by the LL register, subtract the complement of the carry bit, then store the results in the accumulator, transfer the carry bit to the CF, this will affect SF and CF, SF=CF.
6. INC @LL — Increment instruction. Increment the contents of RAM pointed at by the LL register by 1. This will affect SF, SF=/CF.
7. DEC @LL — Decrement instruction. Decrement the contents of RAM pointed at by the LL register by 1. This will affect SF, SF=CF.
8. INC D — Increment instruction. Increment the contents of the D register by 1. This will affect SF, SF=/CF.
9. INC H — Increment instruction. Increment the contents of the H register by 1. This will affect SF, SF=/CF.
10. INC B — Increment instruction. Increment the contents of the B register by 1. This will affect SF, SF=/CF.

11.	DEC D	Decrement instruction. Decrement the contents of the D register by 1. This will affect SF, SF=CF.
12.	DEC H	Decrement instruction. Decrement the contents of the H register by 1. This will affect SF, SF=CF.
13.	DEC B	Decrement instruction. Decrement the contents of the B register by 1. This will affect SF, SF=CF.
14.	INC LL	Increment instruction. Increment the contents of the LL register by 1. This will affect SF, SF=/CF.
15.	DEC LL	Subtract 1 from the content in register LL. SF is affected, SF=/CF.
16.	AND A, @LL	The contents of the accumulator and RAM pointed at by the LL register are ANDed and the results are stored in the accumulator. SF changed, SF=/Z.
17.	OR A, @LL	The contents of the accumulator and RAM pointed at by the LL register are ORed and the results are stored in the accumulator. SF changed, SF=/Z.
18.	XOR A,@LL	The contents of the accumulator and RAM pointed at by the LL register are XORed and the results are stored in the accumulator. SF changed, SF=/Z.

4. Bit operation instructions

Instruction	Operation	CF	SF	Cycle
CLR @LL, b	RAM(LL)b←0	---	1	2
SET @LL, b	RAM(LL)b←1	---	1	2
TEST @LL, b	SF←/RAM(LL)b	---	*	2

a.	CLR @LL, b	Clear the B-bit of the RAM pointed at by the LL register.
b.	SET @LL, b	Set the B-bit of the RAM pointed at by the LL register to be 1.
c.	TEST @LL, b	Test the B-bit of the RAM pointed at by the LL register. If this bit is1, the SF is set to 0; otherwise, the SF is set to 1.

5. Carry operation instructions

Instruction	Operation	CF	SF	Cycle
CLR CF	CF←0	0	1	2
SET CF	CF←1	1	1	2
TESTP CF	SF←CF	---	*	1

a.	CLR CF	Clear the carry flag to logic zero.
b.	SET CF	Set the carry flag to logic 1.
c.	TESTP CF	Test the carry flag, send the carry flag to SF.

6. Branch instructions

Instruction	Operation	CF	SF	Cycle
BSS label		---	1	2
JMPS label		---	1	3

Jump instruction is active only when SF is 1, or else next instruction is executed. Please read the *Pseudo-instruction Set* for details.

BSS label Jump to destination address label with range of 128 bytes

JMPS label Jump to destination address label with range of 2K program.

Symbol description of above instructions:

a. label Destination address of jump
b. #k Immediate (0~15)
c. b Bit addressing (0~3)
d. %p Port address

7. Subroutine instructions

Instruction	Operation	CF	SF	Cycle
CALLS label		---	---	2
RET		---	---	2

When executing subroutine call and return instructions, the subroutine starting address is limited from 000H to 01FH.

8. Other instructions

Instruction	Operation	CF	SF	Cycle
HOLD		---	1	1
NOP		---	---	1
TMRST	Reset timer counter	---	---	1

a. HOLD After executing this instruction, MCU is in the power–save mode, the clock stops oscillation and power consumption reduces dramatically.
b. NOP Null operation. It doesn't affect anything.
c. TMRST Timer clear command. It will clear all values of the timer to 0. This instruction is often used to reset WDT in program.

9. Pseudoinstruction

ORG

Format:

[Label:] ORG address

Function:

Redefine following start address

Expression:

Label: selectable

Address: redefined address, can be binary, decimal or hexadecimal.

Redefined address is an absolute address which could not be returned back. That is, the redefined address

should be higher than that above, or a fault is occurred during compiling. 000H is defaulted if no address is set by ORG instruction.

Example:

ORG 0100H

EQU

Format:

Symbol EQU digital

Function:

Define a digital as a symbol. Symbol ＝ digital.

Expression:

Symbol should be legal, and digital should be binary, decimal or hexadecimal. There is no colone before EQU in definition, and it can only useful after the definition.

Example:

Data1 EQU 12H

Data2 EQU 1001B

DB

Format:

[Label:] [num] DB data

Function:

Define data with number of num.

Expression:

Label: selectable

Num: indicates number of data, default value is 1.

Data: data to be written to ROM. It should smaller than 0X200 as ROM is only 9-bit.lower 9-bit value of data is taken with warning if it is more than 0x200.(only lower 8-bit is taken if the instruction is used for data table)

Example:

DB 12H ; Define one data

DB 10010B ; Define one data

12H DB 55H ; Define continuous 18 data

JMPS

Format:

[Label:] JMPS address

Function:

Jump in ROM.

Expression:

Label: selectable

Address can be a digital, symbol defined by EQU or the address symbol.

Combined by:

LD MBR, #k

BSS label

The instruction is 2-byte long, and it can jump to any position in the ROM.

Example:

```
JMPS MAIN
JMPS 100H
```

VENT

Format:

VENT label

Function:

Define the entry and reset address of sub-program.

Expression:

Label is the sub-program name or the address symbol.

Use VENT to specify the entry and reset address of the sub-program, and it must be at the beginning of the program. The first VENT denotes the reset address and the following VENT instructions denote the entry of the sub-program. In general, 16 sub-programs can be defined at most. All the sub-programs called by CALL instruction should be defined in VENT, or else errors will occur in assembly.

Example:

```
VENT MAIN
VENT SUB1
VENT SUB2
……..
ORG 100H
MAIN:
NOP
NOP
CALLS SUB1
CALLS SUB2
……
SUB1:
……..
SUB2:
……..
```

END

Format:

END

Function:

Use the END instruction to end the assembly of a program.

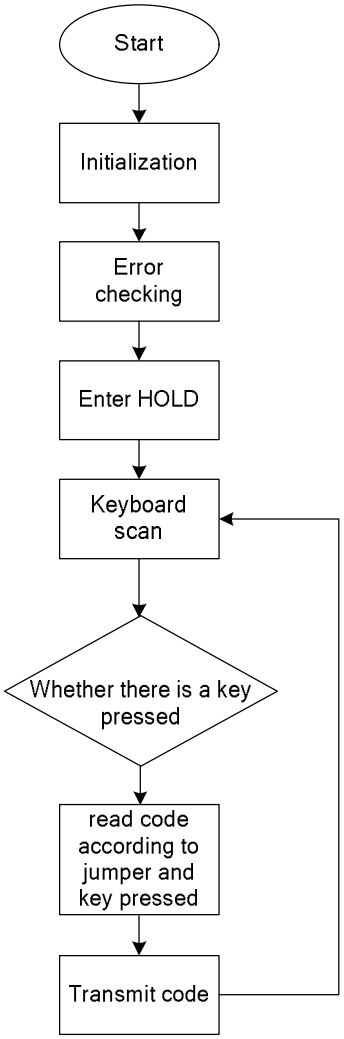
Expression:

END pseudoinstruction ends the assembly of a program and the content after END will not be processed by assembler. If END is omitted, the assembler will process all the lines of the source file.

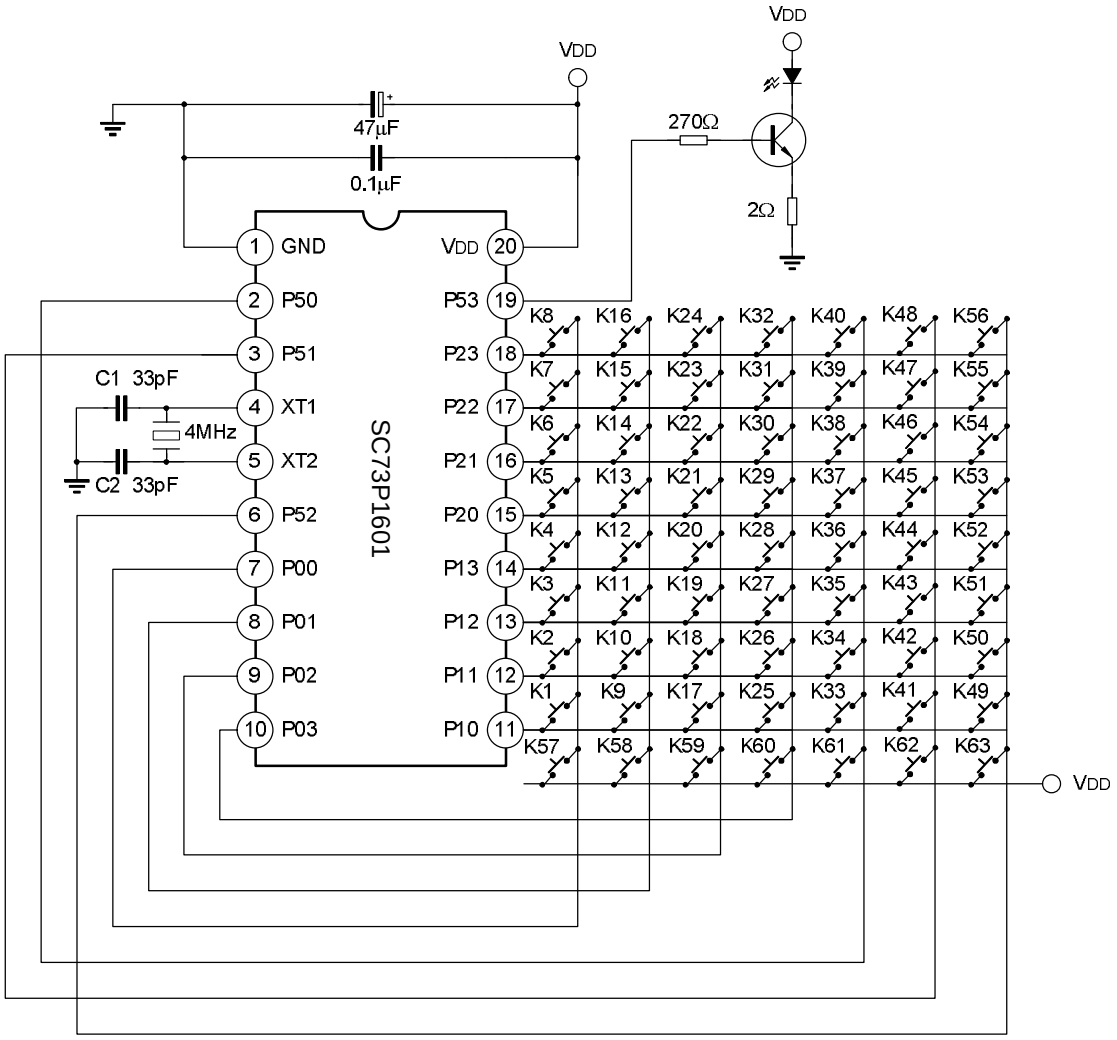
Example:

```
END
```

Remote control flow chart:

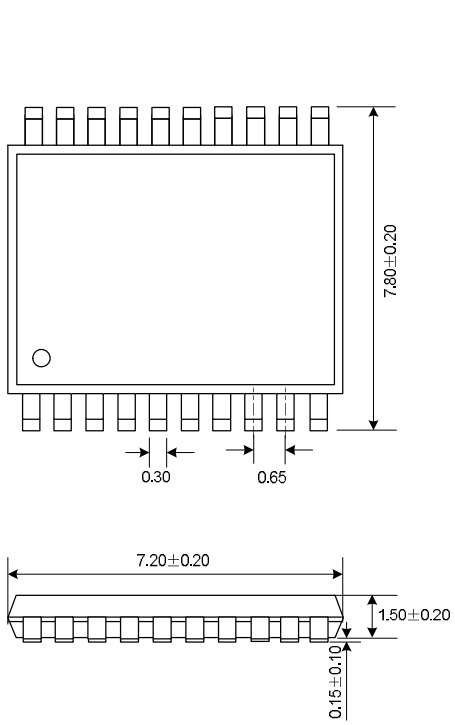


TYPICAL APPLICATION CIRCUIT

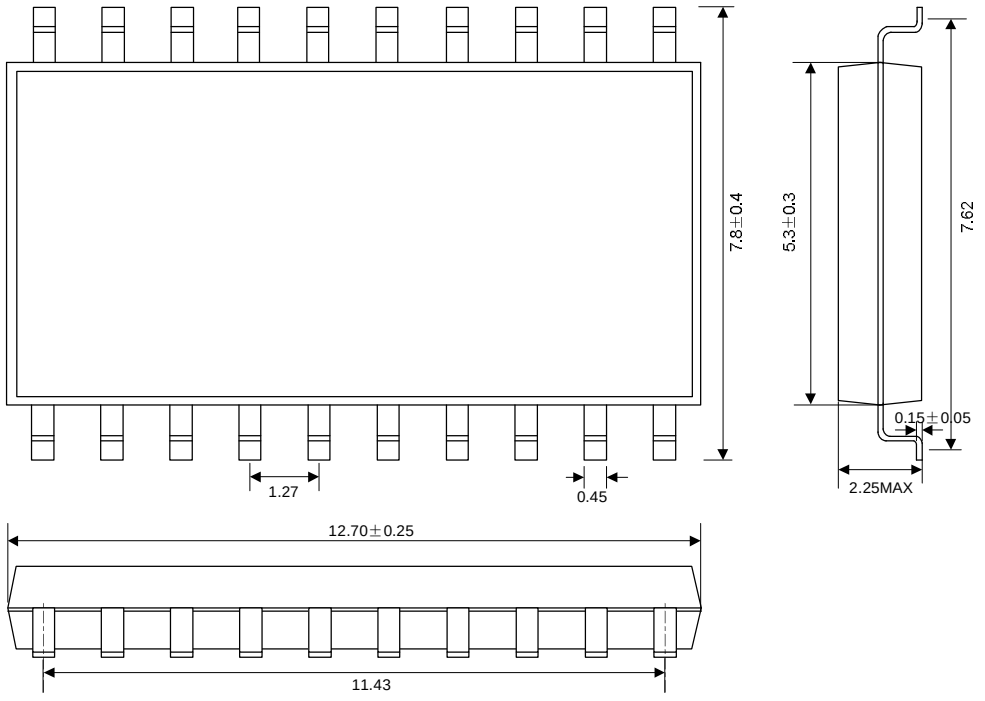


PACKAGE OUTLINE

SSOP-20-300-0.65 Unit: mm

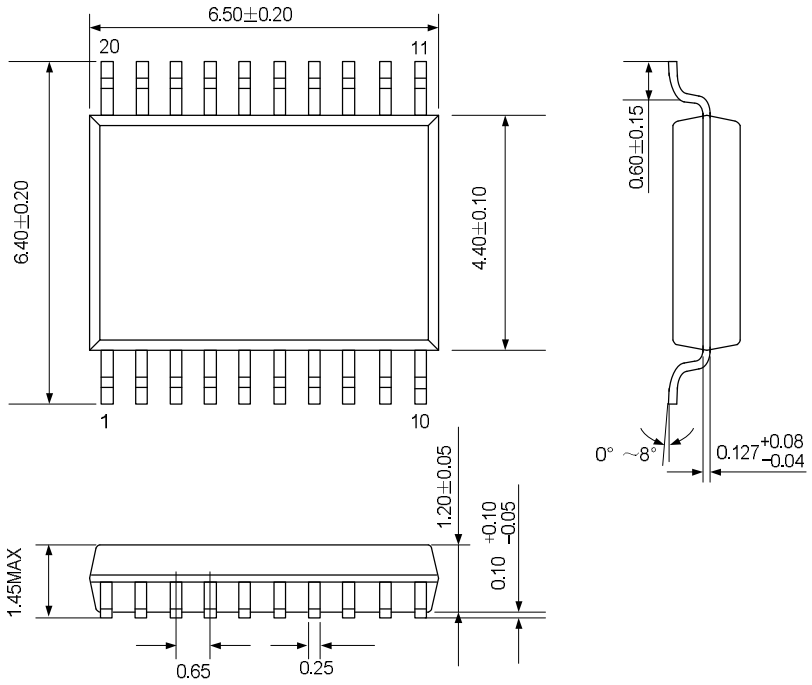


SOP-20-300-1.27 Unit: mm

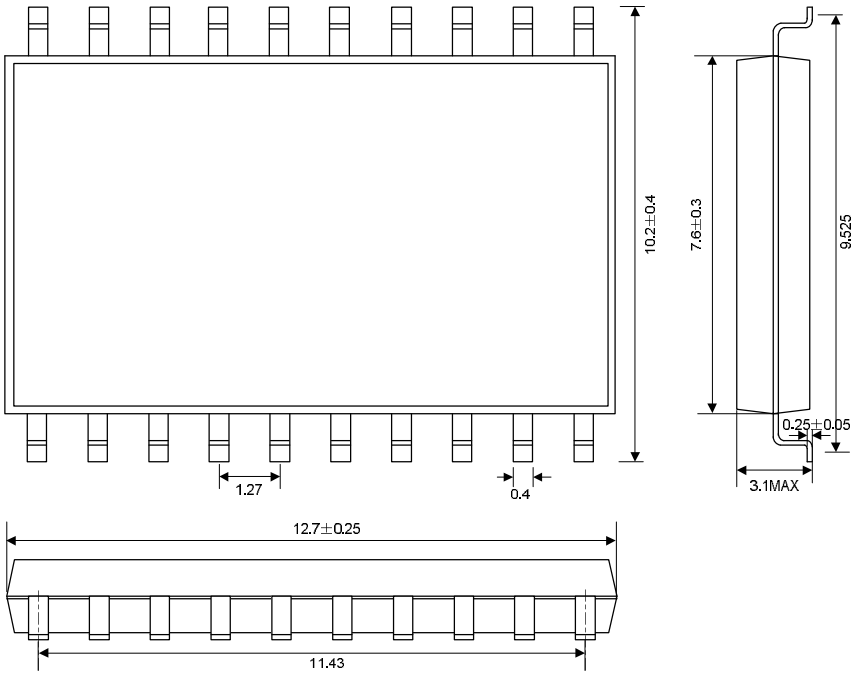


PACKAGE OUTLINE (Continued)

SSOP-20-225-0.65 Unit: mm



SOP-20-375-1.27 Unit: mm





MOS DEVICES OPERATE NOTES:

Electrostatic charges may exist in many things. Please take following preventive measures to prevent effectively the MOS electric circuit as a result of the damage which is caused by discharge:

- The operator must put on wrist strap which should be earthed to against electrostatic.
- Equipment cases should be earthed.
- All tools used during assembly, including soldering tools and solder baths, must be earthed.
- MOS devices should be packed in antistatic/conductive containers for transportation.

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