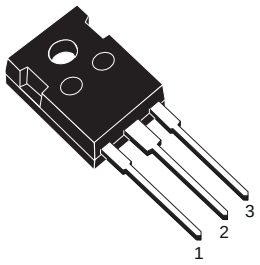
STW12NB60

N-CHANNEL 600V - 0.5Ω - 12A TO-247
PowerMesh™II MOSFET

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STW12NB60	600V	< 0.6Ω	12 A

- TYPICAL $R_{DS}(on)$ = 0.5Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- VERY LOW INTRINSIC CAPACITANCES
- GATE CHARGE MINIMIZED

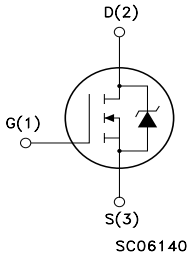


TO-247

DESCRIPTION

Using the latest high voltage MESH OVERLAY™ process, STMicroelectronics has designed an advanced family of power MOSFETs with outstanding performances. The new patent pending strip layout coupled with the Company's proprieraty edge termination structure, gives the lowest RDS(on) per area, exceptional avalanche and dv/dt capabilities and unrivalled gate charge and switching characteristics.

INTERNAL SCHEMATIC DIAGRAM



APPLICATIONS

- SWITCH MODE POWER SUPPLIES (SMPS)
- DC-AC CONVERTERS FOR WELDING EQUIPMENT AND UNINTERRUPTIBLE POWER SUPPLIES AND MOTOR DRIVE

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	600	V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	600	V
V_{GS}	Gate- source Voltage	±30	V
I_D	Drain Current (continuos) at T_C = 25°C	12	A
I_D	Drain Current (continuos) at T_C = 100°C	7.56	A
I_{DM} (●)	Drain Current (pulsed)	48	A
P_{TOT}	Total Dissipation at T_C = 25°C	190	W
	Derating Factor	1.52	W/°C
dv/dt(1)	Peak Diode Recovery voltage slope	4	V/ns
T_{stg}	Storage Temperature	–65 to 150	°C
T_j	Max. Operating Junction Temperature	150	°C

(1)I_{SD} ≤12A, di/dt ≤100A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_j ≤ $T_{JMAX.}$

THERMAL DATA

Rthj-case	Thermal Resistance Junction-case Max	0.658	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	62.5	°C/W
T_l	Maximum Lead Temperature For Soldering Purpose	300	°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	12	A
E_{AS}	Single Pulse Avalanche Energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	450	mJ

ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 µA, V_{GS} = 0	600			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating			1	µA
		V_{DS} = Max Rating, T_C = 125 °C			50	µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ±30V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10V, I_D = 5.5A		0.5	0.60	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs}	Forward Transconductance	V_{DS} > $I_{D(on)}$ x $R_{DS(on)max}$, I_D = 5.5A		9		S
C_{iss}	Input Capacitance	V_{DS} = 25V, f = 1 MHz, V_{GS} = 0		2200		pF
C_{oss}	Output Capacitance			285		pF
C_{rss}	Reverse Transfer Capacitance			30		pF

ELECTRICAL CHARACTERISTICS (CONTINUED)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	V_{DD} = 300V, I_D = 5.5 A		27		ns
t_r	Rise Time	R_G = 4.7Ω, V_{GS} = 10V (see test circuit, Figure 3)		12		ns
Q_g	Total Gate Charge	V_{DD} = 480V, I_D = 11 A,		54	70	nC
Q_{gs}	Gate-Source Charge	V_{GS} = 10V, R_G = 4.7Ω		17		nC
Q_{gd}	Gate-Drain Charge			23		nC

SWITCHING OFF

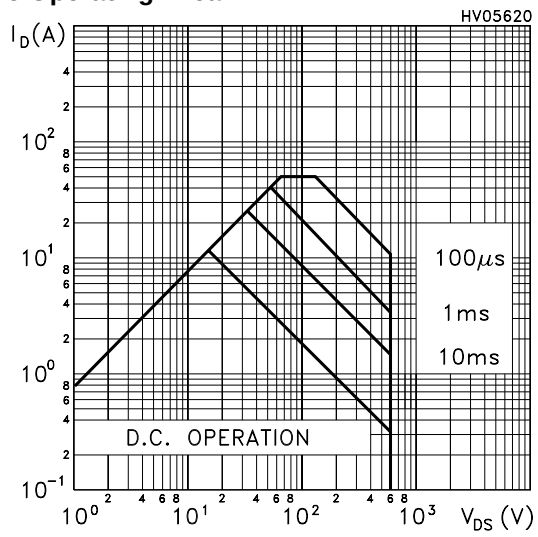
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$	Off-voltage Rise Time	V_{DD} = 480V, I_D = 11 A,		20		ns
t_f	Fall Time	R_G = 4.7Ω, V_{GS} = 10V (see test circuit, Figure 5)		15		ns
t_c	Cross-over Time			32		ns

SOURCE DRAIN DIODE

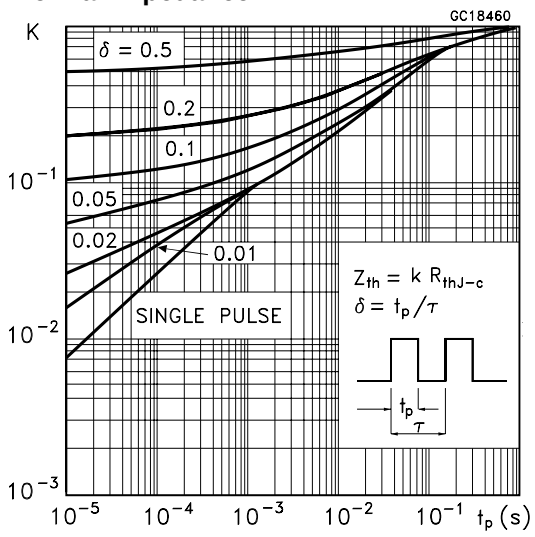
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				12	A
I_{SDM} (2)	Source-drain Current (pulsed)				48	A
V_{SD} (1)	Forward On Voltage	I_{SD} = 12 A, V_{GS} = 0			1.6	V
t_{rr}	Reverse Recovery Time	I_{SD} = 11 A, di/dt = 100 A/µs,		600		ns
Q_{rr}	Reverse Recovery Charge	V_{DD} = 100V, T_j = 150°C (see test circuit, Figure 5)		6.5		µC
I_{RRM}	Reverse Recovery Current			20.5		A

Note: 1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
2. Pulse width limited by safe operating area.

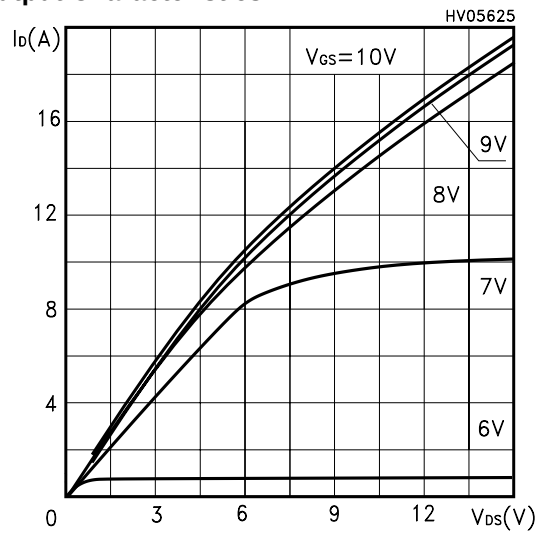
Safe Operating Area



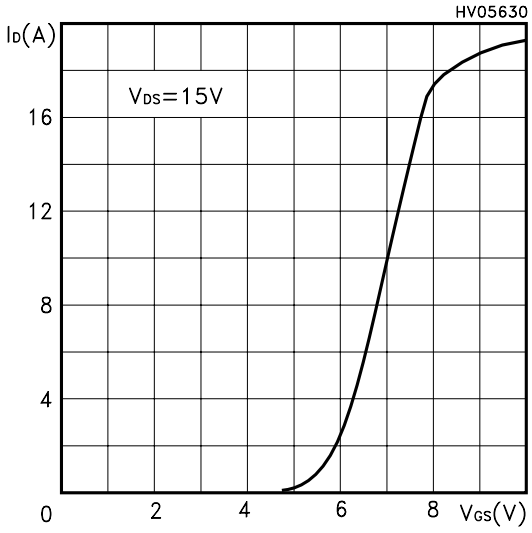
Thermal Impedance



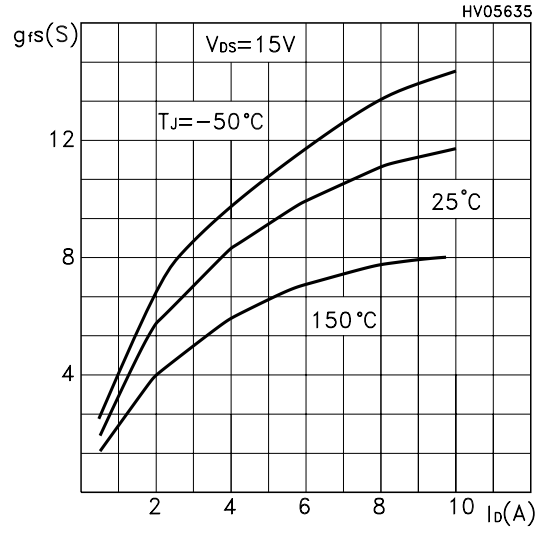
Output Characteristics



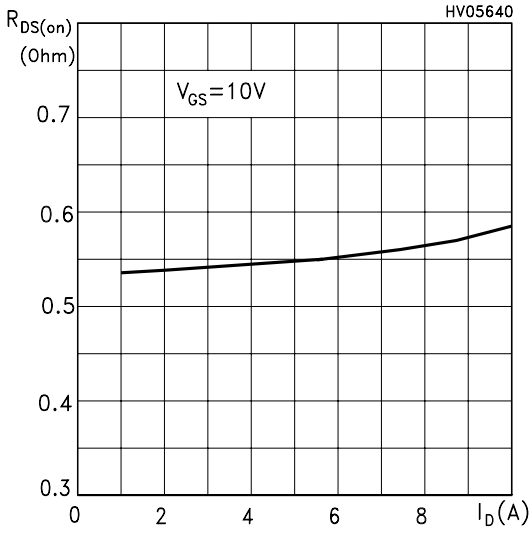
Transfer Characteristics



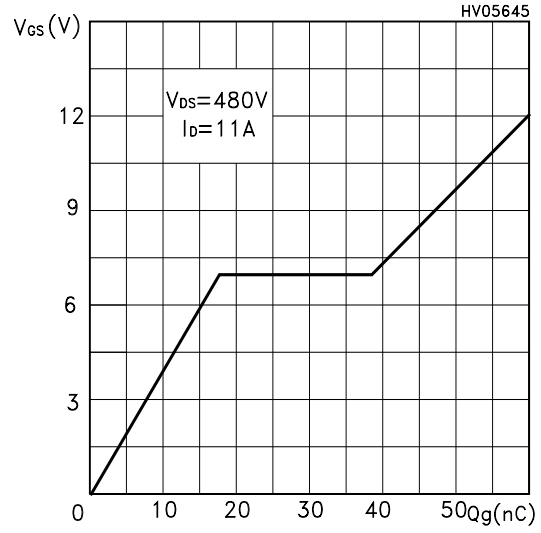
Transconductance



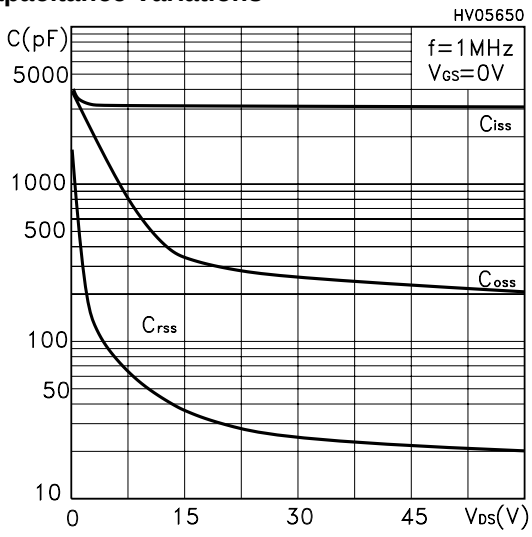
Static Drain-source On Resistance



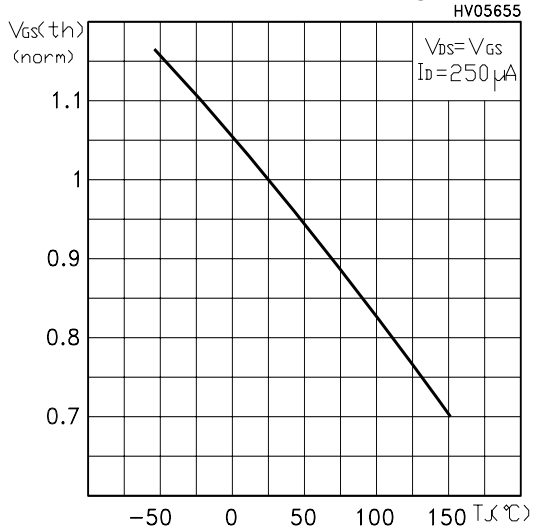
Gate Charge vs Gate-source Voltage



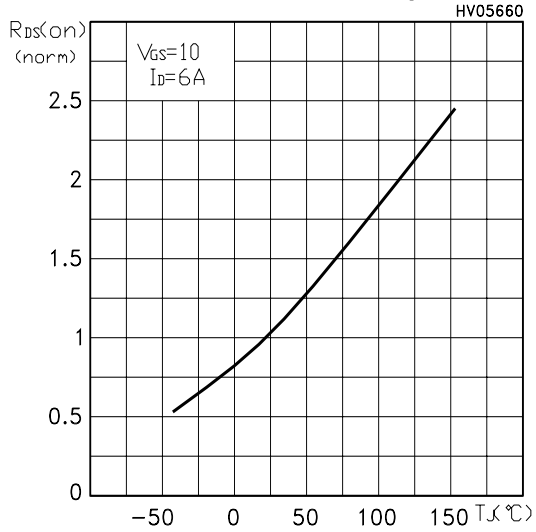
Capacitance Variations



Normalized Gate Thereshold Voltage vs Temp.



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics

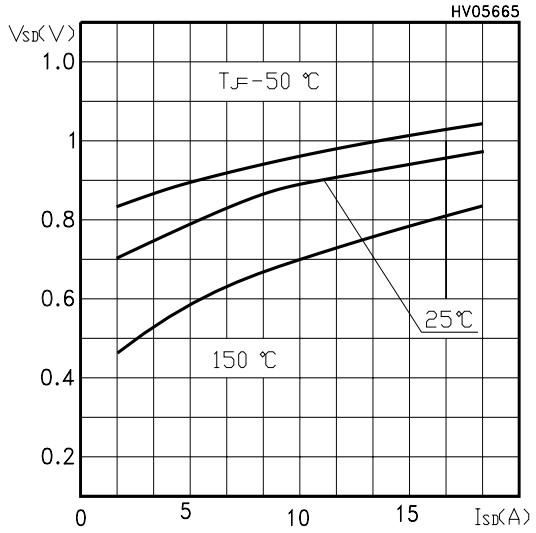


Fig. 1: Unclamped Inductive Load Test Circuit

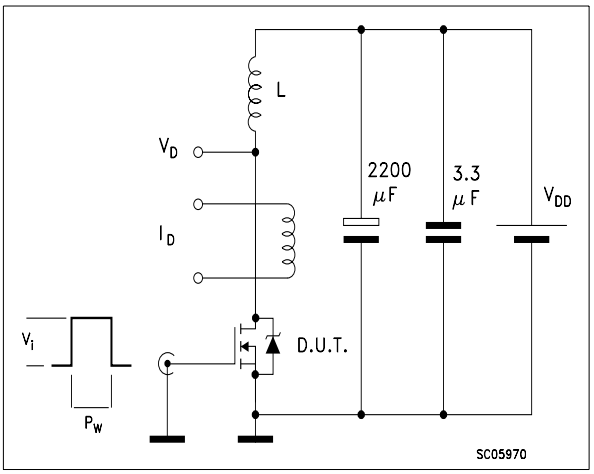


Fig. 2: Unclamped Inductive Waveform

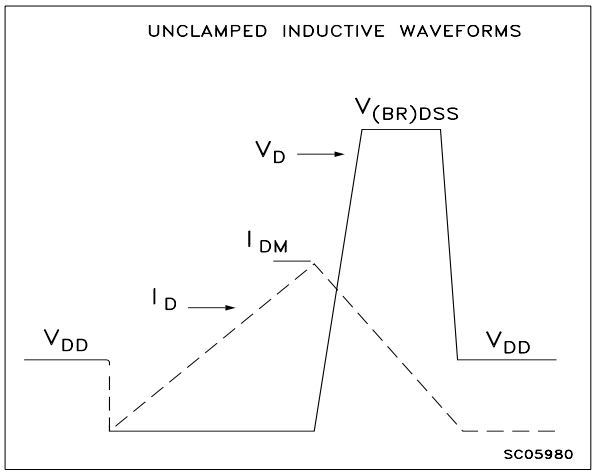


Fig. 3: Switching Times Test Circuit For Resistive Load

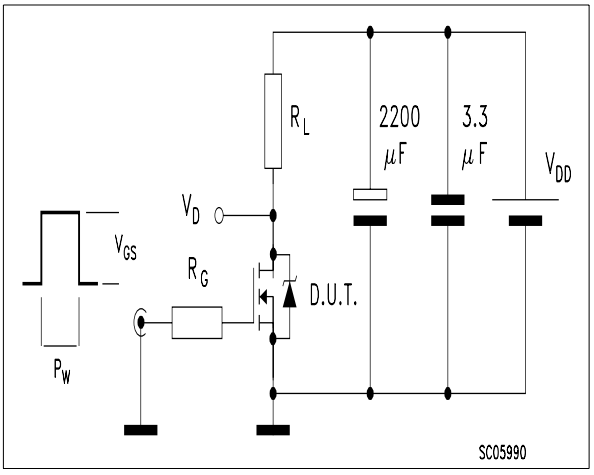


Fig. 4: Gate Charge test Circuit

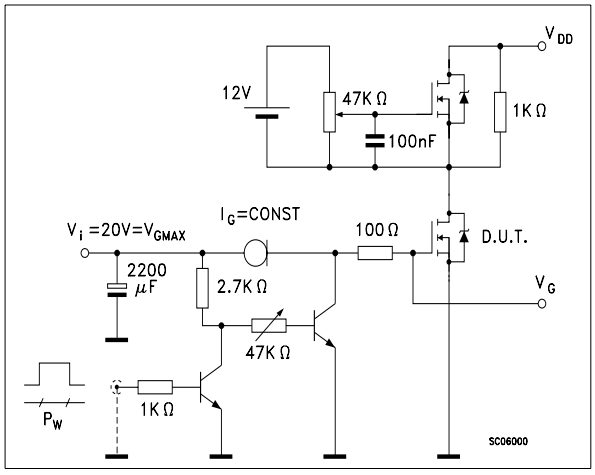
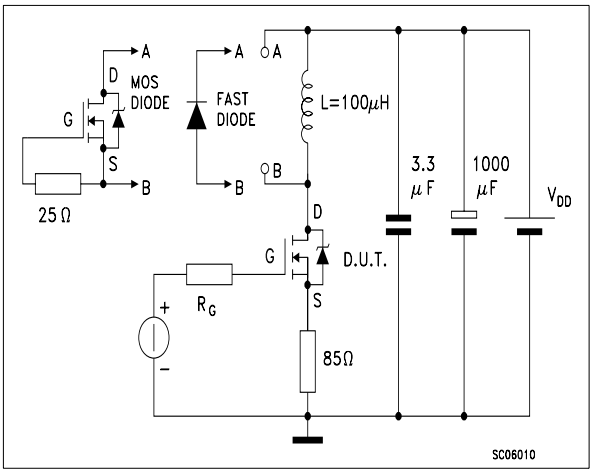
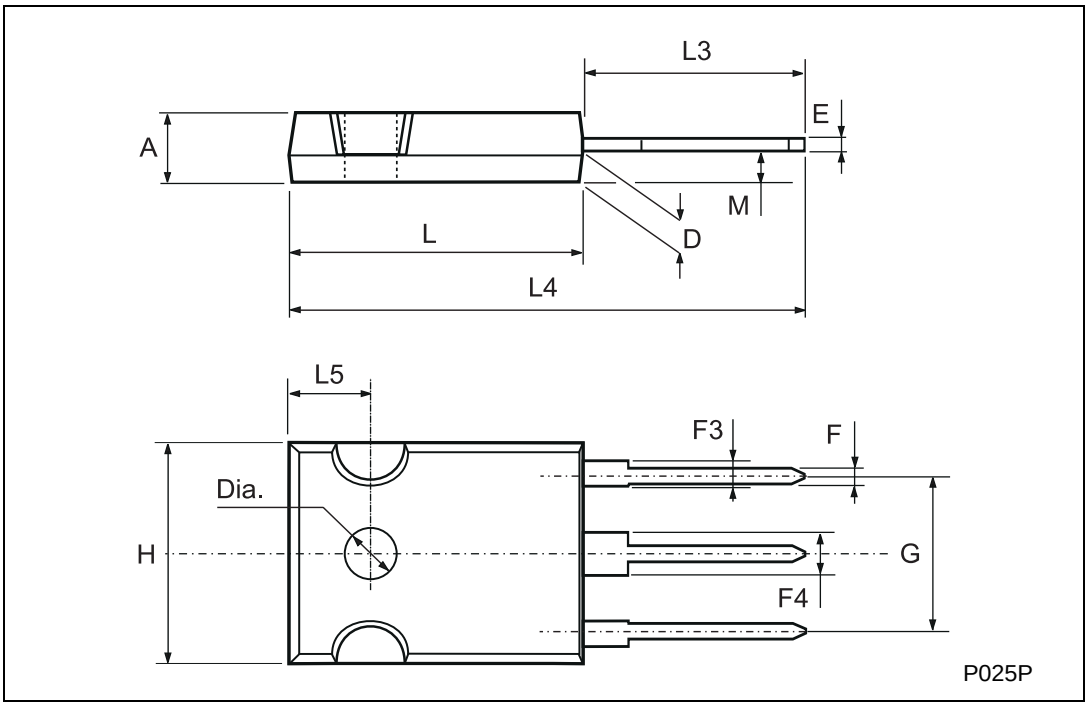


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



TO-247 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.7		5.3	0.185		0.209
D	2.2		2.6	0.087		0.102
E	0.4		0.8	0.016		0.031
F	1		1.4	0.039		0.055
F3	2		2.4	0.079		0.094
F4	3		3.4	0.118		0.134
G		10.9			0.429	
H	15.3		15.9	0.602		0.626
L	19.7		20.3	0.776		0.779
L3	14.2		14.8	0.559		0.582
L4		34.6			1.362	
L5		5.5			0.217	
M	2		3	0.079		0.118



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