



Is Now Part of



ON Semiconductor®

To learn more about ON Semiconductor, please visit our website at
www.onsemi.com

Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

ON Semiconductor and the ON Semiconductor logo are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.



74LVX3245

8-Bit, Dual-Supply Translating Transceiver with 3-State Outputs

Features

- Bidirectional Interface Between 3 V and 5 V Buses
- Inputs Compatible with TTL Level
- 3 V Data Flow at A-Port and 5 V Data Flow at B-Port
- Outputs Source / Sink: 24 mA
- Guaranteed Simultaneous Switching Noise Level and Dynamic Threshold Performance
- Implements Proprietary EMI Reduction Circuitry
- Functionally Compatible with the 74 Series 245

Description

The 74LVX3245 is a dual-supply, 8-bit translating transceiver designed to interface between a 3 V bus and a 5 V bus in a mixed 5 V supply environment. The Transmit/ Receive (T/R) input determines the direction of data flow. Transmit (active-HIGH) enables data from A-ports to B-ports; receive (active-LOW) enables data from B-ports to A-ports. The output enable input, when HIGH, disables both A- and B-ports by placing them in a high-impedance condition. The A-port interfaces with the 3 V bus; the B-port interfaces with the 5 V bus.

The 74LVX3245 is suitable for mixed-voltage applications, such as notebook computers using 3.3 V CPU and 5V peripheral components.

Related Resources

- [AN-5001 — Using Fairchild's LVX Low-Voltage Dual-Supply CMOS Translating Transceivers](#)

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
74LVX3245QSC	-40 to +85°C	24-Lead Quarter-Size Outline Package (QSOP), JEDEC MO-137, 0.150" Wide	Tubes
74LVX3245QSCX			Tape and Reel
74LVX3245MTC		24-Lead Thin-Shrink Small-Outline Package (TSSOP), JEDEC MO-153, 4.4 mm Wide	Tubes
74LVX3245MTCX			Tape and Reel

Logic Symbol

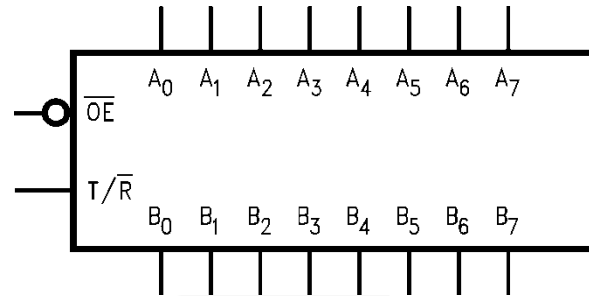


Figure 1. Logic Symbol

Pin Configuration

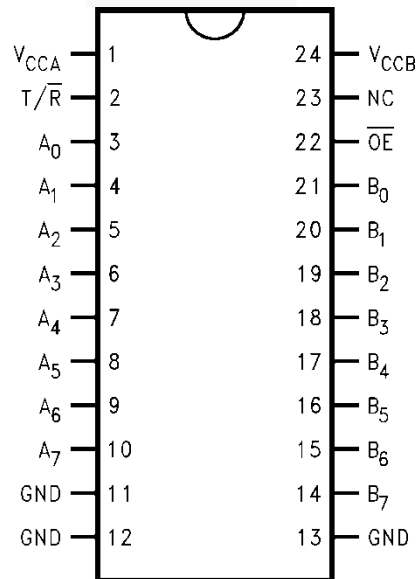


Figure 2. Pin Configuration

Pin Definitions

Pin #	Name	Description
1	V _{CCA}	Supply Voltage
2	T/R	Transmit/Receive Input
3, 4, 5, 6, 7, 8, 9, 10	A ₀ , A ₁ , A ₂ , A ₃ , A ₄ , A ₅ , A ₆ , A ₇	Port-A Inputs or 3-State Outputs
11, 12, 13	GND	Ground
14, 15, 16, 17, 18, 19, 20, 21	B ₇ , B ₆ , B ₅ , B ₄ , B ₃ , B ₂ , B ₁ , B ₀	Port-B Inputs or 3-State Outputs
22	/OE	Output Enable Input
23	NC	No Connect
24	V _{CCB}	Supply Voltage

Logic Diagram

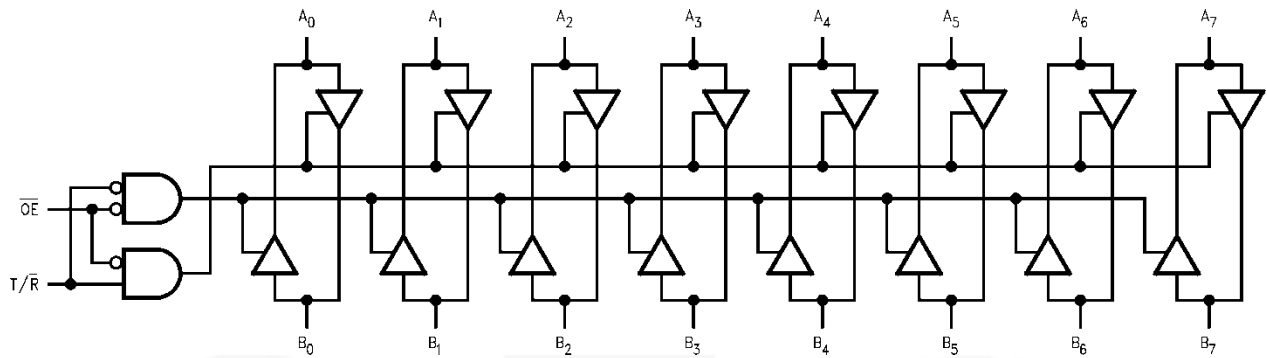


Figure 3. Logic Diagram

Table 1. Truth Table

Inputs		Outputs
/OE	T/R	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	HIGH-Z State

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{CCA}, V_{CCB}	Supply Voltage		-0.5	7.0	V
V_{IN}	DC Input Voltage; (/OE, T/R)		-0.5	$V_{CCA} + 0.5$	V
$V_{I/O}$	DC Input / Output Voltage	A_n	-0.5	$V_{CCA} \text{ to } +0.5$	V
		B_n	-0.5	$V_{CCB} \text{ to } +0.5$	
I_{IN}	DC Input Diode Current (/OE and T/R)			± 20	mA
I_{OK}	DC Output Diode Current			± 50	mA
I_O	DC Output Source or Sink Current			± 50	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	Output Pin		± 50	mA
		Maximum Current at I_{CCA}		± 100	
		I_{CCB}		± 200	
T_{STG}	Storage Temperature Range		-65	+150	°C
I_{SINK}	DC Latch-Up Source or Sink Current			± 300	mA
T_J	Maximum Junction Temperature Under Bias			+150	°C
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114		2500	V

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter		Min.	Max.	Unit
V_{CCA}	Supply Voltage		2.7	3.6	V
V_{CCB}			4.5	5.5	
V_I	Input Voltage (/OE and T/R)		0	V_{CCA}	V
$V_{I/O}$	DC Input / Output Voltage	A_n	0	V_{CCA}	V
		B_n	0	V_{CCB}	
T_A	Operating Temperature, Free Air		-40	+85	°C
$\Delta t / \Delta V$	Minimum Input Edge Rate (V_{IN} from 30 to 70% of V_{CC} , V_{CC} at 3.0 V, 4.5 V, and 5.5 V)			8	ns/V

Note:

1. Unused pins (inputs and I/O's) must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter		Conditions	V _{CCA} (V)	V _{CCB} (V)	T _A = -25°C		T _A =-40 to+85°C		Unit
						Typ.	Guaranteed Limits			
V _{IHA}	Minimum HIGH Level Input Voltage	A _n , T/R , /OE	V _{OUT} ≤ 0.1 V or ≥ V _{CC} - 0.1 V	3.6	5.0		2.0	2.0	V	
				2.7	5.0		2.0	2.0		
V _{IHB}		B _n			3.3	4.5		2.0		2.0
					3.3	5.5		2.0		2.0
V _{ILA}	Minimum LOW Level Input Voltage	A _n , T/R , /OE	V _{OUT} ≤ 0.1 V or ≥ V _{CC} - 0.1 V	3.6	5.0		0.8	0.8	V	
				2.7	5.0		0.8	0.8		
V _{ILB}		B _n			3.3	4.5		0.8		0.8
					3.3	5.5		0.8		0.8
V _{OHA}	Minimum HIGH Level Output Voltage		I _{OUT} =-100 μA	3.0	4.5	2.99	2.90	2.90	V	
			I _{OH} =-24 mA	3.0	4.5	2.65	2.35	2.25		
			I _{OH} =-12 mA	2.7	4.5	2.50	2.30	2.20		
			I _{OH} =-24 mA	2.7	4.5	2.30	2.10	2.00		
V _{OHB}	I _{OUT} =-100 μA	3.0	4.5	4.50	4.40	4.40				
	I _{OH} =-24 mA	3.0	4.5	4.25	3.86	3.76				
V _{OLA}	Minimum LOW Level Output Voltage		I _{OUT} =100 μA	3.0	4.5	0.002	0.100	0.100	V	
			I _{OH} =24 mA	3.0	4.5	0.210	0.360	0.440		
			I _{OH} =12 mA	2.7	4.5	0.110	0.360	0.440		
			I _{OH} =24 mA	2.7	4.5	0.220	0.420	0.500		
V _{OLB}	I _{OUT} =100 μA	3.0	4.5	0.002	0.100	0.100				
	I _{OH} =24 mA	3.0	4.5	0.180	0.360	0.440				
I _{IN}	Maximum Input Leakage Current; /OE, T/R		V _{IN} =V _{CCB} , GND	3.6	5.5		±0.1	±1.0	μA	
I _{OZA}	Maximum 3-State Output Leakage; A _n		V _{IN} =V _{IL} , V _{IH} ; /OE= V _{CCA} ; V _O =V _{CCA} , GND	3.6	5.5		±0.5	±5.0	μA	
I _{OZB}	Maximum 3-State Output Leakage; B _n		V _{IN} =V _{IL} , V _{IH} ; /OE= V _{CCA} ; V _O =V _{CCB} , GND	3.6	5.5		±0.5	±5.0	μA	
ΔI _{CC}	Maximum I _{CCT} /Input at	B _n	V _{IN} =V _{CCB} -2.1 V	3.6	5.5	1.00	1.35	1.50	mA	
		A _n , T/R , /OE	V _{IN} =V _{CCA} -0.6 V	3.6	5.5		0.35	0.50		
I _{CCA}	Quiescent V _{CCA} Supply Current		A _n =V _{CCA} or GND, B _n =V _{CCB} or GND, /OE=GND, T/R =GND	3.6	5.5		5	50	μA	
I _{CCB}	Quiescent V _{CCB} Supply Current		A _n =V _{CCA} or GND, B _n =V _{CCB} or GND, /OE=GND, T/R =V _{CCA}	3.6	5.5		8	80		

Continued on the following page...

DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V _{CCA} (V)	V _{CCB} (V)	T _A = -25°C	T _A =-40 to+85°C		Unit
					Typ.	Guaranteed Limits		
V _{OLPA}	Quiet Output Maximum Dynamic V _{OL} ^(2, 3)		3.3	5.0		0.8		V
V _{OLPB}			3.3	5.0		1.5		
V _{OLVA}	Quiet Output Minimum Dynamic V _{OL} ^(2, 3)		3.3	5.0		-0.8		V
V _{OLVB}			3.3	5.0		-1.2		
V _{IHDA}	Minimum HIGH Level Dynamic Input Voltage ^(2, 4)		3.3	5.0		2.0		V
V _{IHDB}			3.3	5.0		2.0		
V _{ILDA}	Maximum LOW Level Dynamic Input Voltage ^(2, 4)		3.3	5.0		0.8		V
V _{ILDB}			3.3	5.0		0.8		

Notes:

2. Worst-case package.
3. Maximum number of outputs defined as (n). Data inputs are driven 0 V to V_{CC} level; one output at GND.
4. Maximum number of data inputs (n) switching. (n-1) inputs switching 0 V to V_{CC} level. Input-under-test switching; V_{CC} level to threshold (V_{IHD}), 0V to threshold (V_{ILD}), f=1 MHz.

AC Electrical Characteristics

Symbol	Parameter	T _A =+25°C, C _L =50 pF, V _{CCA} =3.3 V ⁽⁵⁾ , V _{CCB} =5.0 V ⁽⁶⁾			T _A =-40 to +85°C, C _L =50 pF, V _{CCA} =3.3 V ⁽⁵⁾ , V _{CCB} =5.0 V ⁽⁶⁾		T _A =-40 to +85°C, C _L =50 pF, V _{CCA} =2.7 V, V _{CCB} =5.0 V		Unit
		Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t _{PHL} , t _{PLH}	Propagation Delay A to B	1.0	5.4	8.0	1.0	8.5	1.0	9.0	ns
		1.0	5.6	7.5	1.0	8.0	1.0	8.5	
	Propagation Delay B to A	1.0	5.1	7.5	1.0	8.0	1.0	8.5	
		1.0	5.7	7.5	1.0	8.0	1.0	8.5	
t _{PZL} , t _{PZH}	Output Enable Time /OE to B	1.0	4.8	8.0	1.0	8.5	1.0	9.0	ns
		1.0	6.3	8.5	1.0	9.0	1.0	9.5	
	Output Enable Time /OE to A	1.0	6.3	8.5	1.0	9.0	1.0	9.5	
		1.0	6.8	9.0	1.0	9.5	1.0	10.0	
t _{PHZ} , t _{PLZ}	Output Disable Time /OE to B	1.0	5.3	7.5	1.0	8.0	1.0	8.5	ns
		1.0	4.2	7.0	1.0	7.5	1.0	8.0	
	Output Disable Time /OE to A	1.0	5.3	8.0	1.0	8.5	1.0	9.0	
		1.0	3.7	6.5	1.0	7.0	1.0	7.5	
t _{OSHL} , t _{OSLH}	Output to Output Skew, Data to Output ⁽⁷⁾		1.0	1.5		1.5		1.5	ns

Notes:

5. Voltage range 3.3 V is 3.3 V ± 0.3 V.
6. Voltage range 5.0 V is 5.0 V ± 0.5 V.
7. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}). Parameter guaranteed by design.

Capacitance

Symbol	Parameter		Conditions	Typ.	Unit
C _{IN}	Input Capacitance		V _{CC} = Open	4.5	pF
C _{I/O}	Input / Output Capacitance		V _{CCA} = 3.3 V, V _{CCB} = 5.0 V	15	pF
C _{PD}	Power Dissipation Capacitance ⁽⁸⁾	A to B	V _{CCA} = 3.3 V, V _{CCB} = 5.0 V	55	pF
		B to A		40	

Note:

8. C_{PD} is measured at 10 MHz.

8-Bit Dual-Supply Translating Transceiver

The 74LVX3245 is a dual-supply device capable of bi-directional signal translation. This level shifting ability provides an efficient interface between low-voltage CPU local bus with memory and a standard bus defined by 5 V I/O levels. The device control inputs can be controlled by the low-voltage CPU and core logic or a bus arbitrator with 5 V I/O levels.

Manufactured on a sub-micron CMOS process, the 74LVX3245 is ideal for mixed voltage applications such as notebook computers using 3.3 V CPUs and 5 V peripheral devices.

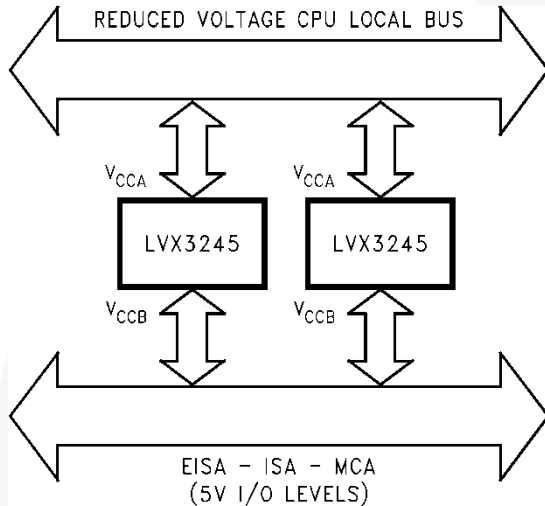


Figure 4. Application Example

Power-Up Considerations

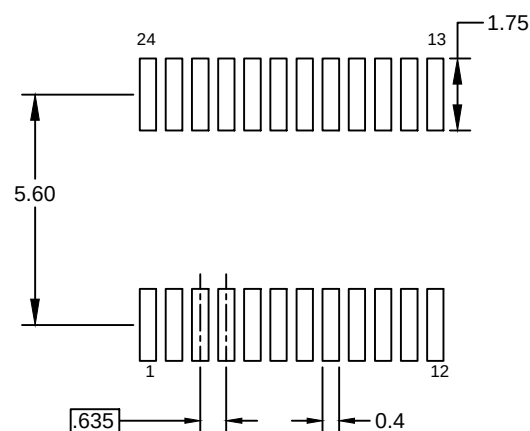
To ensure that the system does not experience unnecessary I_{CC} current draw, bus contention, or oscillations during power up; the following guidelines should be followed to (refer to Table 2):

- Power up the control side of the device first (V_{CCA}).
- /OE should ramp with or ahead of V_{CCA} . This helps guard against bus contention.
- The Transmit/Receive (T/R) control pin should ramp with V_{CCA} . This ensures that the A-port data pins are configured as inputs. With V_{CCA} receiving power first, the I/O port should be configured as an input to help guard against bus contention and oscillations.
- A-side data inputs should be driven to a valid logic level. This prevents excessive current draw.

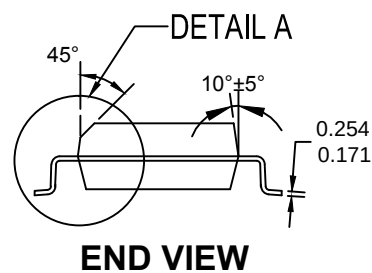
The above steps ensure that there are no bus contentions or oscillations, and therefore no excessive current draw occurs during the power-up cycling. These steps help prevent possible damage to the translator devices and potential damage to other system components.

Table 2. Low Voltage Translator Power-Up Sequencing

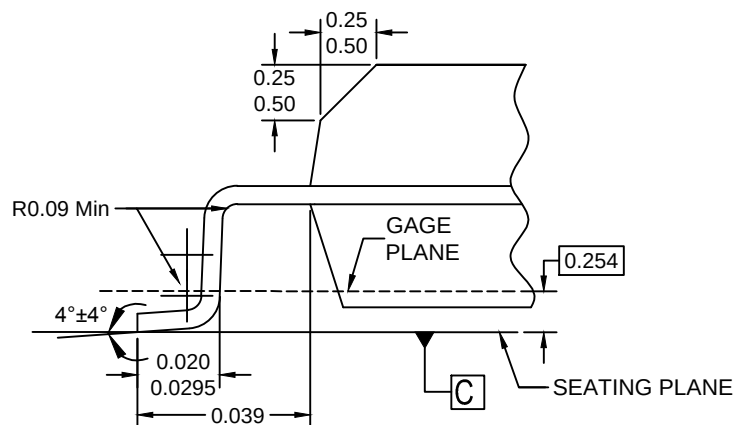
Device	V_{CCA}	V_{CCB}	T/R	/OE	A-Side I/O	B-Side I/O	Floatable Pin Allowed
74LVX3245	3 V (Power-Up First)	5 V Configurable	Ramp with V_{CCA}	Ramp with V_{CCA}	Logic 0 V or V_{CCA}	Outputs	No



LAND PATTERN RECOMMENDATION



END VIEW



DETAIL A

- A. THIS PACKAGE CONFORMS TO JEDEC MO-137 VARIATION AE
- B. ALL DIMENSIONS ARE IN MILLIMETERS
- C. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 2009.
- D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
- E. LAND PATTERN STANDARD: SOP63P600X175-24M.
- F. DRAWING FILE NAME: MKT-MQA24rev3



ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada

Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910

Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local
Sales Representative