Design Example Report

Title	***10 W Power Supply using DPA423P***
Specification	Input: 37-57 VDC Output: 3.3V/2.0A, 5V/200mA, 12V/200mA
Application	VoIP phone
Author	Power Integrations Applications Department
Document Number	DER-96
Date	September 12, 2005
Revision	1.0

Summary and Features

This document is an engineering prototype report describing a VoIP power supply utilizing DPA423P.

- Eliminates LM78xx linear-regulators on 5 V
- Low-cost 12 V linear-reg. with short circuit protection provided by main supply
- High Efficiency (> 70% at 48 VDC)
- Low EMI signature (both radiated and conducted emissions)
- Low Parts Count
- Built-in input short circuit protection on all outputs
- Carefully designed for low EMI

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Important Notes:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolated source to provide power to the prototype board.

Design Reports contain a power supply design specification, schematic, bill of materials, and transformer documentation. Performance data and typical operation characteristics are included. Typically only a single prototype has been built.

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1 Introduction

This document is an engineering prototype report describing a VoIP prototype power supply utilizing DPA423P. The power supply delivers 10 W continuous from an input of 37 to 57 VDC.

The design has been optimized to minimize radiated EMI emissions.

In the EMI section of the report it can be seen that there is a dramatic improvement in radiated EMI over the existing production DPA423 design.

This document provides complete design information including specification, schematic, bill of material and transformer design and construction information. The document also provides performance information.

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2 Power Supply Specification

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	37		57	VDC	
Under-Voltage	V_{IN_UV}		34		VDC	
Over-Voltage	V_{IN_OV}		N/A		VDC	
Output						
Output Voltage 1	V_{OUT1}	3.135	3.3	3.465	V	± 5%
Output Ripple Voltage 1	$V_{RIPPLE1}$			100	mVp-p	20 MHz bandwidth
Output Current 1	I_{OUT1}	0		2	A	
Output Voltage 2	V_{OUT2}	4.75	5	5.25	V	± 5%
Output Ripple Voltage 2	$V_{RIPPLE2}$			100	mVp-p	20 MHz bandwidth
Output Current 2	I_{OUT2}	0		200	mA	
Output Voltage 3	V_{OUT3}	11.4	12	12.6	V	± 5%
Output Ripple Voltage 3	$V_{RIPPLE3}$			250	mVp-p	20 MHz bandwidth
Output Current 3	I_{OUT3}	0		200	mA	
Total Output Power						
Average Output Power	P_{OUT1}		6.6		W	
Average Output Power	P_{OUT2}		1		W	
Average Output Power	P_{OUT2}		2.4		W	
Average Output Power	P_{OUT_TOTAL}		10		W	
Average Output Power	P_{OUT_FAULT}				W	
Full Load Efficiency	η		70		%	
Environmental						
Conducted EMI		Meets CISPR22B / EN55022B				
Safety		Designed to meet IEC950, UL1950 Class II				
Ambient Temperature	T_{AMB}	0		40	^{o}C	Forced airflow

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3 Schematic

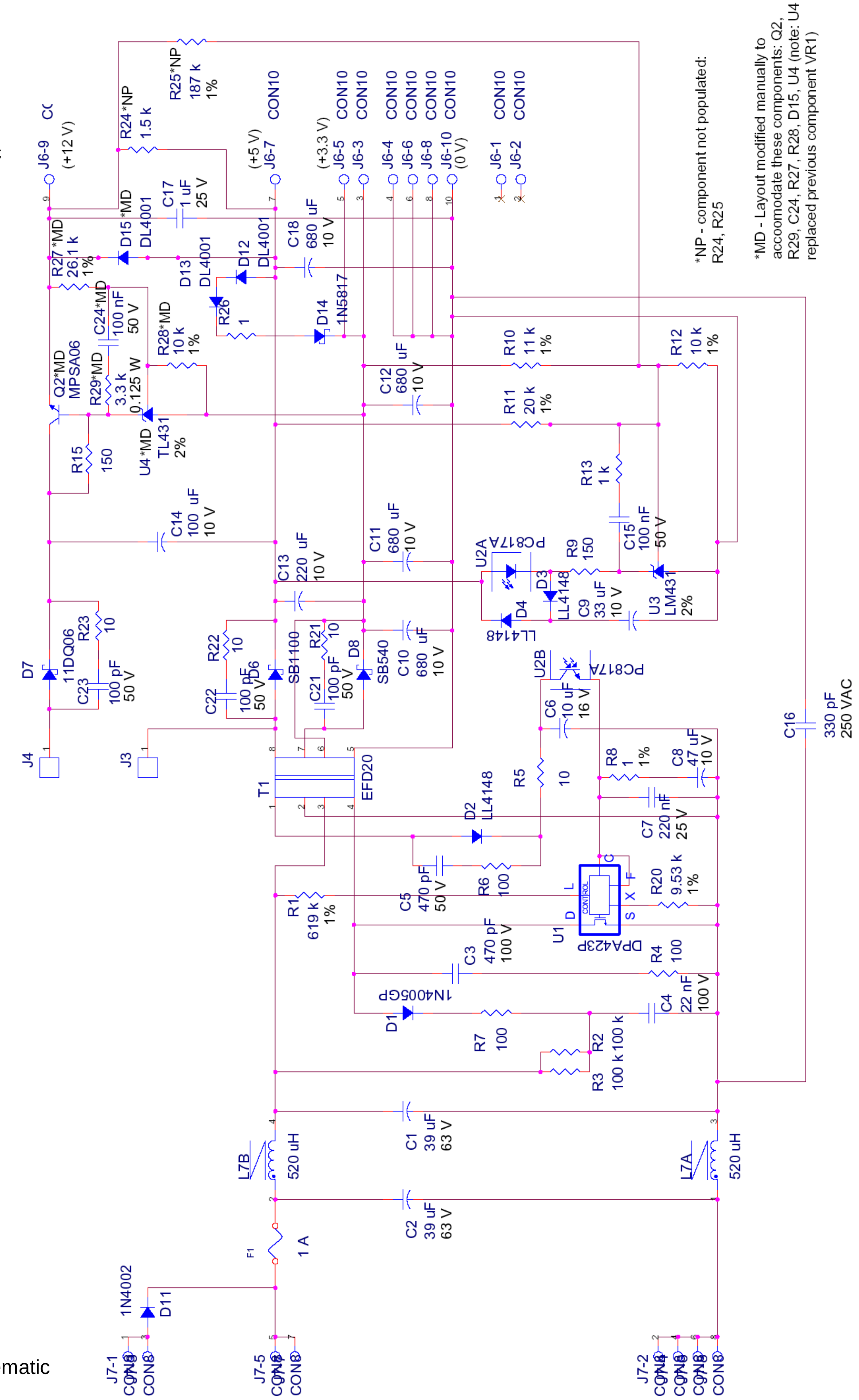

Figure 1 – Schematic

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4 Circuit Operation

4.1 General

The power supply uses a DPA423 device (U1), with integrated MOSFET and controller, in an isolated flyback configuration. The circuit also uses the under-voltage shutdown feature of the device along with current limit setting to minimize transformer size. The device operates at a switching frequency of 300 kHz.

4.2 Description

The input fuse F1 protects the supply against catastrophic failure – although the built-in protection features of the DPA-Switch should render this redundant.

The components C1, C2 and L7 form a pi-filter to limit both conducted and radiated EMI emissions. These components work to limit EMI emissions in conjunction with y-capacitor C16 and the shielding in the transformer. Resistor R1 programs the input under voltage startup threshold (and over voltage shutdown voltage). Diode D1, R7, C4, R2, and R3 implement an RCD clamp circuit to limit the leakage inductance spike on the Drain pin. Capacitor C3 and resistor R4 implement a snubber to limit high frequency ringing on the due to drain switching. Diode D2, R5 and C6 implement a bias voltage supply to provide operating power to the DPA-Switch (U4) with integrated PWM, controller and main switching MOSFET. Resistor R6 and C5 provide diode snubber for D2. Resistor R20 programs the current limit of the DPA-Switch. Capacitors C7 and C8 provide device decoupling with C8 also program the startup and auto-restart period of the device. Resistor R8 provides feedback compensation in conjunction with C8. The inductance of transformer T1 provides the energy storage and conversion component of the circuit.

The 3.3 V output is rectified and filtered by diode D8 and capacitors C10, C11 with C12 provided output decoupling. The 5 V output is DC-stacked on the regulated DC output of 3.3 V and is rectified and filtered by diode D6 and capacitors C13 with capacitor C18 providing output decoupling. The 12 V output is AC-stacked on the 5 V transformer winding and is rectified and filtered by diode D7 and capacitor C14 with capacitor C17 providing output decoupling. Transistor Q2 and components R15, R26, R27, R28, C24, U4 implement a linear regulator to eliminate peak charging voltage from the 12 V output. Resistor R26, D12, D13 and D14 all form pre-load networks between the outputs to improve cross-regulation. Components R21, C21, R22, C22, R23 and C23 provide snubbing on output diodes. Diode pulls down the 5 V output when 12 V output is shorted thus forcing DPA-switch auto-restart. Using this diode removes the need for short-circuit protection in the 12 V linear regulator circuit.

Resistors R11 and R10 sense the voltages on 5 V and 3.3 V outputs respectively. In conjunction with R12 they provide the input signal for the LM431 (U3) reference. Components R13 and C15 provide compensation for U3, to make sure that it’s frequency response is limited only to low-frequency signals. Resistor R9 programs the high-frequency gain of the control loop and with opto-diode U2A transmits the feedback signal. Diode D3 and C9 provide a soft-finish circuit to limit output overshoot at startup. Diode D4

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discharges C9 when the output of the power supply drops out of regulation. Opto-transistor U2B feeds the control signal back to the DPA-Switch.

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5 Bill Of Materials

Item	Qty.	Ref.	Description	Mfg Part Number	Mfg
1	2	C1 C2	39 uF, 63, Electrolytic, Low ESR, 610 mOhm, (6.3 x 15)	LXZ63VB39RM515LL	United Chemi-Con
2	1	C3	470 pF, 100 V, Ceramic, X7R	ECU-S2A471KBA	Panasonic
3	1	C4	22 nF, 100 V, Ceramic, X7R	ECU-S2A223KBA	Panasonic
4	1	C5	470 pF 50 V, Ceramic, X7R, 0603	ECJ-1VC1H471J	Panasonic
5	1	C6	10 uF, 16 V, Electrolytic, Gen. Purpose, (5 x 11)	KME16VB10RM5X11 LL	United Chemi-Con
6	1	C7	220 nF, 25 V, Ceramic, X7R, 0805	ECJ-2YB1E224K	Panasonic
7	1	C8	47 uF, 10 V, Electrolytic, Gen. Purpose, (5 x 11)	KME10VB22RM5X11 LL	United Chemi-Con
8	1	C9	33 uF, 10 V, Electrolytic, Gen. Purpose, (5 x 11)	KME10VB33RM5X11 LL	United Chemi-Con
9	4	C10 C11 C12 C18	680 uF, 10 V, Electrolytic, Very Low ESR, 56 mOhm, (8 x 15)	KZE10VB681MH15LL	United Chemi-Con
10	1	C13	220 uF, 10 V, Electrolytic, Very Low ESR, 130 mOhm, (6.3 x 11)	KZE10VB221MF11LL	United Chemi-Con
11	1	C14	100 uF, 10 V, Electrolytic, Very Low ESR, 300 mOhm, (5 x 11)	KZE10VB101ME11LL	United Chemi-Con
12	1	C15	100 nF, 50 V, Ceramic, X7R, 0805	ECU-V1H221KBN	Panasonic
13	1	C16	330 pF, Ceramic Y1	440LT33	Vishay
14	1	C17	1 uF, 25 V, Ceramic, X7R, 1206	ECJ-3YB1E105K	Panasonic
15	3	C21 C22 C23	100 pF 50 V, Ceramic, X7R, 0603	ECJ-1VC1H101J	Panasonic
16	1	C24	100 nF, 50 V, Ceramic, X7R	ECU-S1H104KBB	Panasonic
17	1	D1	600 V, 1 A, Rectifier, Glass Passivated, 2 us, DO-41	1N4005GP	Vishay
18	3	D2 D3 D4	75 V, 0.15 A, Fast Switching, 4 ns, MELF	LL4148	Diode Inc.
19	1	D6	100 V, 1 A, Schottky, DO-41	SB1100	Fairchild
20	1	D7	60 V, 1.1 A, Schottky, DO-41	11DQ06	International Rectifier
21	1	D8	40 V, 5 A, Schottky, DO-201AD	SB540	Vishay
22	1	D11	100 V, 1 A, Rectifier, DO-41	1N4002	Vishay
23	3	D12 D13 D15	50 V, 1 A, Rectifier, Glass Passivated, DO-213AA (MELF)	DL4001	Diodes Inc
24	1	D14	20 V, 1 A, Schottky, DO-41	1N5817	Vishay
25	1	F1	1 A, 250V, Slow, TR5	3,721,100,041	Wickman
26	2	J3 J4 (FL1, FL2)	PCB Terminal Hole, 18 AWG	N/A	N/A
27	1	J6	10 Position, Fem/Male (5 x 2 header, Top & Bot Entry, 0.1 pitch, Vertical	22-28-4100	Molex
28	1	J7	8 Position, Fem/Male (4 x 2) header, Top &		

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			Bot Entry, 0.1 pitch, Vertical		
29	1	L7	520 uH,xA, Powdered Iron Core, Toroidal, 4 Pin	Custom	Custom
30	1	Q2	NPN, Small Signal BJT, 80 V, 0.5 A, TO-92	MPSA06	Fairchild
31	1	R1	619 k, 1%, 1/8 W, Metal Film, 0805	ERJ-6ENF6193V	Panasonic
32	2	R2 R3	100 k, 5%, 1/4 W, Metal Film, 1206	ERJ-8GEYJ104V	Panasonic
33	1	R4	100 R, 5%, 1/8 W, Metal Film, 0805	ERJ-6GEYJ101V	Panasonic
34	1	R5	10 R, 5%, 1/10 W, Metal Film, 0603	ERJ-3GEYJ106V	Panasonic
35	2	R6 R7	100 R, 5%, 1/10 W, Metal Film, 0603	ERJ-3GEYJ101V	Panasonic
36	1	R8	1 R, 1%, 1/16 W, Metal Film, 0603	ERJ-3EKF1004V	Panasonic
37	2	R9 R15	150 R, 5%, 1/10 W, Metal Film, 0603	ERJ-3GEYJ151V	Panasonic
38	1	R10	8.66 k, 1%, 1/16 W, Metal Film, 0603	ERJ-3EKF8661V	Panasonic
39	1	R11	15.8 k, 1%, 1/4 W, Metal Film, 1206	ERJ-8ENF1582V	Panasonic
40	1	R12	10 k, 1%, 1/8 W, Metal Film, 0805	ERJ-6ENF1002V	Panasonic
41	1	R13	1 k, 5%, 1/10 W, Metal Film, 0603	ERJ-3GEYJ102V	Panasonic
42	1	R20	9.53 k, 1%, 1/4 W, Metal Film, 1206	ERJ-8ENF9531V	Panasonic
43	3	R21 R22 R23	10 R, 5%, 1/10 W, Metal Film, 0603	ERJ-3GEYJ100V	Panasonic
44	0	R24 *NP	1.5 k, 5%, 1/8 W, Metal Film, 0805	ERJ-6GEYJ152V	Panasonic
45	0	R25 *NP	150 k, 1%, 1/16 W, Metal Film, 0603	ERJ-3EKF1503V	Panasonic
46	1	R26	1 R, 5%, 1/8 W, Metal Film, 0805	ERJ-6GEYJ1R0V	Panasonic
47	1	R27	26.1 k, 1%, 1/4 W, Metal Film	MFR-25FBF-26K1	Yageo
48	1	R28	10 k, 1%, 1/4 W, Metal Film	MFR-25FBF-10K0	Yageo
49	1	R29	3.3 k, 5%, 1/8 W, Carbon Film	CFR-12JB-3K3	Yageo
50	1	T1	Bobbin, EFD20, Horizontal, 8 pins	YW-272-03B	Yih-Hwa Enterprises
51	1	U1	DPA-Switch, DPA423P, DIP-8	DPA423P	Power Integrations
52	1	U2	Opto coupler, 35 V, CTR 80-160%, 4-DIP	ISP817A, PC817X1	Isocom, Sharp
53	1	U3	2.495 V Shunt Regulator IC, 2%, -40 to 85C, SOT23	LM431AIM	National Semiconductor
54	1	U4	2.495 V Shunt Regulator IC, 2%, 0 to 70C, TO-92	TL431CLP	Texas Instruments
	68	**Total**			

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6 Layout

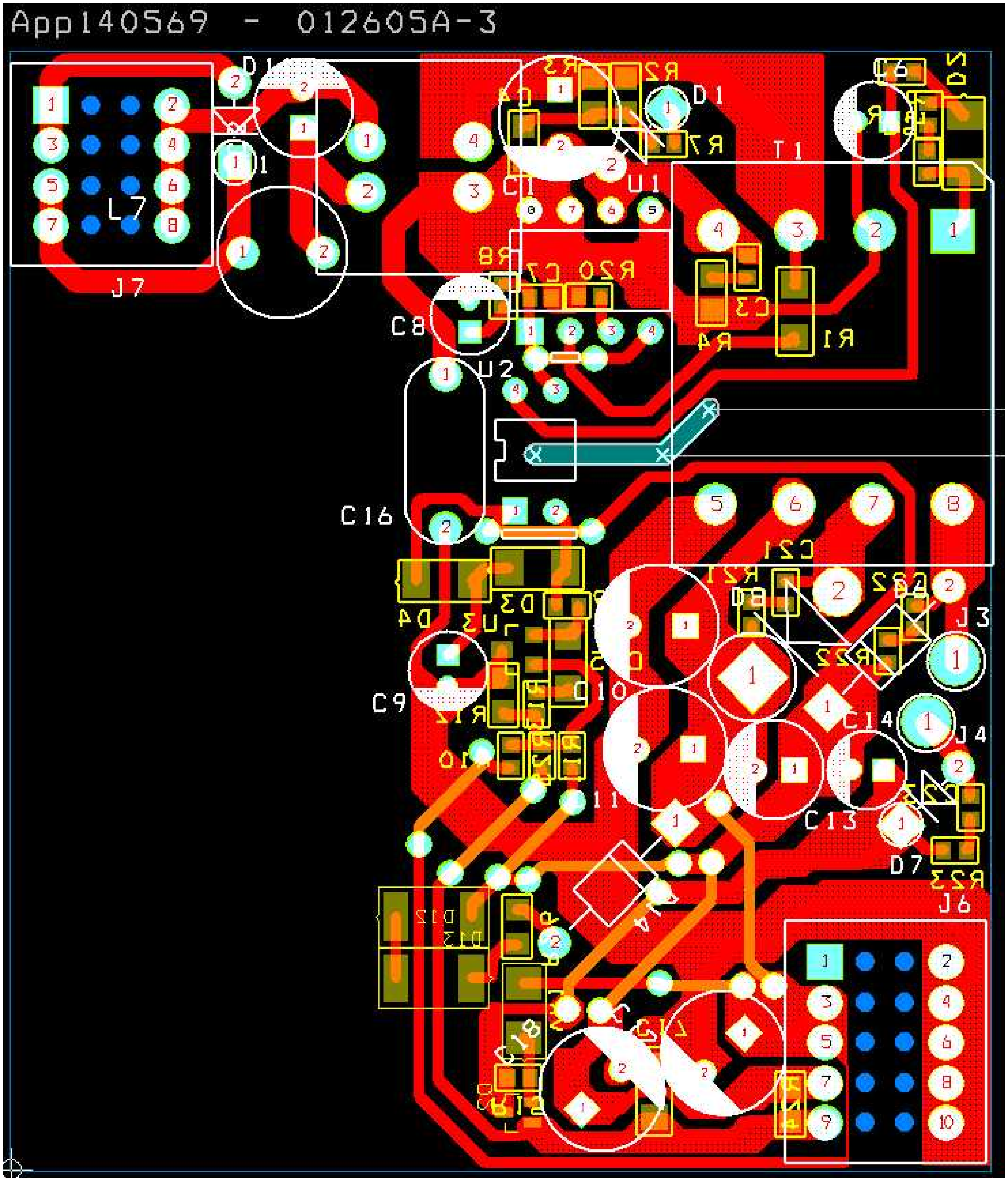

Figure 2 – PC-Board Layout (see schematic for *MP and *NP parts)

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7 Transformer Design Spreadsheet

061704; Rev.1.11; Copyright Power Integrations Inc. 2004	**INPUT**	INFO	OUTPUT	UNITS	DPASwitch_Flyback_061704 - Continuous/Discontinuous mode Spreadsheet. Copyright 2004 Power Integrations
ENTER APPLICATION VARIABLES					**App140569 - EFD20 - 010605a**
VDCMIN	37			Volts	Minimum DC Input Voltage
VDCMAX	57			Volts	Maximum DC Input Voltage
VO	3.3			Volts	Output Voltage
PO	10	Comment		Watts	Verify temperature rise for continuous power. P and G packages may be thermally limited
n	0.8				Efficiency Estimate
Z			0.7		Loss Allocation Factor, (0.7 Recommended)
VB	14			Volts	Bias Voltage (Recommended between 12V and 18V)
UV AND OV PARAMETERS					
		min	max		
VUVOFF		30.8802	34.06899	Volts	Minimum undervoltage On-Off threshold
VUVON		33.11235	35.66338	Volts	Maximum undervoltage Off-On threshold (turn-on)
VOVON		77.1176	-	Volts	Minimum overvoltage Off-On threshold
VOVOFF			97.52584	Volts	Maximum overvoltage On-Off threshold (turn-off)
RL			637.7573	k-Ohms	
ENTER DPASWITCH VARIABLES					
DPASWITCH	**DPA423P**			16VDC	36 VDC
Chosen Device	#N/A		Power Out	6W	13W
ILIMITMAX	#N/A	1.34		Amps	From DPASWITCH Data Sheet
Frequency	F				Enter 'F' for fS = 400KHz and 'L' for fS = 300KHz
fS	#N/A			Hertz	DPASWITCH Switching Frequency
VOR	38		38	Volts	Reflected Output Voltage
KI	0.80		0.8		Current Limit Reduction Factor
ILIMITEXT			0.928	Amps	Minimum External Current limit
RX			9.501216	k-Ohms	Resistor from X pin to source to set external current limit
VDS	1			Volts	DPASWITCH on-state Drain to Source Voltage
VD	0.45			Volts	Output Winding Diode Forward Voltage Drop
VDB	0.7			Volts	Bias Winding Diode Forward Voltage Drop
KRP/KDP	0.40				Ripple to Peak Current Ratio (0.2 < KRP < 1.0 : 1.0< KDP<6.0)
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type	**efd20**				Selected Transformer Core
Core Manuf					
Bobbin Manuf					
Core		EFD20		P/N:	EFD20-3F3-Exxx-xx
Bobbin		EFD20_Bo		P/N:	CPHS-EFD20-1S-10P-T
AE			0.31	cm^2	Core Effective Cross Sectional Area
LE			4.7	cm	Core Effective Path Length
AL			1200	nH/T^2	Ungapped Core Effective Inductance
BW			13.5	mm	Bobbin Physical Winding Width
M	0			mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L	2				Number of Primary Layers
NS	3				Number of Secondary Turns

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CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX			0.513514		Maximum Duty Cycle
IAVG			0.337838	Amps	Average Primary Current
IP			0.822368	Amps	Peak Primary Current
IR			0.328947	Amps	Primary Ripple Current
IRMS			0.476332	Amps	Primary RMS Current
TRANSFORMER PRIMARY DESIGN PARAMETERS					
LP			144.7851	uHenries	Primary Inductance
NP			30.4		Primary Winding Number of Turns
NB			11.76		Bias Winding Number of Turns
ALG			156.6667	nH/T^2	Gapped Core Effective Inductance
BP			1425.727	Gauss	Peak Flux density during transients (Limit to 3000 Gauss)
BM			1263.441	Gauss	Maximum Flux Density
BAC			252.6882	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur			1447.793		Relative Permeability of Ungapped Core
LG			0.216191	mm	Gap Length (Lg >> 0.051 mm)
BWE			27	mm	Effective Bobbin Width
TRANSFORMER SECONDARY DESIGN PARAMETERS					
ISP			8.333333	Amps	Peak Secondary Current
ISRMS			4.698092	Amps	Secondary RMS Current
IO			3.030303	Amps	Power Supply Output Current
IRIPPLE			3.590172	Amps	Output Capacitor RMS Ripple Current
VOLTAGE STRESS PARAMETERS					
VDRAIN			156.8	Volts	Maximum Drain Voltage (Includes Effect of Leakage Inductance)
PIVS			8.925	Volts	Output Rectifier Maximum Peak Inverse Voltage
PIVB			36.05	Volts	Bias Rectifier Maximum Peak Inverse Voltage
ADDITIONAL OUTPUTS					
V_OUT2	1.7330			Volts	Auxiliary Output Voltage
VD_OUT2	0.8000			Volts	Auxiliary Diode Forward Voltage Drop
N_OUT2			2.0264		Auxiliary Number of Turns
PIV_OUT2			5.5325	Volts	Auxiliary Rectifier Maximum Peak Inverse Voltage
V_OUT3	6.9			Volts	Auxiliary Output Voltage
VD_OUT3	0.7			Volts	Auxiliary Diode Forward Voltage Drop
N_OUT3			6.08		Auxiliary Number of Turns
PIV_OUT3			18.3	Volts	Auxiliary Rectifier Maximum Peak Inverse Voltage

Note1: the output Vout2 is DC-stacked on top of Vout1 (after the Vout1 rectifier diode), the output Vout3 is AC-stacked on top of the Vout2 winding (before Vout2 rectifier diode).

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8 Transformer Specification

8.1 Transformer Winding

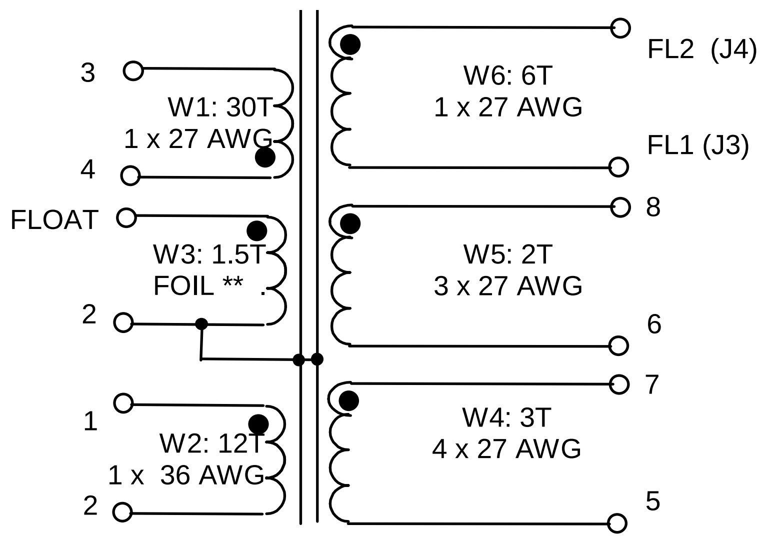

Figure 3 – Transformer Electrical Diagram (** denotes reverse wound)

8.2 Electrical Specifications

Electrical Strength	Non-isolated	N/A
Primary Inductance	Pins 3-4, all other windings open, measured at 300 kHz, 0.4 VRMS	145 µH, -0/+20%
Resonant Frequency	Pins 3-4, all other windings open	5 MHz (Min.)
Primary Leakage Inductance	Pins 3-4, with Pins 5,6,7,8 shorted, measured at 300 kHz, 0.4 VRMS	5 uH (Max.)

8.3 Materials

Item	Description
[1]	Core: EFD20 ALG=157 nH/t^2 (core 3F3 material)
[2]	Bobbin: EFD20 8-pin horizontal
[3a]	27AWG Doubled insulated
[3b]	36 AWG Doubled insulated
[3c]	1 mil foil
[4]	Prepared foil – see assembly diagram.
[6]	Tape:
[8]	Varnish

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8.4 Transformer Build Diagram

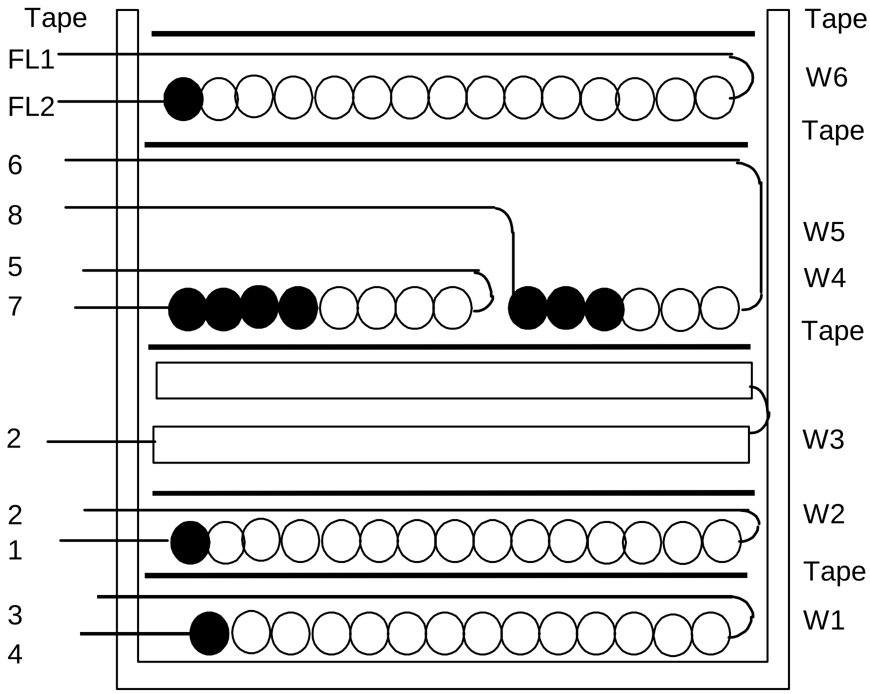

Figure 4 – Transformer Build Diagram

8.5 Transformer Construction

W1	Start at Pin 4. Wind 30 turns item [3a]. Finish on pin 3
Tape	Use layer of item [6].
W2	Start at Pin 1. Wind 12 turns item [3b]. Spread evenly across bobbin. Finish on pin 2
Tape	Use layer of item [6].
W3	Start at Pin 2. Wind reverse direction 1.5 turns of item [4]. Finish winding and leave floating in stack.
Tape	Use layer of item [6].
W4	Start at Pins 7. Wind 3 turns quad-filar item [3a]. Spread evenly across bobbin. Finish temporarily on pin 1.
W5	Start at Pin 8. Wind 2 turns tri-filar item [3a]. Spread evenly across bobbin, filling in the gaps in the previous W3. Finish on pin 6.
	Move temporary connection from Pin 1 to Pin 5.
Tape	Use layer of item [6].
W6	Start at FL2. Wind 6 turns item [3a]. Spread evenly across bobbin. Finish on FL1.
Outer Wrap	Wrap windings with 3 layers of tape [item [7].
Core Ground	Use copper self-adhesive tape touching core on all four sides. Make connection from this tape to pin 2 of bobbin. Note: this is not a “belly-band”, this is instead purely to electrically ground the core
Final Assembly	Assemble and secure core halves. Varnish impregnate (item [8]).

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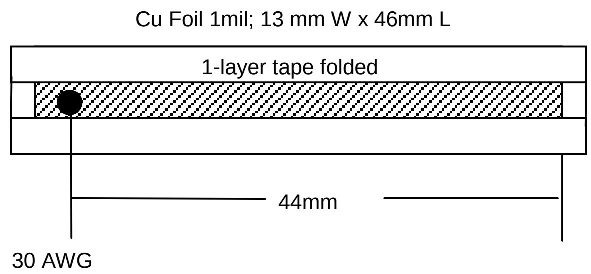
8.5.1 WD#3 Copper Foil build diagram:



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9 Inductor Specification

9.1 Inductor Winding

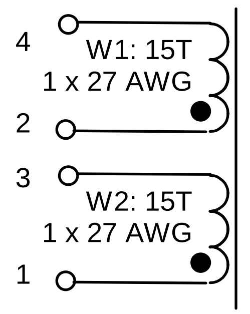

Figure 5 – Inductor Electrical Diagram

9.2 Electrical Specifications

Electrical Strength	Non-isolated	N/A
Primary Inductance	Pins 4-2, all other windings open, measured at 300 kHz, 0.4 VRMS	520 µH, -0/+20%
Resonant Frequency	Pins 4-2, all other windings open	3.9 MHz (Min.)
Primary Leakage Inductance	Pins 4-2, with Pins 1,2,3,5,6,8 shorted, measured at 300 kHz, 0.4 VRMS	3.5 uH (Max.)

9.3 Materials

Item	Description
[1]	Core: Fair-rite - 5975000201 (diameter 9.5mm, Al=4400)
[2]	Bobbin – 8 pin former
[3a]	27AWG Doubled insulated
[8]	Hot-set glue

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9.4 Inductor Footprint Diagram

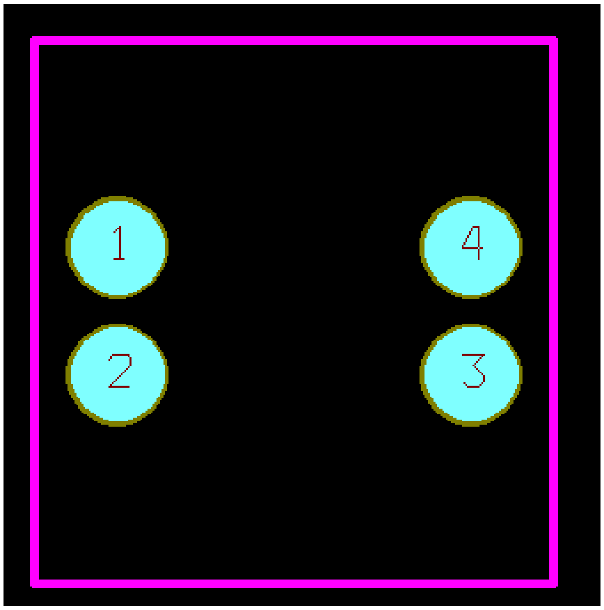

Figure 6 – Transformer Footprint – Top Side View Diagram

9.5 Inductor Construction

W1	Start at Pin 2. Wind 15 turns item [3a]. Finish on pin 4
W2	Start at Pin 1. Wind 15 turns item [3a]. Finish on pin 3
Outer Wrap	Wrap windings with 3 layers of tape [item [7].
Final Assembly	Assemble and secure core halves. Impregnate (item [8]).

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10 Performance

10.1 Efficiency

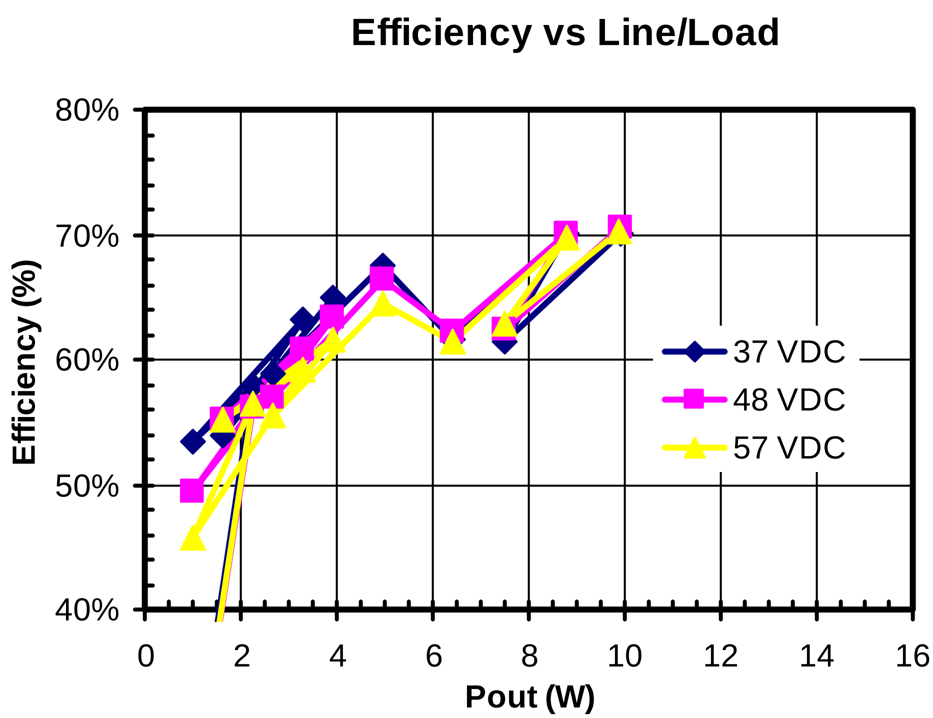

Figure 7 – Efficiency vs. Input Voltage and Output Load, Room Temperature

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10.2 Regulation vs. Load

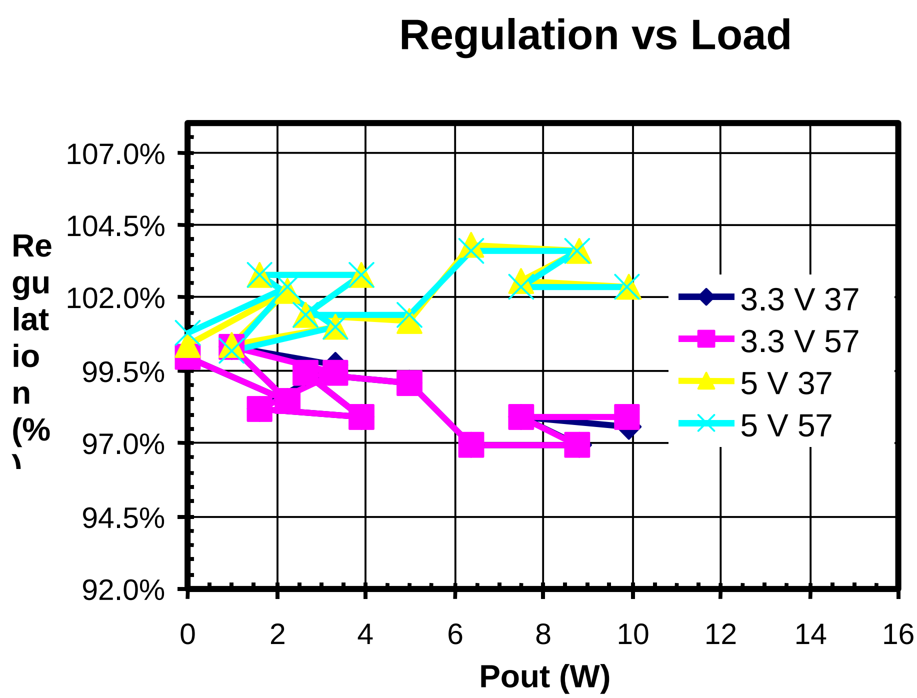

Figure 8 – Output Regulation vs. Output Load for 3.3 V and 5 V Outputs, Room Temperature

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10.3 Regulation vs. Load

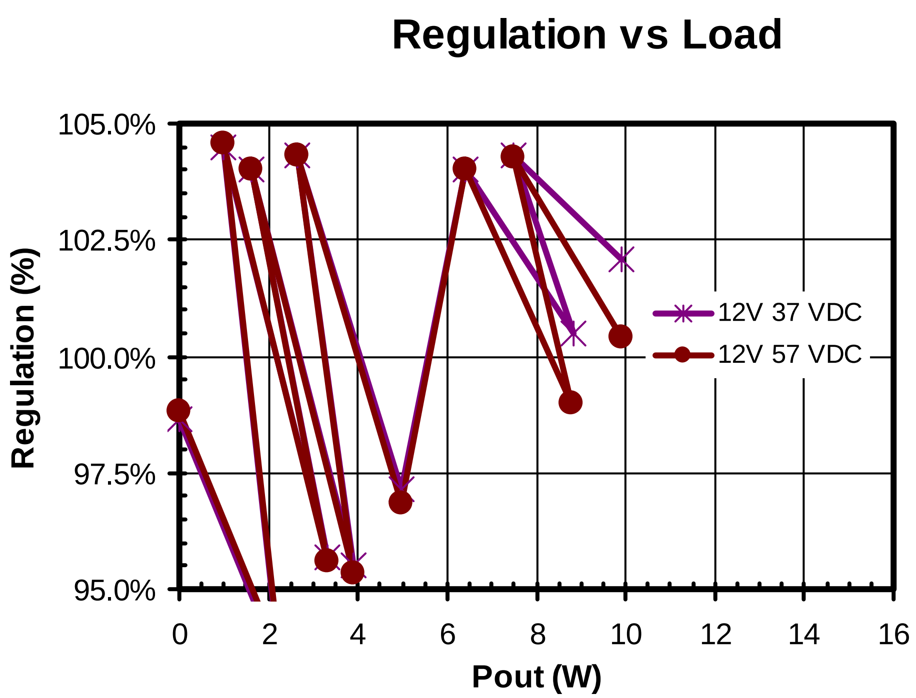

Figure 9 – Output Regulation vs. Output Load for 12 V Output, Room Temperature

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10.4 Raw Performance Data

It can be seen from the data below, that the power supply meets the regulation requirements even without need for a linear-regulator on the 5 V output. Also the efficiency of 70.5% at 48 VDC very high compared to alternate solutions.

Vin (DC)	Iin (A)	Vout1 (V)	Iout1 (A)	Vout2 (V)	Iout2 (A)	Vout3 (V)	Iout3 (A)
37.6	0.021	3.3	0	5.02	0	11.84	0
37.6	0.103	3.25	0	5.11	0	11.21	0.2
37.6	0.05	3.31	0	5.02	0.2	12.54	0
37.6	0.139	3.29	0	5.05	0.2	11.48	0.2
37.6	0.08	3.24	0.5	5.14	0	12.48	0
37.6	0.16	3.23	0.5	5.14	0	11.46	0.2
37.6	0.12	3.28	0.5	5.07	0.2	12.52	0
37.6	0.196	3.27	0.5	5.06	0.2	11.66	0.2
37.5	0.277	3.2	2	5.19	0	12.48	0
37.5	0.335	3.2	2	5.18	0	12.06	0.2
37.5	0.325	3.23	2	5.13	0.2	12.52	0
37.5	0.377	3.22	2	5.12	0.2	12.25	0.2
48.2	0.019	3.3	0	5.04	0	11.87	0
48.2	0.083	3.25	0	5.11	0	11.23	0.2
48.2	0.042	3.31	0	5.01	0.2	12.55	0
48.1	0.113	3.28	0	5.05	0.2	11.48	0.2
48.1	0.061	3.24	0.5	5.14	0	12.48	0
48.1	0.128	3.23	0.5	5.14	0	11.44	0.2
48.1	0.097	3.28	0.5	5.07	0.2	12.52	0
48.1	0.156	3.27	0.5	5.08	0.2	11.64	0.2
48.1	0.214	3.2	2	5.18	0	12.47	0
48.1	0.261	3.2	2	5.18	0	11.94	0.2
48.1	0.249	3.23	2	5.11	0.2	12.51	0
48.1	0.292	3.23	2	5.12	0.2	12.12	0.2
57.6	0.017	3.3	0	5.04	0	11.86	0
57.6	0.069	3.25	0	5.12	0	11.23	0.2
57.6	0.038	3.31	0	5.01	0.2	12.55	0
57.6	0.097	3.28	0	5.05	0.2	11.47	0.2
57.6	0.051	3.24	0.5	5.14	0	12.48	0
57.6	0.11	3.23	0.5	5.14	0	11.44	0.2
57.6	0.083	3.28	0.5	5.07	0.2	12.52	0
57.6	0.134	3.27	0.5	5.07	0.2	11.62	0.2
57.5	0.181	3.2	2	5.18	0	12.48	0
57.5	0.219	3.2	2	5.18	0	11.88	0.2
57.5	0.207	3.23	2	5.12	0.2	12.51	0
57.5	0.245	3.23	2	5.12	0.2	12.05	0.2
	Max	**3.31**	0.3%	**5.19**	3.8%	**12.54**	4.5%
	Min	**3.2**	-3.0%	**5.02**	0.4%	**11.21**	-6.6%
	Delta	**0.11**	3.3%	**0.17**	3.4%	**1.33**	11.1%

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Vnom1=	3.3	Vnom3=	12						
Vnom2=	5								
%Vout1 **(%)**	%Vout2 (%)	%Vout3 **(%)**	Pin (W)	Eff (%)	Pout1 (W)	Pout2 (W)	Pout3 (W)	Pout6 (W)	Pout (W)
100.0%	100.4%	98.7%	0.7896	0.0%	0.0	0.0	0.0	0.0	0.0
98.5%	102.2%	93.4%	3.8728	57.9%	0.0	0.0	2.2	0.0	2.2
100.3%	100.4%	104.5%	1.88	53.4%	0.0	1.0	0.0	0.0	1.0
99.7%	101.0%	95.7%	5.2264	63.3%	0.0	1.0	2.3	0.0	3.3
98.2%	102.8%	104.0%	3.008	53.9%	1.6	0.0	0.0	0.0	1.6
97.9%	102.8%	95.5%	6.016	64.9%	1.6	0.0	2.3	0.0	3.9
99.4%	101.4%	104.3%	4.512	58.8%	1.6	1.0	0.0	0.0	2.7
99.1%	101.2%	97.2%	7.3696	67.6%	1.6	1.0	2.3	0.0	5.0
97.0%	103.8%	104.0%	10.3875	61.6%	6.4	0.0	0.0	0.0	6.4
97.0%	103.6%	100.5%	12.5625	70.1%	6.4	0.0	2.4	0.0	8.8
97.9%	102.6%	104.3%	12.1875	61.4%	6.5	1.0	0.0	0.0	7.5
97.6%	102.4%	102.1%	14.1375	70.1%	6.4	1.0	2.5	0.0	9.9
100.0%	100.8%	98.9%	0.9158	0.0%	0.0	0.0	0.0	0.0	0.0
98.5%	102.2%	93.6%	4.0006	56.1%	0.0	0.0	2.2	0.0	2.2
100.3%	100.2%	104.6%	2.0244	49.5%	0.0	1.0	0.0	0.0	1.0
99.4%	101.0%	95.7%	5.4353	60.8%	0.0	[illegible]	[illegible]	[illegible]	[illegible]
98.2%	102.8%	104.0%	2.9341	55.2%	1.6	[illegible]	[illegible]	[illegible]	[illegible]
97.9%	102.8%	95.3%	6.1568	63.4%	1.6	[illegible]	[illegible]	[illegible]	[illegible]
99.4%	101.4%	104.3%	4.6657	56.9%	1.6	[illegible]	[illegible]	[illegible]	[illegible]
99.1%	101.6%	97.0%	7.5036	66.4%	1.6	1.0	2.3	0.0	5.0
97.0%	103.6%	103.9%	10.2934	62.2%	6.4	0.0	0.0	0.0	6.4
97.0%	103.6%	99.5%	12.5541	70.0%	6.4	0.0	2.4	0.0	8.8
97.9%	102.2%	104.3%	11.9769	62.5%	6.5	1.0	0.0	0.0	7.5
97.9%	102.4%	101.0%	14.0452	70.5%	6.5	1.0	2.4	0.0	9.9
100.0%	100.8%	98.8%	0.9792	0.0%	0.0	0.0	0.0	0.0	0.0
98.5%	102.4%	93.6%	3.9744	56.5%	0.0	0.0	2.2	0.0	2.2
100.3%	100.2%	104.6%	2.1888	45.8%	0.0	1.0	0.0	0.0	1.0
99.4%	101.0%	95.6%	5.5872	59.1%	0.0	1.0	2.3	0.0	3.3
98.2%	102.8%	104.0%	2.9376	55.1%	1.6	0.0	0.0	0.0	1.6
97.9%	102.8%	95.3%	6.336	61.6%	1.6	0.0	2.3	0.0	3.9
99.4%	101.4%	104.3%	4.7808	55.5%	1.6	1.0	0.0	0.0	2.7
99.1%	101.4%	96.8%	7.7184	64.4%	1.6	1.0	2.3	0.0	5.0
97.0%	103.6%	104.0%	10.4075	61.5%	6.4	0.0	0.0	0.0	6.4
97.0%	103.6%	99.0%	12.5925	69.7%	6.4	0.0	2.4	0.0	8.8
97.9%	102.4%	104.3%	11.9025	62.9%	6.5	1.0	0.0	0.0	7.5
97.9%	102.4%	100.4%	14.0875	70.2%	6.5	1.0	2.4	0.0	9.9
100.3%	**103.8%**	**104.5%**	**14.1**	**70.1%**					**9.9**
97.0%	**100.4%**	**93.4%**	**1.9**	**53.4%**					**1.0**
3.3%	3.4%	11.1%	12.3	16.7%					

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10.5 Thermal Performance

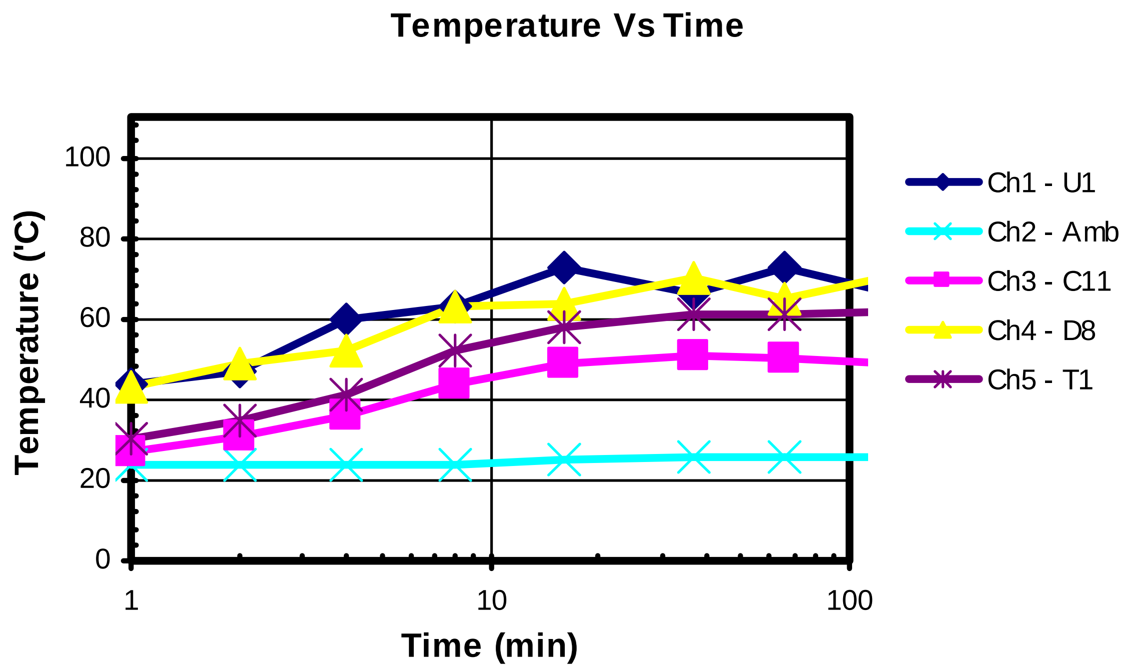

Figure 10 – Thermal Performance of Key Power Supply Components

Time			Temperature		
	U1 (Drain)	Amb	C11	D8	T1
(Mins.)	('C)	('C)	('C)	('C)	('C)
0	24	24	25	25	25
1	44	24	27	43	30
2	47	24	31	49	35
4	60	24	36	52	41
8	63	24	44	63	52
16	73	25	49	64	58
37	66	26	51	70	61
66	73	26	50	65	61
132	66	26	49	71	62

Figure 11 – Raw Test Data

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11 Waveforms

11.1 Drain Current and Voltage

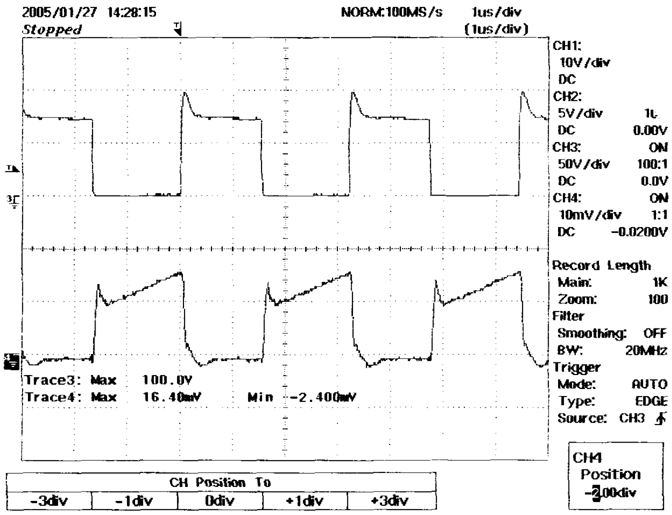

Figure 12 – 37 VDC, full load
Upper Ch3: Drain Voltage 50 V,
Lowr Ch4: Drain Current 0.5 A / Div,
1 µs / div

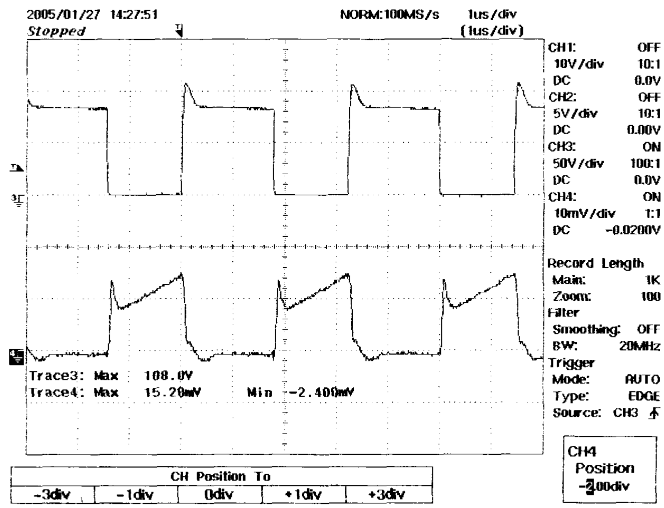

Figure 13 – 48 VDC, full load
Upper Ch3: Drain Voltage 50 V,
Lowr Ch4: Drain Current 0.5 A / Div,
1 µs / div

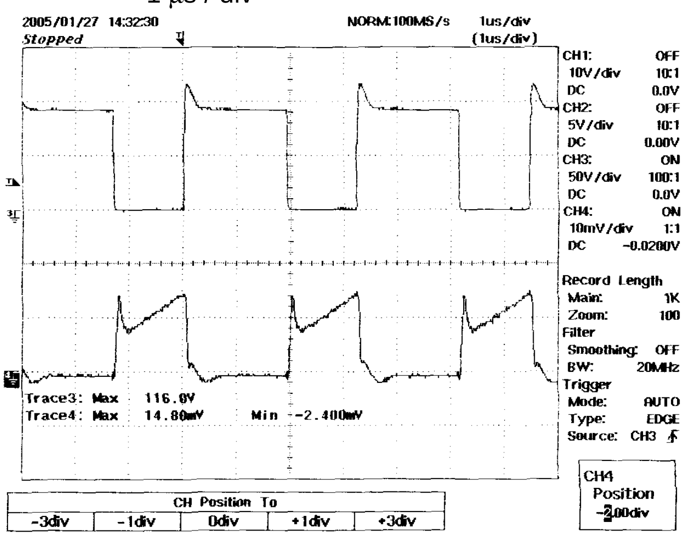

Figure 14 – 57 VDC, full load
Upper Ch3: Drain Voltage 50 V,
Lowr Ch4: Drain Current 0.5 A / Div,
1 µs / div

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11.2 Output Transient Load Response

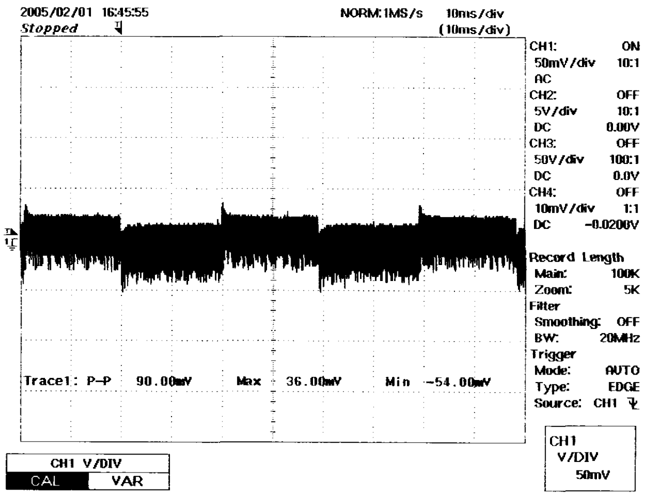

Figure 15 – 48 VDC, full load (3.3 V 1.6 A to 2.0 A step)
3.3 V Output Voltage
50 mV / Div, 10 ms / div

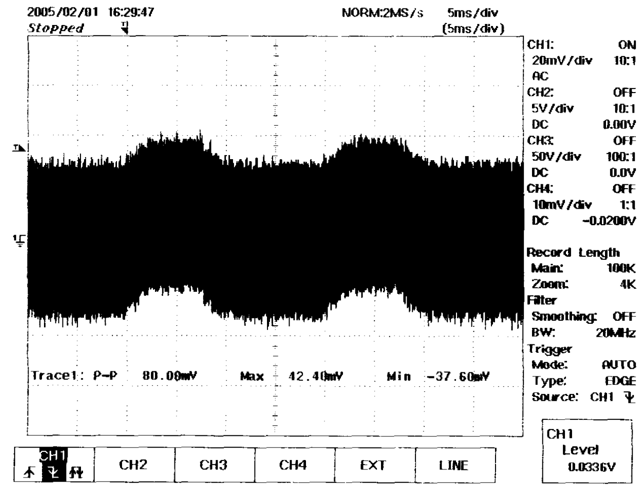

Figure 16 – 48 VDC, full load (5 V 0.16 A to 0.2 A step)
5 V Output Voltage
20 mV / Div, 10 ms / div

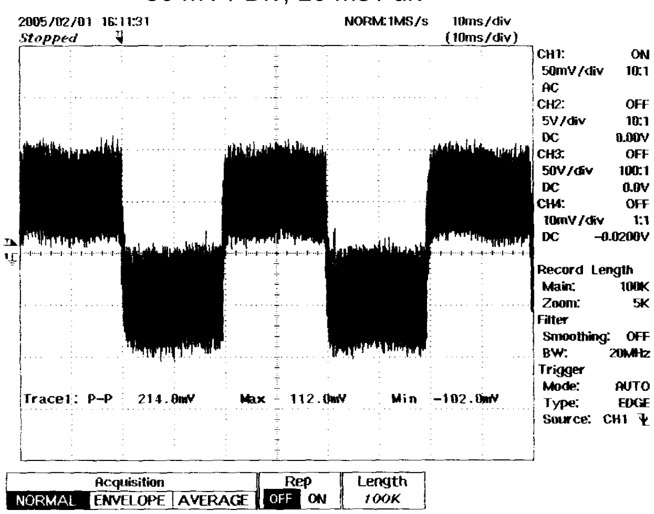

Figure 17 – 48 VDC, full load (12 V 0.16 A to 0.2 A step)
12 V Output Voltage
50 mV / Div, 10 ms / div

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11.3 Output Ripple Voltage

It can be seen from the waveforms below that the power supply comfortably meets the output ripple specifications. This is possible even without the need for an output inductor.

Measurements made with 0.1 uF ceramic capacitor in parallel with a 1 uF / 50 V electrolytic capacitor, and also made using very short lead length connections to the output pins of the power supply.

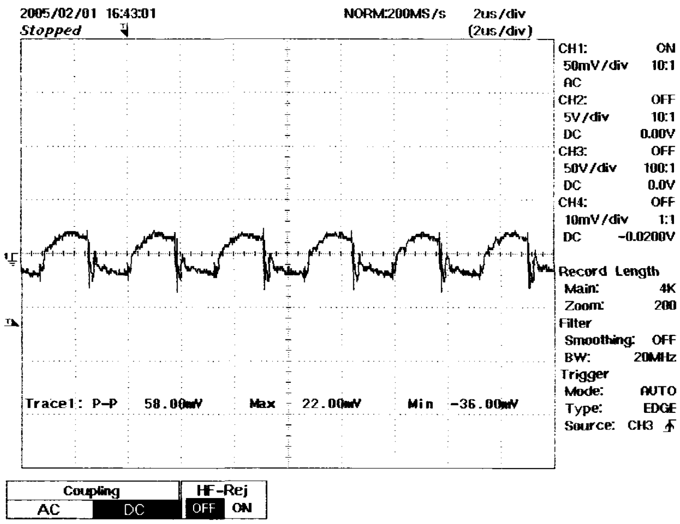

Figure 18 – 48 VDC, Full Load
3.3 V Output Ripple, 50 mV,
2 µs / div

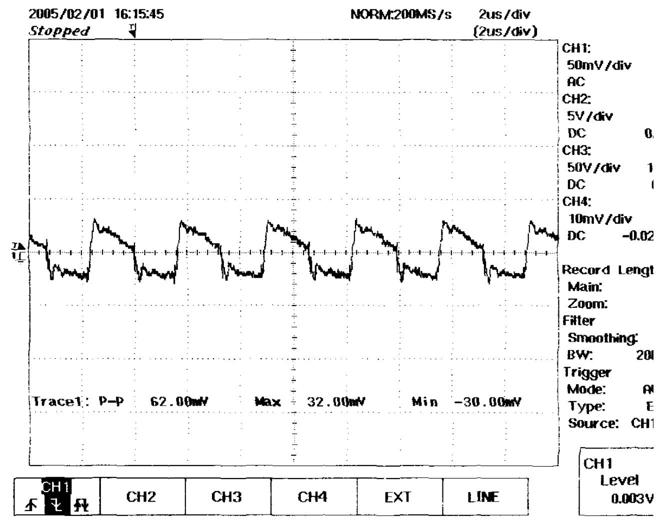

Figure 19 – 48 VDC, Full Load
5V Output Ripple, 50 mV,
2 µs / div

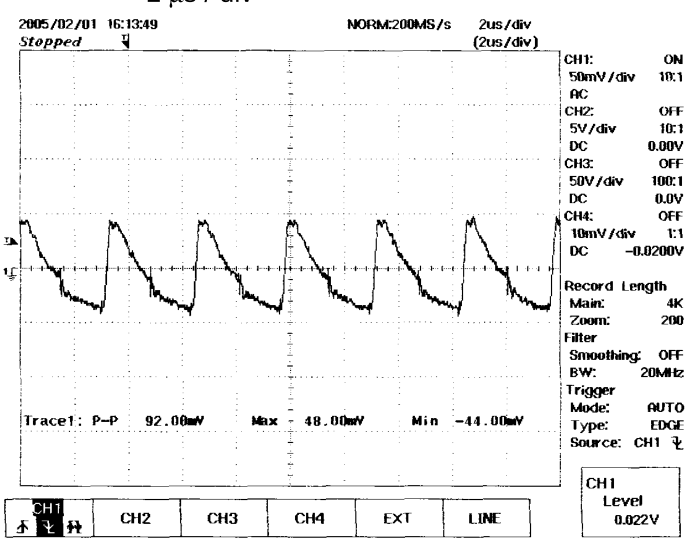

Figure 20 – 48 VDC, Full Load
12 V Output Ripple, 50 mV,
2 µs / div

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11.4 Output Voltage Start-up Profile

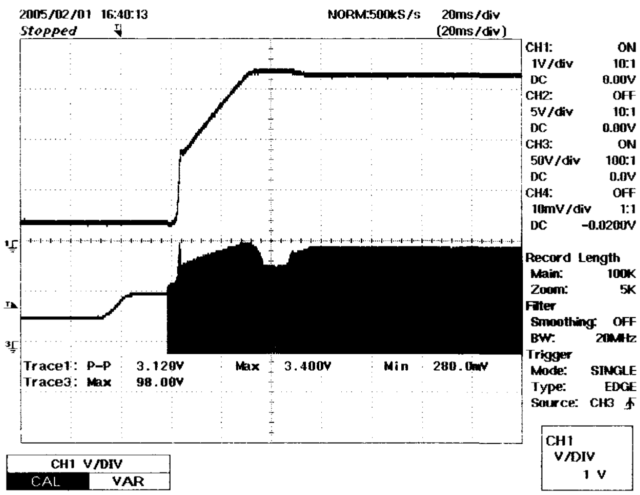

Figure 21 – 3.3 V Start-up at No Load, 48 VDC
Upper Ch1: 3.3 V output, 1 V / div,
Lower Ch3: Drain Voltage 50 V / div,
20 ms / div.

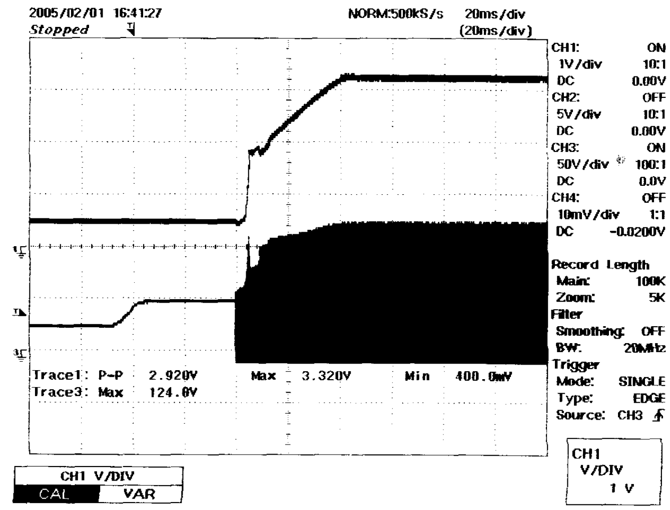

Figure 22 – 3.3 V Start-up at Full Load, 48 VDC
Upper Ch1: 3.3 V output, 1 V / div,
Lower Ch3: Drain Voltage 50 V / div,
20 ms / div.

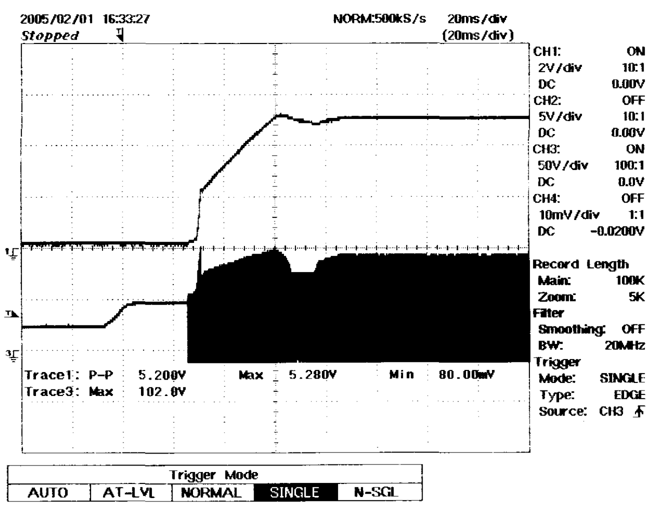

Figure 23 – 5 V Start-up at No Load, 48 VDC
Upper Ch1: 5 V output, 2 V / div,
Lower Ch3: Drain Voltage 50 V / div,
20 ms / div.

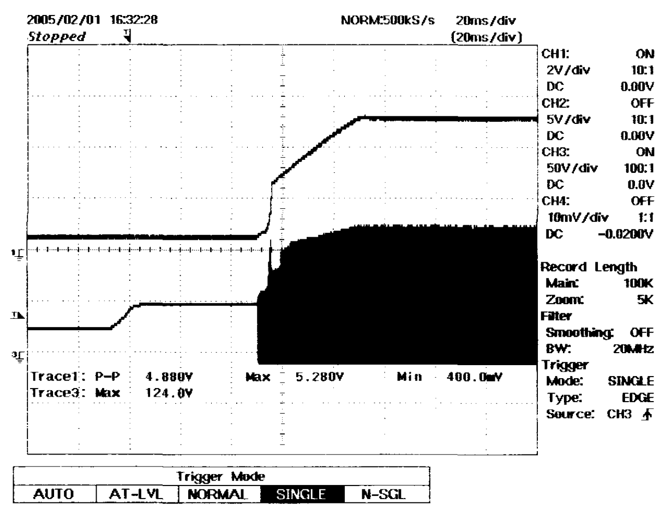

Figure 24 – 5 V Start-up at Full Load, 48 VDC
Upper Ch1: 5 V output, 2 V / div,
Lower Ch3: Drain Voltage 50 V / div,
20 ms / div.

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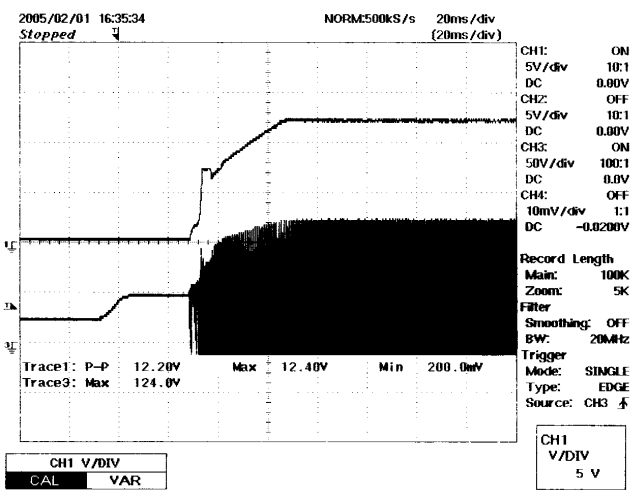

Figure 25 – Start-up Profile at No Load, 48 VDC
Upper Ch1: 12 V output, 2 V / div,
Lower Ch3: Drain Voltage 50 V / div,
20 ms / div.

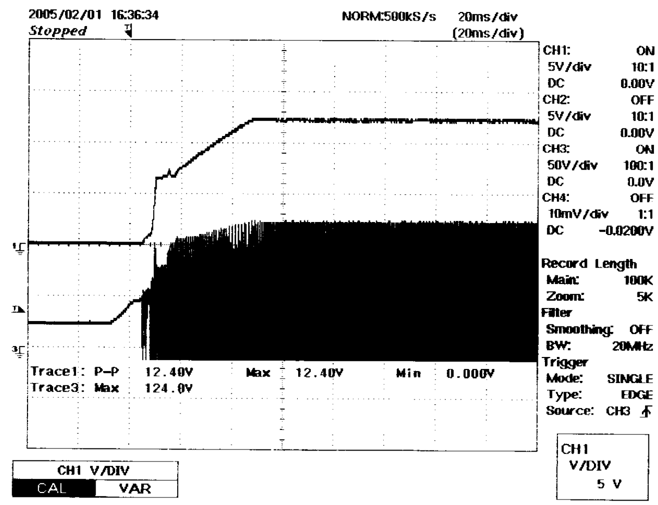

Figure 26 – Start-up Profile at Full Load, 48 VDC
Upper Ch1: 12 V output, 2 V / div,
Lower Ch3: Drain Voltage 50 V / div,
20 ms / div.

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12 Conducted EMI

EMI was tested at room temperature and at 230 VAC input. An AC-DC (48 V output) adapter was plugged into the LISN (AC-output). The DC-DC converter (using DPA423 was plugged into the 48 VDC output from the AC-DC adapter.

In some tests the output of the DC-DC converter was left floating and in other cases the output (0 VDC) was connected to Earth ground.

12.1 230V High Line EMI

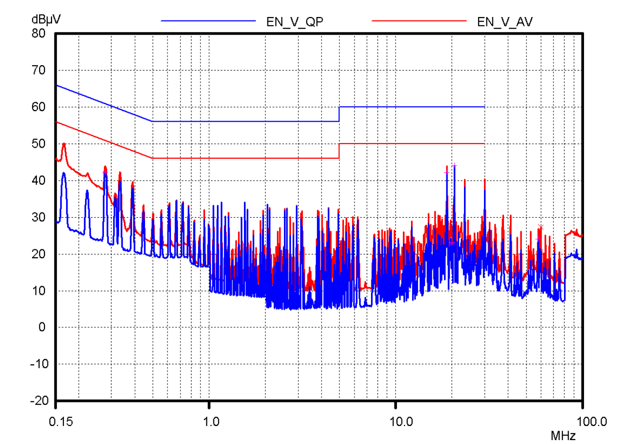

Figure 27 – 230 VAC - N1 - full system grounded output - full-load

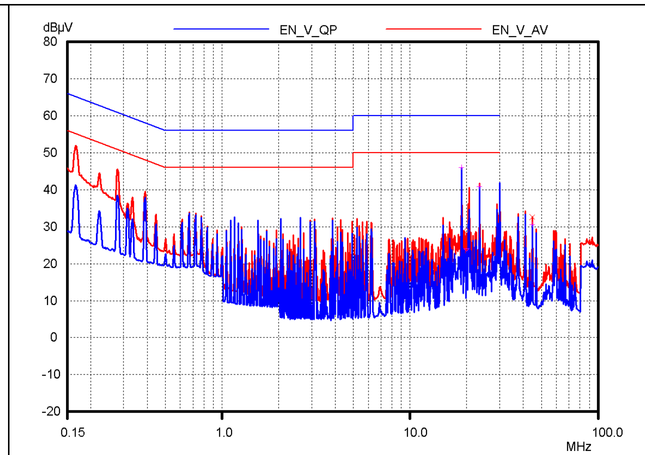

Figure 28 – 230 VAC - L1 - full system grounded output - full-load

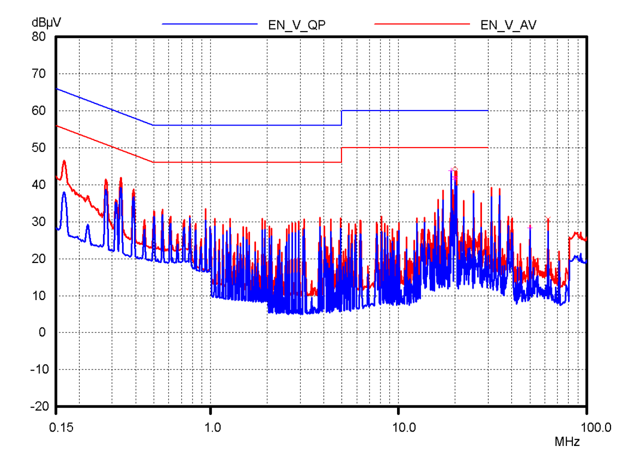

Figure 29 – 230 VAC - N1 - full system floating output - full-load

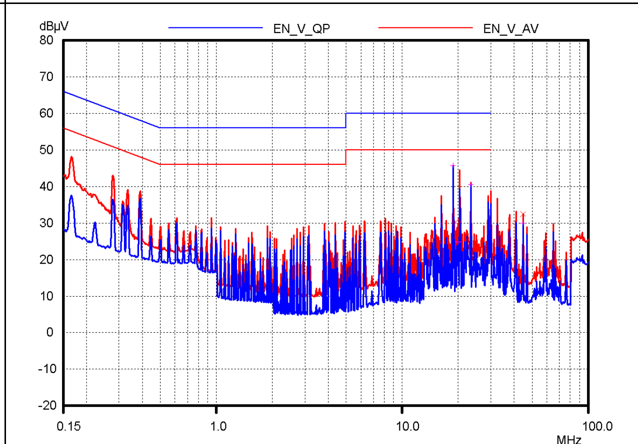

Figure 30 – 230 VAC - L1 - full system floating output - full-load

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13 Radiated EMI scans

As can be seen from the radiated EMI scans below, the new board performs extremely well compared to the original DPA423 power supply. This is because of optimal layout and power supply filtering (including transformer shielding design).

The measurements were made in an open-field test site, with the AC-adapter (which outputs 48 VDC). This AC-adapter was connected to 115 VAC via a LISN and the output 48 VDC was input to the DPA423 DC-DC converter.

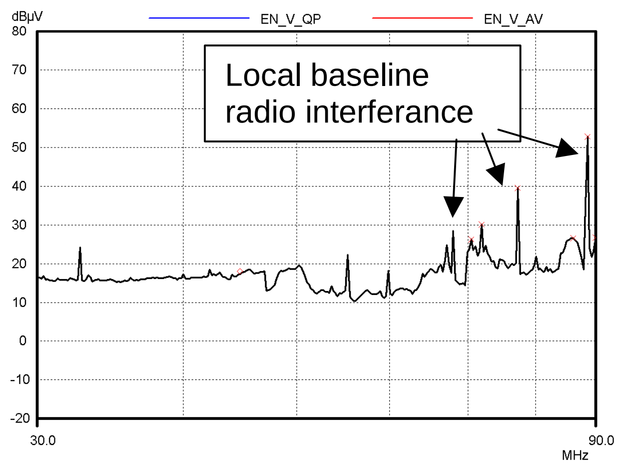

Figure 31 – Radiated no-power Baseline

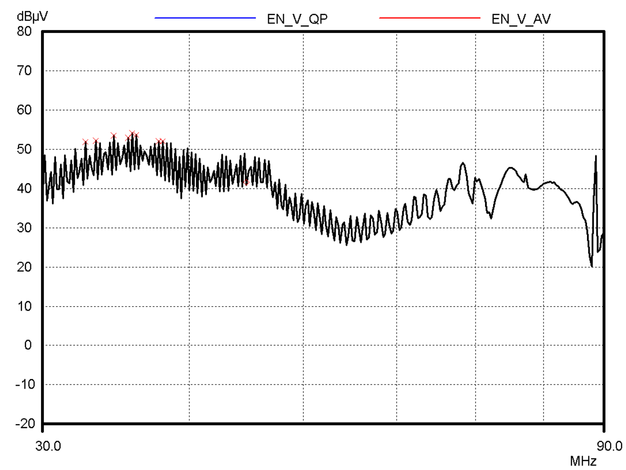

Figure 32 – Original board with DPA423 and AC-adapter (230 VAC) – Output Floating

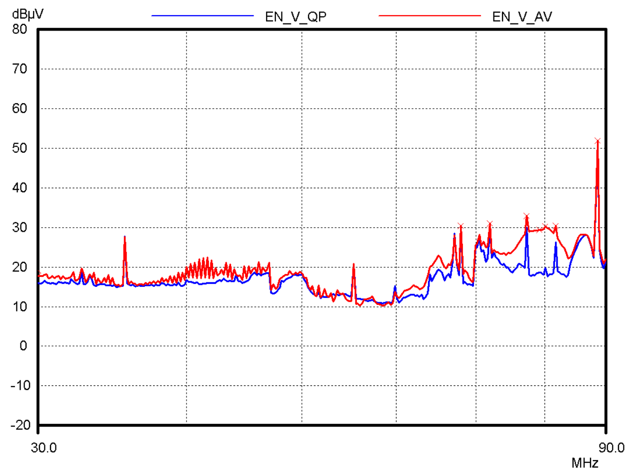

Figure 33 – New prototype board using DPA423 and AC-adapter (230 VAC) – **Output Floating**

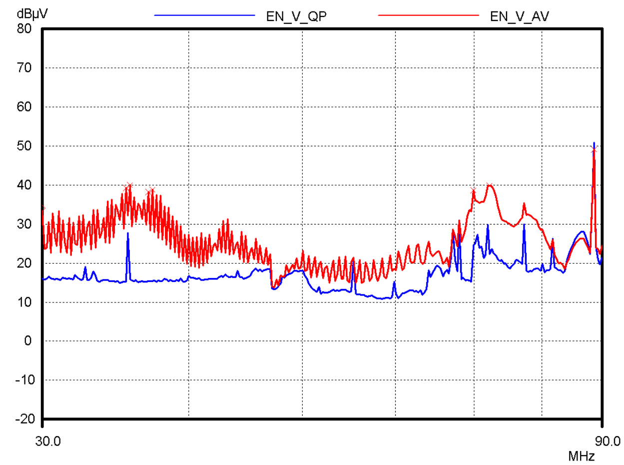

Figure 34 – New prototype board using DPA423 and AC-adapter (230 VAC) – **Output Hard Grounded**

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14 Revision History

Date	Author	Revision	Description & changes	Reviewed
September 12, 2005	RM	1.0	Initial release	VC / AM

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The products and applications illustrated herein (including circuits external to the products and transformer construction) may be covered by one or more U.S. and foreign patents or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations' patents may be found at *www.powerint.com*.

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