SC68C652B

5 V, 3.3 V and 2.5 V dual UART, 5 Mbit/s (max.) with 32-byte FIFOs, IrDA encoder/decoder, and 68 mode μP interface

Rev. 02 — 2 November 2009 Product data sheet

1. General description

The SC68C652B is a 2 channel Universal Asynchronous Receiver and Transmitter (UART) used for serial data communications. Its principal function is to convert parallel data into serial data and vice versa. The UART can handle serial data rates up to 5 Mbit/s. The SC68C652B is pin compatible with the SC68C2550B. The SC68C652B provides enhanced UART functions with 32-byte FIFOs, modem control interface, DMA mode data transfer, and infrared (IrDA) encoder/decoder. The DMA mode data transfer is controlled by the FIFO trigger levels and the $\overline{\text{TXRDYn}}$ and $\overline{\text{RXRDYn}}$ signals. On-board status registers provide the user with error indications and operational status. System interrupts and modem control features may be tailored by software to meet specific user requirements. An internal loopback capability allows on-board diagnostics. Independent programmable baud rate generators are provided to select transmit and receive baud rates.

The SC68C652B operates at 5 V, 3.3 V and 2.5 V and the industrial temperature range, and is available in the plastic LQFP48 package.

2. Features

- 2 channel UART with 68 mode (Motorola) μP interface
- 5 V, 3.3 V and 2.5 V operation
- 5 V tolerant on input only pins[1]
- Industrial temperature range (–40 °C to +85 °C)
- Software compatible with industry standard 16C450, 16C550, and SC16C650
- Up to 5 Mbit/s baud rate at 5 V and 3.3 V, and 3 Mbit/s at 2.5 V
- 32-byte transmit FIFO to reduce the bandwidth requirement of the external CPU
- 32-byte receive FIFO with error flags to reduce the bandwidth requirement of the external CPU
- Independent transmit and receive UART control
- Four selectable receive and transmit FIFO interrupt trigger levels
- Automatic software (Xon/Xoff) and hardware ($\overline{\text{RTSn}}$/$\overline{\text{CTSn}}$) flow control
- Programmable Xon/Xoff characters
- Software selectable baud rate generator
- Standard modem interface or infrared IrDA encoder/decoder interface
- Supports IrDA version 1.0 (up to 115.2 kbit/s)
- Sleep mode

1. For data bus pins D7 to D0, see Table 27 “Limiting values”.

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- Standard asynchronous error and framing bits (Start, Stop, and Parity Overrun Break)
- Transmit, Receive, Line Status, and Data Set interrupts independently controlled
- Fully programmable character formatting:
  - 5, 6, 7, or 8-bit characters
  - Even, odd, or no parity formats
  - 1, $1\frac{1}{2}$, or 2 stop bit generation
  - Baud generation (DC to 5 Mbit/s)
- False start bit detection
- Complete status reporting capabilities
- 3-state output TTL drive capabilities for bidirectional data bus and control bus
- Line break generation and detection
- Internal diagnostic capabilities:
  - Loopback controls for communications link fault isolation
- Prioritized interrupt system controls
- Modem control functions ($\overline{CTS}$, $\overline{RTS}$, $\overline{DSR}$, $\overline{DTR}$, $\overline{RI}$, and $\overline{CD}$)

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
SC68C652BIB48	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2

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4. Block diagram

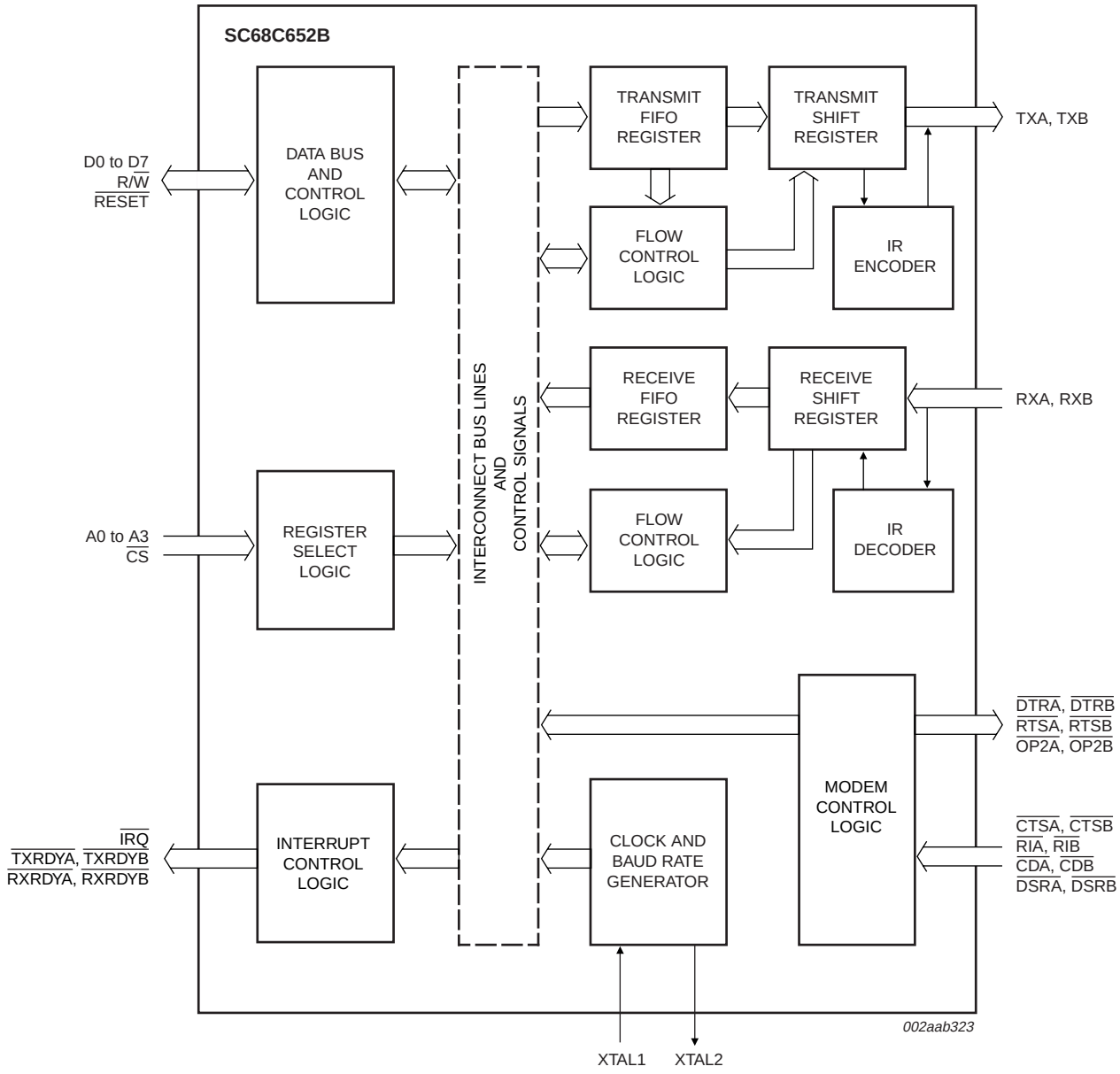


Fig 1. Block diagram of SC68C652B

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5. Pinning information

5.1 Pinning

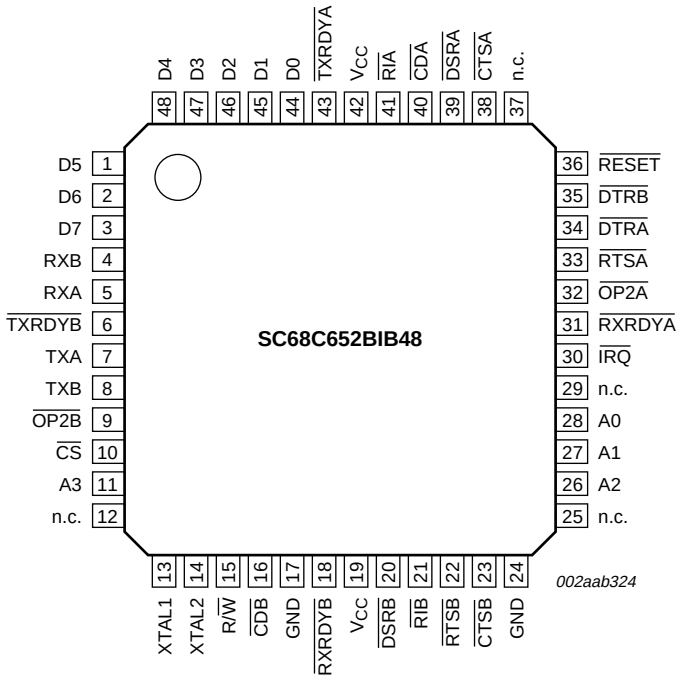


Fig 2. Pin configuration for LQFP48

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Type	Description
A0	28	I	**Address 0 select bit.** Internal registers address selection.
A1	27	I	**Address 1 select bit.** Internal registers address selection.
A2	26	I	**Address 2 select bit.** Internal registers address selection.
A3	11	I	**Address 3 select bit.** A3 is used to select Channel A or Channel B. A logic LOW selects Channel A, and a logic HIGH selects Channel B. (See Table 3.)
$\overline{CDA}$	40	I	**Carrier Detect (active LOW).** These inputs are associated with individual UART channels A and B. A logic 0 on these pins indicates that a carrier has been detected by the modem for that channel.
$\overline{CDB}$	16	I	
$\overline{CS}$	10	I	**Chip Select (active LOW).** This pin enables data transfers between the user CPU and the SC68C652B for the channel(s) addressed. Individual UART sections (A, B) are addressed by A3. See Table 3.

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Table 2. Pin description *...continued*

Symbol	Pin	Type	Description
$\overline{CTSA}$	38	I	**Clear to Send (active LOW).** These inputs are associated with individual UART channels A and B. A logic 0 (LOW) on the $\overline{CTSn}$ pins indicates the modem or data set is ready to accept transmit data from the SC68C652B. Status can be tested by reading MSR[4]. These pins have no effect on the UART's transmit or receive operation.
$\overline{CTSB}$	23	I	
D0	44	I/O	**Data bus (bidirectional).** These pins are the 8-bit, 3-state data bus for transferring information to or from the controlling CPU. D0 is the least significant bit and the first data bit in a transmit or receive serial data stream.
D1	45	I/O	
D2	46	I/O	
D3	47	I/O	
D4	48	I/O	
D5	1	I/O	
D6	2	I/O	
D7	3	I/O	
$\overline{DSRA}$	39	I	**Data Set Ready (active LOW).** These inputs are associated with individual UART channels A and B. A logic 0 (LOW) on these pins indicates the modem or data set is powered-on and is ready for data exchange with the UART. These pins have no effect on the UART's transmit or receive operation.
$\overline{DSRB}$	20	I	
$\overline{DTRA}$	34	O	**Data Terminal Ready (active LOW).** These outputs are associated with individual UART channels A and B. A logic 0 (LOW) on these pins indicates that the SC68C652B is powered-on and ready. These pins can be controlled via the modem control register. Writing a logic 1 to MCR[0] will set the $\overline{DTRn}$ output pin to logic 0 (LOW), enabling the modem. The output of these pins will be a logic 1 after writing a logic 0 to MCR[0], or after a reset. These pins have no effect on the UART's transmit or receive operation.
$\overline{DTRB}$	35	O	
GND	17, 24	I	**Signal and power ground**
$\overline{IRQ}$	30	O	**Interrupt Request.** Interrupts from UART channels A-B are wire-ORed internally to function as a single $\overline{IRQ}$ interrupt. This pin transitions to a logic 0 (if enabled by the interrupt enable register) whenever a UART channel(s) requires service. Individual channel interrupt status can be determined by addressing each channel through its associated internal register, using $\overline{CS}$ and A3. An external pull-up resistor must be connected between this pin and V_{CC}.
R/$\overline{W}$	15	I	A logic LOW on this pin will transfer the contents of the data bus (D[7:0]) from an external CPU to an internal register that is defined by address bits A[2:0]. A logic HIGH on this pin will load the contents of an internal register defined by address bits A[2:0] on the SC68C652B data bus (D[7:0]) for access by an external CPU.
n.c.	12, 25, 29, 37	-	not connected
$\overline{OP2A}$	32	O	**Output 2 (user-defined).** This function is associated with individual channels A and B. The state of these pins is defined by the user through the software settings of MCR[3]. $\overline{OP2A}$/$\overline{OP2B}$ is a logic 0 when MCR[3] is set to a logic 1. $\overline{OP2A}$/$\overline{OP2B}$ is a logic 1 when MCR[3] is set to a logic 0. The output of these two pins is HIGH after reset.
$\overline{OP2B}$	9	O	

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Table 2. Pin description *...continued*

Symbol	Pin	Type	Description
$\overline{\text{RESET}}$	36	I	**Reset (active LOW).** This pin will reset the internal registers and all the outputs. The UART transmitter output and the receiver input will be disabled during reset time. See Section 7.11 "SC68C652B external reset condition" for initialization details.
$\overline{\text{RIA}}$	41	I	**Ring Indicator (active LOW).** These inputs are associated with individual UART channels A and B. A logic 0 on these pins indicates the modem has received a ringing signal from the telephone line. A logic 1 transition on these input pins generates an interrupt.
$\overline{\text{RIB}}$	21	I	
$\overline{\text{RTSA}}$	33	O	**Request to Send (active LOW).** These outputs are associated with individual UART channels, A and B. A logic 0 on the $\overline{\text{RTSn}}$ pin indicates the transmitter has data ready and waiting to send. Writing a logic 1 in the modem control register MCR[1] will set this pin to a logic 0, indicating data is available. After a reset these pins are set to a logic 1. These pins have no effect on the UART's transmit or receive operation.
$\overline{\text{RTSB}}$	22	O	
RXA	5	I	**Receive data input.** These inputs are associated with individual serial channel data to the SC68C652B receive input circuits A and B. The RXn pin will be a logic 1 during reset, idle (no data), or when the transmitter is disabled. During the local loopback mode, these RXn input pins are disabled and transmit data is connected to the UART receive input internally.
RXB	4	I	
$\overline{\text{RXRDYA}}$	31	O	**Receive Ready (active LOW).** $\overline{\text{RXRDYA}}$ or $\overline{\text{RXRDYB}}$ goes LOW when the trigger level has been reached or the FIFO has at least one character. It goes HIGH when the receive FIFO is empty.
$\overline{\text{RXRDYB}}$	18	O	
TXA	7	O	**Transmit data A, B.** These outputs are associated with individual serial transmit channel data from the SC68C652B. The TXn pin will be a logic 1 during reset, idle (no data), or when the transmitter is disabled. During the local loopback mode, the TXn output pins are disabled and transmit data is internally connected to the UART receive input.
TXB	8	O	
$\overline{\text{TXRDYA}}$	43	O	**Transmit Ready A, B (active LOW).** These outputs provide the transmit FIFO/THR status for individual transmit channels A and B. $\overline{\text{TXRDYn}}$ is primarily intended for monitoring DMA mode 1 transfers for the transmit data FIFOs. An individual channel's $\overline{\text{TXRDYA}}$, $\overline{\text{TXRDYB}}$ buffer ready status is indicated by logic 0, that is, at least one location is empty and available in the FIFO or THR. This pin goes to a logic 1 (DMA mode 1) when there are no more empty locations in the FIFO or THR. This signal can also be used for single mode transfers (DMA mode 0).
$\overline{\text{TXRDYB}}$	6	O	

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Table 2. Pin description *...continued*

Symbol	Pin	Type	Description
V_{CC}	19, 42	I	**Power supply input.**
XTAL1	13	I	**Crystal or external clock input.** Functions as a crystal input or as an external clock input. A crystal can be connected between this pin and XTAL2 to form an internal oscillator circuit (see Figure 3). This configuration requires an external 1 MΩ resistor between the XTAL1 and XTAL2 pins. Alternatively, an external clock can be connected to this pin to provide custom data rates. See Section 6.8 "Programmable baud rate generator".
XTAL2	14	O	**Output of the crystal oscillator or buffered clock.** (See also XTAL1.) XTAL2 is used as a crystal oscillator output or a buffered clock output. Should be left open if an external clock is connected to XTAL1. For extended frequency operation, this pin should be tied to V_{CC} via a 2 kΩ resistor.

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6. Functional description

The SC68C652B UART is pin-compatible with the SC68C2550B UART. It provides more enhanced features. All additional features are provided through a special enhanced feature register.

The UART will perform serial-to-parallel conversion on data characters received from peripheral devices or modems, and parallel-to-parallel conversion on data characters transmitted by the processor. The complete status of each channel of the SC68C652B UART can be read at any time during functional operation by the processor.

The SC68C652B can be placed in an alternate mode (FIFO mode) relieving the processor of excessive software overhead by buffering received/transmitted characters. Both the receiver and transmitter FIFOs can store up to 64 bytes (including three additional bits of error status per byte for the receiver FIFO) and have selectable or programmable trigger levels. Primary outputs $\overline{\text{RXRDYn}}$ and $\overline{\text{TXRDYn}}$ allow signalling of DMA transfers.

The SC68C652B has selectable hardware flow control and software flow control. Hardware flow control significantly reduces software overhead and increases system efficiency by automatically controlling serial data flow using the $\overline{\text{RTSn}}$ output and $\overline{\text{CTSn}}$ input signals. Software flow control automatically controls data flow by using programmable Xon/Xoff characters.

The UART includes a programmable baud rate generator that can divide the timing reference clock input by a divisor between 1 and $(2^{16} - 1)$.

6.1 UART A-B functions

The UART provides the user with the capability to bidirectionally transfer information between an external CPU, the SC68C652B package, and an external serial device. A logic 0 on chip select pin $\overline{\text{CS}}$ and A3 (LOW or HIGH) allows the user to configure, send data, and/or receive data via UART channels A and B. Individual channel select functions are shown in Table 3.

Table 3. Channel selection using $\overline{\text{CS}}$ pin

$\overline{\text{CS}}$	A3	UART channel
1	-	none
0	0	channel A
0	1	channel B

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6.2 Internal registers

The SC68C652B provides two sets of internal registers (A and B) consisting of 17 registers each for monitoring and controlling the functions of each channel of the UART. These registers are shown in Table 4. The UART registers function as data holding registers (THR/RHR), interrupt status and control registers (IER/ISR), a FIFO control register (FCR), line status and control registers (LCR/LSR), modem status and control registers (MCR/MSR), programmable data rate (clock) control registers (DLL/DLM), and a user accessible scratchpad register (SPR), along with advanced feature registers EFR and Xon1, Xon2, Xoff1 and Xoff2.

Table 4. Internal registers decoding

A2	A1	A0	Read mode	Write mode
General register set (THR/RHR, IER/ISR, MCR/MSR, FCR, LSR, SPR)[1]				
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1	Interrupt Enable Register	Interrupt Enable Register
0	1	0	Interrupt Status Register	FIFO Control Register
0	1	1	Line Control Register	Line Control Register
1	0	0	Modem Control Register	Modem Control Register
1	0	1	Line Status Register	n/a
1	1	0	Modem Status Register	n/a
1	1	1	Scratchpad Register	Scratchpad Register
Baud rate register set (DLL/DLM)[2]				
0	0	0	LSB of Divisor Latch	LSB of Divisor Latch
0	0	1	MSB of Divisor Latch	MSB of Divisor Latch
Enhanced register set (EFR, Xon1, Xon2, Xoff1, Xoff2)[3]				
0	1	0	Enhanced Feature Register	Enhanced Feature Register
1	0	0	Xon1 word	Xon1 word
1	0	1	Xon2 word	Xon2 word
1	1	0	Xoff1 word	Xoff1 word
1	1	1	Xoff2 word	Xoff2 word

[1] These registers are accessible only when LCR[7] is a logic 0.

[2] These registers are accessible only when LCR[7] is a logic 1.

[3] Enhanced Feature Register, Xon1, Xon2, and Xoff1, Xoff2 are accessible only when the LCR is set to ‘BFh’.

6.3 FIFO operation

The 32-byte transmit and receive data FIFOs are enabled by the FIFO Control Register bit 0 (FCR[0]). With SC68C2550B devices, the user can set the receive trigger level, but not the transmit trigger level. The SC68C652B provides independent trigger levels for both receiver and transmitter. To remain compatible with SC68C2550B, the transmit interrupt trigger level is set to 16 following a reset. It should be noted that the user can set the transmit trigger levels by writing to the FCR register, but activation will not take place until EFR[4] is set to a logic 1. The receiver FIFO section includes a time-out function to ensure data is delivered to the external CPU. An interrupt is generated whenever the Receive Holding Register (RHR) has not been read following the loading of a character or the receive trigger level has not been reached.

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Table 5. Flow control mechanism

Selected trigger level (characters)	IRQ pin activation		Negate RTS or send Xoff	Assert RTS or send Xon
	RX	TX		
8	8	16	8	0
16	16	8	16	7
24	24	24	24	15
28	28	30	28	23

6.4 Hardware flow control

When automatic hardware flow control is enabled, the SC68C652B monitors the CTSn pin for a remote buffer overflow indication and controls the RTSn pin for local buffer overflows. Automatic hardware flow control is selected by setting EFR[6] (RTS) and EFR[7] (CTS) to a logic 1. If CTSn transitions from a logic 0 to a logic 1 indicating a flow control request, ISR[5] will be set to a logic 1 (if enabled via IER[6:7]), and the SC68C652B will suspend TXn transmissions as soon as the stop bit of the character in process is shifted out. Transmission is resumed after the CTSn input returns to a logic 0, indicating more data may be sent.

With the auto-RTS function enabled, an interrupt is generated when the receive FIFO reaches the programmed trigger level. The RTSn pin will not be forced to a logic 1 (RTS off), until the receive FIFO reaches the next trigger level. However, the RTSn pin will return to a logic 0 after the data buffer (FIFO) is unloaded to the next trigger level below the programmed trigger level. However, under the above described conditions, the SC68C652B will continue to accept data until the receive FIFO is full.

6.5 Software flow control

When software flow control is enabled, the SC68C652B compares one or two sequential receive data characters with the programmed Xon or Xoff character value(s). If received character(s) match the programmed Xoff values, the SC68C652B will halt transmission as soon as the current character(s) has completed transmission. When a match occurs, the receive ready (if enabled via Xoff IER[5]) flags will be set and the interrupt output pin (if receive interrupt is enabled) will be activated. Following a suspension due to a match of the Xoff characters' values, the SC68C652B will monitor the receive data stream for a match to the Xon1/Xon2 character value(s). If a match is found, the SC68C652B will resume operation and clear the flags (ISR[4]).

Reset initially sets the contents of the Xon/Xoff 8-bit flow control registers to a logic 0. Following reset, the user can write any Xon/Xoff value desired for software flow control. Different conditions can be set to detect Xon/Xoff characters and suspend/resume transmissions. When double 8-bit Xon/Xoff characters are selected, the SC68C652B compares two consecutive receive characters with two software flow control 8-bit values (Xon1, Xon2, Xoff1, Xoff2) and controls TXn transmissions accordingly. Under the above described flow control mechanisms, flow control characters are not placed (stacked) in the user accessible receive data buffer or FIFO. When using a software flow control, the Xon/Xoff characters cannot be used for data transfer.

In the event that the receive buffer is overfilling and flow control needs to be executed, the SC68C652B automatically sends an Xoff message (when enabled) via the serial TXn output to the remote modem. The SC68C652B sends the Xoff1/Xoff2 characters as soon

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as received data passes the programmed trigger level. To clear this condition, the SC68C652B will transmit the programmed Xon1/Xon2 characters as soon as receive data drops below the programmed trigger level.

6.6 Special feature software flow control

A special feature is provided to detect an 8-bit character when EFR[5] is set. When 8-bit character is detected, wit will be placed on the user-accessible data stack along with normal incoming receive data. This condition is selected in conjunction with EFR[3:0]. Note that software flow control should be turned off when using this special mode by setting EFR[3:0] to a logic 0.

The SC68C652B compares each incoming receive character with Xoff2 data. If a match exists, the received data will be transferred to the FIFO, and ISR[4] will be set to indicate detection of a special character. Although Table 9 “SC68C652B internal registers” shows each X-register with eight bits of character information, the actual number of bits is dependent on the programmed word length. Line Control Register bits LCR[1:0] define the number of character bits, that is, either 5 bits, 6 bits, 7 bits or 8 bits. The word length selected by LCR[1:0] also determine the number of bits that will be used for the special character comparison. Bit 0 in the X-registers corresponds with the LSB bit for the receive character.

6.7 Hardware/software and time-out interrupts

The interrupts are enabled by IER[3:0]. Care must be taken when handling these interrupts. Following a reset, if Interrupt Enable Register (IER) bit 1 = 1, the SC68C652B will issue a Transmit Holding Register interrupt. This interrupt must be serviced prior to continuing operations. The ISR register provides the current singular highest priority interrupt only. It could be noted that CTS and RTS interrupts have lowest interrupt priority. A condition can exist where a higher priority interrupt may mask the lower priority CTS/RTS interrupt(s). Only after servicing the higher pending interrupt will the lower priority CTS/RTS interrupt(s) be reflected in the status register. Servicing the interrupt without investigating further interrupt conditions can result in data errors.

When two interrupt conditions have the same priority, it is important to service these interrupts correctly. Receive Data Ready and Receive Time-Out have the same interrupt priority (when enabled by IER[0]). The receiver issues an interrupt after the number of characters have reached the programmed trigger level. In this case, the SC68C652B FIFO may hold more characters than the programmed trigger level. Following the removal of a data byte, the user should re-check LSR[0] for additional characters. A Receive Time-Out will not occur if the receive FIFO is empty. The time-out counter is reset at the center of each stop bit received or each time the receive holding register (RHR) is read. The actual time-out value is 4 character time, including data information length, start bit, parity bit, and the size of stop bit, that is, 1×, 1.5×, or 2× bit times.

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6.8 Programmable baud rate generator

The SC68C652B supports high speed modem technologies that have increased input data rates by employing data compression schemes. For example, a 33.6 kbit/s modem that employs data compression may require a 115.2 kbit/s input data rate. A 128.0 kbit/s ISDN modem that supports data compression may need an input data rate of 460.8 kbit/s. The SC68C652B can support a standard data rate of 921.6 kbit/s.

A single baud rate generator is provided for the transmitter and receiver, allowing independent transmit/receive channel control. The programmable baud rate generator is capable of operating with a frequency of up to 80 MHz. To obtain maximum data rate, it is necessary to use full rail swing on the clock input. The SC68C652B can be configured for internal or external clock operation. For internal clock oscillator operation, an industry standard microprocessor crystal is connected externally between the XTAL1 and XTAL2 pins. Alternatively, an external clock can be connected to the XTAL1 pin to clock the internal baud rate generator for standard or custom rates (see Table 6).

The generator divides the input 16× clock by any divisor from 1 to ($2^{16} - 1$). The SC68C652B divides the basic external clock by 16. The basic 16× clock provides table rates to support standard and custom applications using the same system design. The rate table is configured via the DLL and DLM internal register functions. Customized baud rates can be achieved by selecting the proper divisor values for the MSB and LSB sections of baud rate generator.

Programming the baud rate generator registers DLM (MSB) and DLL (LSB) provides a user capability for selecting the desired final baud rate. The example in Table 6 shows the selectable baud rate table available when using a 1.8432 MHz external clock input.

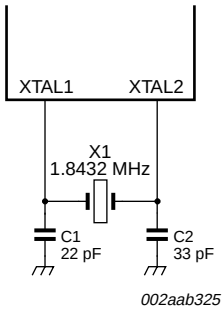


Fig 3. Crystal oscillator connection

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Table 6. Baud rate generator programming table using a 1.8432 MHz clock

Output baud rate	Output 16× clock divisor (decimal)	Output 16× clock divisor (HEX)	DLM program value (HEX)	DLL program value (HEX)
50	2304	900	09	00
75	1536	600	06	00
110	1047	417	04	17
150	768	300	03	00
300	384	180	01	80
600	192	C0	00	C0
1200	96	60	00	60
2400	48	30	00	30
3600	32	20	00	20
4800	24	18	00	18
7200	16	10	00	10
9600	12	0C	00	0C
19.2 k	6	06	00	06
38.4 k	3	03	00	03
57.6 k	2	02	00	02
115.2 k	1	01	00	01

6.9 DMA operation

The SC68C652B FIFO trigger level provides additional flexibility to the user for block mode operation. The user can optionally operate the transmit and receive FIFOs in the DMA mode (FCR[3]). The DMA mode affects the state of the $\overline{\text{RXRDY}}$n and $\overline{\text{TXRDY}}$n output pins. Table 7 and Table 8 show this.

Table 7. Effect of DMA mode on state of $\overline{\text{RXRDY}}$n pin

Non-DMA mode	DMA mode
1 = FIFO empty	0-to-1 transition when FIFO empties
0 = at least 1 byte in FIFO	1-to-0 transition when FIFO reaches trigger level, or time-out occurs

Table 8. Effect of DMA mode on state of $\overline{\text{TXRDY}}$n pin

Non-DMA mode	DMA mode
1 = at least 1 byte in FIFO	0-to-1 transition when FIFO becomes full
0 = FIFO empty	1-to-0 transition when FIFO goes below trigger level

6.10 Loopback mode

The internal loopback capability allows on-board diagnostics. In the loopback mode, the normal modem interface pins are disconnected and reconfigured for loopback internally (see Figure 4). MCR[3:0] register bits are used for controlling loopback diagnostic testing. In the loopback mode, the transmitter output pin (TXn) and the receiver input pin (RXn) are disconnected from their associated interface pins, and instead are connected together internally. The $\overline{\text{CTS}}$n, $\overline{\text{DSR}}$n, $\overline{\text{CD}}$n, and $\overline{\text{RI}}$n pins are disconnected from their normal modem control inputs pins, and instead are connected internally to MCR[1] $\overline{\text{RTS}}$,

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MCR[0] $\overline{DTR}$, MCR[3] ($\overline{OP2}$) and MCR[2] ($\overline{OP1}$). Loopback test data is entered into the transmit holding register via the user data bus interface, D0 to D7. The transmit UART serializes the data and passes the serial data to the receive UART via the internal loopback connection. The receive UART converts the serial data back into parallel data that is then made available at the user data interface D0 to D7. The user optionally compares the received data to the initial transmitted data for verifying error-free operation of the UART transmit/receive circuits.

In this mode, the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational.

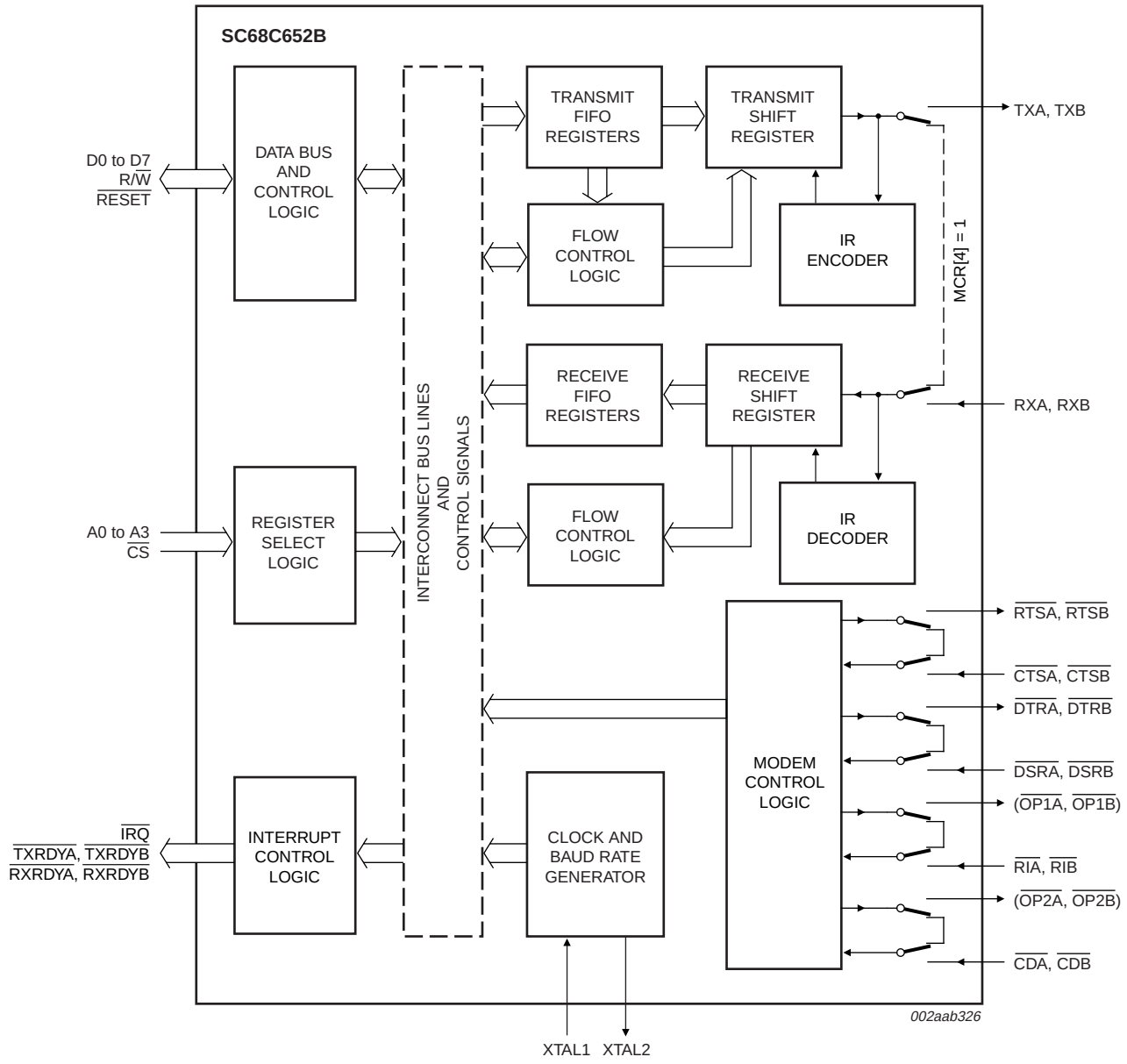


Fig 4. Internal loopback mode diagram

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7. Register descriptions

Table 9 details the assigned bit functions for the SC68C652B internal registers. The assigned bit functions are more fully defined in Section 7.1 through Section 7.11.

Table 9. SC68C652B internal registers

A2	A1	A0	Register	Default[1]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
General register set[2]												
0	0	0	RHR	XX	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	0	0	THR	XX	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	0	1	IER	00	CTS interrupt [3]	RTS interrupt [3]	Xoff interrupt [3]	Sleep mode[3]	modem status interrupt RX	receive line status interrupt	transmit holding register interrupt	receive holding register
0	1	0	FCR	00	RCVR trigger (MSB)	RCVR trigger (LSB)	TX trigger (MSB)[3]	TX trigger (LSB)[3]	DMA mode select	XMIT FIFO reset	RCVR FIFO reset	FIFOs enable
0	1	0	ISR	01	FIFOs enabled	FIFOs enabled	INT priority bit 4	INT priority bit 3	INT priority bit 2	INT priority bit 1	INT priority bit 0	INT status
0	1	1	LCR	00	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit 1	word length bit 0
1	0	0	MCR	00	clock select[3]	IRDA enable	0	loopback	$\overline{OP2}$ control	($\overline{OP1}$)	$\overline{RTS}$	$\overline{DTR}$
1	0	1	LSR	60	FIFO data error	THR and TSR empty	THR empty	break interrupt	framing error	parity error	overrun error	receive data ready
1	1	0	MSR	X0	CD	RI	DSR	CTS	$\Delta\overline{CD}$	$\Delta\overline{RI}$	$\Delta\overline{DSR}$	$\Delta\overline{CTS}$
1	1	1	SPR	FF	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Special register set[4]												
0	0	0	DLL	XX	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	0	1	DLM	XX	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
Enhanced register set[5]												
0	1	0	EFR	00	Auto-CTS	Auto-RTS	Special character detect	Enable IER[4:7], ISR[4:5], FCR[4:5], MCR[5:7]	Cont-3 TX, RX Control	Cont-2 TX, RX Control	Cont-1 TX, RX Control	Cont-0 TX, RX Control
1	0	0	Xon1	00	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
1	0	1	Xon2	00	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
1	1	0	Xoff1	00	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
1	1	1	Xoff2	00	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8

[1] The value shown in represents the register's initialized hexadecimal value; X = not applicable.

[2] Accessible only when LCR[7] is logic 0.

[3] These bits are only accessible when EFR[4] is set.

[4] Baud rate registers accessible only when LCR[7] is logic 1.

[5] Enhanced Feature Register, Xon1/Xon2 and Xoff1/Xoff2 are accessible only when LCR is set to 'BFh'.

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7.1 Transmit Holding Register (THR) and Receive Holding Register (RHR)

The serial transmitter section consists of an 8-bit Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the THR is provided in the Line Status Register (LSR). Writing to the THR transfers the contents of the data bus (D[7:0]) to the TSR and UART via the THR, providing that the THR is empty. The THR empty flag in the LSR register will be set to a logic 1 when the transmitter is empty or when data is transferred to the TSR. Note that a write operation can be performed when the THR empty flag is set (logic 0 = at least one byte in FIFO/THR, logic 1 = FIFO/THR empty).

The serial receive section also contains an 8-bit Receive Holding Register (RHR) and a Receive Serial Shift Register (RSR). Receive data is removed from the SC68C652B and receive FIFO by reading the RHR register. The receive section provides a mechanism to prevent false starts. On the falling edge of a start or false start bit, an internal receiver counter starts counting clocks at the 16× clock rate. After $7\frac{1}{2}$ clocks, the start bit time should be shifted to the center of the start bit. At this time the start bit is sampled, and if it is still a logic 0 it is validated. Evaluating the start bit in this manner prevents the receiver from assembling a false character. Receiver status codes will be posted in the LSR.

7.2 Interrupt Enable Register (IER)

The Interrupt Enable Register (IER) masks the interrupts from receiver ready, transmitter empty, line status and modem status registers. These interrupts would normally be seen on the $\overline{IRQ}$ output pin.

Table 10. Interrupt Enable Register bits description

Bit	Symbol	Description
7	IER[7]	CTS interrupt logic 0 = disable the CTS interrupt (normal default condition) logic 1 = enable the CTS interrupt. The SC68C652B issues an interrupt when the $\overline{CTSn}$ pin transitions from a logic 0 to a logic 1.
6	IER[6]	RTS interrupt logic 0 = disable the RTS interrupt (normal default condition) logic 1 = enable the RTS interrupt. The SC68C652B issues an interrupt when the $\overline{RTSn}$ pin transitions from a logic 0 to a logic 1.
5	IER[5]	Xoff interrupt logic 0 = disable the software flow control, receive Xoff interrupt (normal default condition) logic 1 = enable the software flow control, receive Xoff interrupt
4	IER[4]	Sleep mode logic 0 = disable Sleep mode (normal default condition) logic 1 = enable Sleep mode
3	IER[3]	Modem Status Interrupt. This interrupt will be issued whenever there is a modem status change as reflected in MSR[3:0]. logic 0 = disable the modem status register interrupt (normal default condition) logic 1 = enable the modem status register interrupt

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Table 10. Interrupt Enable Register bits description *…continued*

Bit	Symbol	Description
2	IER[2]	Receive Line Status interrupt. This interrupt will be issued whenever a receive data error condition exists as reflected in LSR[4:1]. logic 0 = disable the receiver line status interrupt (normal default condition) logic 1 = enable the receiver line status interrupt
1	IER[1]	Transmit Holding Register interrupt. In the 16C450 mode, this interrupt will be issued whenever the THR is empty, and is associated with LSR[5]. In the FIFO modes, this interrupt will be issued whenever the FIFO is empty. logic 0 = disable the Transmit Holding Register Empty (TXRDY) interrupt (normal default condition) logic 1 = enable the TXRDY (ISR level 3) interrupt
0	IER[0]	Receive Holding Register. In the 16C450 mode, this interrupt will be issued when the RHR has data, or is cleared when the RHR is empty. In the FIFO mode, this interrupt will be issued when the FIFO has reached the programmed trigger level or is cleared when the FIFO drops below the trigger level. logic 0 = disable the receiver ready (ISR level 2, RXRDY) interrupt (normal default condition) logic 1 = enable the RXRDY (ISR level 2) interrupt

7.2.1 IER versus Transmit/Receive FIFO interrupt mode operation

When the receive FIFO (FCR[0] = logic 1), and receive interrupts (IER[0] = logic 1) are enabled, the receive interrupts and register status will reflect the following:

- The receive RXRDY interrupt (Level 2 ISR interrupt) is issued to the external CPU when the receive FIFO has reached the programmed trigger level. It will be cleared when the receive FIFO drops below the programmed trigger level.
- Receive FIFO status will also be reflected in the user accessible ISR register when the receive FIFO trigger level is reached. Both the ISR register receive status bit and the interrupt will be cleared when the FIFO drops below the trigger level.
- The receive data ready bit (LSR[0]) is set as soon as a character is transferred from the shift register (RSR) to the receive FIFO. It is reset when the FIFO is empty.
- When the Transmit FIFO and interrupts are enabled, an interrupt is generated when the transmit FIFO is empty due to the unloading of the data by the TSR and UART for transmission via the transmission media. The interrupt is cleared either by reading the ISR register, or by loading the THR with new data characters.

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7.2.2 IER versus Receive/Transmit FIFO polled mode operation

When FCR[0] = logic 1, resetting IER[0:3] enables the SC68C652B in the FIFO polled mode of operation. In this mode, interrupts are not generated and the user must poll the LSR register for transmit and/or receive data status. Since the receiver and transmitter have separate bits in the LSR either or both can be used in the polled mode by selecting respective transmit or receive control bit(s).

- LSR[0] will be a logic 1 as long as there is one byte in the receive FIFO.
- LSR[4:1] will provide the type of receive errors, or a receive break, if encountered.
- LSR[5] will indicate when the transmit FIFO is empty.
- LSR[6] will indicate when both the transmit FIFO and transmit shift register are empty.
- LSR[7] will show if any FIFO data errors occurred.

7.3 FIFO Control Register (FCR)

This register is used to enable the FIFOs, clear the FIFOs, set the receive FIFO trigger levels, and select the DMA mode.

7.3.1 DMA mode

7.3.1.1 Mode 0 (FCR bit 3 = 0)

Set and enable the interrupt for each single transmit or receive operation, and is similar to the 16C450 mode. Transmit Ready pin ($\overline{\text{TXRDYn}}$) will go to a logic 0 whenever the FIFO (THR, if FIFO is not enabled) is empty. Receive Ready pin ($\overline{\text{RXRDYn}}$) will go to a logic 0 whenever the Receive Holding Register (RHR) is loaded with a character.

7.3.1.2 Mode 1 (FCR bit 3 = 1)

Set and enable the interrupt in a block mode operation. The transmit interrupt is set when the transmit FIFO is below the programmed trigger level. The receive interrupt is set when the receive FIFO fills to the programmed trigger level. However, the FIFO continues to fill regardless of the programmed level until the FIFO is full. $\overline{\text{RXRDYn}}$ remains a logic 0 as long as the FIFO fill level is above the programmed trigger level.

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7.3.2 FIFO mode

Table 11. FIFO Control Register bits description

Bit	Symbol	Description
7:6	FCR[7:6]	RCVR trigger. These bits are used to set the trigger level for the receive FIFO interrupt. An interrupt is generated when the number of characters in the FIFO equals the programmed trigger level. However, the FIFO will continue to be loaded until it is full. Refer to Table 12.
5:4	FCR[5:4]	TX trigger. Logic 0 or cleared is the default condition; TX trigger level = 16. These bits are used to set the trigger level for the transmit FIFO interrupt. The SC68C652B will issue a transmit empty interrupt when the number of characters in FIFO drops below the selected trigger level. Refer to Table 13.
3	FCR[3]	DMA mode select logic 0 = set DMA mode ‘0’ (normal default condition) logic 1 = set DMA mode ‘1’ **Transmit operation in mode ‘0’:** When the SC68C652B is in the 16C450 mode (FIFOs disabled; FCR[0] = logic 0) or in the FIFO mode (FIFOs enabled; FCR[0] = logic 1; FCR[3] = logic 0), and when there are no characters in the transmit FIFO or transmit holding register, the $\overline{\text{TXRDYn}}$ pin will be a logic 0. Once active, the $\overline{\text{TXRDYn}}$ pin will go to a logic 1 after the first character is loaded into the transmit holding register. **Receive operation in mode ‘0’:** When the SC68C652B is in 16C450 mode, or in the FIFO mode (FCR[0] = logic 1; FCR[3] = logic 0) and there is at least one character in the receive FIFO, the $\overline{\text{RXRDYn}}$ pin will be a logic 0. Once active, the $\overline{\text{RXRDYn}}$ pin will go to a logic 1 when there are no more characters in the receiver. **Transmit operation in mode ‘1’:** When the SC68C652B is in FIFO mode (FCR[0] = logic 1; FCR[3] = logic 1), the $\overline{\text{TXRDYn}}$ pin will be a logic 1 when the transmit FIFO is completely full. It will be a logic 0 when the trigger level has been reached. **Receive operation in mode ‘1’:** When the SC68C652B is in FIFO mode (FCR[0] = logic 1; FCR[3] = logic 1) and the trigger level has been reached, or a Receive Time-Out has occurred, the $\overline{\text{RXRDYn}}$ pin will go to a logic 0. Once activated, it will go to a logic 1 after there are no more characters in the FIFO.
2	FCR[2]	XMIT FIFO reset logic 0 = no FIFO transmit reset (normal default condition) logic 1 = clears the contents of the transmit FIFO and resets the FIFO counter logic (the transmit shift register is not cleared or altered). This bit will return to a logic 0 after clearing the FIFO.
1	FCR[1]	RCVR FIFO reset logic 0 = no FIFO receive reset (normal default condition). logic 1 = clears the contents of the receive FIFO and resets the FIFO counter logic (the receive shift register is not cleared or altered). This bit will return to a logic 0 after clearing the FIFO.
0	FCR[0]	FIFO enable logic 0 = disable the transmit and receive FIFO (normal default condition) logic 1 = enable the transmit and receive FIFO. **This bit must be a ‘1’ when other FCR bits are written to, or they will not be programmed.**

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Table 12. RCVR trigger levels

FCR[7]	FCR[6]	Receive FIFO trigger level (bytes)
0	0	8
0	1	16
1	0	24
1	1	28

Table 13. TX FIFO trigger levels

FCR[5]	FCR[4]	TX FIFO trigger level (bytes)
0	0	16
0	1	8
1	0	24
1	1	30

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7.4 Interrupt Status Register (ISR)

The SC68C652B provides six levels of prioritized interrupts to minimize external software interaction. The Interrupt Status Register (ISR) provides the user with six interrupt status bits. Performing a read cycle on the ISR will provide the user with the highest pending interrupt level to be serviced. No other interrupts are acknowledged until the pending interrupt is serviced. A lower level interrupt may be seen after servicing the higher level interrupt and re-reading the interrupt status bits. Table 14 “Interrupt source” shows the data values (bit 0 to bit 5) for the six prioritized interrupt levels and the interrupt sources associated with each of these interrupt levels.

Table 14. Interrupt source

Priority level	ISR[5]	ISR[4]	ISR[3]	ISR[2]	ISR[1]	ISR[0]	Source of the interrupt
1	0	0	0	1	1	0	LSR (Receiver Line Status Register)
2	0	0	0	1	0	0	RXRDY (Received Data Ready)
2	0	0	1	1	0	0	RXRDY (Receive Data time-out)
3	0	0	0	0	1	0	TXRDY (Transmitter Holding Register Empty)
4	0	0	0	0	0	0	MSR (Modem Status Register)
5	0	1	0	0	0	0	RXRDY (received Xoff signal)/ special character
6	1	0	0	0	0	0	CTS, RTS change-of-state

Table 15. Interrupt Status Register bits description

Bit	Symbol	Description
7:6	ISR[7:6]	FIFOs enabled. These bits are set to a logic 0 when the FIFOs are not being used in the 16C450 mode. They are set to a logic 1 when the FIFOs are enabled in the SC68C652B mode. logic 0 or cleared = default condition
5:4	ISR[5:4]	INT priority bits 4:3. These bits are enabled when EFR[4] is set to a logic 1. ISR[4] indicates that matching Xoff character(s) have been detected. ISR[5] indicates that CTS, RTS have been generated. Note that once set to a logic 1, the ISR[4] bit will stay a logic 1 until Xon character(s) are received. logic 0 or cleared = default condition
3:1	ISR[3:1]	INT priority bits 2:0. These bits indicate the source for a pending interrupt at interrupt priority levels 1, 2, and 3 (see Table 14). logic 0 or cleared = default condition
0	ISR[0]	INT status logic 0 = an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine logic 1 = no interrupt pending (normal default condition)

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7.5 Line Control Register (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The word length, the number of stop bits, and the parity are selected by writing the appropriate bits in this register.

Table 16. Line Control Register bits description

Bit	Symbol	Description
7	LCR[7]	Divisor latch enable. The internal baud rate counter latch and Enhanced Feature mode enable. logic 0 = divisor latch disabled (normal default condition) logic 1 = divisor latch enabled
6	LCR[6]	Set break. When enabled, the Break control bit causes a break condition to be transmitted (the TXn output pin is forced to a logic 0 state). This condition exists until disabled by setting LCR[6] to a logic 0. logic 0 = no break condition (normal default condition) logic 1 = forces the transmitter output pin (TXn) to a logic 0 for alerting the remote receiver to a line break condition
5:3	LCR[5:3]	Set parity; even parity; parity enable. Programs the parity conditions (see Table 17).
2	LCR[2]	Stop bits. The length of stop bit is specified by this bit in conjunction with the programmed word length (see Table 18). logic 0 or cleared = default condition
1:0	LCR[1:0]	Word length bits 1, 0. These two bits specify the word length to be transmitted or received (see Table 19). logic 0 or cleared = default condition

Table 17. LCR[5:3] parity selection

LCR[5]	LCR[4]	LCR[3]	Parity selection
X	X	0	no parity
X	0	1	odd parity
0	1	1	even parity
0	0	1	forced parity ‘1’
1	1	1	forced parity ‘0’

Table 18. LCR[2] stop bit length

LCR[2]	Word length	Stop bit length (bit times)
0	5, 6, 7, 8	1
1	5	$1\frac{1}{2}$
1	6, 7, 8	2

Table 19. LCR[1:0] word length

LCR[1]	LCR[0]	Word length
0	0	5
0	1	6
1	0	7
1	1	8

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7.6 Modem Control Register (MCR)

This register controls the interface with the modem or a peripheral device.

Table 20. Modem Control Register bits description

Bit	Symbol	Description
7	MCR[7]	Clock select logic 0 = divide-by-1 clock input logic 1 = divide-by-4 clock input
6	MCR[6]	IR enable (see Figure 16) logic 0 = enable the standard modem receive and transmit input/output interface (normal default condition) logic 1 = enable infrared IrDA receive and transmit inputs/outputs. While in this mode, the TXn/RXn output/inputs are routed to the infrared encoder/decoder. The data input and output levels will conform to the IrDA infrared interface requirement. As such, while in this mode, the infrared TXn output will be a logic 0 during idle data conditions.
5	MCR[5]	reserved; set to '0'
4	MCR[4]	Loopback. Enable the local loopback mode (diagnostics). In this mode the transmitter output (TXn) and the receiver input (RXn), $\overline{CTSn}$, $\overline{DSRn}$, $\overline{CDn}$, and $\overline{RIn}$ pins are disconnected from the SC68C652B I/O pins. Internally the modem data and control pins are connected into a loopback data configuration (see Figure 4). In this mode, the receiver and transmitter interrupts remain fully operational. The Modem Control Interrupts are also operational, but the interrupts' sources are switched to the lower four bits of the Modem Control. Interrupts continue to be controlled by the IER register. logic 0 = disable loopback mode (normal default condition) logic 1 = enable local loopback mode (diagnostics)
3	MCR[3]	$\overline{OP2}$ control logic 0 = forces $\overline{OP2n}$ output pin to HIGH state logic 1 = forces $\overline{OP2n}$ output pin to LOW state. In loopback mode, controls MSR[7].
2	MCR[2]	($\overline{OP1}$). $\overline{OP1A}$/$\overline{OP1B}$ are not available as an external signal in the SC68C652B. This bit is instead used in the loopback mode only. In the loopback mode, this bit is used to write the state of the modem $\overline{RIn}$ pin interface signal.
1	MCR[1]	$\overline{RTS}$ logic 0 = force $\overline{RTSn}$ output pin to a logic 1 (normal default condition) logic 1 = force $\overline{RTSn}$ output pin to a logic 0
0	MCR[0]	$\overline{DTR}$ logic 0 = force $\overline{DTRn}$ output pin to a logic 1 (normal default condition) logic 1 = force $\overline{DTRn}$ output pin to a logic 0

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7.7 Line Status Register (LSR)

This register provides the status of data transfers between the SC68C652B and the CPU.

Table 21. Line Status Register bits description

Bit	Symbol	Description
7	LSR[7]	FIFO data error logic 0 = no error (normal default condition) logic 1 = at least one parity error, framing error or break indication is in the current FIFO data. This bit is cleared when there are no remaining error flags associated with the remaining data in the FIFO.
6	LSR[6]	THR and TSR empty. This bit is the Transmit Empty indicator. This bit is set to a logic 1 whenever the transmit holding register and the transmit shift register are both empty. It is reset to logic 0 whenever either the THR or TSR contains a data character. In the FIFO mode, this bit is set to '1' whenever the transmit FIFO and transmit shift register are both empty.
5	LSR[5]	THR empty. This bit is the Transmit Holding Register Empty indicator. This bit indicates that the UART is ready to accept a new character for transmission. In addition, this bit causes the UART to issue an interrupt to CPU when the THR interrupt enable is set. The THR bit is set to a logic 1 when a character is transferred from the transmit holding register into the transmitter shift register. The bit is reset to a logic 0 concurrently with the loading of the transmitter holding register by the CPU. In the FIFO mode, this bit is set when the transmit FIFO is empty; it is cleared when at least 1 byte is written to the transmit FIFO.
4	LSR[4]	Break interrupt logic 0 = no break condition (normal default condition) logic 1 = the receiver received a break signal (RXn pin was a logic 0 for one character frame time). In the FIFO mode, only one break character is loaded into the FIFO.
3	LSR[3]	Framing error logic 0 = no framing error (normal default condition) logic 1 = framing error. The receive character did not have a valid stop bit(s). In the FIFO mode, this error is associated with the character at the top of the FIFO.
2	LSR[2]	Parity error logic 0 = no parity error (normal default condition logic 1 = parity error. The receive character does not have correct parity information and is suspect. In the FIFO mode, this error is associated with the character at the top of the FIFO.
1	LSR[1]	Overrun error logic 0 = no overrun error (normal default condition) logic 1 = overrun error. A data overrun error occurred in the receive shift register. This happens when additional data arrives while the FIFO is full. In this case, the previous data in the shift register is overwritten. Note that under this condition, the data byte in the receive shift register is not transferred into the FIFO, therefore the data in the FIFO is not corrupted by the error.
0	LSR[0]	Receive data ready logic 0 = no data in receive holding register or FIFO (normal default condition). logic 1 = data has been received and is saved in the receive holding register or FIFO.

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7.8 Modem Status Register (MSR)

This register provides the current state of the control interface signals from the modem, or other peripheral device to which the SC68C652B is connected. Four bits of this register are used to indicate the changed information. These bits are set to a logic 1 whenever a control input from the modem changes state. These bits are set to a logic 0 whenever the CPU reads this register.

Table 22. Modem Status Register bits description

Bit	Symbol	Description
7	MSR[7]	CD. During normal operation, this bit is the complement of the $\overline{CDn}$ input pin. Reading this bit in the loopback mode produces the state of MCR[3] ($\overline{OP2}$).
6	MSR[6]	RI. During normal operation, this bit is the complement of the $\overline{RIn}$ input pin. Reading this bit in the loopback mode produces the state of MCR[2] ($\overline{OP1}$).
5	MSR[5]	DSR. During normal operation, this bit is the complement of the $\overline{DSRn}$ input pin. During the loopback mode, this bit is equivalent to the state of MCR[0].
4	MSR[4]	CTS. During normal operation, this bit is the complement of the $\overline{CTSn}$ input pin. During the loopback mode, this bit is equivalent to the state of MCR[1].
3	MSR[3]	$\Delta\overline{CD}$ [1] logic 0 = no change of state on $\overline{CDn}$ pin (normal default condition) logic 1 = the $\overline{CDn}$ input pin to the SC68C652B has changed state since the last time it was read. A modem Status Interrupt will be generated.
2	MSR[2]	$\Delta\overline{RI}$ [1] logic 0 = no change of state on $\overline{RIn}$ pin (normal default condition) logic 1 = the $\overline{RIn}$ input pin to the SC68C652B has changed from a logic 0 to a logic 1. A modem Status Interrupt will be generated.
1	MSR[1]	$\Delta\overline{DSR}$ [1] logic 0 = no change of state on $\overline{DSRn}$ pin (normal default condition) logic 1 = the $\overline{DSRn}$ input pin to the SC68C652B has changed state since the last time it was read. A modem Status Interrupt will be generated.
0	MSR[0]	$\Delta\overline{CTS}$ [1] logic 0 = no change of state on $\overline{CTSn}$ pin (normal default condition) logic 1 = the $\overline{CTSn}$ input pin to the SC68C652B has changed state since the last time it was read. A modem Status Interrupt will be generated.

[1] Whenever any MSR bit 3:0 is set to logic 1, a Modem Status Interrupt will be generated.

7.9 Scratchpad Register (SPR)

The SC68C652B provides a temporary data register to store 8 bits of user information.

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7.10 Enhanced Feature Register (EFR)

Enhanced features are enabled or disabled using this register.

Bits 0 through 4 provide single or dual character software flow control selection. When the Xon1 and Xon2 and/or Xoff1 and Xoff2 modes are selected, the double 8-bit words are concatenated into two sequential numbers.

Table 23. Enhanced Feature Register bits description

Bit	Symbol	Description
7	EFR[7]	Automatic CTS flow control logic 0 = automatic CTS flow control is disabled (normal default condition) logic 1 = enable automatic CTS flow control. Transmission will stop when $\overline{\text{CTSn}}$ goes to a logic 1. Transmission will resume when the $\overline{\text{CTSn}}$ pin returns to a logic 0.
6	EFR[6]	Automatic RTS flow control. Automatic RTS may be used for hardware flow control by enabling EFR[6]. When Auto-RTS is selected, an interrupt will be generated when the receive FIFO is filled to the programmed trigger level and $\overline{\text{RTSn}}$ will go to a logic 1 at the next trigger level. $\overline{\text{RTSn}}$ will return to a logic 0 when data is unloaded below the next lower trigger level (programmed trigger level 1). The state of this register bit changes with the status of the hardware flow control. $\overline{\text{RTSn}}$ functions normally when hardware flow control is disabled. logic 0 = automatic RTS flow control is disabled (normal default condition) logic 1 = enable automatic RTS flow control.
5	EFR[5]	Special character detect logic 0 = Special character detect disabled (normal default condition) logic 1 = Special character detect enabled. The SC68C652B compares each incoming receive character with Xoff2 data. If a match exists, the received data will be transferred to FIFO and ISR[4] will be set to indicate detection of special character. Bit-0 in the X-registers corresponds with the LSB bit for the receive character. When this feature is enabled, the normal software flow control must be disabled (EFR[3:0] must be set to a logic 0).
4	EFR[4]	Enhanced function control bit. The content of IER[7:4], ISR[5:4], FCR[5:4], and MCR[7:5] can be modified and latched. After modifying any bits in the enhanced registers, EFR[4] can be set to a logic 0 to latch the new values. This feature prevents existing software from altering or overwriting the SC68C652B enhanced functions. logic 0 = disable/latch enhanced features. IER[7:4], ISR[5:4], FCR[5:4], and MCR[7:5] are saved to retain the user settings, then IER[7:4] ISR[5:4], FCR[5:4], and MCR[7:5] are set to a logic 0 to be compatible with SC16C554 mode. (Normal default condition.) logic 1 = enables the enhanced functions. When this bit is set to a logic 1, all enhanced features of the SC68C652B are enabled and user settings stored during a reset will be restored.
3:0	EFR[3:0]	Cont-3:0 TX, RX control. Logic 0 or cleared is the default condition. Combinations of software flow control can be selected by programming these bits. See Table 24.

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Table 24. Software flow control functions[1]

Cont-3	Cont-2	Cont-1	Cont-0	TX, RX software flow controls
0	0	X	X	no transmit flow control
1	0	X	X	transmit Xon1/Xoff1
0	1	X	X	transmit Xon2/Xoff2
1	1	X	X	transmit Xon1 and Xon2/Xoff1 and Xoff2
X	X	0	0	no receive flow control
X	X	1	0	receiver compares Xon1/Xoff1
X	X	0	1	receiver compares Xon2/Xoff2
1	0	1	1	transmit Xon1/Xoff1
				receiver compares Xon1 and Xon2/Xoff1 and Xoff2
0	1	1	1	transmit Xon2/Xoff2
				receiver compares Xon1 and Xon2/Xoff1 and Xoff2
1	1	1	1	transmit Xon1 and Xon2/Xoff1 and Xoff2
				receiver compares Xon1 and Xon2/Xoff1 and Xoff2

[1] When using a software flow control the Xon/Xoff characters cannot be used for data transfer.

7.11 SC68C652B external reset condition

Table 25. Reset state for registers

Register	Reset state
IER	IER[7:0] = 0
FCR	FCR[7:0] = 0
ISR	ISR[7:1] = 0; ISR[0] = 1
LCR	LCR[7:0] = 0
MCR	MCR[7:0] = 0
LSR	LSR[7] = 0; LSR[6:5] = 1; LSR[4:0] = 0
MSR	MSR[7:4] = input signals; MSR[3:0] = 0
SPR	SFR[7:0] = 1
DLL	DLL[7:0] = X
DLM	DLM[7:0] = X

Table 26. Reset state for outputs

Output	Reset state
TXA, TXB	logic 1
$\overline{\text{OP2A}}$, $\overline{\text{OP2B}}$	logic 1
$\overline{\text{RTSA}}$, $\overline{\text{RTSB}}$	logic 1
$\overline{\text{DTRA}}$, $\overline{\text{DTRB}}$	logic 1
$\overline{\text{IRQ}}$	3-state condition

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8. Limiting values

Table 27. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-	7	V
V_n	voltage on any other pin	at D7 to D0 pins	GND – 0.3	V_{CC} + 0.3	V
		at input only pins	GND – 0.3	5.3	V
T_{amb}	ambient temperature	operating	–40	+85	°C
T_{stg}	storage temperature		–65	+150	°C
P_{tot}/pack	total power dissipation per package		-	500	mW

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9. Static characteristics

Table 28. Static characteristics

T_{amb} = −40 °C to +85 °C; tolerance of V_{CC} ± 10 %, unless otherwise specified.

Symbol	Parameter	Conditions	V_{CC} = 2.5 V		V_{CC} = 3.3 V		V_{CC} = 5.0 V		Unit
			Min	Max	Min	Max	Min	Max	
$V_{IL(clk)}$	clock LOW-level input voltage		−0.3	0.45	−0.3	0.6	−0.5	0.6	V
$V_{IH(clk)}$	clock HIGH-level input voltage		1.8	V_{CC}	2.4	V_{CC}	3.0	V_{CC}	V
V_{IL}	LOW-level input voltage	except X1 clock	−0.3	0.65	−0.3	0.8	−0.5	0.8	V
V_{IH}	HIGH-level input voltage	except X1 clock	1.6	-	2.0	-	2.2	-	V
V_{OL}	LOW-level output voltage	on all outputs [1]							
		I_{OL} = 5 mA (data bus)	-	-	-	-	-	0.4	V
		I_{OL} = 4 mA (other outputs)	-	-	-	0.4	-	-	V
		I_{OL} = 2 mA (data bus)	-	0.4	-	-	-	-	V
		I_{OL} = 1.6 mA (other outputs)	-	0.4	-	-	-	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = −5 mA (data bus)	-	-	-	-	2.4	-	V
		I_{OH} = −1 mA (other outputs)	-	-	2.0	-	-	-	V
		I_{OH} = −800 µA (data bus)	1.85	-	-	-	-	-	V
		I_{OH} = −400 µA (other outputs)	1.85	-	-	-	-	-	V
I_{LIL}	LOW-level input leakage current		-	±10	-	±10	-	±10	µA
$I_{L(clk)}$	clock leakage current		-	±30	-	±30	-	±30	µA
I_{CC}	supply current		-	3.5	-	4.5	-	4.5	mA
$I_{CC(sleep)}$	sleep mode supply current		-	200	-	200	-	200	µA
C_i	input capacitance		-	5	-	5	-	5	pF

[1] Except XTAL2; V_{OL} = 1 V typical.

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10. Dynamic characteristics

Table 29. Dynamic characteristics

T_{amb} = −40 °C to +85 °C; tolerance of V_{CC} ± 10 %, unless specified otherwise.

Symbol	Parameter	Conditions	V_{CC} = 2.5 V		V_{CC} = 3.3 V and 5 V		Unit
			Min	Max	Min	Max	
t_{d1}	R/$\overline{W}$ to chip select		10	-	10	-	ns
t_{d2}	read cycle delay	25 pF load	20	-	20	-	ns
t_{d3}	delay from $\overline{CS}$ to data	25 pF load	-	77	-	26	ns
t_{d4}	data disable time	25 pF load	-	15	-	15	ns
t_{d6}	write cycle delay		25	-	25	-	ns
t_{d7}	delay from write to output	25 pF load	-	100	-	33	ns
t_{d8}	delay to set interrupt from modem input	25 pF load	-	100	-	24	ns
t_{d9}	delay to reset interrupt from read	25 pF load	-	100	-	24	ns
t_{d10}	delay from stop to set interrupt		-	$1T_{RCLK}$[1]	-	$1T_{RCLK}$[1]	ns
t_{d11}	delay from read to reset interrupt	25 pF load	-	100	-	29	ns
t_{d12}	delay from start to set interrupt		-	100	-	100	ns
t_{d13}	delay from write to transmit start		$8T_{RCLK}$[1]	$24T_{RCLK}$[1]	$8T_{RCLK}$[1]	$24T_{RCLK}$[1]	ns
t_{d14}	delay from write to reset interrupt		-	100	-	70	ns
t_{d15}	delay from stop to set $\overline{RXRDY}$		-	$1T_{RCLK}$[1]	-	$1T_{RCLK}$[1]	ns
t_{d16}	delay from read to reset $\overline{RXRDY}$		-	100	-	75	ns
t_{d17}	delay from write to set $\overline{TXRDY}$		-	100	-	70	ns
t_{d18}	delay from start to reset $\overline{TXRDY}$		-	$16T_{RCLK}$[1]	-	$16T_{RCLK}$[1]	ns
t_{h2}	R/$\overline{W}$ hold time from $\overline{CS}$		10	-	10	-	ns
t_{h3}	data hold time		15	-	15	-	ns
t_{h4}	address hold time		15	-	15	-	ns
t_{WH}	pulse width HIGH		10	-	6	-	ns
t_{WL}	pulse width LOW		10	-	6	-	ns
f_{XTAL}	clock speed	[2][3]	-	48	-	80	MHz
$t_{(RESET)}$	$\overline{RESET}$ pulse width	[4]	200	-	200	-	ns
t_{su1}	address set-up time		10	-	10	-	ns
t_{su2}	data set-up time		16	-	16	-	ns
t_{w1}	$\overline{CS}$ strobe width		77	-	30	-	ns

[1] RCLK is an internal signal derived from Divisor Latch LSB (DLL) and Divisor Latch MSB (DLM) divisor latches.

[2] Applies to external clock; crystal oscillator max 24 MHz.

[3] $$f_{XTAL} = \frac{1}{t_{w(clk)}}$$

[4] Reset pulse must happen when $\overline{CS}$ is inactive.

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10.1 Timing diagrams

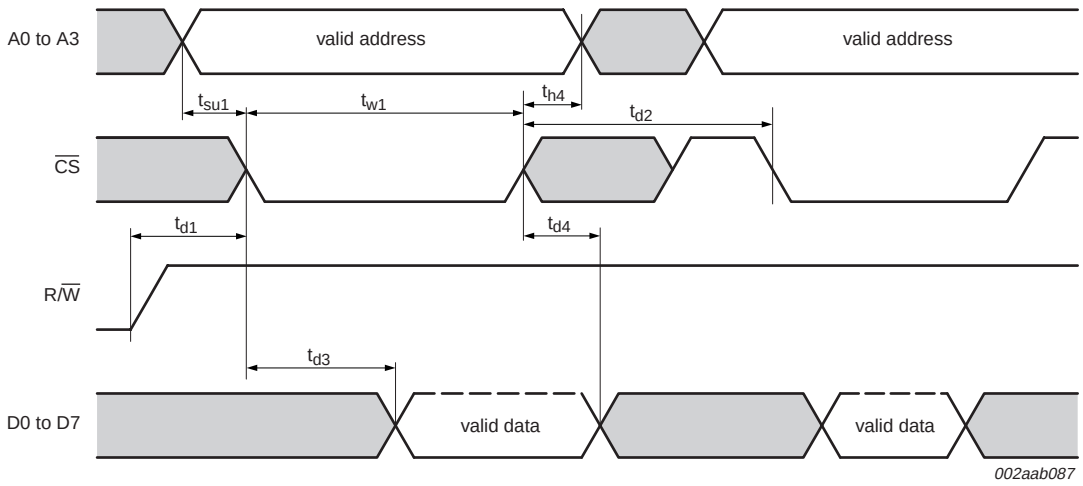


Fig 5. General read timing

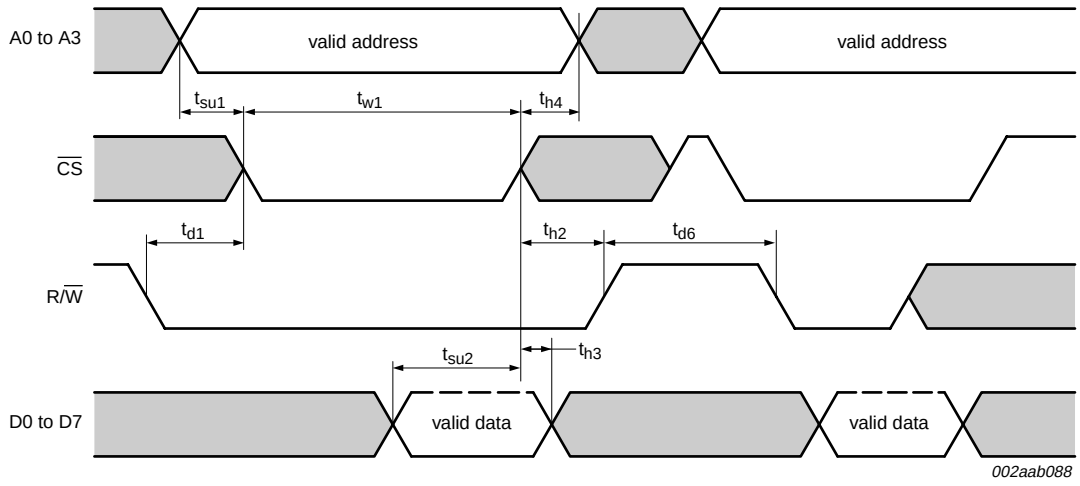
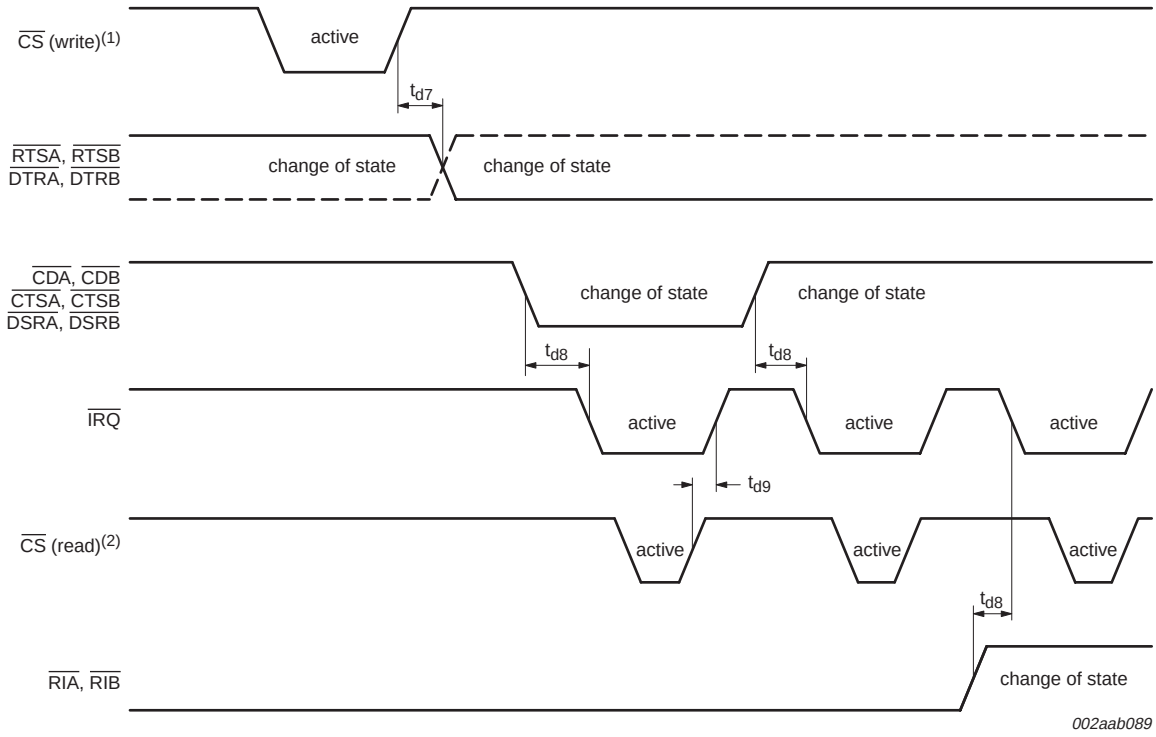


Fig 6. General write timing

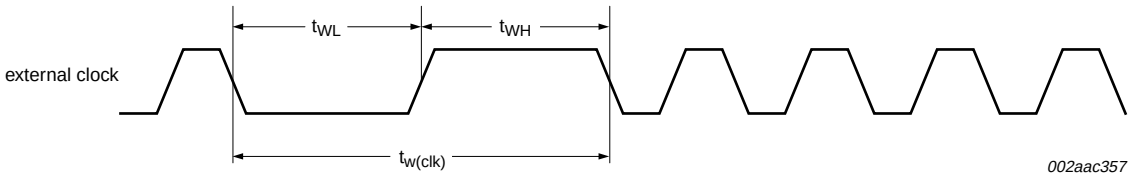
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(1) $\overline{CS}$ timing during a write cycle. See Figure 6.

(2) $\overline{CS}$ timing during a read cycle. See Figure 5.

Fig 7. Modem input/output timing



$$f_{XTAL} = \frac{1}{t_{w(clk)}}$$

Fig 8. External clock timing

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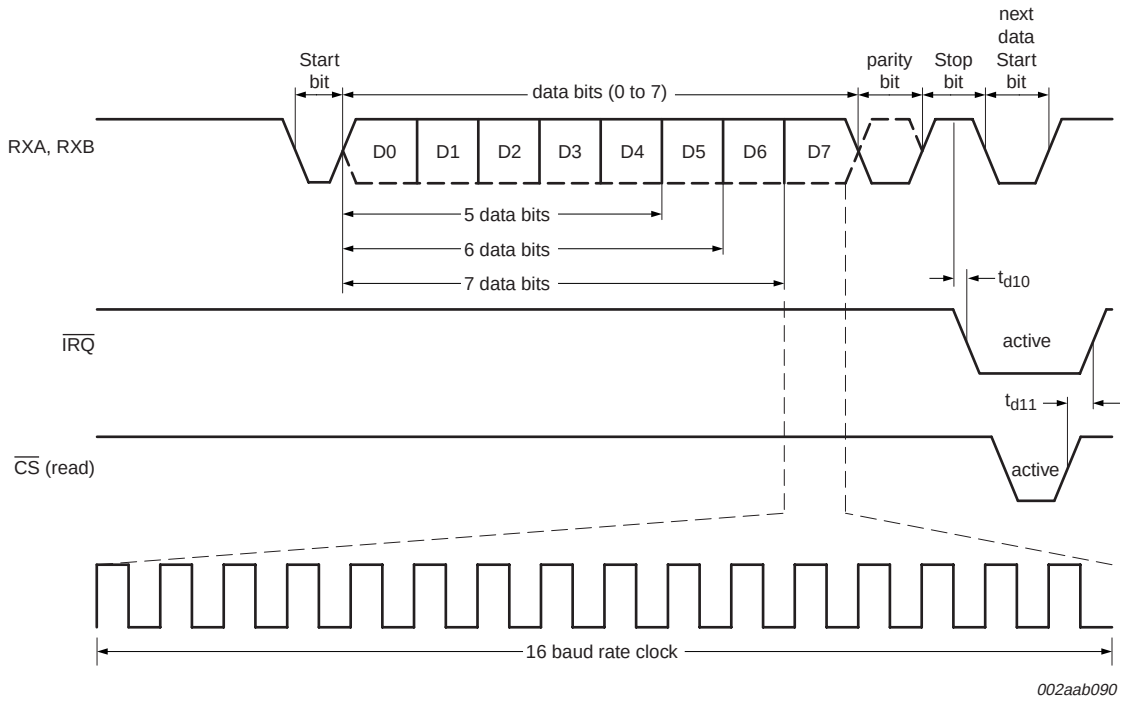


Fig 9. Receive timing

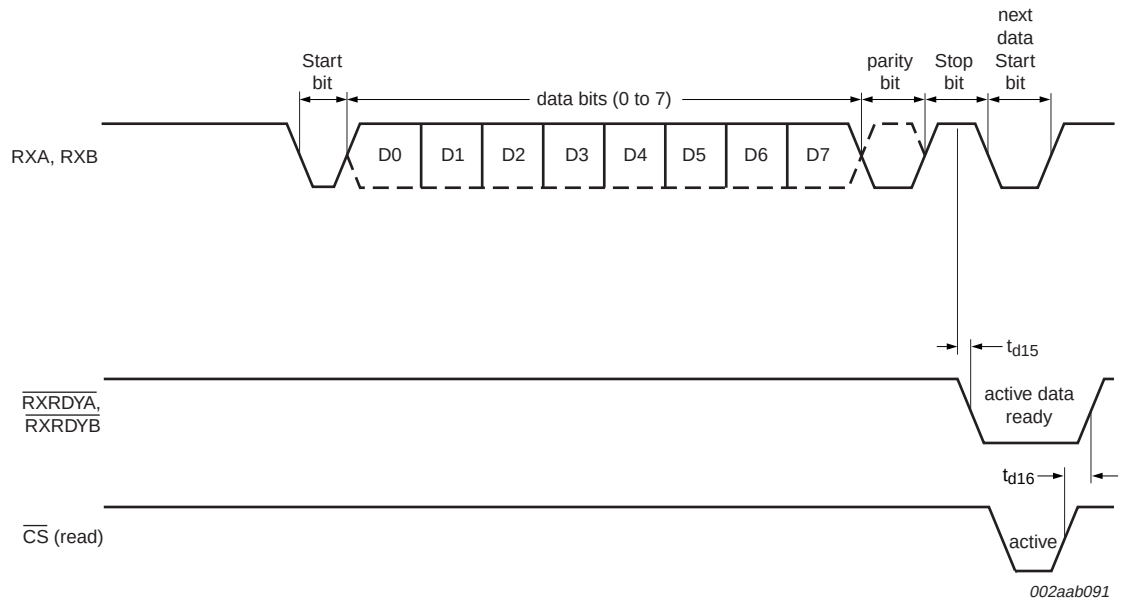


Fig 10. Receive ready timing in non-FIFO mode

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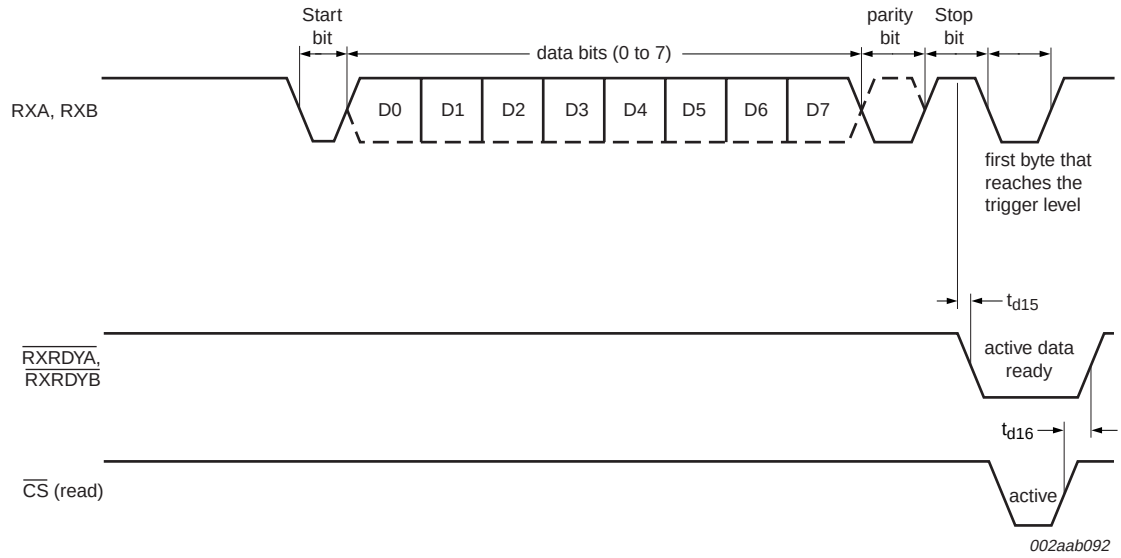


Fig 11. Receive ready timing in FIFO mode

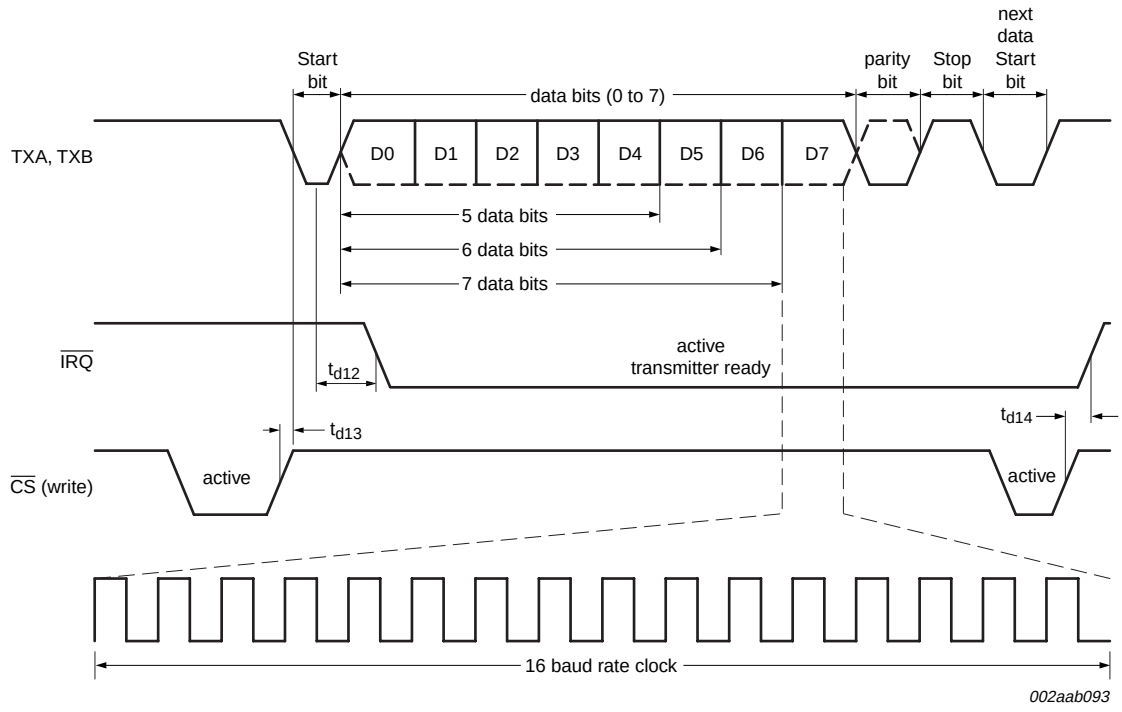


Fig 12. Transmit timing

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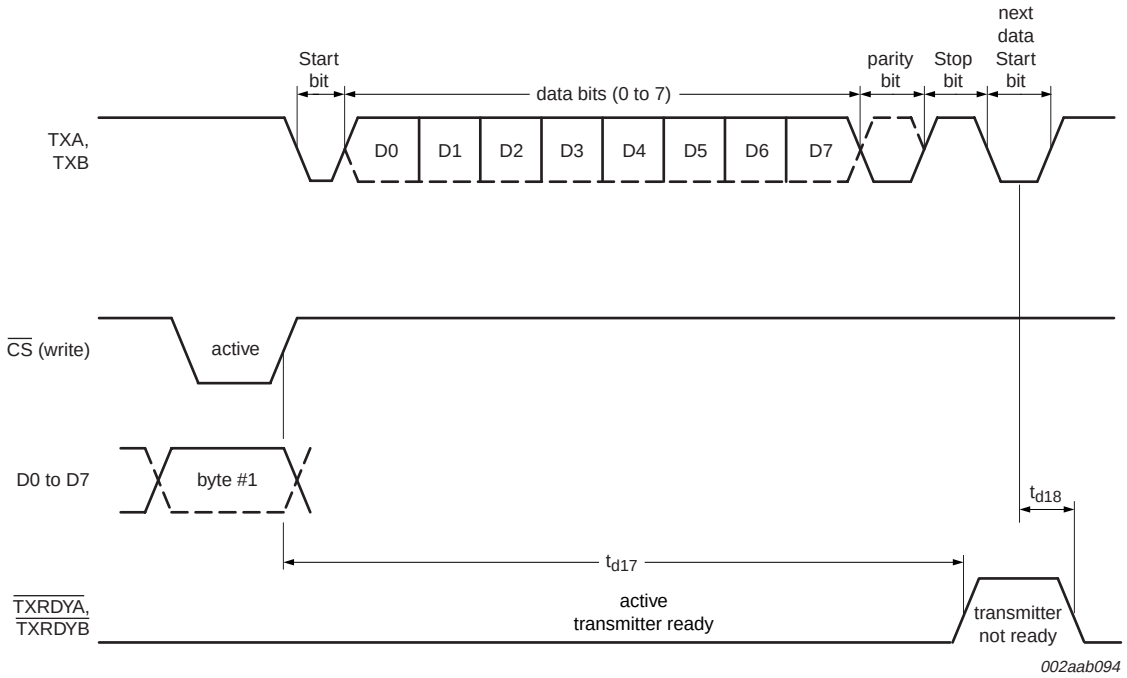


Fig 13. Transmit ready timing in non-FIFO mode

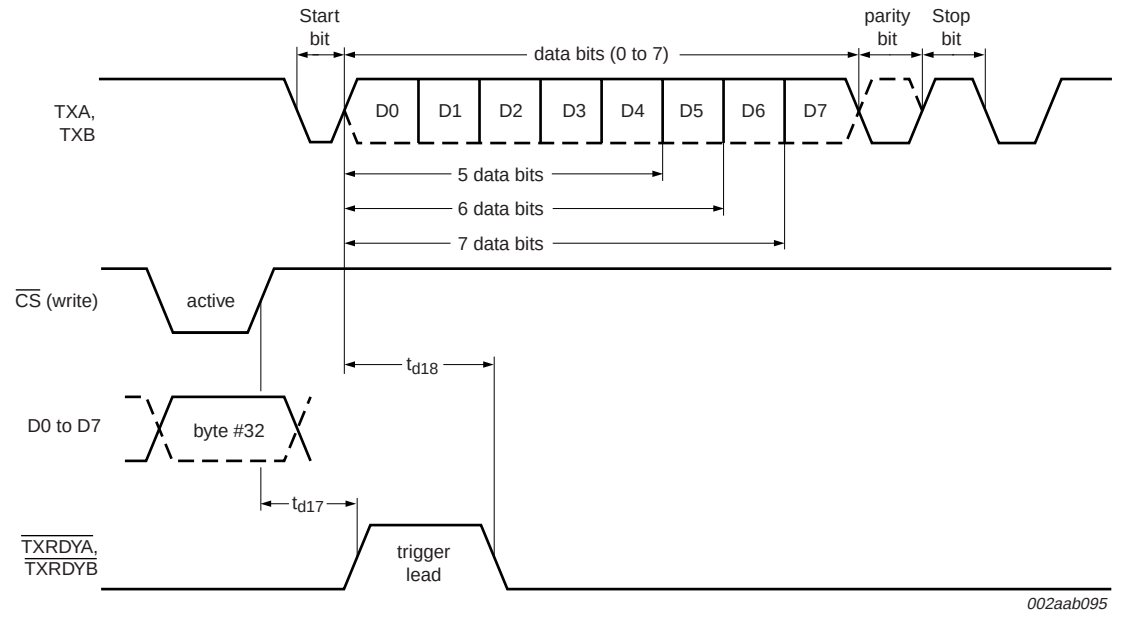


Fig 14. Transmit ready timing in FIFO mode

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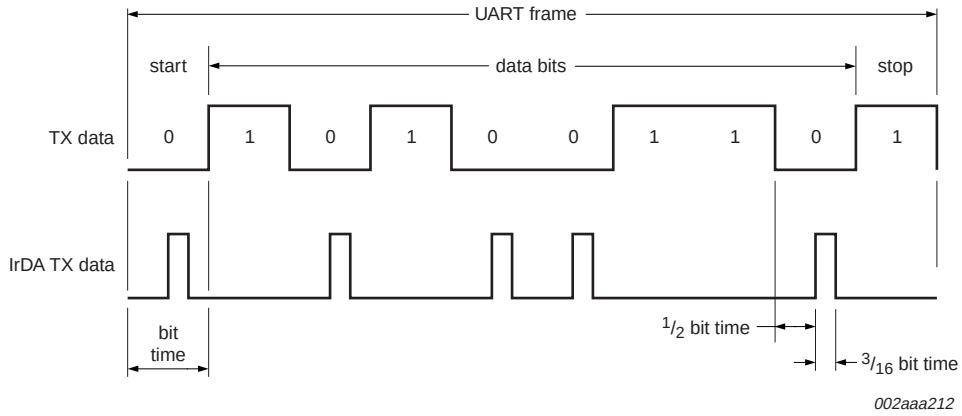


Fig 15. Infrared transmit timing

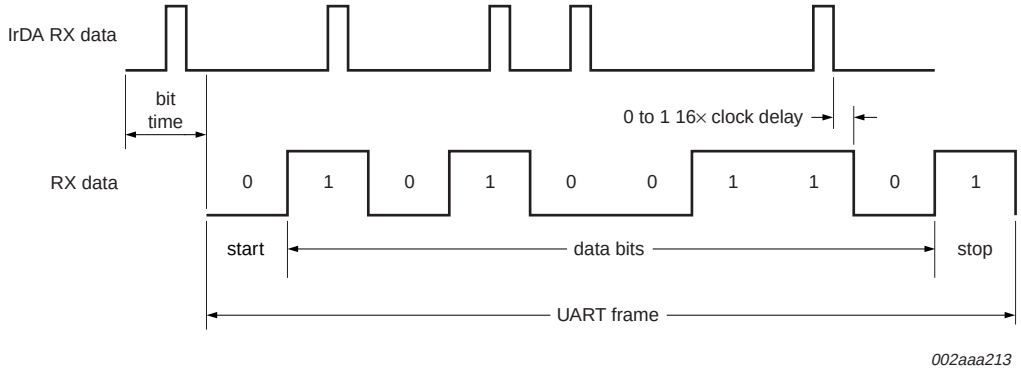
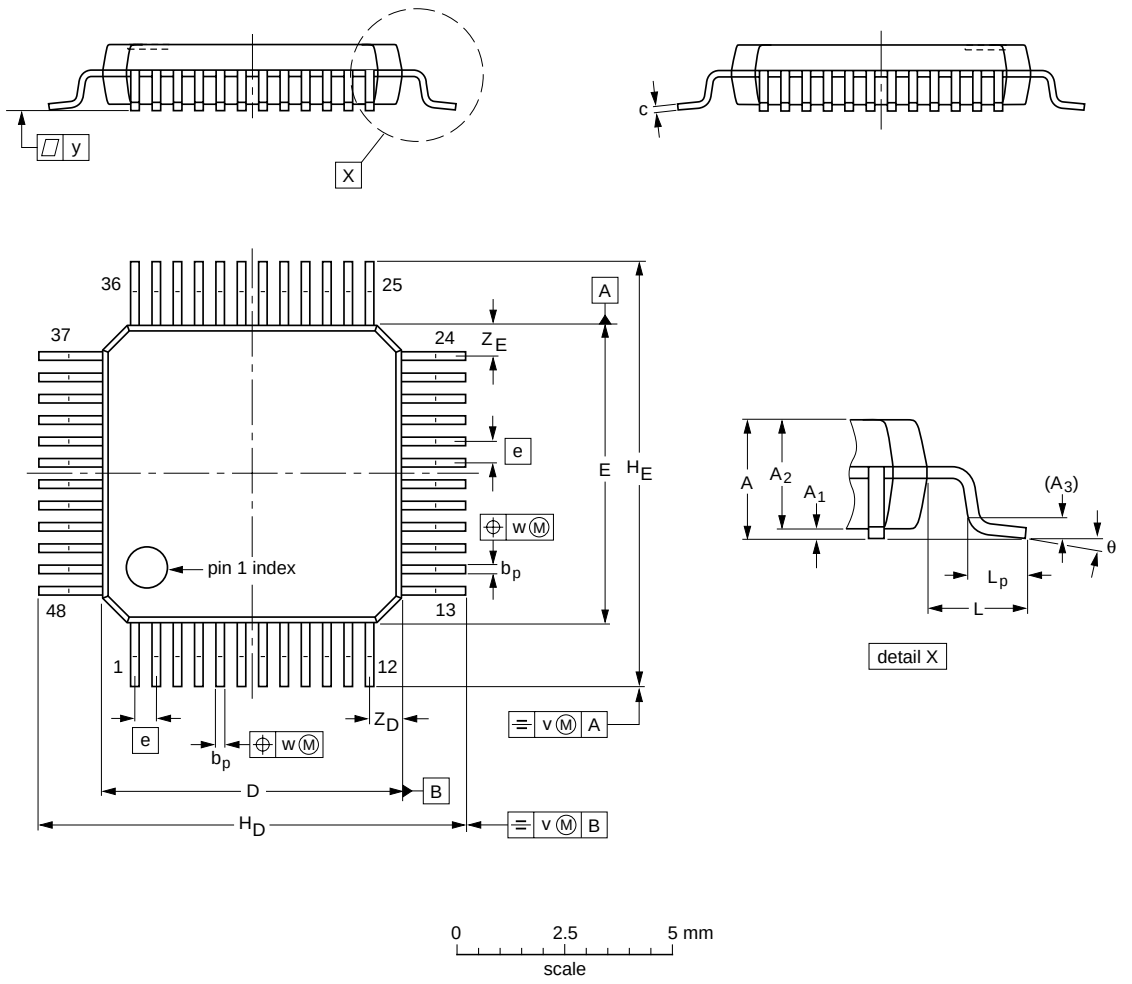


Fig 16. Infrared receive timing

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11. Package outline

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm **SOT313-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT313-2	136E05	MS-026				~~00-01-19~~ 03-02-25

Fig 17. Package outline SOT313-2 (LQFP48)

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12. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

12.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

12.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

12.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

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12.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 18) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 30 and 31

Table 30. SnPb eutectic process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

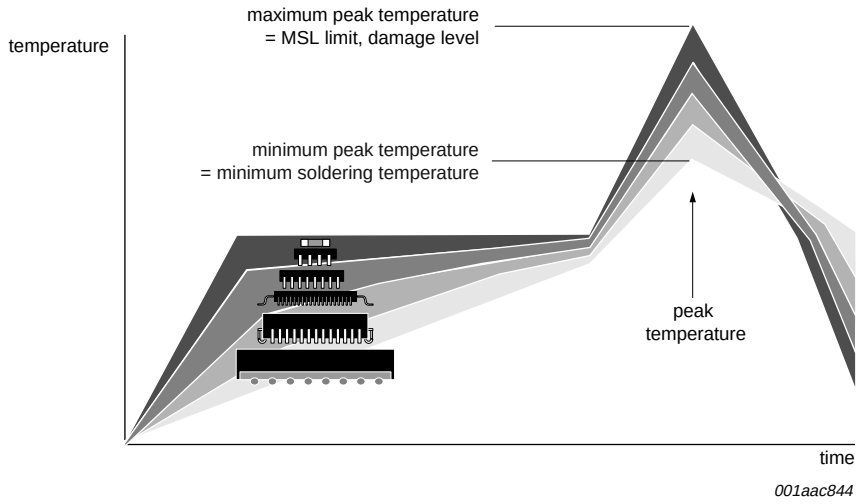
Table 31. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 18.

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MSL: Moisture Sensitivity Level

Fig 18. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

13. Abbreviations

Table 32. Abbreviations

Acronym	Description
CPU	Central Processing Unit
DMA	Direct Memory Access
FIFO	First In, First Out
IrDA	Infrared Data Association
ISDN	Integrated Service Digital Network
LSB	Least Significant Bit
MSB	Most Significant Bit
UART	Universal Asynchronous Receiver and Transmitter

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14. Revision history

Table 33. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
SC68C652B_2	20091102	Product data sheet	-	SC68C652B_1
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Data sheet title modified from "... and Motorola µP interface" to "... and 68 mode µP interface" • Section 2 "Features", 3rd bullet item re-written; added Footnote 1 • Table 10 "Interrupt Enable Register bits description", description of bit 0: changed from "In the 68C450 mode" to "In the 16C450 mode" • Table 11 "FIFO Control Register bits description", description of bit 3: changed from "in the 68C450 mode" to "in the 16C450 mode" (in 2 places) • Table 27 "Limiting values": – Symbol V_n split to show 2 separate conditions: "at D7 to D0 pins" and "at input only pins" – Symbol "$P_{tot(pack)}$" changed to "P_{tot}/pack" – Parameter for T_{amb} changed from "operating temperature" to "ambient temperature"; "operating" moved to Conditions column • Table 28 "Static characteristics": – Descriptive line below table title changed from "V_{CC} = 2.5 V, 3.3 V ± 10 % or 5 V ± 10 %" to "tolerance of V_{CC} ± 10 %" – Symbol/parameter changed from "$V_{IL(CK)}$, LOW-level clock input voltage" to "$V_{IL(clk)}$, clock LOW-level input voltage" – Symbol/parameter changed from "$V_{IH(CK)}$, HIGH-level clock input voltage" to "$V_{IH(clk)}$, clock HIGH-level input voltage" – Symbol changed from "I_{CL}" to "$I_{L(clk)}$" – Parameter for $I_{CC(sleep)}$ changed from "sleep current" to "sleep mode supply current" • Table 29 "Dynamic characteristics": – Descriptive line below table title changed from "V_{CC} = 2.5 V, 3.3 V ± 10 % or 5 V ± 10 %" to "tolerance of V_{CC} ± 10 %" – Symbol/parameter "t_{1w}, t_{2w}, clock cycle period" is split into "t_{WH}, pulse width HIGH" and "t_{WL}, pulse width LOW" – Table note [3]: denominator in equation changed from "t_{3w}" to "$t_{w(clk)}$" – added Table note [4] and its reference at $t_{(RESET)}$ • Figure 8 "External clock timing": – "t_{w2}" changed to "t_{WL}" – "t_{w1}" changed to "t_{WH}" – "t_{w3}" changed to "$t_{w(clk)}$" • Updated soldering information			
SC68C652B_1 (9397 750 14657)	20050425	Product data sheet	-	-

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15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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