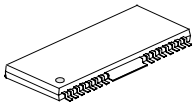
UTC UA9392 LINEAR INTEGRATED CIRCUIT

4-CHANNEL BTL DRIVE FOR CD PLAYERS



HSOP-28

DESCRIPTION

The UTC UA9392 is a 4-channel BTL driver for CD plsyer motors and actuators. It has an internal primary filter, and can be directly connected (without attached components) to the servo PWM output of all drivers other than the spindle driver.

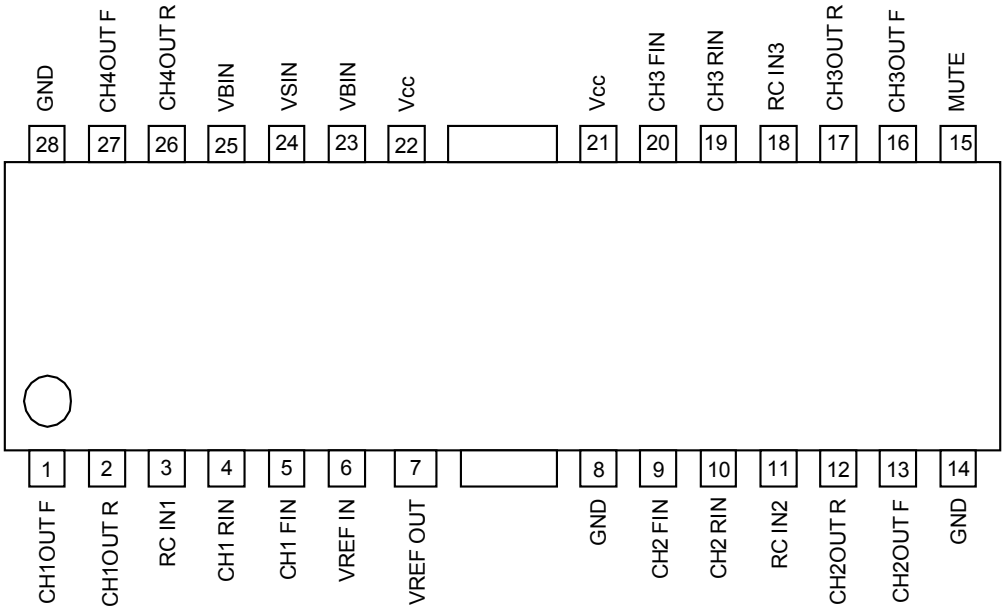
FEATURES

*PWM input is filtered by the internal primary filter, eliminating the need for attached resistors and capacitors, thereby helping reduce the number of components. Resistor and capacitor time constant can be changed with attached components.
*Internal mute circuit.
*Thermal shutdown circuit is contained.
*Level-shift circuit is contained.

APPLICATIONS

CD players, CD-ROM drives.

PIN CONFIGURATION

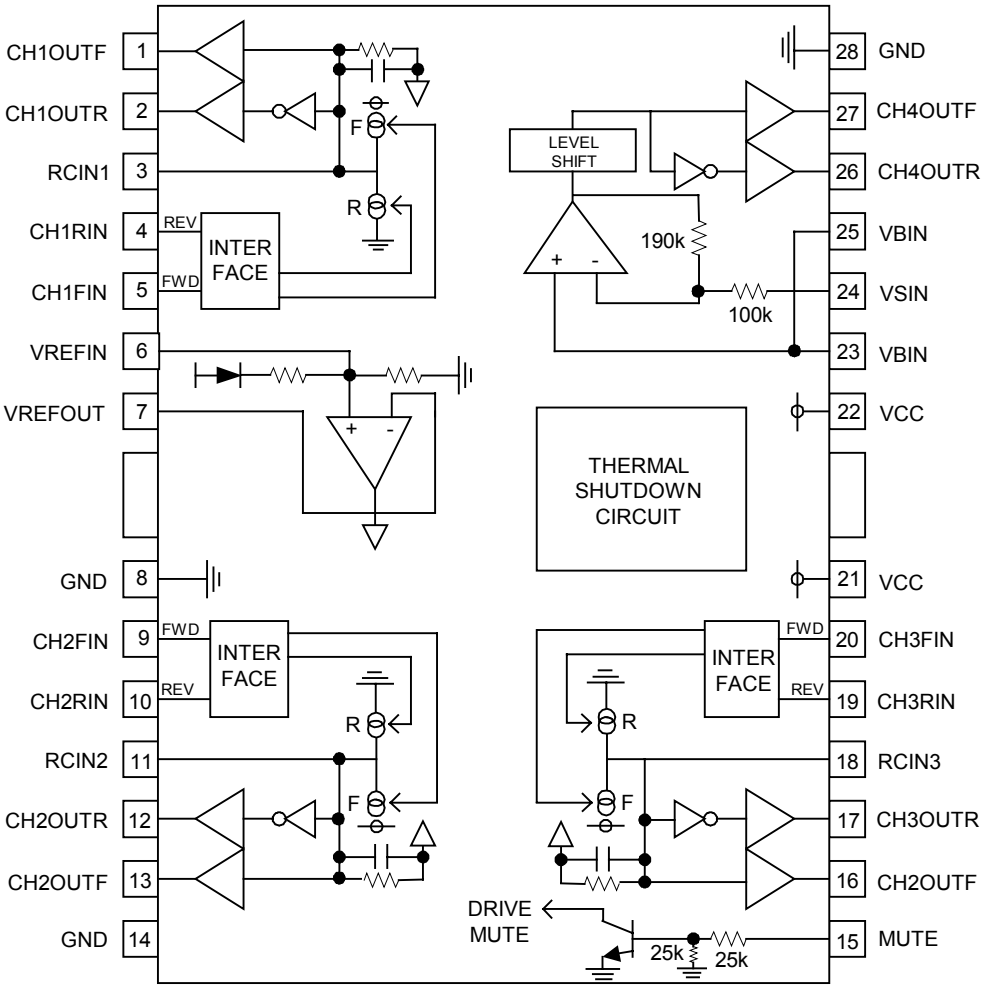


PIN DESCRIPTIONS

PIN NO.	PIN NAME	DESCRIPTION
1	CH1OUT F	Drive channel 1 forward output
2	CH1OUT R	Drive channel 1 reverse output
3	RC IN1	Connect to attach resistor/capacitor(1)
4	CH1 RIN	Drive channel 1 reverse input
5	CH1 FIN	Drive channel 1 forward input
6	VREF IN	Internal reference amplifier input
7	VREF OUT	Internal reference amplifier output
8	GND	Ground for internal reference and internal power circuit
9	CH2 FIN	Drive channel 2 forward input
10	CH2 RIN	Drive channel 2 reverse input
11	RC IN2	Connect to attach resistor/capacitor(2)
12	CH2OUT R	Drive channel 2 reverse output
13	CH2OUT F	Drive channel 2 forward output
14	GND	Ground for internal reference and internal power circuit
15	MUTE	Drive mute control input
16	CH3OUT F	Drive channel 3 forward output
17	CH3OUT R	Drive channel 3 reverse output
18	RC IN3	Connect to attach resistor/capacitor(3)
19	CH3 RIN	Drive channel 3 reverse input
20	CH3 FIN	Drive channel 3 forward input
21	Vcc	Power supply
22	Vcc	Power supply
23	VBIN	Drive channel 4 bias input*
24	VSIN	Drive channel 4 input
25	VBIN	Drive channel 4 bias input*
26	CH4OUT R	Drive channel 4 reverse output
27	CH4OUT F	Drive channel 4 forward output
28	GND	Ground for internal reference and internal power circuit

*Pin23 and Pin25 are shorted internally.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Power supply voltage	Vcc	16	V
Power dissipation	Pd	1.6 *1	W
Operating temperature	Topr	-30 ~ +80	℃
Storage temperature	Tstg	-55 ~ +150	℃

*1: Reduce by 13.6mW for each increase in Ta of 1℃ over 25℃,When mounted on a 50 * 50 * 1.0 mm phenol paper PCB.

RECOMMENDED OPEATING CONDITIONS(Ta=25℃)

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	Vcc	5 ~ 10 *2	V

*2 Set the power supply voltage according to power dissipation.

ELECTRICAL CHARACTERISTICS(Ta=25℃,Vcc=8V,f=1kHz,RL=8Ω, unless otherwise specified)

ITEMS	SYMBOL	TEST CONDITIONS	MIN	TYP.	MAX	UNIT
Quiescent current	I_Q	No load	5	12	18	mA
Bias pin voltage	V_{BIAS}		3.4	3.68	4.00	V
Bias pin voltage reguration	$\triangle V_{BIAS}$	1mA source, sink	-30		30	mV
Mute-off voltage	V_{MOFF}		2.0			V
Mute-on voltage	V_{MON}				0.5	V
<Drive(other than spindle)>						
Input high level voltage	V_{IH}		2.4			V
Input low level voltage	V_{IL}				0.5	V
Input high level current	I_{IH}	V_{IN}=5V	170	310	450	μA
Input low level current	I_{IL}	V_{IN}=0V	-10		0	μA
Output voltage,offset	V_{OO}	(Same for spindle)	-30		30	mV
Output high level voltage	V_{OHD}	F_{IN}=5V, R_{IN}=0V	4.90	5.40		V
Output low level voltage	V_{OLD}	F_{IN}=0V, R_{IN}=5V		1.50	2.00	V
Constant current	I_{CONST}		14	22	30	μA
Internal integral capacitance	C			24		pF
Current pulse rise time 1	△tr	At startup		0.08	1	μs
Current pulse fall time 2	△tf	At shutdown		0.55	1	μs
Current pulse time differential	△tr-f		-160		160	μs
Driver linearity	LIN	$V_{IN}=V_{REF}\pm0.5,1,1.5$*1	90	100	110	%
Ripple rejection	RR	V_{IN}=100mVrms,100Hz		70		dB
<Spindle driver>						
Input bias current	I_B			10	300	nA
Synchronous input voltage	V_{ICM}		1.6		6.4	V
Max.output voltage high	V_{OHD}		4.90	5.40		V
Max.output voltage low	V_{OLD}			1.50	2.00	V
Voltage gain	G_{VC}		8.0	10.5	13	dB
Slew rate	SR			2		V/μs
Ripple rejection	RR_S	V_{IN}=100mVrms, 100Hz		70		dB

*1: if Vo=V01 when $V_{IN}=V_{REF}\pm0.5$V,Vo=V02 when $V_{IN}=V_{REF}\pm1.0$V,and Vo=V03 when $V_{IN}=V_{REF}\pm1.5$V,then L_{IN}=(V03 * V02)/(V02 * V01) *100%.

CIRCUIT OPERATION

(1) Fig. 2 shows the inputs from the digital servo IC for CH1-CH3 drivers(all drivers except the spindle).SW1 is on when the forward input signal(HIGH level, over 2.4V) is present,SW2 I on when the reverse input signal is present (Fig. 1) The constant current (I_1) at this time enters the RC and generates an integral waveform based on the duty of the input waveform. The BTL is output from BUF1 and BUF2 (Fig.3).

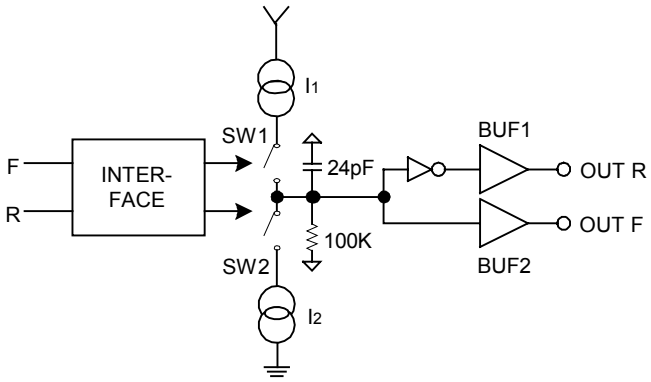


Fig. 1

To maintain the HIGH level with forward (or reverse) in-put, the DC voltage generated at point A is:
$I_1 \times R \fallingdotseq 2.5V$ (reverse : - 2.5V)

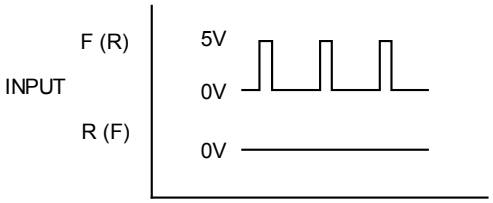


Fig. 2

This is the voltage generated relative V_{REF}. The setting is such that a voltage differential of 5V is generated be-tween output pins. The time constant is:

$$R \times C = 2.4\ \mu sec$$

This can be increased by inserting a capacitor between point A (pin3,11and 18) and V_{REF} •The constant current (Iconst) given in the electrical characteristics refers to I_1 and I_2 in Fig.1.

(2) CH4 driver (spindle driver) Pins 23 and 25 are shorted inside the IC.Bias amplitudes are the primarytype of inputs assumed.

F	R	SW2	SW1
L	L	OFF	OFF
L	H	OFF	ON
H	L	ON	OFF
H	H	OFF	OFF

H: 2.4V Max.
L: 0.5V Min.

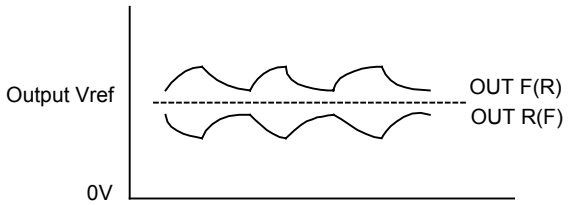


Fig. 3

The level shift circuit converts the pre-stage amplifier output (centered on the bias level and impressed on pins 23 and 25) to positive and negative amplitudes centered on $V_{REF.}$ The level shift circuit' s output is BTL-output from the buffer amplifier.

Because of the high input impedance, the IC is designed to accommodate filter comprising attached resistors and capacitors.

(Example) For secondary filters

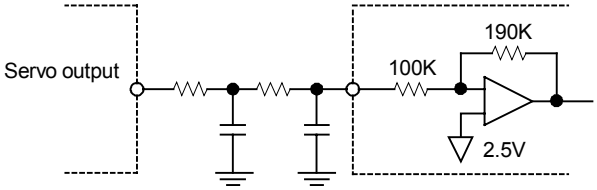
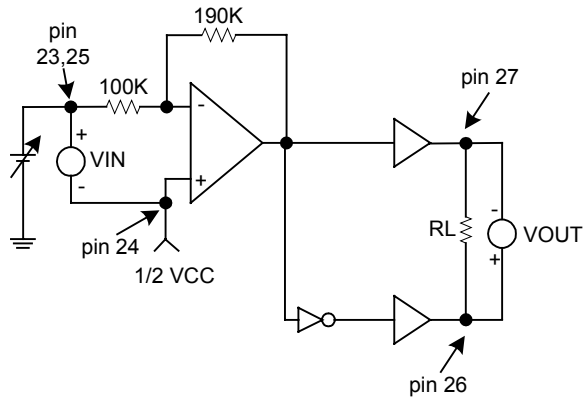


Fig. 4

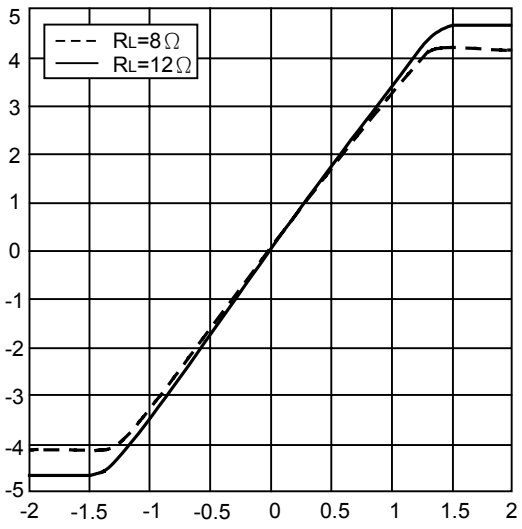
OPERATION NOTES

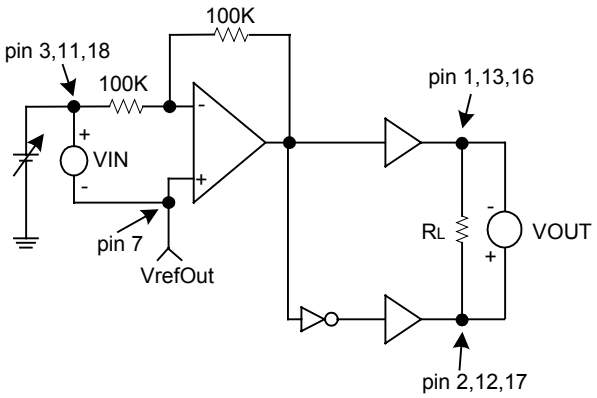
(1) The UTC UA9392 has an internal thermal shutdown circuit. Output current is muted when the chip temperature exceeds 180℃(typically).
(2) The output current can also be muted by lower the mute pin (pin 15) voltage below 0.5V.
(3) All four driver output channels are muted during thermal shutdown, muting and a drop in bias pin voltage. No other components are muted.

I/O ELECTRICAL CHARACTERISTICS

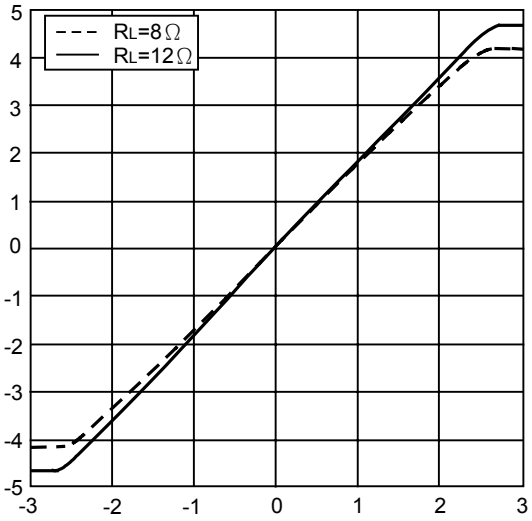


CH4 Output Drive

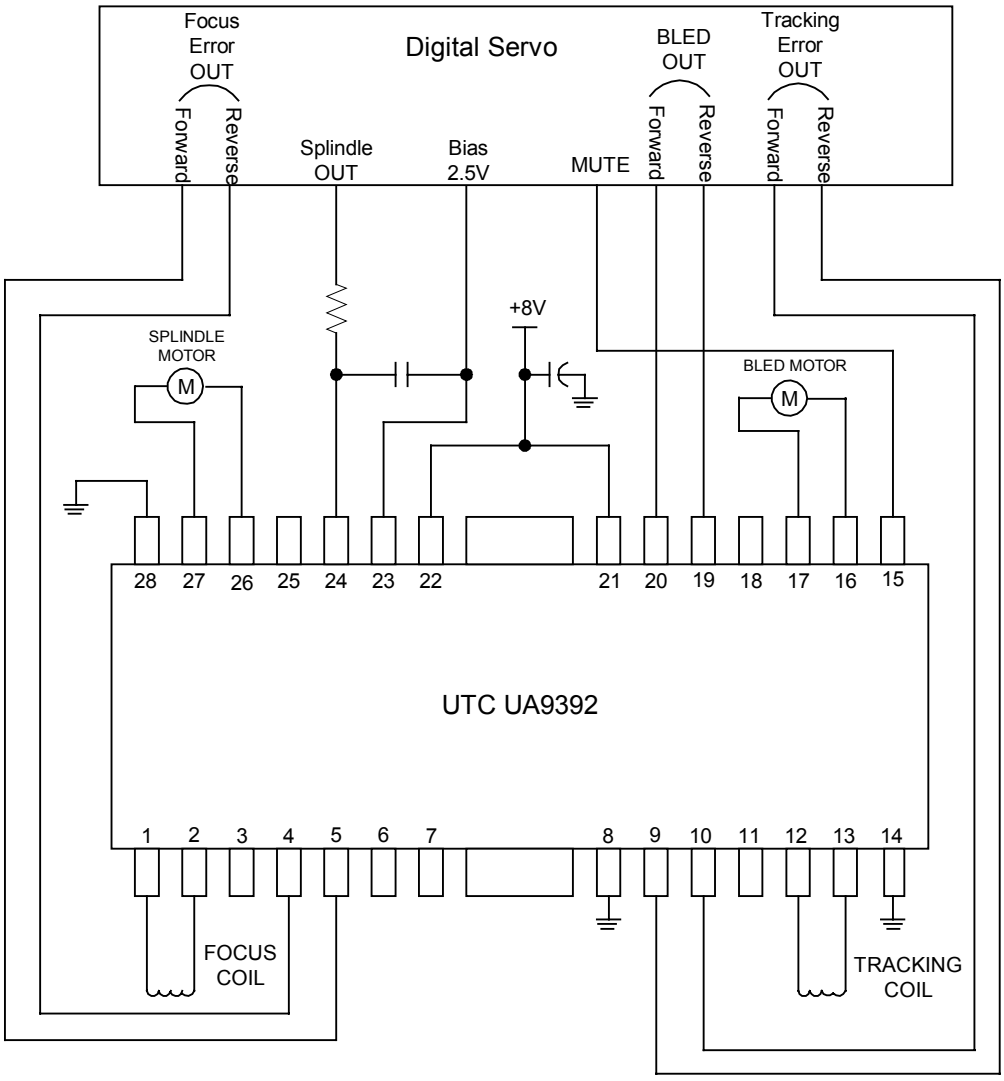




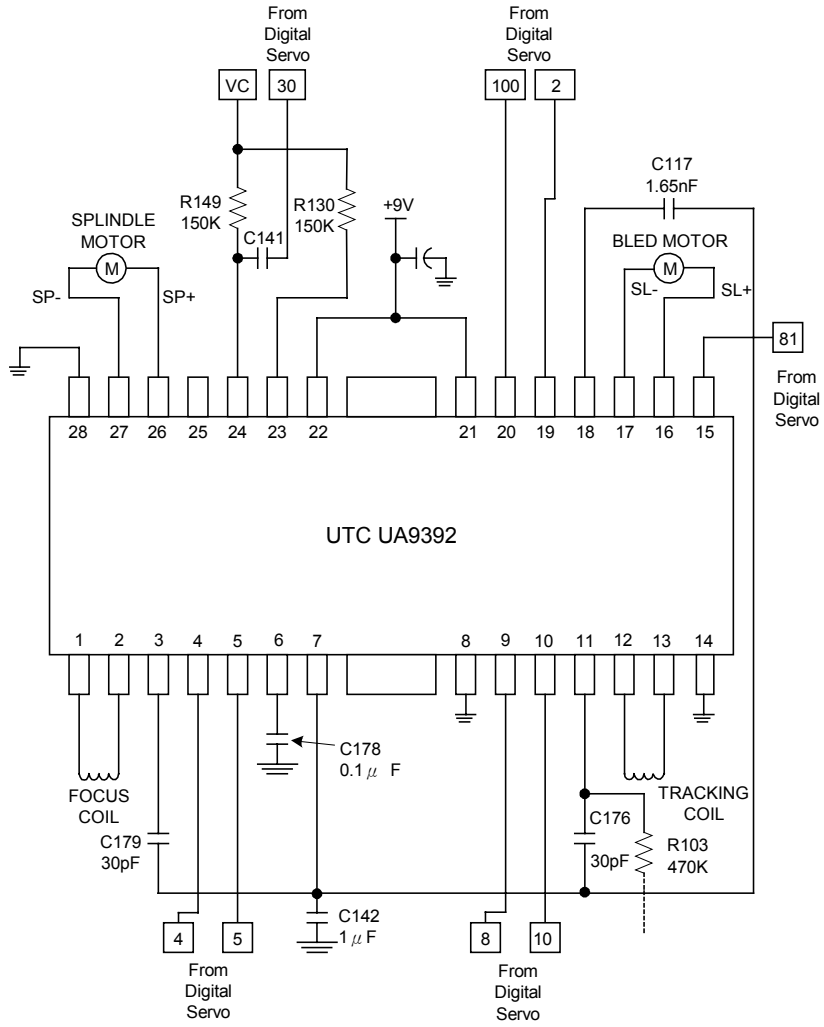
CH1/2/3 Output Drive



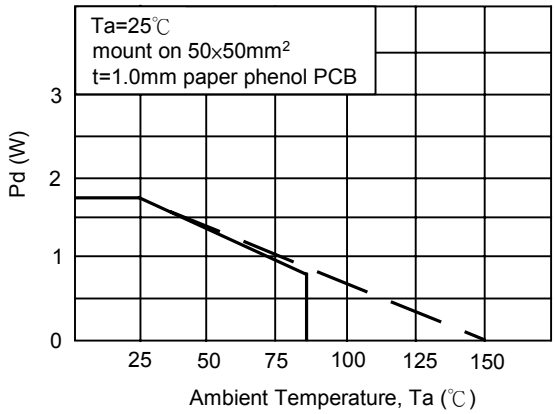
APPLICATION CIRCUIT



VCD PLAYER MOTOR DRIVER CIRCUIT



POWER DISSIPATION



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