Edge7725

900 MHz Dual Pin Electronics Driver, Window Comparator, and Load

SEMTECH

TEST AND MEASUREMENT PRODUCTS

Description

The Edge7725 dual channel, monolithic ATE pin electronics solution is manufactured in a high-performance complementary bipolar process.

The Edge7725 operates greater than 900 MHz/1.8 Gbps. The power supplies to the Edge7725 are specified over a wide range to accommodate between –2V, +7V and –0.5V, +4.2V input, output voltages.

The three-statable Edge7725 tri-level driver is capable of generating 8V swings over a –2 to +7V range, with a minimum swing of 100 mV. The driver's third level is used when the driver acts as a switched termination, and the load is not being used. The differential driver mode permits the inverse of DHI driving of Channel 0 to be output on Channel 1, creating differential outputs having a minimum of skew. An input power down mode lowers the DOUT leakage current.

The Edge7725 window comparator can span a 9V common mode range. Programmable voltage clamps at the input to the comparator provide a means to clamp voltage overshoots and excessive ringing for unterminated comparator input signals. An input power down mode lowers the VINP input leakage currents.

The Edge7725 differential comparator can compare input differences of up to 800mV to input levels which are separate from those of the window comparators.

The Edge7725 load supports programmable source and sink currents of ±32 mA over a –2V to +7V range, or it can be completely disabled. The load may be configured as a "split load" whereby the load can act as a voltage clamp as an alternate to the comparator's clamp. For operating modes requiring no load, the Edge7725's load may be depowered to conserve power.

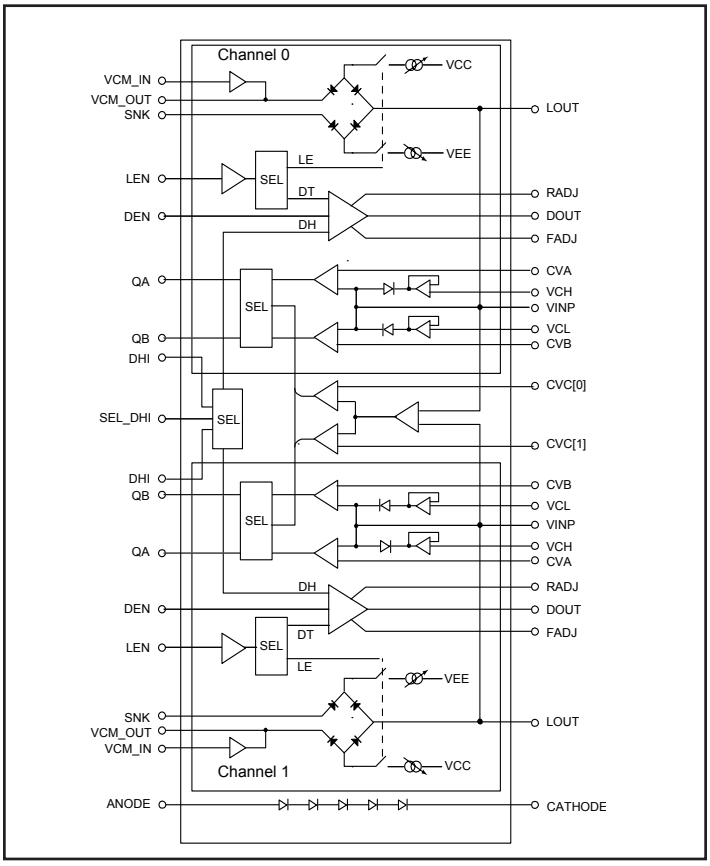
Features

- Fully Integrated Three-Statable, Tri-Level Driver, Window Comparator, and Dynamic Active Load
- Wide Choice of Range, Performance vs. Power
- Differential Driver and Comparator Modes
- Programmable Driver Rise, Fall Times
- Programmable Voltage Clamps on Comparator Input
- –2V, +7V Driver, Compare, Load Range
- ±32 mA Programmable Load
- Comparator Input Tracking to >3V/ns
- Small, 128-Pin MQFP Package

Applications

- Logic Testers
- Mixed-Signal Test Equipment
- Memory Testers
- Flash Memory Testers
- ASIC Verifiers

Functional Block Diagram



PIN Description

[0:1] Refers to Channels 0 or 1

Pin #	Pin Name	Description
Control		
17, 22	CONFA[0:1]	TTL inputs to configure the mode of the channel.
16, 23	CONFB[0:1]	TTL inputs to configure the mode of the channel.
21	SEL_DHI	TTL input that selects the Differential Drive Mode when a logical high.
18	SEL_CMP	TTL input that selects window comparators or differential comparator. Differential comparator is selected when SEL_CMP is a logical high.
Driver		
105, 106; 61, 62	DOUT[0:1]	Driver output.
89, 78 90, 77	DHI[0:1] DHI*[0:1]	Flex differential input digital pins which select the driver high or low
91, 76 92, 75	DEN[0:1] DEN*[0:1]	Flex differential input pins which control the driver being active or in a high impedance state.
98, 69 96, 71 94, 73	DVH[0:1] DVL[0:1] DVT[0:1]	High impedance analog voltage inputs which determine the driver high, low, and termination levels.
103, 64 102, 65	RADJ[0:1] FADJ[0:1]	Input currents which determine the driver transition, rise and fall times.
86, 81	DBIAS[0:1]	Analog current input that sets an internal bias current for the driver.
Comparator		
128, 39	VINP[0:1]	Analog voltage input to the positive input of the A and B comparators.
3, 36 2, 37 1, 38	CVA[0:1] CVB[0:1] CVC[0:1]	Analog inputs which set the A, B, and C comparator thresholds.
10, 29 11, 28	VCH[0:1] VCL[0:1]	Voltage clamp high and low inputs.
122, 45 121, 46 123, 44 124, 43	QA[0:1] QA*[0:1] QB[0:1] QB*[0:1]	Differential digital outputs of comparators A and B.
7, 32	CBIAS[0:1]	Analog current input that sets an internal bias current for the comparator.
120, 47	CVC_GND[0:1]	Ground sense line for the differential comparator circuit. Connect to ground reference for the CVC[0:1] voltage level generating circuit.

PIN Description *(continued)*

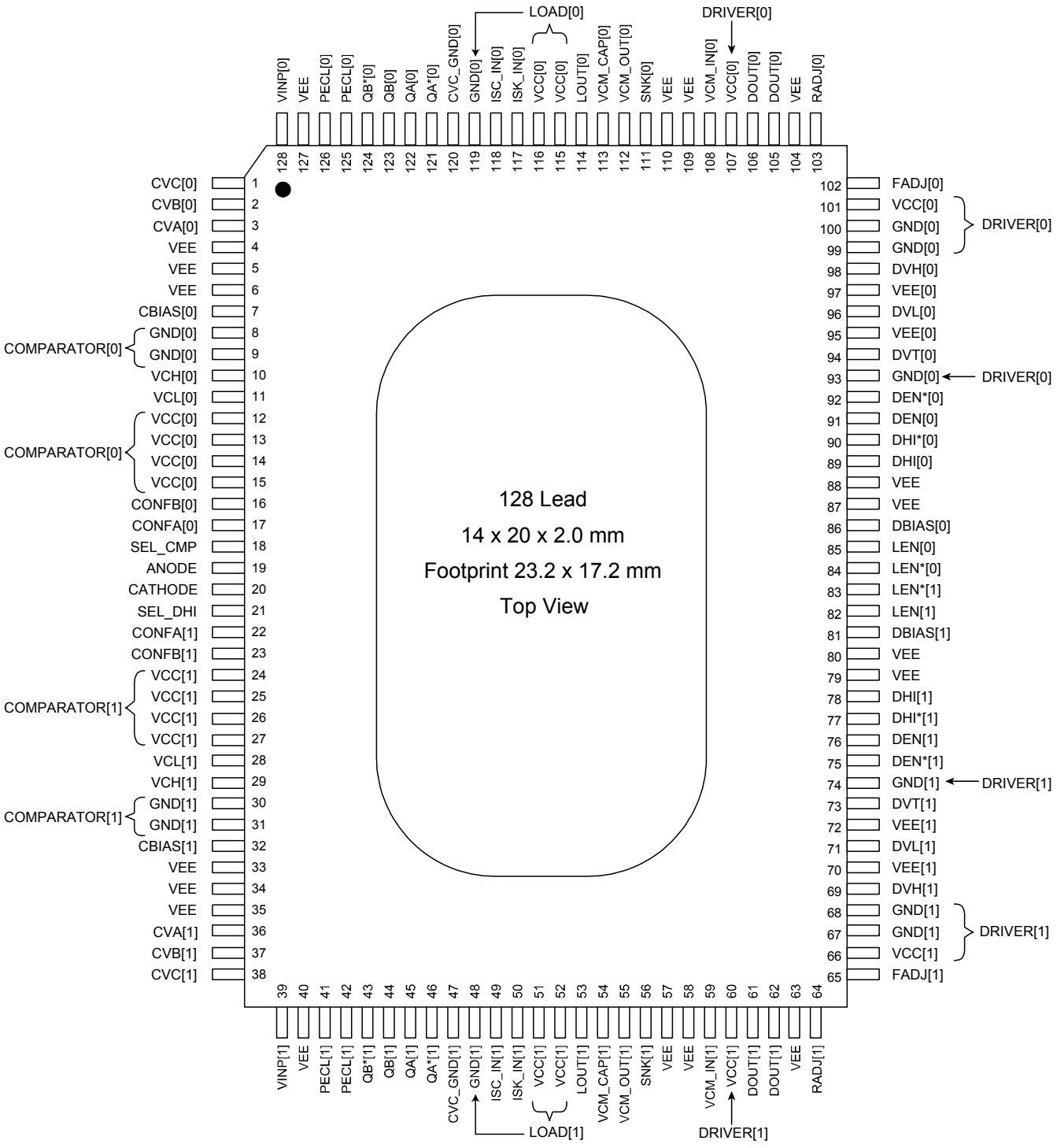
[0:1] Refers to Channels 0 or 1

Pin #	Pin Name	Description
Load		
114, 53	LOUT[0:1]	Load Output
85, 82 84, 83	LEN[0:1] LEN*[0:1]	Flex differential inputs which activate and disable the load or driver tri-level.
118, 49 117, 50	ISC_IN[0:1] ISK_IN[0:1]	Analog current inputs which program the load source and sink currents. Should be connected to external voltage or current source through minimum 500Ω (min.) series resistors.
108, 59	VCM_IN[0:1]	High impedance analog voltage inputs that program the commutating voltage.
112, 55	VCM_OUT[0:1}	Commutating voltage buffer output.
113, 54	VCM_CAP[0:1]	Commutating buffer op amp compensation pins (10 nanofarad, high frequency).
111, 56	SNK[0:1]	Sink input current to load.
Power Supplies		
12, 13, 14, 15, 101, 107, 115, 116, 24, 25, 26, 27, 51, 52, 66, 60	VCC[0:1]	Positive power supply. See pin diagram for notations of which pins supply power for which circuit functions.
4, 5, 6, 33, 34, 35, 40, 57, 58, 63, 70, 72, 79, 80, 87, 88, 95, 97, 104, 109, 110, 127	VEE	Negative power supply. Common for all circuit functions. Internally connected together. NOTE: Exposed heat slug is connected to VEE.
126, 125, 42, 41	PECL[0:1]	Positive power supply to the comparators.
8, 9, 93, 99, 100; 119, 74, 30, 31, 48, 67, 68	GND[0:1]	Device ground. See pin diagram for notations of which pins supply ground for which circuit functions.
Miscellaneous		
19, 20	ANODE, CATHODE	Terminals of the on-chip thermal diode string.

Note 1: All VEEs must be connected, externally, to the same supply.
All VCCs must be connected, externally, to the same supply.
All PECLs must be connected, externally, to the same supply.
All GNDs must be connected, externally.

PIN Description (continued)

128 Lead MQFP Package
with Exposed Heat Slug (Top)



Circuit Description

Introduction

Figure 1 shows a detailed block diagram of the Edge7725.

Table 1 shows the modes of the Edge7725 as configured by the TTL inputs, CONFA and CONFB. These "configuration" inputs will put the channel's driver, comparator, and load circuits into specific operating modes and power down states.

The configuration inputs are asynchronous and, therefore, when they are switching from one state to another, there could be decoding glitches. The user should be aware of this and keep the skew among the three inputs to a minimum to minimize any unwanted conditions at the driver and load outputs. It is also recommended that the driver and load outputs be disabled when changing modes.

NOTE: Do not leave the CONF inputs floating. They should be forced to valid high or low logic levels at all times.

	Mode	Conf Mode Inputs		Internally Powered Down	Driver, Load Control			Function States				
		B	A		DHI	DEN	LEN	DOUT	LOAD	COMP	CLAMPS	Comments
All Off	**0**	**0**	**0**	Driver, Load, Comp, Clamp	X	X	X	Off	Off	Off	Off	Powered Down, Low Leakage Mode
Drive/ Receive Pin	**1**	**0**	**1**	None	0	1	0	DVL	Off	On	On	Driver, Comparator, and Load Enabled (no Driver Tri-Level) (Clamps On)
					1	1	0	DVH				
					X	0	0	HiZ				
					0	1	1	DVL	On			
					1	1	1	DVH				
					X	0	1	HiZ				
Drive/ Receive Pin with DVT	**2**	**1**	**0**	Load	0	1	0	DVL	Off	On	Off	Driver, Comparator Enabled. Driver Tri-Level Clamps Off (No Load)
					1	1	0	DVH				
					X	1	1	DVT				
					X	0	X	HiZ				
Drive Pin	**3**	**1**	**1**	Load, Comp, Clamp	0	1	X	DVL	Off	Off	Off	Driver Enabled, (No Load, Comparator, or Driver Tri-Level). (Clamps Off)
					1	1	X	DVH				
					X	0	X	HiZ				

KEY:
- X (Don't Care)
- DVH (Drive High)
- DVL (Drive Low)
- DVT (Drive third, termination level)
- HiZ (High Impedance)

NOTE: The entire table above is valid for SEL_CMP and SEL_DHI in any high or low state.

Table 1: Edge7725 Modes of Operation

Circuit Description *(continued)*

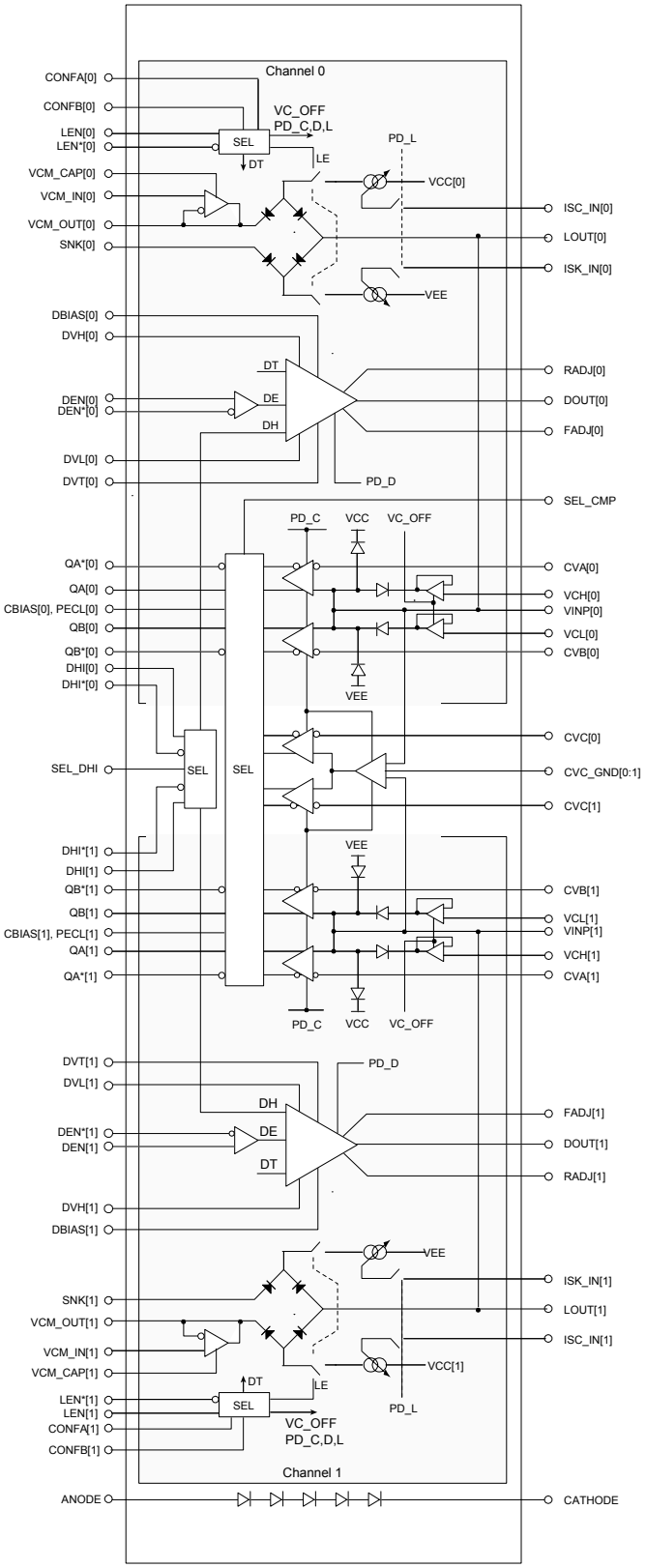


Figure 1. Edge7725 Detailed Block Diagram

Circuit Description *(continued)*

Driver

Both driver digital control inputs (DHI/DHI*, DEN/DEN*) are “Flex Inputs” – wide voltage differential inputs capable of receiving ECL, TTL, CMOS, or custom level signals. Single-ended operation is supported by connecting the inverting input to the appropriate DC threshold level. Differential input drive is recommended for highest performance.

Drive Enable

In the driver enabled mode (Table 1), the drive enable inputs (DEN / DEN*) control whether the driver is forcing a voltage, or is placed in a high-impedance state. If DEN is more positive than DEN*, the output will force either DVH, DVL, or DVT. If DEN is more negative than DEN*, the output goes into a high impedance state.

Do NOT leave DEN / DEN* floating.

Driver Data

When the driver is enabled (Table 1) the drive data inputs (DHI / DHI*) determine whether the driver output is forcing a high or a low. If DHI is more positive than DHI*, the driver will force DVH when the driver is active. If DHI is more negative than DHI*, the driver will force DVL when active.

Do NOT leave DHI / DHI* floating.

Driver Differential Mode Selection

The TTL input SEL_DHI selects the channel from which the DHI/DHI* signal is applied to each driver.

SEL_DHI	DH[0] from:	DH[1] from:
0	DHI/DHI*[0]	DHI/DHI*[1]
1	DHI/DHI*[0]	DHI*/DHI[0]

SEL_DHI = 1 is used for outputting a differential signal where DOUT[1] is the inverse of DOUT[0] with the minimum of skew, and both drivers respond to the DHI/DHI*[0] signal. The DEN/DEN* signals are still valid when the drivers are in the differential mode.

Driver Tri-Level

When the load is not being used (Table 1) and the driver is enabled, then (LEN/LEN*) will switch the driver to its third level, DVT, independent of DHI, whereupon the driver can act as a termination inclusive of an external series resistor (e.g. driver can act as a switched 50Ω termination).

Do NOT leave LEN / LEN* floating.

Driver Levels

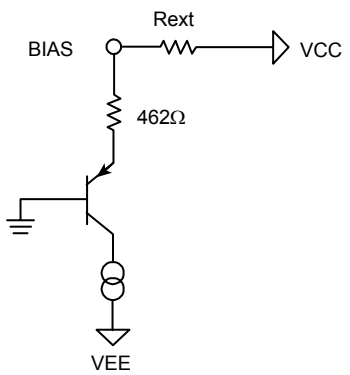
DVH, DVL, and DVT are high input impedance voltage inputs which establish the driver’s high, low, and third (termination) levels.

Bias Inputs

The DBIAS, CBIAS, RADJ and FADJ input pins are analog current inputs which establish on-chip bias currents. These currents, to some degree, also establish the overall power consumption and performance of the circuits. Ideally, an adjustable external current source would be used to fine-tune and minimize any part-to-part performance variation within a test system. However, a precision external resistor tied to a large positive voltage is typically acceptable. (See figure below.) The optimal settings are dependent on required system performance and power requirements.

The established bias currents have the typical circuit below and follow the equation:

$$BIAS = (VCC - 0.7) / (Rext + 462\Omega).$$



Circuit Description *(continued)*

Driver Power Down Modes

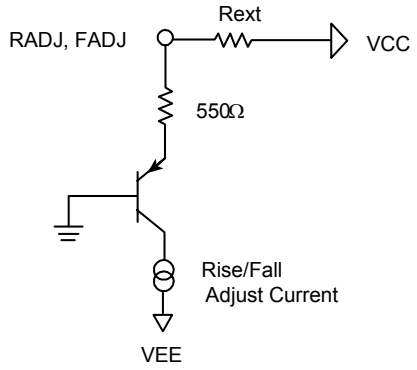
Referring to Table 1, Mode 0, “ALL_OFF” is a configuration in which the driver can be put into a power down mode (reducing power supply currents, power dissipation and output leakage currents), and others in which the driver is powered and ready for operation.

Driver Slew Rate Adjustment

The driver rising and falling transition times are independently adjustable. The RADJ and FADJ pins are analog current inputs which establish the driver rise and fall times.

Ideally, an adjustable external current source would be used for RADJ and FADJ. However, for applications where the rise and fall times are fixed, precision external resistors to a positive voltage can be used. The currents into RADJ and FADJ follow the equation:

RADJ, FADJ = (VCC - 0.7) / (Rext + 550Ω).

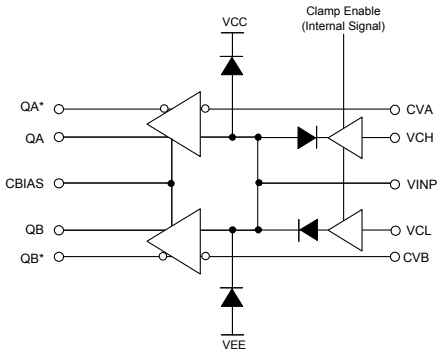


Circuit Description *(continued)*

Window Comparator

Two comparators are connected on-chip to form a window comparator to determine whether the DUT is high, low, or in an intermediate state. VINP is tied to the positive inputs of both comparators. The selection of either comparator A or B for the DUT high or the DUT low comparison is arbitrary.

The figure below shows the correct polarity for the comparator connections.



Comparator truth table, where CVA > CVB:

	QA	QB
VINP > CVA	H	H
CVB < VINP < CVA	L	H
VINP < CVB	L	L

Thresholds

CVA and CVB are the window comparator's two threshold levels. These inputs are high impedance voltage controlled inputs that determine at which VINP voltage the comparators will change output states.

CVC[0], CVC[1] are the two differential comparator's threshold levels. The window and differential comparators cannot be used at the same time because they share output pins QA, QA*, QB, QB*. Since they are not used at the same time, the compare voltages can be shared between the window and differential comparators to save in reference level DACs and power. CVC[0] may be connected to CVA[0] or CVB[0], and the same is true for CVC[1], CVA[1] and CVB[1].

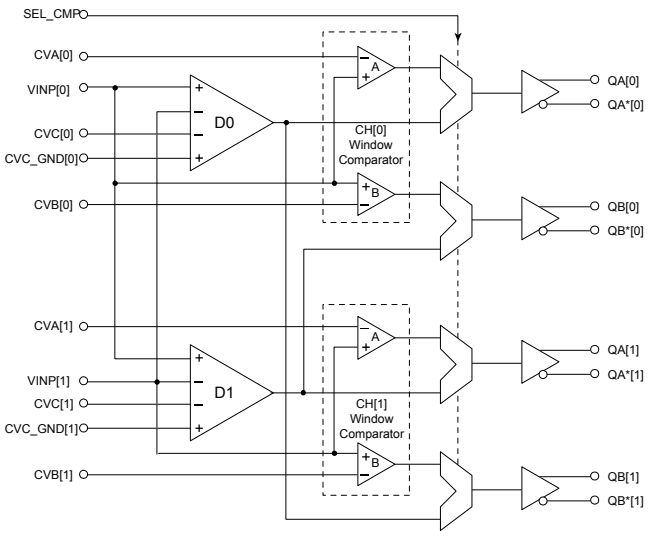
The QA, QA*, QB, QB* output voltages are relative to the PECL supply voltage input. The DC Specifications section will specify the differential output voltage swings and common mode voltages to expect.

Differential Amplifier and Comparator

VINP[0], VINP[1] are also input to a differential amplifier. The differential amplifier output (VINP[0] minus VINP[1]) is then compared against CVC[0] and CVC[1] inputs over a ±800mV range, where

$$0.1V < |VINP[0] - VINP[1]| < 0.8V$$

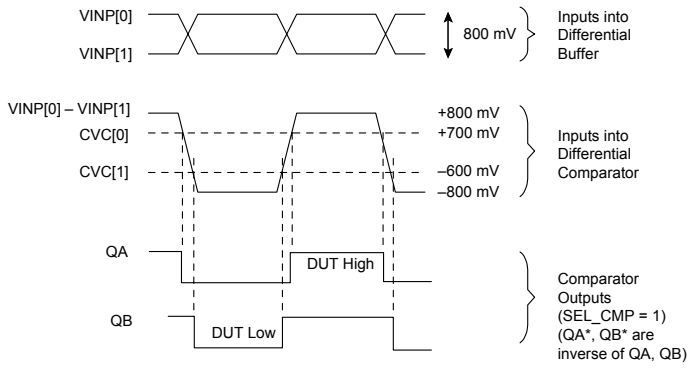
The figure below is a functional diagram of the window and differential comparators.



The difference amplifiers will subtract the voltage at VINP[1] from VINP[0] and the result is presented to a comparator that compares this result against an input voltage CVC[0] or CVC[1]. These input voltages may well be referenced to a different ground than analog ground at the E7725. They more than likely will be referenced to a buffered version of the DUT ground. In order for the difference amplifiers to operate correctly each of the them has a ground reference input, CVC_GND[0:1]. This high impedance input should be connected to the ground reference point of the level DAC that is generating the CVC[0] and the CVC[1] voltages respectively. The voltages at CVC_GND[0:1] can be +/-0.25V from analog ground at the E7725.

Circuit Description *(continued)*

Differential Comparison Example



Comparator Selection

The TTL input SEL_CMP selects the comparators for output on QA, QB[0] and QA, QB[1]. SEL_CMP in a low state is the normal window comparator mode. The outputs of the window comparators A & B for each channel are output to their respective Q and Q* outputs. SEL_CMP in the high state enables the differential comparator mode. The outputs of the differential comparators are fed to the Q and Q* outputs for both channel 0 and 1. NOTE: Refer to the preceding functional diagram. The D0 and D1 differential comparators will output to QA[0] and QB[0], respectively, but they output to QB[1] and QA[1], respectively, also. Either pair of outputs may be used. The table below further clarifies this.

	Comparator Output Mapping			
SEL_CMP	QA[0]	QB[0]	QA[1]	QB[1]
0	CVA[0] Window Comparator	CVB[0] Window Comparator	CVA[1] Window Comparator	CVB[1] Window Comparator
1	CVC[0] Differential Comparator	CVC[1] Differential Comparator	CVC[1] Differential Comparator	CVC[0] Differential Comparator

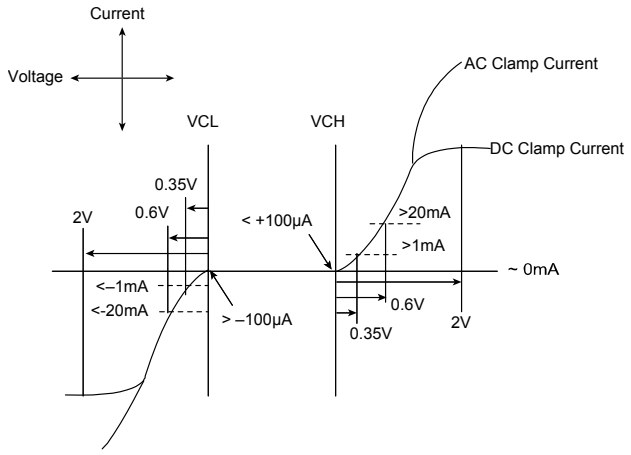
Waveform Clamps

VCH and VCL provide for programmable voltage clamps to the comparator input, VINP.

These clamps are used when a device being tested is not designed to drive a 50Ω transmission line load. In such a case, the signal from the test device can be amplified to almost double the original voltage if the output impedance of the test device is very low, and the 50Ω transmission line between the device and the E7725 is not terminated. This signal can then be reflected back to the test device, potentially stressing or damaging the device. Subsequent reflections can also cause false triggers in the timing circuitry that receive the comparator outputs. So, the clamps limit the minimum and maximum amplitude of the signal when it reaches the comparator input.

Under transient conditions, these clamps will source or sink relatively large amounts of current as needed to limit the voltage. Under DC conditions (after ~100 ns), however, the maximum current is limited to a lower current. This is done to limit the amount of power dissipation under fault conditions. For instance, if the VCH voltage is set to 3V when the part being tested puts out 5V. See the figure below for clamp current vs. input voltage curves.

The “clamps off” mode (Table 1) causes the internal clamp levels to be set outside the operating range, independent of VCH or VCL inputs. Clamp characteristic:



Refering to Table 1, where the clamps are in the ON condition, it is still possible to turn the clamps off by setting the VCL voltage level above the VCH level. By reversing the operating polarity, the clamps will turn off. The VCH and VCL levels should still remain in their recommended operating ranges.

Comparator Input Protection

VINP is also connected to protection diodes to VCC and VEE as shown on the previous page. These diodes can handle up to 100 mA.

Circuit Description *(continued)*

Comparator Power Down Modes

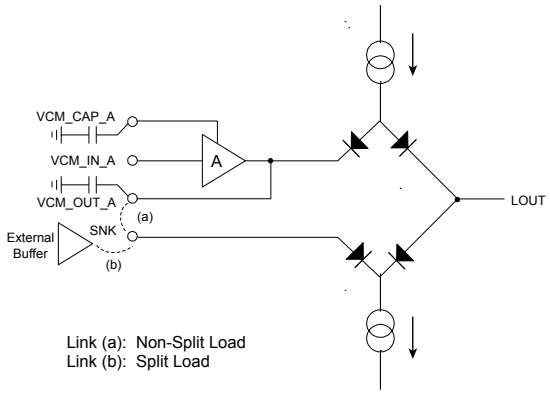
Referring to Table 1, the comparators can be placed in a power down mode in certain configurations. Other configurations have the comparators powered and ready for operation.

When the comparator sections are put into one of the power down modes, the QA, QA*, QB, QB* outputs are placed in a fixed differential logic state. The state could be a logic "0" or "1" depending upon internal levels at the time the circuit enters the power down mode. The outputs will not respond to changes at the VINP pins when in power down modes.

Minimum leakage occurs when CVA, CVB > VINP.

Load

The load is configurable as a split or non-split load:



The load is capable of sourcing and sinking at least 32 mA dynamically, or being placed into a high impedance state.

Load Enable

LEN/LEN* are "Flex In" – wide voltage differential inputs capable of receiving ECL, TTL, CMOS, or custom levels. Single-ended operation is supported by connecting the inverting input to the appropriate DC threshold level.

When the load is powered on (Table 1), the load enable differential inputs determine whether the load is active or in high impedance. If LEN is more positive than LEN*, the load is active and is capable of sourcing and sinking currents. If LEN is more negative than LEN*, the load is placed into a high impedance state (disabled).

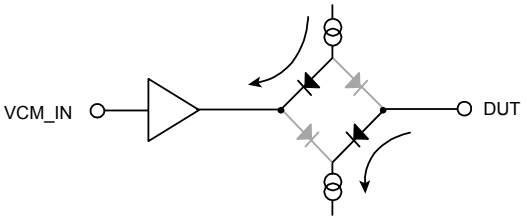
Do NOT leave LEN / LEN* floating.

Circuit Description *(continued)*

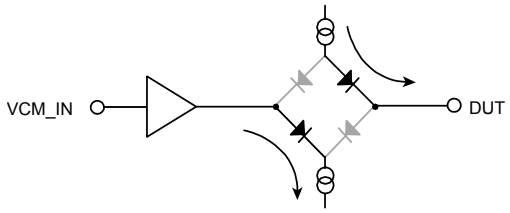
Load Commutating Voltage

The load has one commutating voltage input, or two if used as a “split load”. The following describes the “non-split” load operation. The “split load” operation is similar.

VCM_IN is a high input impedance analog voltage input which sets the commutating voltage of the load. If DUT is more positive than VCM_IN, the bridge will sink current from the DUT into the load. If DUT is more negative than VCM_IN, the load will source current from the load into the DUT.



Load Sinking Current: DUT > VCM_IN



Loading Sourcing Current: DUT < VCM_IN

Load Source and Sink Current Levels

The amount of current that the diode bridge can source and sink is adjustable from 0 mA to 32 mA. The source and sink levels are separate and independent.

ISC_IN and ISK_IN are current controlled inputs whose voltage level is held very close to ground (<100 mV variation) over the entire legal current input range.

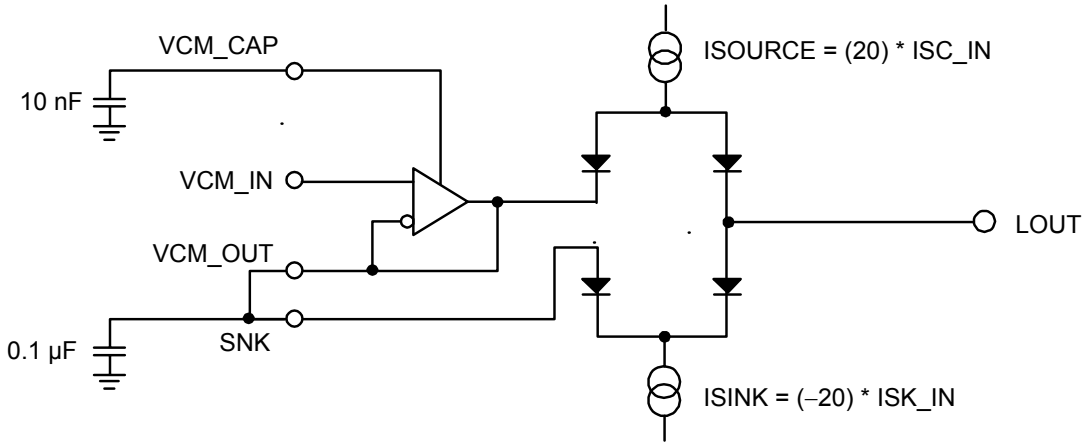
There is a nominal gain of 20 between the ISC_IN current and the bridge source current.

$$ISOURCE = 20 * ISC_IN$$

There is a nominal gain of –20 between the ISK_IN current and the bridge sink current.

$$ISINK = -20 * ISK_IN$$

To avoid instabilities in the circuit, care should be given to avoid capacitive coupling of the ISC_IN and ISK_IN inputs to the LOUT output.



Load Commutating Voltage

Circuit Description *(continued)*

Load Commutating Voltage Compensation

The VCM_CAP pin is an op amp compensation node that requires a fixed 10 nanofarad chip capacitor (with good high frequency characteristics) to ground. This capacitor is used to compensate an internal node on the on-chip buffer for the commutating voltage input.

The VCM_OUT is the actual commutating voltage generated by the on-chip buffer. VCM_OUT is also connected to the diode bridge. A capacitor of 0.1 µF to ground is also needed on the VCM_OUT pin for high speed switching of the load currents.

Load Power Down Mode

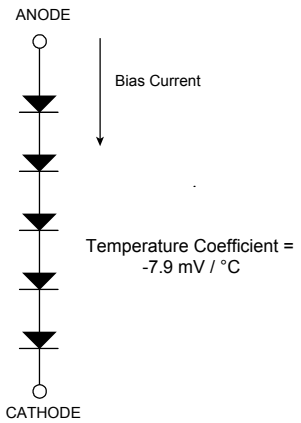
Referring to Table 1, the load circuit can be placed in the power down state in certain configurations which reduces overall power consumption. In other configurations, the load remains powered and ready for operation.

Thermal Monitor

An on-chip thermal diode string of five diodes in series exists (see figure below). This string allows accurate die temperature measurements.

An external bias current of 100 µA is injected through the string, and the measured voltage corresponds to a specific junction temperature with the following equation:

$$Tj[°C]=\{(ANODE - CATHODE) / 5 - 0.768\} / (-0.00169).$$



Power Supply Sequencing

In order to avoid the possibility of latch-up, the following power-up requirements must be satisfied:

1. VEE < GND < VCC at all times
2. VEE < Analog Inputs < VCC
3. VEE < Digital Iputs < input max voltage or VCC, whichever is less

The following sequencing can be used as a guideline when powering up the Edge7725:

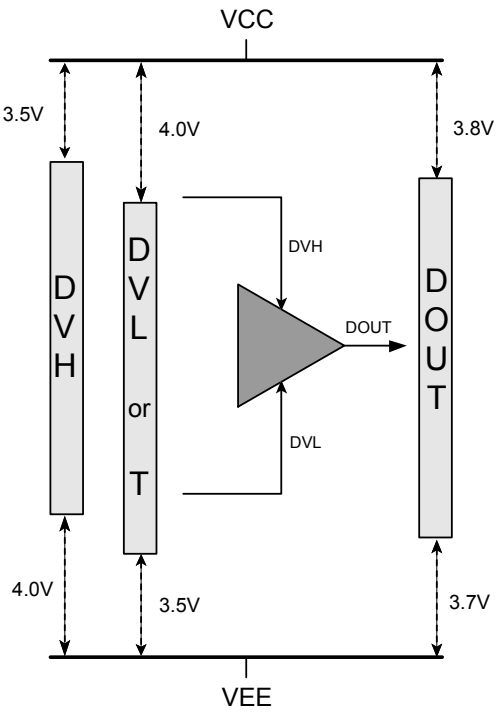
1. VEE
2. VCC
3. Digital Inputs
4. Analog Inputs

The recommended power-down sequence is the reverse order of the power-up sequence.

Computing the Driver Output Voltage Range

The output voltage range of the driver at the DOUT pin is defined by two fundamental calculations. First is the relationship to the power supply voltages at the device (VCC and VEE) and second to the range of programmability of the DVH, DVL and DVT input voltages. Remaining in the calculated output voltage range is required to maintain all the DC and AC accuracy specifications for the driver function.

The DOUT range relative to the power supply voltages is straightforward and depicted in the following figure at the output of the driver. The required DOUT range must comply with the noted headrooms to the VCC and VEE power supplies. Headrooms larger than noted are also acceptable but must remain within the power supply recommended operating ranges.



The DOUT range is also dependant on the allowable programming voltages at the DVH, DVL and DVT inputs. Each of these inputs have similar requirements for power supply headrooms as DOUT does. These headrooms are also depicted in the above figure. Furthermore, the DVH/L/T inputs will have voltage offsets and gain error specifications. These specifications require that the DVH/L/T input programming range be greater than the required DOUT voltage range if the worst case offset and gain figures are used. The equation for the resulting minimum and maximum voltage at DOUT is;

$$V_{DOUT(MIN/MAX)} = V_{OFFSET(MIN/MAX)} + [\ V_{IN} * GAIN_{(MIN)}\ ]$$

Solving for VIN;

$$V_{IN} = [\ V_{DOUT(MIN/MAX)} = V_{OFFSET(MIN/MAX)}\ ] / GAIN_{(MIN)}$$

To solve for the range of V_{IN}, first select the Vout ranges required. For example, if we choose -2.0V for the minimum end and +6.5V for the maximum end of V_{DOUT}, and an offset min/max of -100mV/+100mV and a minimum gain of 0.975 the equations solve as;

For -2.0V;

$$V_{IN(-2V)} = [\ -2.0V - 100mV\ ] / 0.975 = -2.154V$$

For +6.5V;

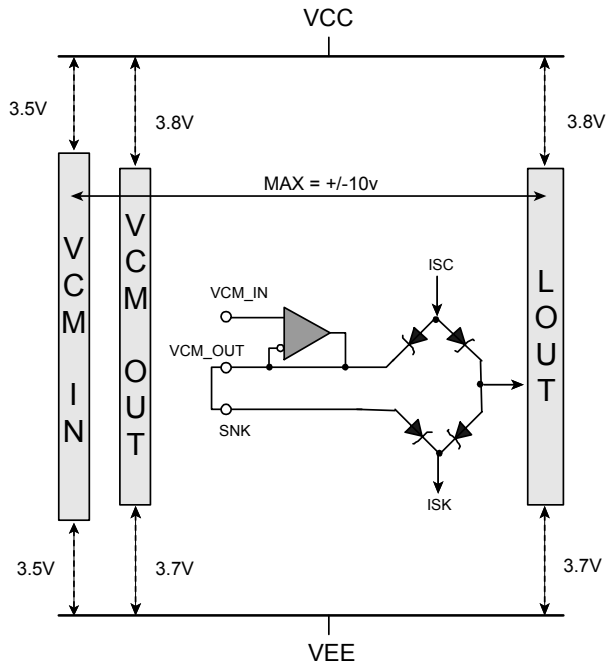
$$V_{IN(+6.5V)} = [\ +6.5V + 100mV\ ] / 0.975 = +6.769V$$

These resulting V_{IN} values then need to meet the headroom requirements previously mentioned as well as the absolute (relative to ground) voltage limitations specified in the DC specifications data.

Computing the Load Commutating Voltage Range

The load circuit also has power supply headroom requirements similar to the driver circuit mentioned previously in order for the load circuit to maintain its DC accuracy specifications. The figure below shows the necessary headrooms for LOUT, VCM_IN and VCM_OUT. There is an additional voltage restriction between VCM_IN (and therefore VCM_OUT) and a voltage being impressed on LOUT. This maximum is 10.0V of either polarity.

Application Information *(continued)*



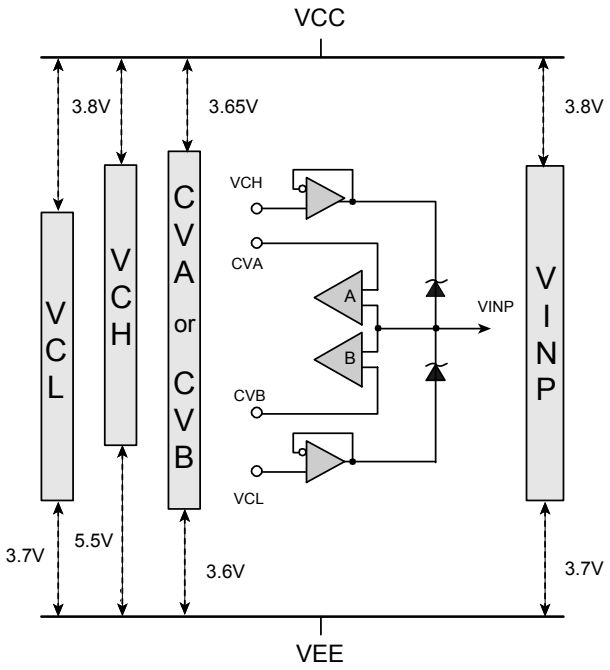
The LOUT restriction of headroom to the power supplies is identical to the restriction placed on the VCM_OUT pin. Because there is a possible offset from VCM_IN to VCM_OUT the headroom restriction for the VCM_IN input is lower. This allows the VCM_IN pin to be adjusted higher to account for the worst case offset of the buffer amplifier.

LOUT and VCM_IN inputs also have with them restrictions on absolute (relative to ground) voltage limitations. Refer to the DC specifications data for these values.

Computing the Comparator and Clamp Input Voltage Ranges

The window comparator and clamp circuitry are have headroom requirements also. The next figure depicts the requirements. Because the offsets and hysteresis of the comparators are so low (as compared to some driver and load offsets) there is no need to allow for special considerations in the restrictions. Once the user chooses the VINP operating range, the CVA, CVB, VCL and VCH operating areas will follow naturally with no special consideration for offsets needed.

Refer to the DC specifications data to insure that the absolute (relative to ground) voltage restrictions are not violated.



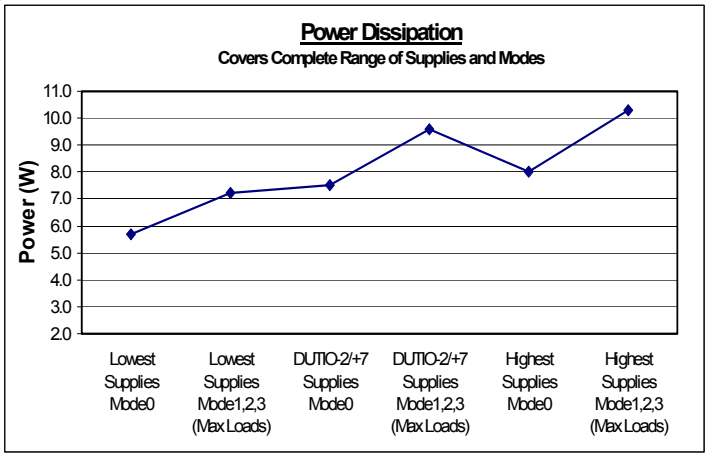
Input Levels

From Table 1, the load function is only operable when the driver tri-level is off (not used). Hence, input levels to these may be shared. For example, DVT may be connected to VCM-IN.

Application Information *(continued)*

Computing Maximum Power Consumption

The diagram below shows the power consumption of the Edge7725 as a function of power supply and performance bias settings.



The power consumption goes up as the power supplies are raised in voltage, modes are changed, and load circuits are programmed. Refer to the Specifications Section for choosing the power supply settings for a particular system voltage range. This section deals with how to heatsink the various power dissipation levels.

Cooling Considerations

Depending on the applied power supply levels and bias conditions the Edge7725 will use, various methods of heatsinking will be required to keep the maximum die junction termperature within a safe range and below the specified maximum of 100°C.

The Edge7725 package has an integral heat slug located at the top side of the package to efficiently conduct heat away from the die to the package top. The thermal resistance of the package to the top is the θ_{JC} (junction-to-case) and is specified at 0.53°C/Watt.

In order to calculate what type of heatsinking should be applied to the Edge7725, the designer needs to determine the worst case power dissipation of the device in the application. The graph above gives a good visual relationship of the range of power dissipation that can be expected from the E7725. The range of power covers the different modes of operation, power supply settings, and performance bias adjustments available. Use the data and graphs in subsequent sections to determine a particular applications power dissipation.

Another variable that needs to be determined is the maximum ambient air temperature that will be surrounding or blowing on the device and/or the heatsink system in the application (assuming an air cooled system). A heatsinking solution should be chosen to be at or below a certain thermal impedance known as R_θ in units of °C/Watt. The heatsinking system is a combination of factors including the actual heatsink chosen and the selection of the interface material between the Edge7725 and the heatsink itself. This could be thermal grease or thermal epoxy, and they also have their own thermal impedances. The heatsinking solution will also depend on the volume of air passing over the heatsink and at what angle the air is impacting the heatsink. There are many options available in selecting a heatsinking system. The formula below shows how to calculate the required maximum thermal impedance for the entire heatsink system. Once this is known, the designer can evaluate the options that best fit the system design and meet the required R_θ.

$R_\theta(\text{heatsink_system}) = (T_{Jmax} - T_{ambient} - P * \theta_{JC}) / P$

where, R_θ (heatsink_system) is the thermal resistance of the entire heatsink system

T_{Jmax} is the maximum die temperature (100°C)

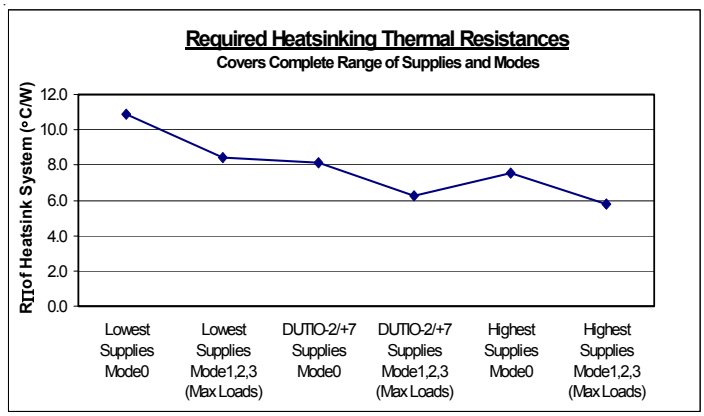
$T_{ambient}$ is the maximum ambient air temp expected at the heatsink (°C)

P is the maximum expected power dissipation of the Edge7725 (Watts)

θ_{JC} is the thermal impedance of the Edge7725 junction to case (0.53°C/W)

The following graph uses the power estimates from the previous graph and indicates the required maximum thermal impedances required for the heatsinking system using the above formula with $T_{ambient}$ at 35°C.

Application Information *(continued)*



More information on heatsink system selections can be read on heatsink vendors' web sites and in the Semtech Application Note #ATE-A2 *Cooling High Power, High Density Pin Electronics*.

Protection Considerations

The Edge7725 has ESD protection on its inputs and outputs as well as programmable clamps on its comparator's inputs.

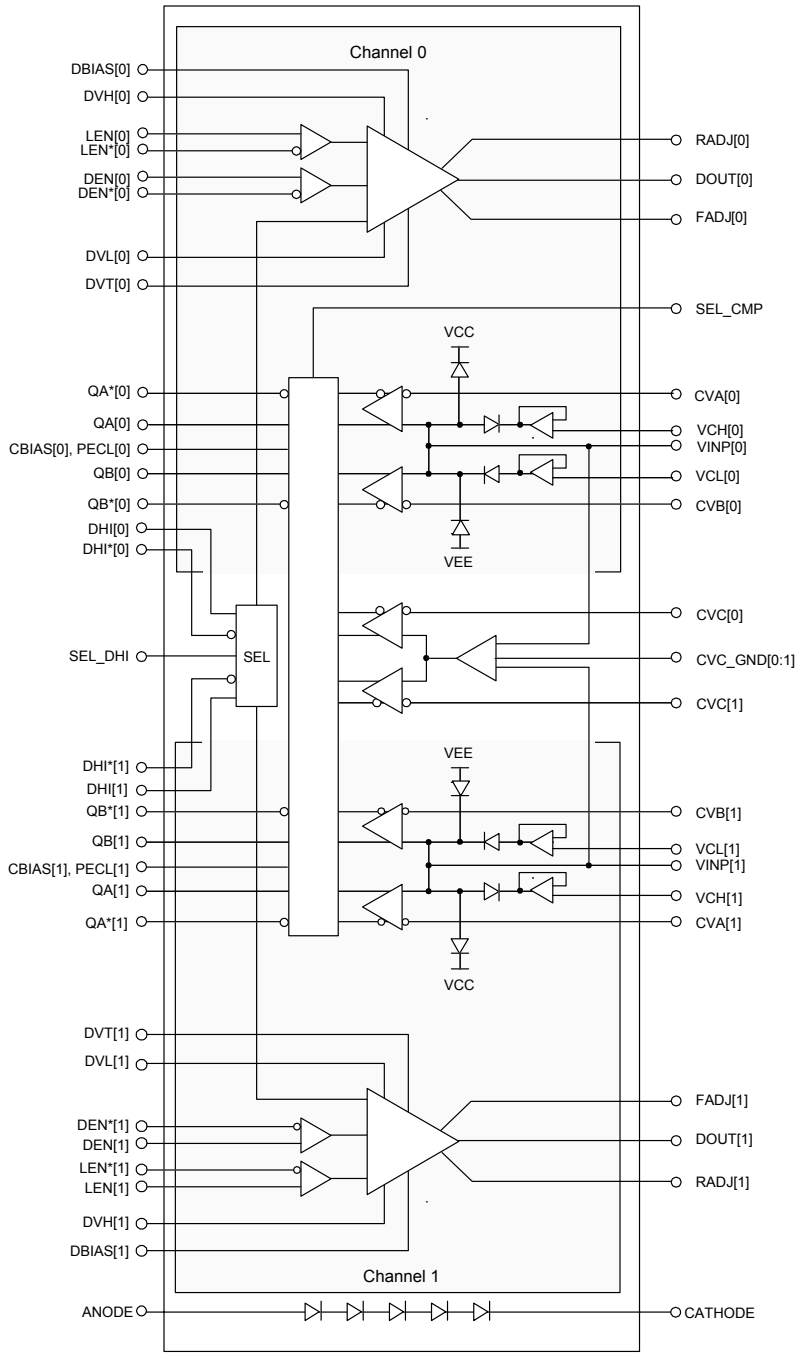
The appropriate circuit (e.g. parallel R and C) may need to be added to the comparator inputs and load outputs to protect against more stressful conditions; for example, a short to a high voltage power supply.

Application Information *(continued)*

Edge7725 as a Dual Driver with Dual Comparators

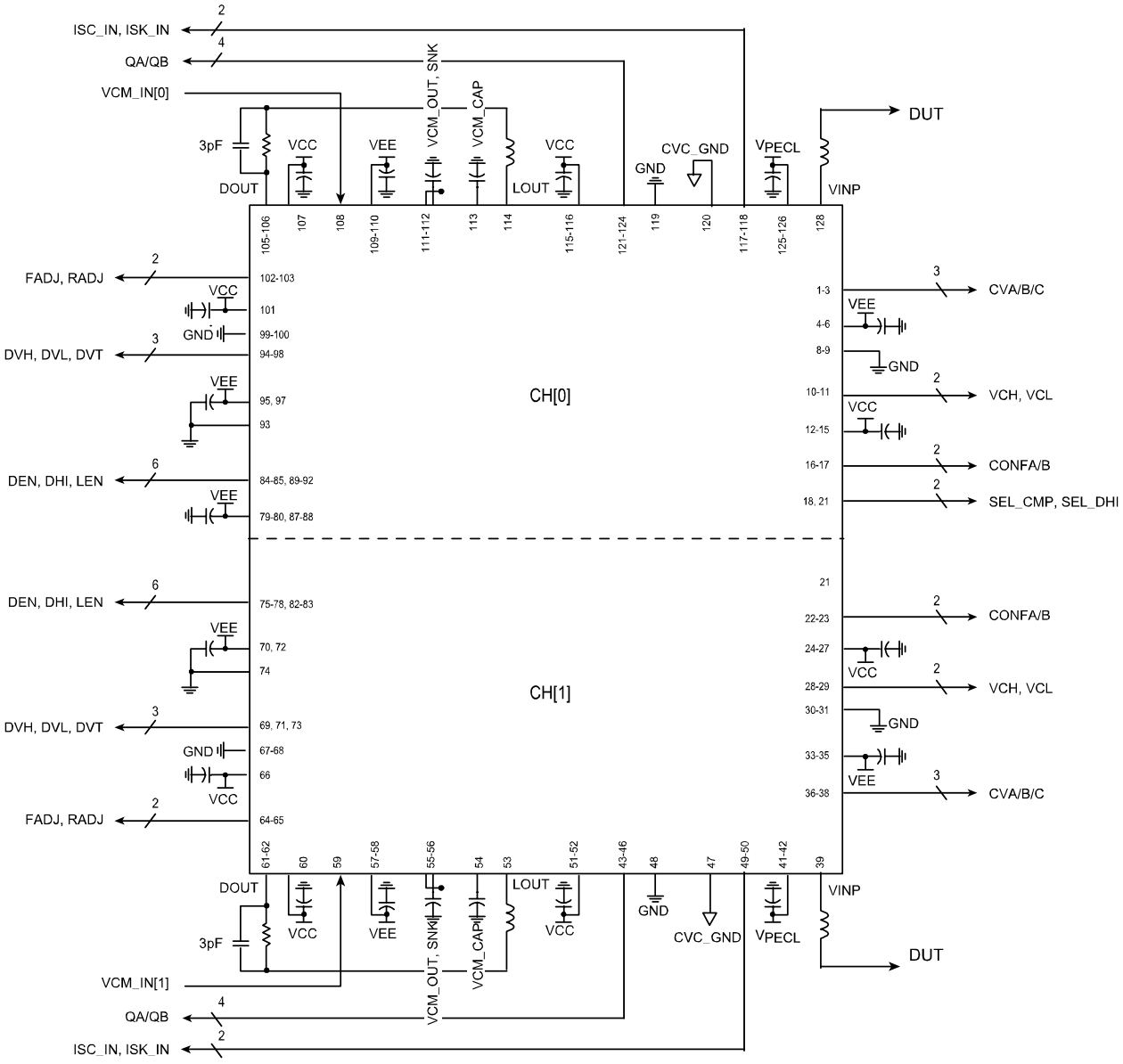
With the load powered down (see Table 1), the load consumes minimum power, and the Edge7725 acts as a Dual Driver with Dual Comparators as shown below.

If the loads are never to be used in a certain circuit, their VCM_IN inputs should be connected to GND, and other inputs and outputs can be open-circuit. No capacitors are required on VCM_CAP or VCM_OUT. With Driver tri-level enabled (Table 1), then the LEN/LEN* inputs to each channel provide tri-level switching.



Application Information *(continued)*

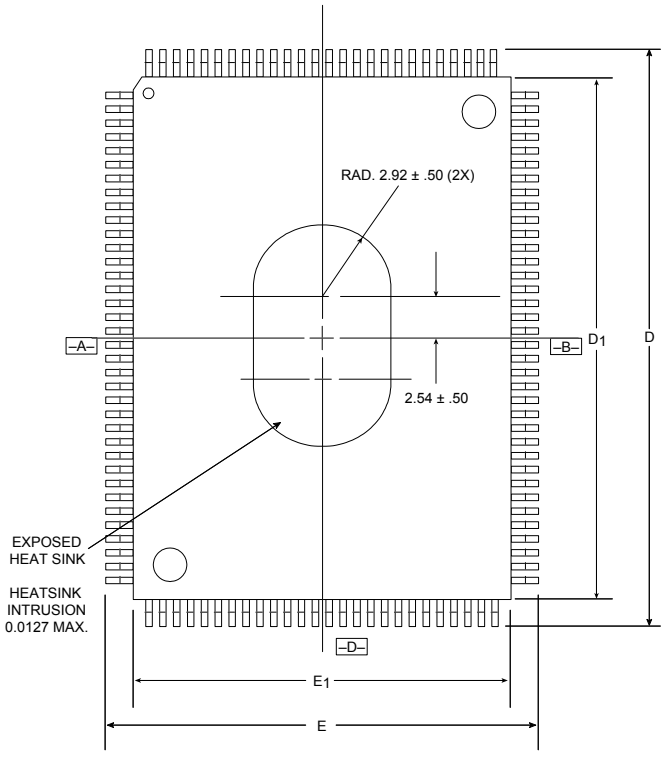
E7725 Hookup



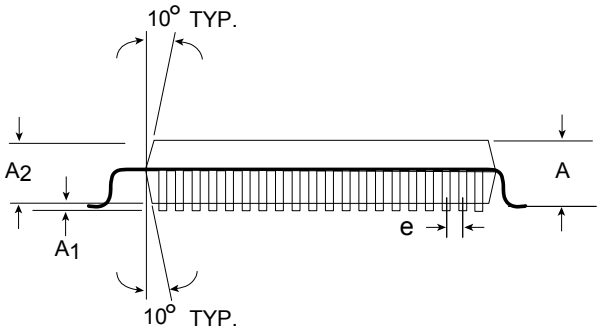
VEEs of both channels must be connected together; same for VCC, PECL and GND.
NOTE: All capacitors are 0.1µF unless otherwise noted.

Package Information

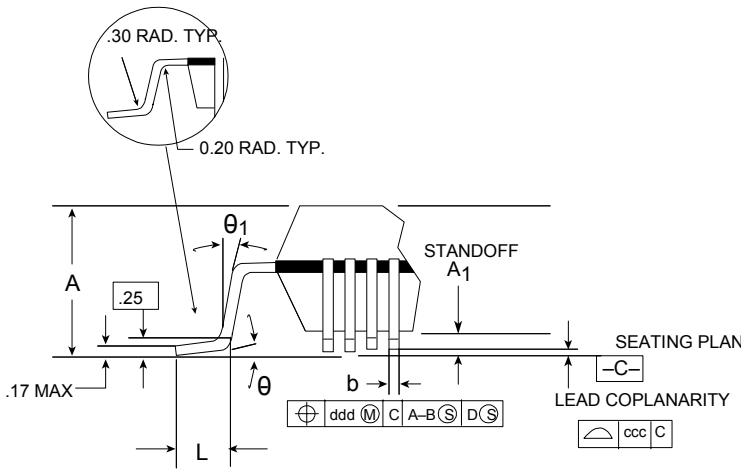
14 x 20 x 2.0 mm, 128-Pin MQFP Package
(with Exposed Metal Heat Slug on Top)



Top View



DIMS.	TOL.	
A	MAX	2.35
A_1	MIN / MAX	0.00 / 0.25
A_2	±.10	2.00
D	±.20	23.20
D_1	±.10	20.00
E	±.20	17.20
E_1	±.10	14.00
L	±.15	.88
e	BASIC	.50
b		0.19 min / 0.27 max
θ		0° - 7°
θ_1	±4°	6°
ddd	MAX	.08
ccc	MAX	.08



NOTES:
1) All dimensions in mm.
2) Dimensions shown are nominal with tol. as indicated.
3) L/F: EFTEC 64T copper or equivalent, 0.127 mm (.005”) or 0.15 mm (.006”) THICK.
4) Foot length “L” is measured at gage plane at 0.25 above the seating plane.
5) Lead finish 85/15 Sn/Pb.

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
VCC (relative to GND)	VCC	0	+11.75	V
VEE (relative to GND)	VEE	-6.5	0	V
Total Power Supply	VCC – VEE		+18.25	V
Comparator Supply	PECL	-1.0	+5.5	V
Digital Input Voltages	DHI(*), DEN(*), LEN(*)	VEE	VCC	V
Digital Differential Input Voltages	DHI(*), DEN(*), LEN(*)	-2.5	+2.5	V
Digital TTL Inputs	CONFA, CONFB	-2.5	VCC	V
Input Voltages Voltage Inputs	VINP, CVA, CVB, CVC, DVH DVL, DVT, VCM_IN, VCH, VCL	VEE	VCC	V
Load Voltages	(VCC–VCM_IN), (VCM_IN–VEE), (VCC–LOUT), (LOUT–VEE)	0	14.5	V
Current Inputs	ISC_IN, ISK_IN, RADJ, FADJ, CBIAS, DBIAS	-0.5	2.5	V
Analog Input Currents	ISC_IN, ISK_IN RADJ, FADJ DBIAS, CBIAS	0 0 0	2 2 2	mA mA mA
Digital Output Currents Per Pin	QA/QA*; QB/QB*	0	50	mA
Driver Output Current	Iout	-40	+40	mA
Driver Swing	DVH – DVL	0	11.5	V
Load Input Voltage	LOAD – VCM_IN	-11	+11	V
Storage Temperature	TS	–65	+150	°C
Junction Temperature	TJ		+125	°C
Soldering Temperature (5 seconds, 0.25" from the pin)	TSOL		+260	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these, or any other conditions beyond those “recommended”, is not implied. Exposure to conditions above those “recommended” for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Positive Power Supply	VCC	+8.0	+10	+11.6	V
Negative Power Supply (Note 1)	VEE	-6.25	-5	-4.2	V
Total Analog Supply	VCC – VEE	12.2	15.0	17.85	V
Comparator Output Supply	PECL	+3.0	+3.3	+4.5	V
CVC_GND Compliance	CVC_GND	-0.3	0	+0.3	V
Analog Inputs					
Driver Bias Current	DBIAS	0.7		1.15	mA
Comparator Bias Current	CBIAS	0.5		1.25	mA
Driver Slew Rate Adjustments	RADJ, FADJ	0.3		1.4	mA
Voltage Clamps	VCH VCL	VEE + 5.5 VEE + 3.7		VCC - 3.8 VCC - 5.5	V V
Load Commutating Voltage	VCM_IN	VEE + 3.5		VCC - 3.5	V
Source, Sink Currents	ISC_IN, ISK_IN	0		1.78	mA
Thermal Resistance of Package (Note 2)	θ_{JC}		0.53		°C/W
Junction Temperature	TJ	+40		+100	°C

Note 1: For 'Negative' ECL "Flex" inputs (DHI, DEN, LEN) with range down to –2V input voltage, VEE ≤ –4.75V.
Note 2: Measured at top of package on exposed heat slug.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Configuration Inputs (CONFA, CONFB, SEL_DHI, SEL_CMP)					
Input Low Level	VIL	0		0.8	V
Input High Level	VIH	2		5	V
Input Bias Current					
SEL_DHI	IIN	-25		+25	µA
CONFA, CONFB, SEL_CMP	IIN	-3		+3	µA

Parameter	Symbol	Min	Typ	Max	Units
DCL Node Leakage Characteristics					
All Off (Mode 0, DEN = 0)	I_{DCL_LEAK}	-10		+10	µA
Drive/Receive (Mode 1, LEN = DEN = 0, Clamps Off)	I_{DCL_LEAK}	-20		+20	µA
Drive/Receive with DVT (Mode 2, DEN = 0)	I_{DCL_LEAK}	-20		+20	µA
Drive Pin (Mode 3, DEN = 0)	I_{DCL_LEAK}	-10		+10	µA

DC test conditions (unless otherwise specified): Over the full “Recommended Operating Conditions".

DC Characteristics *(continued)*

Parameter	Symbol	Min	Typ	Max	Units
DRIVER Circuit					
(no Load unless otherwise specified)					
Output Range	DOUT	-2.0		+7.0	V
	DOUT	VEE + 3.7		VCC - 3.8	V
Analog Inputs					
High Level	DVH	VEE + 4.0		VCC - 3.5	V
	DVH	-1.5		+7.4	V
Low Level	DVL, DVT	VEE + 3.5		VCC - 4.0	V
	DVL, DVT	-2.25		+6.5	V
	DOUTSW	0.1		8.0	V
Driver Swing					
Input Current	I_in	-50		+50	µA
Driver Bias (Note 4)	DBIAS	0.7		1.15	mA
Slew Rate Adjustments (Note 4)	RADJ, FADJ	0.3		1.4	mA
RADJ, FADJ, DBIAS Voltage Compliance	VDBIAS, VRADJ, VFADJ	-0.2		+2.0	V
Part-to-Part Variation @ Imin	VDBIAS, VRADJ, VFADJ			100	mV
Part-to-Part Variation @ Imax	VDBIAS, VRADJ, VFADJ			250	mV
Driver Output (Note 1)					
DC Output Current	Imax	-35		+35	mA
Output Impedance (@ ±25 mA) (Note 3)	Rout	4.0	5.5	7.5	Ω
DC Accuracy (Note 1)					
Offset Voltage (@ DVT = DVH = DVL = 0)	DVT, DVH, DVL – DOUT	-100		+150	mV
Offset Tempco (@ DVL = DVT = 0V, DVH = 3V)	ΔDOUT/˚C		0.5		mV/˚C
Gain (Measured @ allowable –FS and +FS)	ΔDOUT/ΔDVT, DVH, DVL	0.975		1.0	V/V
Linearity	DOUT INL	-10		+10	mV
Digital Inputs (DHI, DEN)					
Input Voltage Range (Note 2)	DHI(*), DEN(*)	-2.0		+5.0	V
Differential Input Swing	|Input – Input*|	0.24		2.0	V
Input Current	Iin	-100		+100	µA
Input Capacitance	Cin			3.0	pF

DC conditions (unless otherwise specified): Over the full "Recommended Operating Conditions".

Note 1: See Applications Section describing the applicable “DRIVER OUTPUT RANGE” as a function of VCC and VEE.
Note 2: Digital Input Voltage Range also ≥ (VEE + 2.75V).
Note 3: Typical value of Rout should be used to calculate the external resistor for matching to the application’s transmission line impedance.
Note 4: All DC characteristics tested with DBIAS = 0.7mA, RADJ = FADJ = 0.7mA.

DC Characteristics *(continued)*

Parameter	Symbol	Min	Typ	Max	Units
COMPARATOR Circuits (CBIAS = 0.5mA)					
Analog Inputs					
Voltage Range	CVA, CVB	VEE + 3.6		VCC - 3.65	V
	CVA, CVB	-2.15		+7.25	V
	CVC	-800		+800	mV
Input Current	ICVC	-50		+50	µA
Input Current (VEE +2.0V < V < VCC – 1.25V)	ICVA, ICVB, ICVC	-100		+100	µA
Comparator Bias	CBIAS	0.5		1.25	mA
CBIAS Voltage Compliance	CBIAS	-0.2		+2.0	V
Part-to-Part Variation @ 0.5 mA	CBIAS			200	mV
Part-to-Part Variation @ 1.25 mA	CBIAS			350	mV
VINP Range of Window Comparator	VINP	VEE + 3.7		VCC - 3.8	V
	VINP	-2.0		7.0	V
VINP Range of Differential Comparator	VINP	VEE + 3.7		VCC - 4.7	V
Differential Range of Differential Comparator (Note 1)	|VINP[0]–VINP[1]|	0.1		1.0	V
VINP Hysteresis	VHYS		15		mV
Offset Voltage					
Window Comparators	Vos	-10		+10	mV
Differential Comparators	Vos	-30		+30	mV
Differential Output Swing (Note 2)	|QA – QA*|, |QB – QB*|	400		550	mV
Common Mode Output Range	(QA + QA*) / 2, (QB + QB*) / 2	PECL - 1.6		PECL - 1.2	V

DC test conditions (unless otherwise specified): Over the full “Recommended Operating Conditions".

Note 1: To achieve a differential of 1V, then VEE < –4.7V

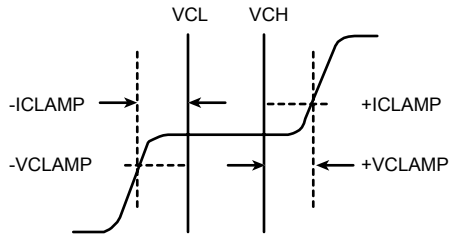
Note 2: Window comparators need 30 mV of overdrive to meet the minimum differential output swing.

DC Characteristics *(continued)*

Parameter	Symbol	Min	Typ	Max	Units
COMPARATOR Voltage Clamps					
Voltage Clamp Range (Clamps On, VC_OFF=0)	VCH	VEE + 5.5		VCC – 3.8	V
	VCH	-0.25		+7.1	V
	VCL	VEE + 3.7		VCC - 5.5	V
	VCL	-2.05		+4.4	V
Voltage Clamp Difference (Note 2)	VCH – VCL	+1.0			V
Voltage Clamp Input Currents					
VCH (VEE + 4V < VCH < VCC - 1.25V)	IVCH	–20		+20	µA
VCL (VEE + 1.25V < VCL < VCC - 4V)	IVCL	–20		+20	µA
Clamp Disable Voltage (Note 2)	VCH – VCL			0.0	V
Clamp Current, Dynamic (Note 1)					
@ VCLAMP = 0V	ICLAMP			600	µA
@ VCLAMP = 0.6V	ICLAMP	15	30		mA
Clamp Current, Static, Short Circuit (measured 2 volts above/below VCH/VCL)	ICLAMPSC		40	100	mA
Short Circuit Protection Delay Timing (Note 3)	Tsc	100	200		ns
Clamp Accuracy					
Offset Voltage (ICLAMP = ±100 µA, VCLAMP = -FS)	VOS	–160		+160	mV

DC test conditions (unless otherwise specified): Over the full “Recommended Operating Conditions".

Note 1: Clamp Characteristics:



Note 2: If (VCH – VCL) < 1.0V, then the clamp function is indeterminate between being active and turning off. A difference of zero volts or negative will ensure the clamps are turned off.

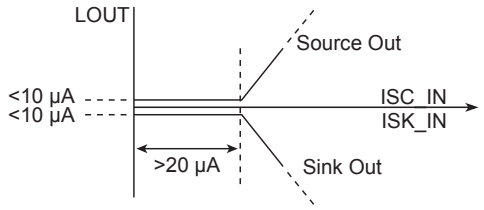
Note 3: Short circuit protection delay time is the period of time that the clamp circuit will provide high dynamic clamp current before switching into the lower, short circuit current condition.

DC Characteristics *(continued)*

Parameter	Symbol	Min	Typ	Max	Units
LOAD Circuit					
Source/Sink Currents					
@ ISK_IN = ISC_IN = 0 to 20 µA (Note 3)	Imin			20	µA
@ ISK_IN = ISC_IN = 1.78 mA (Note 1)	Imax	32			mA
Current Programming Inputs					
Input Voltage @ ISK_IN, ISC_IN =0 to 1.78 mA	V(ISK_IN), V(ISC_IN)	-0.4		+0.3	V
Commutating Voltage Range	VCM_IN	VEE + 3.5		VCC - 3.5	V
	VCM_IN	-2.2		+7.3	V
Commutating Voltage Output, SNK Voltage Input	VCM_OUT, SNK	VEE + 3.7		VCC - 3.8	V
	VCM_OUT, SNK	-2		+7	V
Input Voltage into Load	LOUT	VEE + 3.7		VCC - 3.8	V
	LOUT	-2		+7	V
Load Differential Voltage	|LOUT – VCM_IN|	0.75		+10	V
Commutating Buffer					
Input Current @ VCM_IN	IVCM_IN	0		+10	µA
Load Enabled (LE high, Load On)					
Input Voltage Range (Note 2)	LEN, LEN*	-2.0		+5.0	V
Differential Input Swing	|LEN – LEN*|	0.24		2.0	V
Input Current	ILEN, ILEN*	-100		+100	µA
Load Output Impedance (ILOUT = ±32mA)	ZLOUT	5	7	9	Ω
VCM Buffer Accuracy					
Offset Voltage (@ VCM_IN = 0V)	VCM_OUT – VCM_IN	-185		+185	mV
Current Source Accuracy					
Source/Sink Current Turn-On Point (Note 1)	ISC, ISK	20		40	µA
Source /Sink Current Gain (Note 1)	Ai	20		24	
Source/Sink Linearity (Note 4)		-200		+200	µA

DC test conditions (unless otherwise specified): Over the full "Recommended Operating Conditions".

Note 1: (VCM_IN + 0.75V) ≤ LOUT, or LOUT≤ (VCM_IN – 0.75V).
Note 2: Load Enable Input Voltage also > (VEE + 2.75V).
Note 3: Load characteristics:



Note 4: Calibrated at input points of 100µA, 500µA, 1mA, 1.4mA.

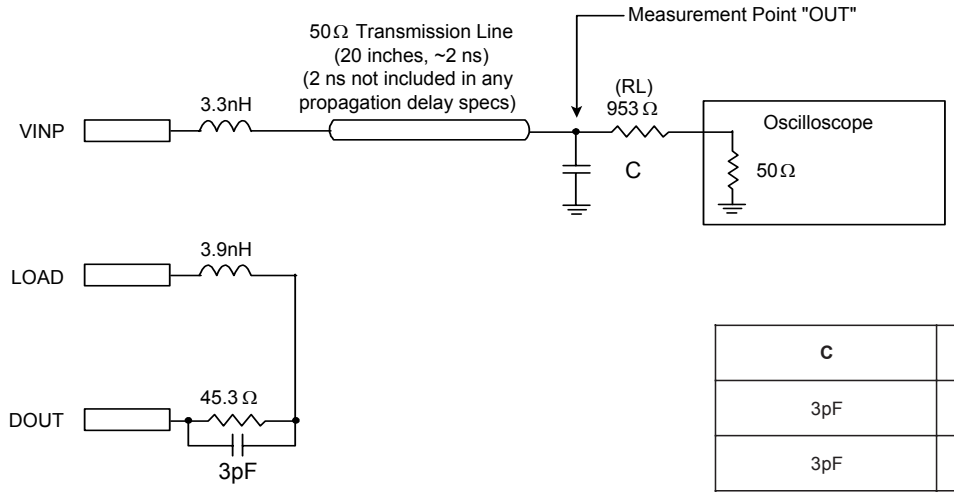
DC Characteristics *(continued)*

Parameter	Symbol	Min	Typ	Max	Units
Power Supply Currents					
PECL Power Supply Current	IPECL	155	176	198	mA
Mode 0 - All Off - Lowest Power					
(Driver, Comp, Load Powered OFF)					
Positive Supply	ICC		350	409	mA
Negative Supply	IEE	-421	-365		mA
Modes 1, 2, 3 - Higher Power					
Positive Supply	ICC		406	480	mA
Negative Supply	IEE	-500	-430		mA

DC conditions: DVL = 0V, DVH = 3V, CVA = 0.5V, CVB = 2.4V, CVC = 1V, VCM_IN = 0V, ISK = ISC = 0 mA, PECL = 3.3V, comparator outputs terminated 50Ω to PECL –2V. All conditions with DHI[0:1], SEL_DHI, SEL_CMP = Low. Designers should add the maximum currents expected for the programmable Load functions to the respective power supplies (ICC and/or IEE). CBIAS = 0.5mA, DBIAS = 0.7mA, RADJ = FADJ = 0.7mA.

AC Characteristics

AC Test Circuit



C	V_{SWING}
3pF	0.8V (ECL)
3pF	0.3V (LVDS)
5pF	0.3V (LVTTL)
8pF	5.0V (CMOS/TTL)

Parameter	Symbol	Min	Typ	Max	Units
Configuration Inputs Settling Time of CONFA, CONFB, SEL_DHI, SEL_CMP				100	ns

AC Characteristics *(continued)*

Parameter	Symbol	Min	Typ	Max	Units
LOAD Circuit					
Propagation Delay (Note 1)					
Inhibit to Iout (to 90% of programmed Iout)	Tpd_on	2.25	2.7	3.5	ns
Iout to Inhibit (to 10% of programmed Iout)	Tpd_off	2.25	2.3	3.5	ns
Output Capacitance					
Load Active (ISC_IN, ISK_IN = 0)	Cout		3.2		pF
Load Off	Cout		3.2		pF
COMPARATOR Circuits					
Propagation Delay (Figure 4 with VINP 0.4V to 1.2V) (Note 6)	TPLH, TPHL	0.5		1.5	ns
Input Waveform Tracking (Figure 6) (Note 6) (3V step, 100 ps error, 0.6V to 2.4V)		3.0			V/ns
Dispersion Related Specifications					
Common Mode Dispersion (Note 6) (Figure 2)	ΔTPLH, ΔTPHL		10	30	ps
Pulse Width (Notes 2,6) (Figure 3)		1.0			ns
Overdrive (from 200 mV to 800 mV, 1V/ns slew rate) (Figure 4) (Note 6)	ΔTPLH, ΔTPHL			70	ps
Delay Symmetry (same comparator) (0 to 800 mV input) (Figure 4)	|TPHL – TPLH|		25	50	ps
Slew Rate (Figure 5) (Note 6)	ΔTpd		25	50	ps
COMP_A to COMP_B Delay Matching (Figure 4)	|TPLH – TPLH| or |TPHL – TPHL|		35	60	ps
Differential Delay Tracking (VINP1 vs VINP0 in differential mode) (Figure 4)	|TPLH – TPLH| or |TPHL – TPHL|			50	ps
Input Capacitance	Cin		4.9		pF
Digital Output Rise and Fall Times (20% - 80%) (into 50Ω load to (PECL – 2V))	Tr, Tf		200	250	ps
Delay TempCo (Note 6)	ΔTpd/˚C		2.5		ps/˚C
DRIVER Circuit					
Propagation Delay (0 to 800 mV Output) (Note 1)					
Data (DHI) to Output (Figure 10)	TPLH, TPHL	1.0		2.0	ns
Output Active to HiZ (Figure 9)	TPAZ	1.25		2.5	ns
HiZ to Output Active (Figure 9)	TPZA	2.0		4.0	ns
Rise/Fall Times (Figure 11)					
0 to 800 mV (20% - 80%)	Tr/Tf			0.3	ns
0 to 3V (10% - 90%)	Tr/Tf		0.7	0.9	ns
0 to 3V (10% - 90%) (Note 3)	Tr/Tf	1.5			ns
0 to 5V (10% - 90%)	Tr/Tf		1.0	1.2	ns
Crossover Voltage Error (Figure 15)	VXOVER	45		55	%

AC Characteristics *(continued)*

Parameter	Symbol	Min	Typ	Max	Units
DRIVER Circuit (continued)					
Fmax (Note 4) (Figure 12)					
0 to 800 mV	Fmax	500			MHz
0 to 3V	Fmax	300			MHz
0 to 5V	Fmax	200			MHz
Fmax (R_L=50Ω, swing = programmed value) (Note 4) (Figure 14)					
0 to 0.5V	Fmax		900		MHz
0 to 1.0V	Fmax		450		MHz
0 to 3.0V	Fmax		400		MHz
Minimum Pulse Width (Note 4) (Figure 8)	Tpw+, Tpw–				
0 to 800 mV				0.6	ns
0 to 3V				1.2	ns
0 to 5V				1.5	ns
Pulse Width Dispersion to Minimum Pulse Width (PWmin = 0.8 ns) (Figure 7)	ΔTpw			125	ps
Driver-to-Driver Skew (Diff. Driver Mode) (Note 5)				60	ps
Output Capacitance	Cout		7.0		pF
Delay Tempco (Figure 10) (Switching DVH and DVL)	ΔTpd/°C		1.5	2.0	ps/°C
Delay Symmetry (same driver, 0.8V swing) (Figure 10)	|TPHL – TPLH|			100	ps
DVT Enable/Disable Times (Figure 13)					
DVL to DVT	TPLT	3.0		4.5	ns
DVT to DVL	TPTL	2.0		3.5	ns
DVH to DVT	TPHT	3.25		4.5	ns
DVT to DVH	TPTH	2.0		3.5	ns
Trans. Time Matching (same driver) (Figure 11)					
DOUT = 0.8V	ΔTr,f			100	ps
DOUT = 3.0V	ΔTr,f			100	ps
DOUT = 5V	ΔTr,f			150	ps
Overshoot/Undershoot (Figure 14)					
DOUT = 0.8V		0		100	mV
DOUT = 3.0V		0		150	mV
DOUT = 5V		0		300	mV
Ringback (Figure 14)					
DOUT = 0.8V				50	mV
DOUT = 3.0V				100	mV
DOUT = 5V				200	mV
Voltage Crosstalk (when switching adjacent channel)					
DOUT = 0.8V				±10	mV
DOUT = 3.0V				±10	mV
DOUT = 5V				±10	mV
Timing Crosstalk					
DOUT = 0.8V				±10	ps
DOUT = 3.0V				±10	ps
DOUT = 5V				±10	ps

AC test conditions (unless otherwise specified): "Recommended Operating Conditions". VCC = +10V, VEE = –5V, DBIAS = 0.7mA, RADJ = 0.7mA, FADJ = 0.7mA, CBIAS = 0.5mA.

Note 1: Propagation delays for LV_PECL, differential logic inputs. LOUT has 50Ω to GND for Load tests.

Note 2: For 800 mV input while maintaining Tpd Error <100 ps.

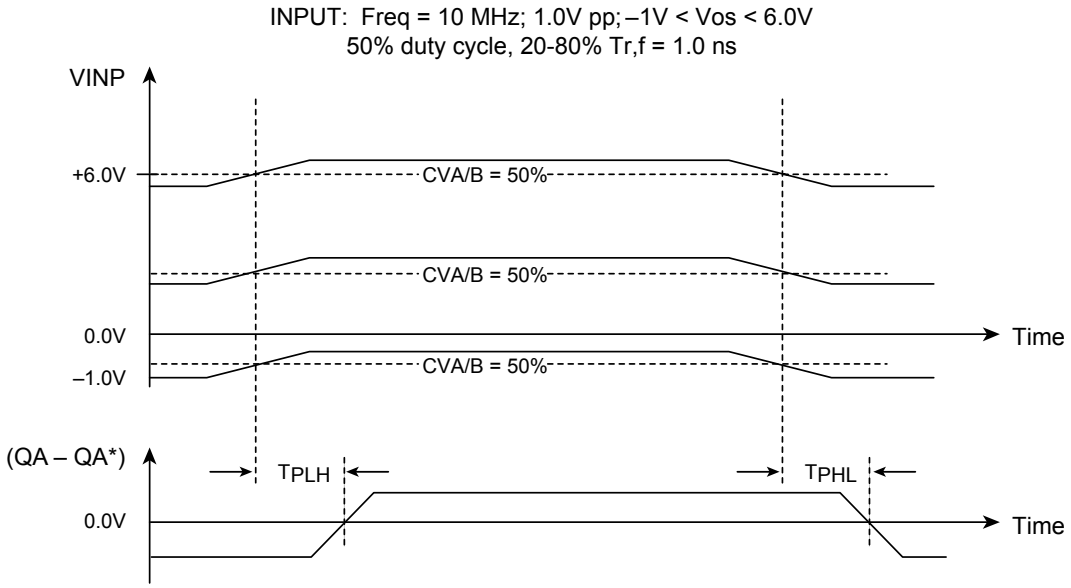
Note 3: Min Rise/Fall Times for RADJ = FADJ = 0.3 mA.

Note 4: At 10% output amplitude attenuation.

Note 5: 0 to 800 mV outputs.

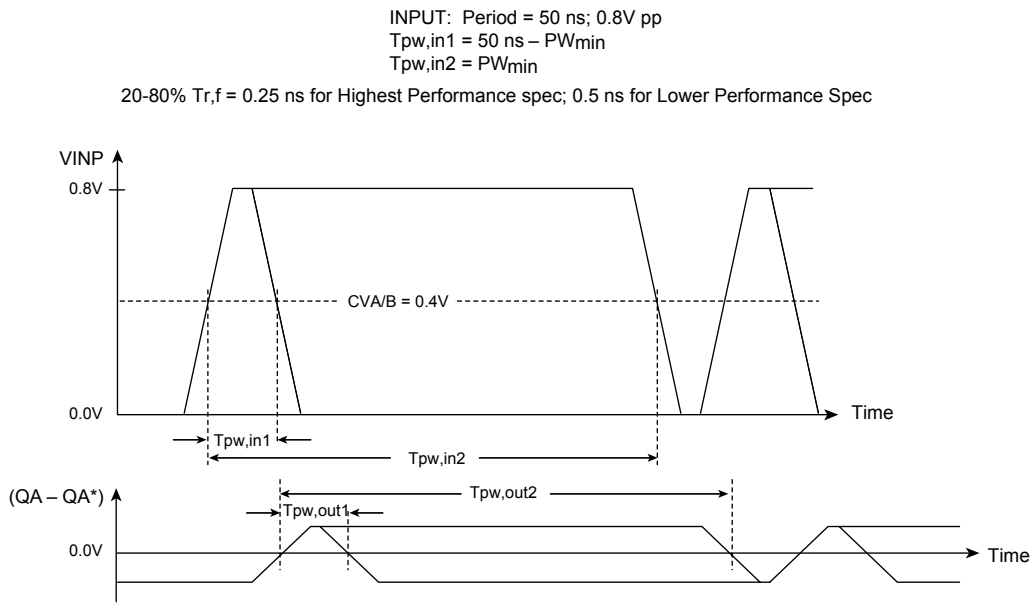
Note 6: Applies to single-ended and differential comparators.

AC Characteristics *(continued)*



The measured result is the maximum absolute value change in TPLH or TPHL over the different common mode levels.

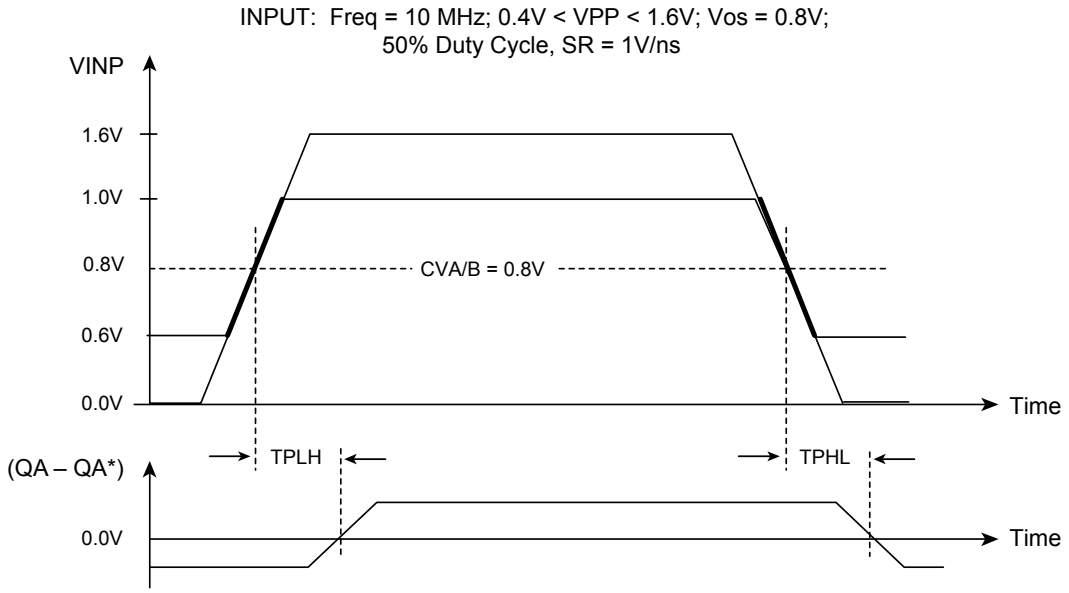
Figure2. Comparator Dispersion: Common Mode Measurement Definition



The measured result is the maximum absolute value change in [Tpw,in – Tpw,out] as the P.W. changes from 25 ns to the endpoints of PW_{min} and [50ns – PW_{min}].

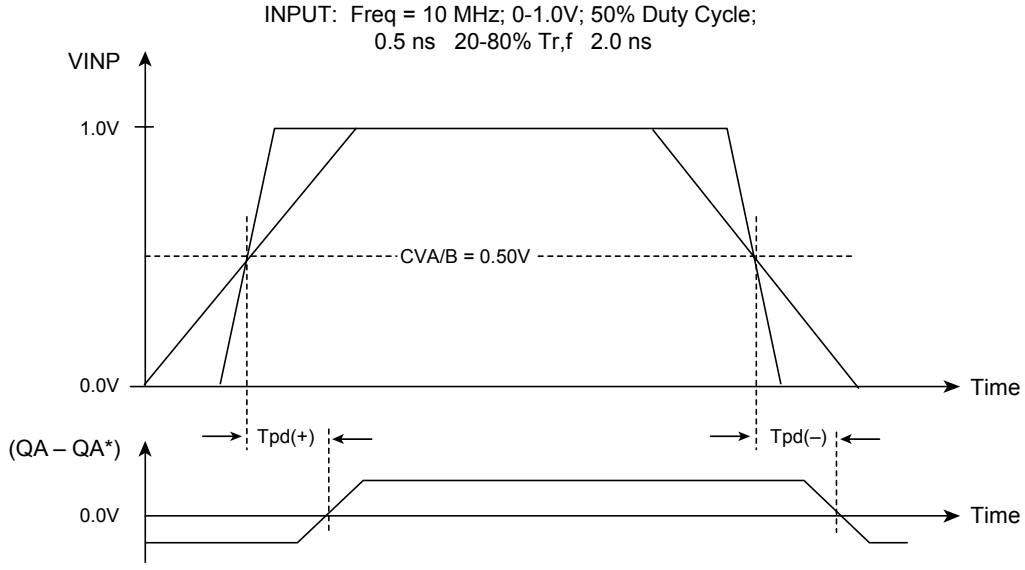
Figure 3. Comparator Dispersion: Pulse Width Measurement Definition

AC Characteristics *(continued)*



The measured result is the maximum absolute value of the change in TPLH or TPHL when the overdrive changes from 800 mV to 200 mV.

Figure 4. Comparator Dispersion: Overdrive Measurement Definition

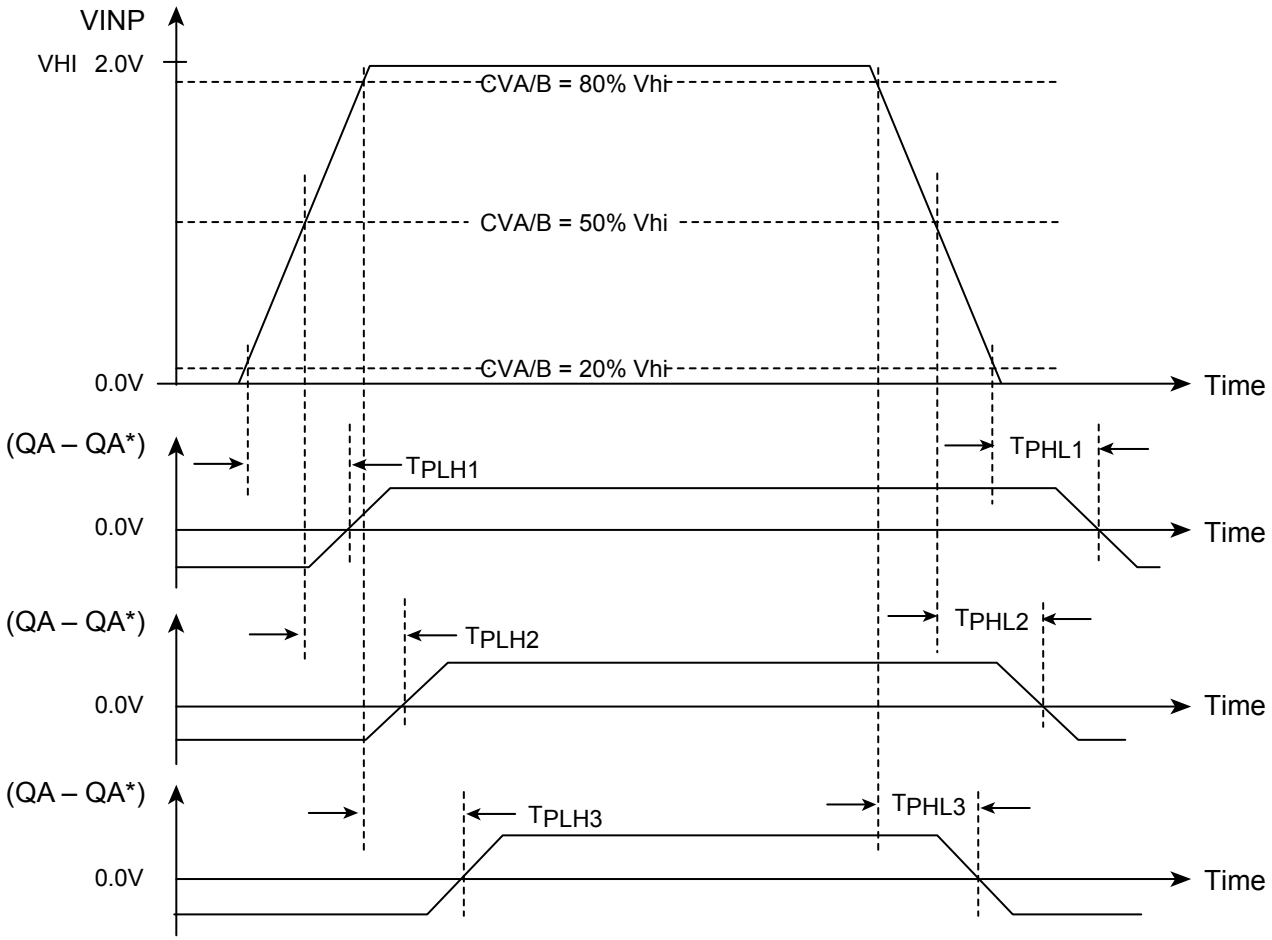


The measured result is the maximum absolute value of the change in Tpd(+) or Tpd(–) as the input signal slew rate changes from minimum to maximum as defined in the figure.

Figure 5. Comparator Input Slew Rate Measurement Definition

AC Characteristics *(continued)*

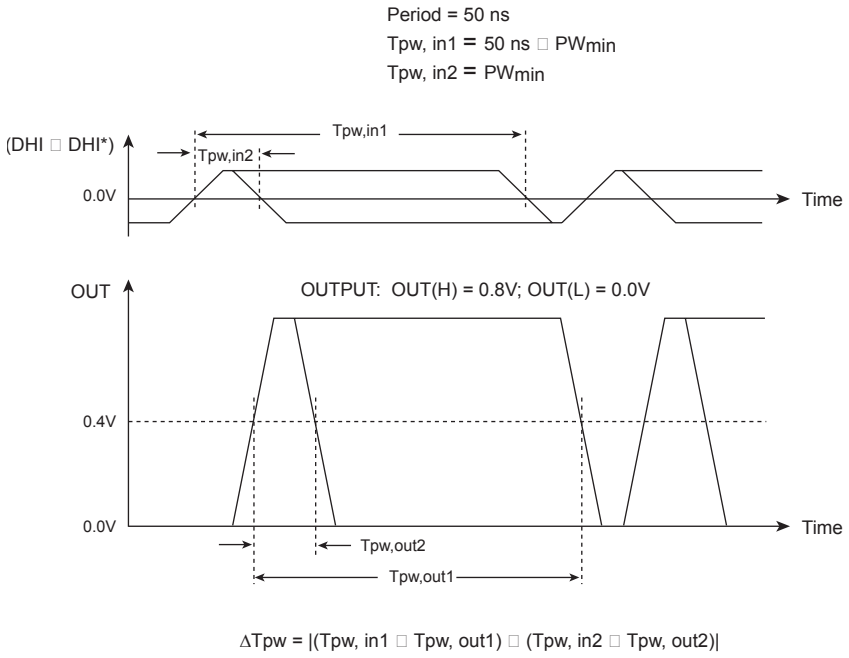
INPUT: Freq = 10 MHz; 0-VHI; 50% Duty Cycle;



The measured result is the maximum absolute value of the change in Tpd(+) or Tpd(–) among the three measurement points for each edge as depicted above.

Figure 6. Comparator Dispersion: Waveform Tracking Measurement Definition

AC Characteristics *(continued)*



The measured result is the maximum absolute value of the change in [Tpw,in – Tpw,out] as the P.W. changes from 25 ns to the endpoints of PW_{min} and [50ns – PW_{min}].

Figure 7. Driver Dispersion: Pulse Width Measurement Definition

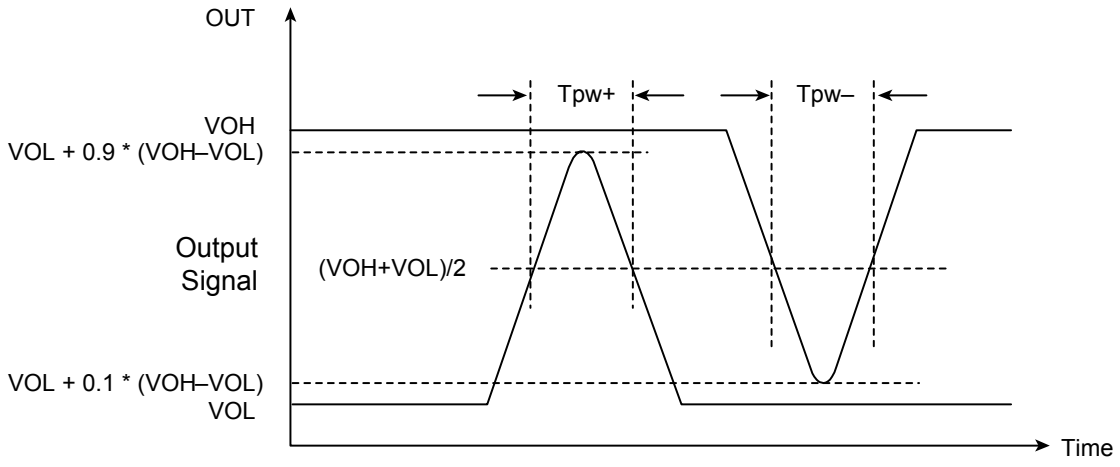


Figure 8. Driver Minimum Pulse Width Measurement Definition

AC Characteristics *(continued)*

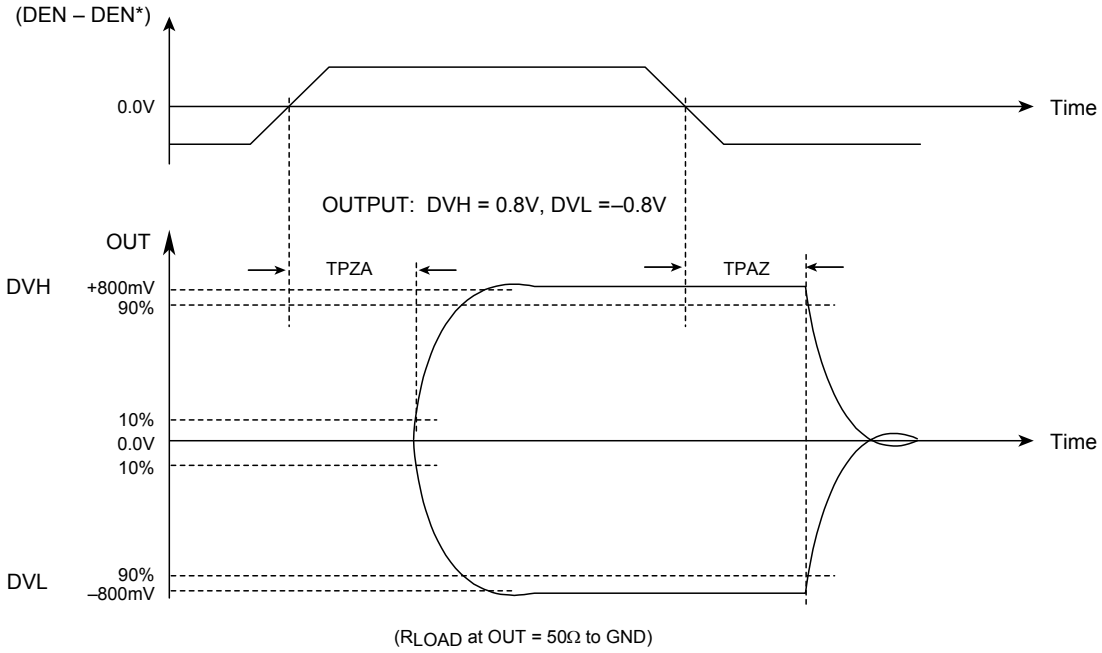


Figure 9. Driver HiZ Enable/Disable Delay Measurement Definition

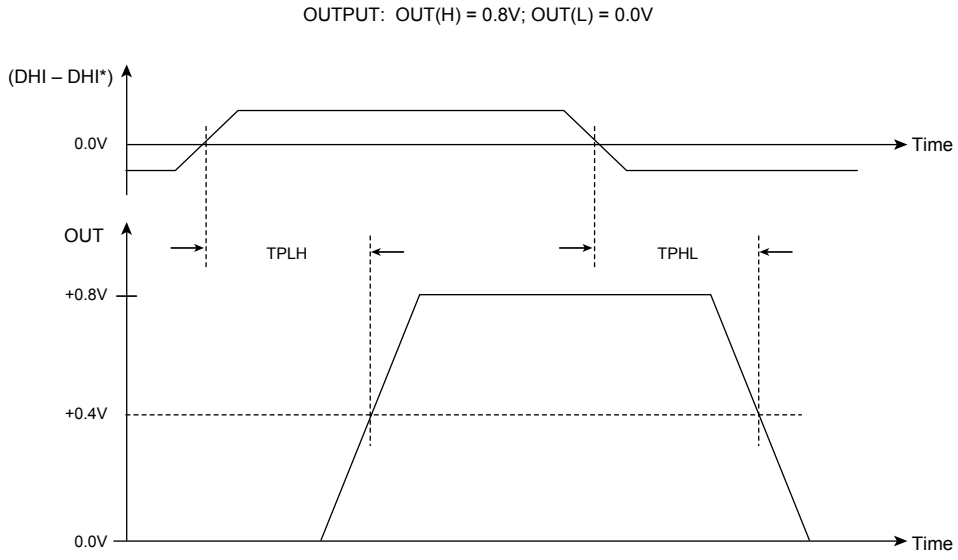
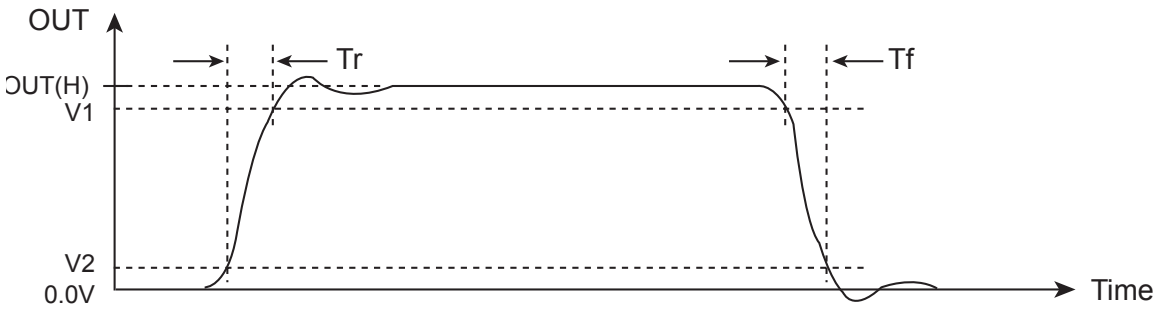


Figure 10. Driver Propagation Delay: DHI to OUT, Symmetry, and Tracking Skew Measurement Definition

AC Characteristics *(continued)*



V1 is 0.9 * OUT(H) for 3V and 5V, 0.8 * OUT(H) for 0.8V and lower
V2 is 0.1 * OUT(H) for 3V and 5V, 0.2 * OUT(H) for 0.8V and lower

Figure 11. Driver Transition Times and Transition Time Matching Measurement Definition

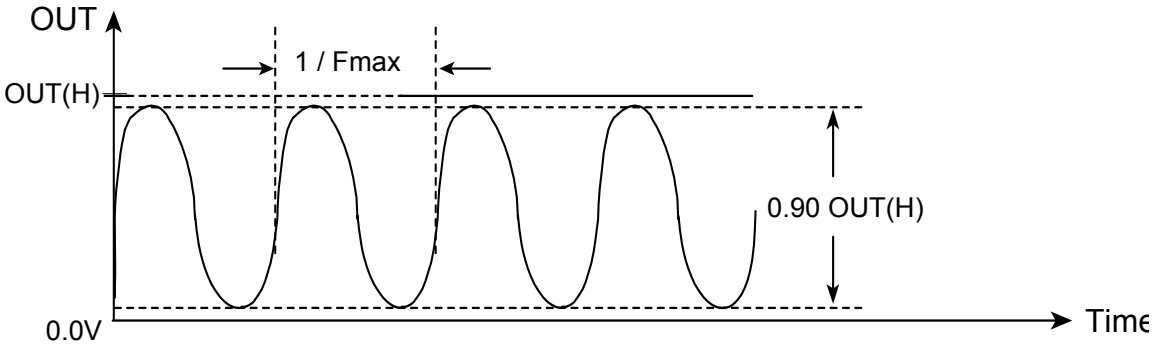


Figure 12. Driver Fmax Measurement Definition

AC Characteristics *(continued)*

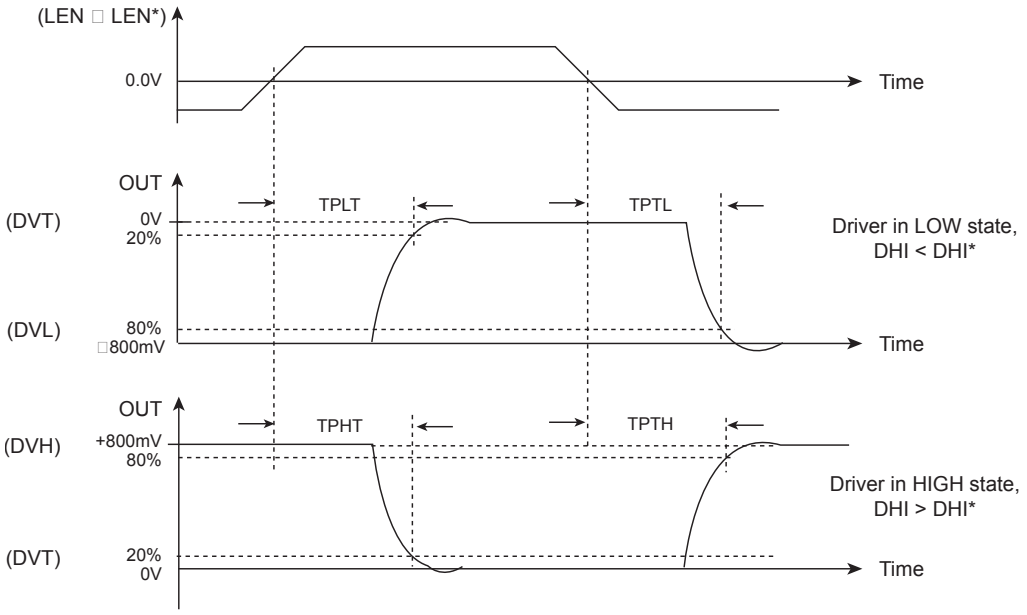
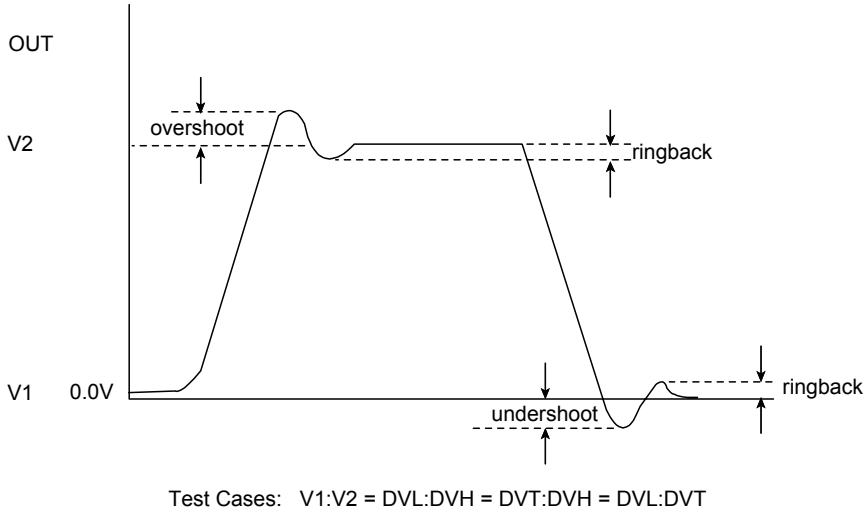


Figure 13. Driver DVT (Third Driver Level) Enable/Disable Delay Measurement Definition



Test Cases: V1:V2 = DVL:DVH = DVT:DVH = DVL:DVT

Figure 14. Driver Overshoot, Undershoot, and Ringback

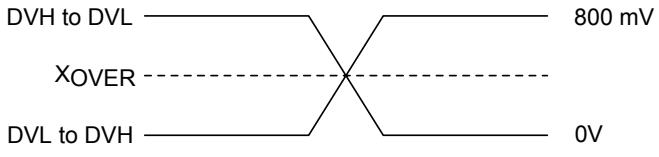


Figure 15. Driver Output Crossover Voltage Measurement

Ordering Information

Model Number	Package
E7725AXF	14 x 20 x 2.0mm, 128-Pin MQFP with Exposed Heat Slug
EVM7725AXF	Edge7725 Evaluation Board

Contact Information

Semtech Corporation
Test and Measurement Division
10021 Willow Creek Rd., San Diego, CA 92131
Phone: (858)695-1808 FAX (858)695-2633