TUSB9260
USB 3.0 TO SATA BRIDGE

Data Manual

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USB 3.0 TO SATA BRIDGE

Check for Samples: TUSB9260

1 Introduction

1.1 TUSB9260 Features

- Universal Serial Bus Support
  - SuperSpeed USB 3.0 Compatible
    - Integrated SuperSpeed USB 3.0 Tranceiver
    - Integrated USB 2.0 High-Speed Tranceiver
    - Integrated SuperSpeed USB 3.0 Controller
    - Integrated USB 2.0 High-Speed Controller
  - USB Class Support
    - USB Attached SCSI Protocol (UASP)
    - USB Mass Storage Class Bulk-Only Transport (BOT)
    - USB Bootability Support
    - USB Human Interface Device (HID)
  - Supports Firmware Update Via USB Using a TI Provided Application
- SATA Interface
  - Serial ATA Specification Revision 2.6 Supports
    - gen1i, gen1m, gen2i, and gen2m
  - Support for Mass-Storage Devices Compatible With the ATA/ATAPI-8 Specification
- Integrated ARM Cortex M3 Core
  - Customizable Application Code Loaded From EEPROM Via SPI Interface
  - One Additional SPI Port Chip Select for Peripheral Connection
  - Up to 12 GPIOs for End-User Configuration
    - 2 GPIOs Have PWM Functionality for LED Blink Speed Control
- General Features
  - Operates From a Single Low Cost Crystal or From a Clock Oscillator That Supports 20, 25, 30, and 40 MHz
    - Integrated Spread Spectrum Clock Generation
  - Available in a Fully RoHS Compliant Package

1.2 Target Applications

- External HDD
- External DVD
- External CD
- HDD-Based Portable Media Player

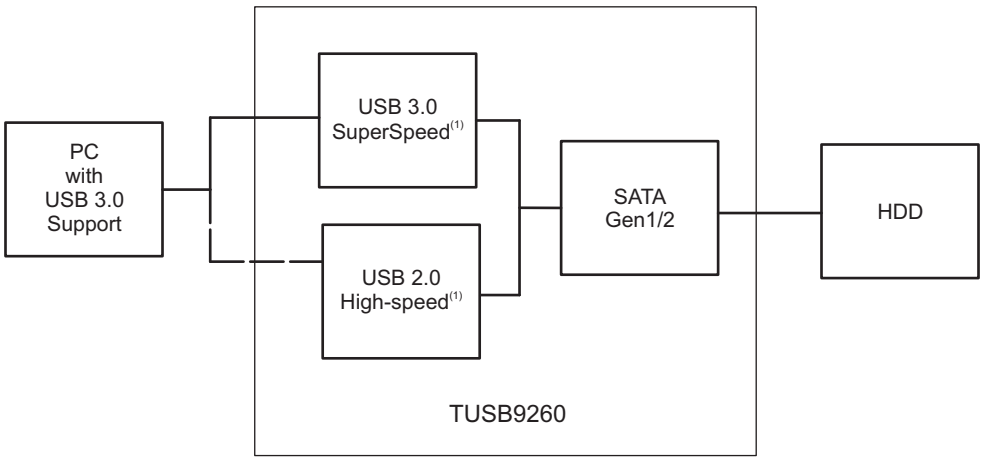
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1.3 Typical System Diagram



(1) USB connection is made at either SuperSpeed or High-Speed depending on the upstream connection support.

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2 Overview

2.1 Description

The TUSB9260 is an ARM cortex M3 microcontroller based USB 3.0 to serial ATA bridge. It provides the necessary hardware and firmware to implement a USB attached SCSI protocol (UASP) compliant mass storage device suitable for bridging hard disk drives (HDD), solid state disk drives (SSD), optical drives and other compatible SATA 1.5-Gbps or SATA 3.0-Gbps devices to a USB 3.0 bus. In addition, to UASP support the firmware implements the mass storage class bulk-only transport, and USB human interface device interfaces.

The TUSB9260 ROM contains boot code that executes after a global reset which performs the initial configuration required to load a firmware image from an attached SPI flash memory to local RAM. In the absence of an attached SPI flash memory or a valid image in the SPI flash memory, the firmware will idle and wait for a connection from a USB host through its HID interface which is also configured from the boot code. The latter can be accomplished using a custom application or driver to load the firmware from a file resident on the host system.

Once the firmware is loaded it configures the SATA advanced host controller interface host bus adapter (AHCI) and the USB device controller.

The configuration of the AHCI includes allocation of memory for the command list and the FIS receive area, programming of the port command list (CL) and frame information structure (FIS) base address registers and enabling the port to receive FISs, as well as configuration of interrupt sources for event notification such as device connections.

In addition, the configuration of the AHCI includes a port reset which initiates an out of band (OOB) TX sequence from the AHCI link layer to determine if a device is connected, and if so negotiate the connection speed with the device (3.0 Gbps or 1.5 Gbps).

The OOB TX sequence starts by transmitting a COMRESET to the device. If no COMINIT is detected after a timeout period, the link transmits a COMRESET again, and continues the sequence until a COMINIT is detected. When a COMINIT is detected from a device, the link transmits a COMWAKE to the device and waits for the device to return a COMWAKE. Following the receipt of COMWAKE, the device should begin speed negotiation by transmitting ALIGN primitives at the highest data rate; the speed negotiation is completed by the host decoding the ALIGN (either 3 Gbps or 1.5 Gbps depending on the device). After speed negotiation is complete, the OOB TX sequence is complete and the link and phy are in the ready state. Note, the only time a COMINIT is expected is after the transmission of COMRESET; the receipt of COMINIT at any other time is an unsolicited COMINIT which transitions the link layer to the beginning of OOB TX sequence.

Following speed negotiation, the device should transmit a device to host (D2H) FIS with the device signature. This first D2H FIS is received by the link layer and copied to the port signature register. When firmware is notified of the device connection it queries the device for capabilities using the IDENTIFY DEVICE command. Firmware then configures the device as appropriate for its interface and features supported, for example an HDD that supports native command queuing (NCQ).

The configuration of the USB device controller includes creation of the descriptors, configuration of the device endpoints for support of UASP and USB mass storage class bulk-only transport (BOT), allocation of memory for the transmit request blocks (TRBs), and creation of the TRBs necessary to transmit and receive packet data over the USB. In addition, the firmware provides any other custom configuration required for application specific implementation, for example a HID interface for user initiated backup.

After USB device controller configuration is complete, if a SATA device was detected during the AHCI configuration the firmware connects the device to the USB bus when VBUS is detected. According to the USB 3.0 specification, the TUSB9260 will initially try to connect at SuperSpeed, if successful it will enter U0; otherwise, after the training time out it will enable the DP pull up and connect as a USB 2.0 high-speed or full-speed device depending on the speed supported by host or hub port.

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When connected as a SuperSpeed device, the firmware presents the UASP interface as the primary interface, and the BOT interface as a secondary interface. If the host stack is not UASP aware, it can enable the BOT interface using a SET_INTERFACE request for alternate interface 1.

When connected as a high-speed or full-speed device, the firmware presents the BOT interface as the primary interface and the UASP interface as the secondary interface. If the host stack is UASP aware, it can enable the UASP interface using a SET_INTERFACE request for alternate interface 1.

When configured for BOT, the firmware performs the following functions:

- Receives the command block wrapper (CBW) from the OUT endpoint on the USB interface.
- Deconstructs the encapsulated command in the CBW and creates the appropriate command table (CT) entry, including the physical region descriptor table (PRDT), as necessary for the AHCI to deliver command to the SATA device.
- Performs management as required for delivery of the command response received from the SATA device, including data for read commands, as packet data to the USB bulk transfer pipe. This includes setting up TRBs for the USB device controller.
- Performs management as required for delivery of packet data for write commands from the USB bulk interface pipe to the SATA device. This includes setting up the TRBs for the device controller.
- Creates the command list (CL) entry pointing to the CT entry and enable the command slot for delivery of the command from the AHCI to the SATA device.
- Creates the command status wrapper (CSW) for each CBW received for delivery to the USB host on the IN endpoint.
- Monitors for error conditions per the 13 cases (defined in the BOT specification).
- Performs other necessary operations, including hardware initialization or manipulation of GPIOs, to support device activity indication, hot plug, media notifications, one-touch back up if supported, or other required functionality.

When the UASP configuration is enabled, the firmware performs the following functions:

- Receives the command information units (IU) from the command OUT endpoint on the USB interface.
- Creates the appropriate command table (CT) entry based on the received command IU, including the physical region descriptor table (PRDT), as necessary for the AHCI to deliver command to the SATA device.
  - Performs management as required for delivery of the command response IU received from the SATA device, this includes read ready IU, write ready IU, and response IU. These are delivered on the status IN endpoint. This includes setting up TRBs on the USB device controller. Note, when operating in SuperSpeed mode the device does not have to return the read ready IU or write ready IU if it returns ERDY with the initiator port transfer tag (see the UAS specification) as the stream ID.
  - Performs management as necessary to deliver data from target for read commands, on the DFT IN endpoint. This includes setting up TRBs on the USB device controller.
  - Performs management as required for delivery of packet data from initiator for write commands from the DFI OUT endpoint to the SATA device. This includes setting up TRBs on the USB device controller.
- Creates the command list (CL) entry pointing to the CT entry and enable the command slot for delivery of the command from the AHCI to the SATA device. This includes maintaining a list of command tags and associated command slots.
- Monitors for error conditions and provide appropriate status.
- Performs other necessary operations, including hardware initialization or manipulation of GPIOs, to support device activity indication, hot plug, media notifications, one-touch back up if supported, or other required functionality.

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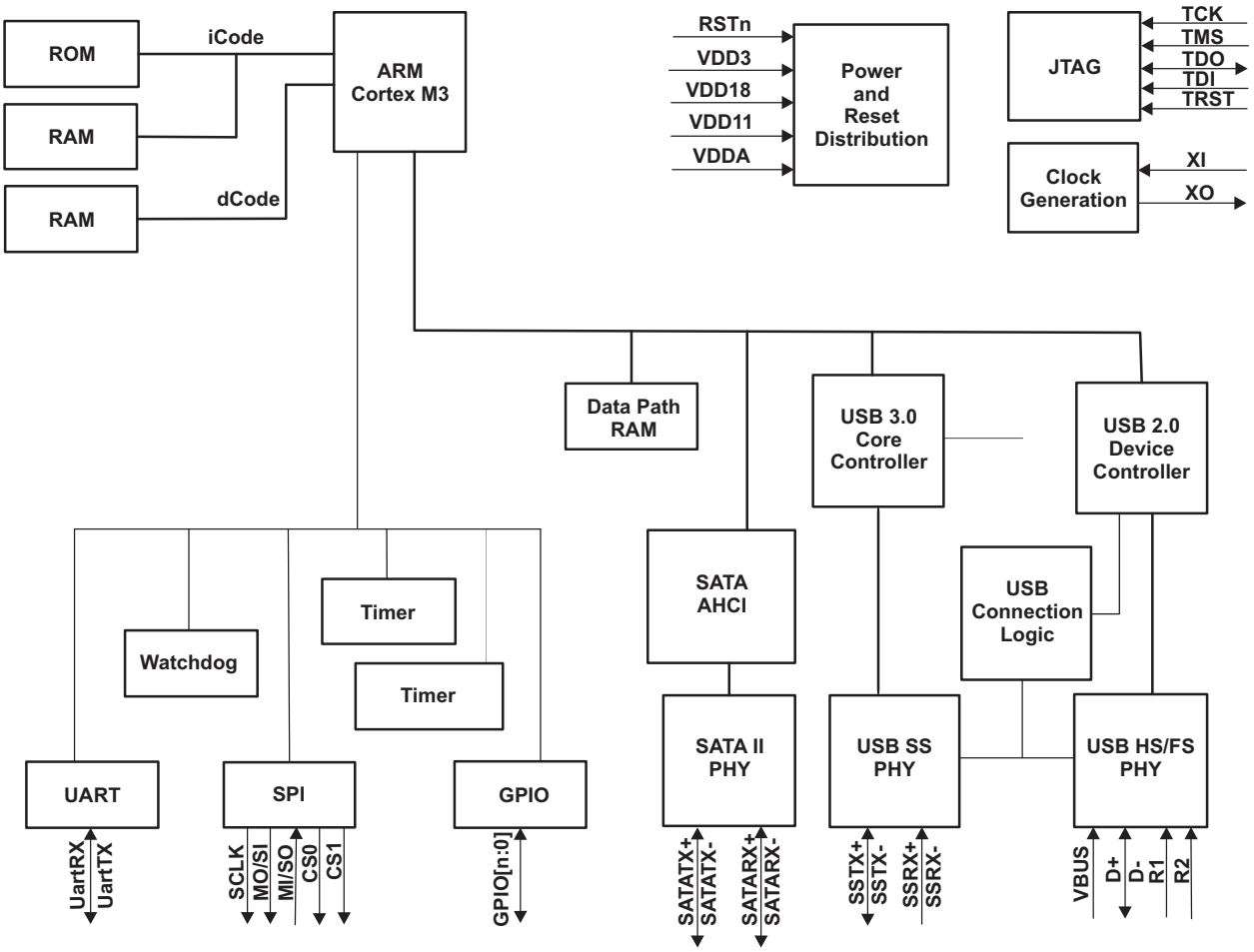
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2.2 ORDERING INFORMATION

PACKAGE	VOLTAGE	ORDERABLE PART NUMBER
100-terminal (Lead-Free) PBGA — ZAW	3.3-V and 1.5-V power terminals	TUSB9260ZAW

2.3 DEVICE INFORMATION

Device Block Diagram



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2.4 Terminal Descriptions

Table 2-1. Clock and Reset Signals

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
GRSTN		I/O	Global power reset. This reset brings all of the TUSB9260 internal registers to their default states. When GRSTN is asserted, the device is completely nonfunctional.
XI		I	Crystal input. This terminal is the crystal input for the internal oscillator. The input may alternately be driven by the output of an external oscillator. When using a crystal a 1-MΩ feedback resistor is required between X1 and XO.
XO		O	Crystal output. This terminal is the crystal output for the internal oscillator. If XI is driven by an external oscillator this pin may be left unconnected. When using a crystal a 1-MΩ feedback resistor is required between X1 and XO.
FREQSEL[1:0]		I	Frequency select. These terminals indicate the oscillator input frequency and used to configure the correct PLL multiplier. The field encoding is as follows: 00b 20 MHz 01b 25 MHz 10b 30 MHz 11b 40 MHz

Table 2-2. USB signals

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
USB_SSTXP		O	USB SuperSpeed transmitter differential pair (positive)
USB_SSTXM		O	USB SuperSpeed transmitter differential pair (negative)
USB_SSRXP		I	USB SuperSpeed receiver differential pair (positive)
USB_SSRXM		I	USB SuperSpeed receiver differential pair (negative)
USB_DP		I/O	USB High-speed differential transceiver (positive)
USB_DM		I/O	USB High-speed differential transceiver (negative)
USB_VBUS		I	USB bus power
USB_R1		I	Precision resistor reference. A 10K +/- 1% resistor should be connected between R1 and R2.
USB_R2		I	Precision resistor reference return
CEXT1		PT	PLL loop capacitor. External loop capacitor for the SS PHY PLL. The value of the loop capacitor is TBD.
CEXT0		PT	PLL loop capacitor. External loop capacitor for the USB 2.0 PHY PLL. The value of the loop capacitor is TBD.

Table 2-3. SATA Signals

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
SATA_TXP		O	Serial ATA transmitter differential pair (positive)
SATA_TXM		O	Serial ATA transmitter differential pair (negative)
SATA_RXP		I	Serial ATA receiver differential pair (positive)
SATA_RXM		I	Serial ATA receiver differential pair (negative)
CEXT2		PT	PLL loop capacitor. External loop capacitor for the SATA PLL. The value of the loop capacitor is TBD.

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Table 2-4. Serial peripheral Interface (SPI) signals

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
SPI_SCLK		I/O	SPI clock
SPI_MOSI		I/O	SPI master out, slave in
SPI_MISO		I/O	SPI master in, slave out
SPI_CS0		I/O	Primary SPI chip select for Flash RAM
SPI_CS[2:1]/ GPIO[11:10]		I/O	SPI chip select. SPCI chip selects for additional peripherals. When not used for SPI chip selects they may be used as general purpose I/O.

Table 2-5. Test and Miscellaneous Signals

TERMINAL		I/O	DESCRIPTION
NAME	No.		
JTAG_TCK		I/O	JTAG test clock
JTAG_TDI		I/O	JTAG test data in
JTAG_TDO		I/O	JTAG test data out
JTAG_TMS		I/O	JTAG test mode select
JTAG_RSTN		I/O	JTAG reset
GPIO9/UART_TX		I/O	GPIO/UART transmitter. This terminal can be configured as a GPIO or as the transmitter for a UART channel. This pin defaults to a general purpose output.
GPIO8/UART_RX		I/O	GPIO/UART receiver. This terminal can be configured as a GPIO or as the receiver for a UART channel. This pin defaults to a general purpose output.
GPIO[7:0]		I/O	GPIO input/outputs. These pins are configurable as general purpose input/outputs.
PWM[1:0]		I/O	PWM input/outputs. These pins provide PWM capabilities for example to drive status LEDs.

Table 2-6. Power Signals

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
VDD33		PWR	3.3 V power rail
VDDA		PWR	1.1 V analog power rail
VDD18		PWR	1.8 V power rail
VDD11		PWR	1.1 V power rail
VSS		PWR	Ground, digital
VSSOSC		PWR	Oscillator return

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TUSB9260ZAW	PREVIEW	BGA	ZAW	100	1	TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
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OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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