Data Sheet

CADEKA
Amplify the Human Experience

Comlinear® CLC1201
Instrumentation Amplifier

FEATURES
- ±2.3V to ±18V supply voltage range
- Gain range of 1 to 10,000
- Gain set with one external resistor
- ±125µV maximum input offset voltage
- 0.1µV/°C input offset drift
- 700kHz bandwidth at G = 1
- 1.2V/µs slew rate
- 90dB minimum CMRR at G = 10
- 2.2mA maximum supply current
- 6.6nV/√Hz input voltage noise
- 70nV/√Hz output voltage noise
- 0.2μV_{pp} noise (0.1Hz to 10Hz)
- DIP-8 or Pb-free SOIC-8

APPLICATIONS
- Bridge amplifier
- Scales
- Thermocouple amplifier
- ECG and medical instrumentation
- MRI (Magnetic Resonance Imaging)
- Patient Monitors
- Transducer interface
- Data acquisition systems
- Strain gauge amplifier
- Industrial process controls

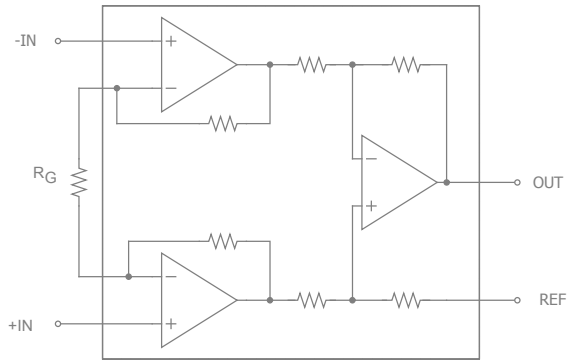
General Description

The CLC1201 is a low power, general purpose instrumentation amplifier with a gain range of 1 to 10,000. The CLC1201 is offered in 8-lead SOIC or DIP packages and requires only one external gain setting resistor making it smaller and easier to implement than discrete, 3-amp designs.

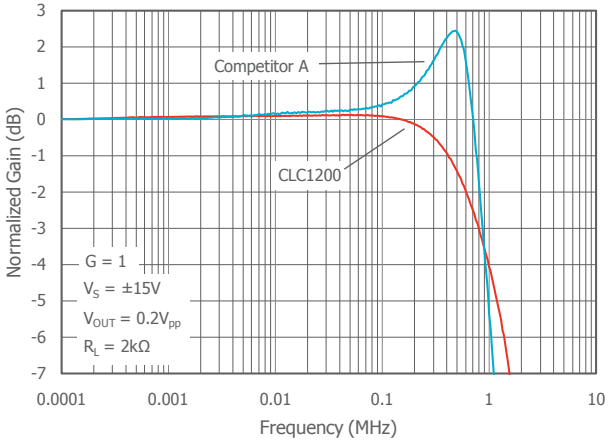
While consuming only 2.2mA of supply current, the CLC1201 offers a low 6.6nV/Hz input voltage noise and 0.2μV_{pp} noise from 0.1Hz to 10Hz.

The CLC1201 offers a low input offset voltage of ±125µV that only varies 0.1µV/°C over it's operating temperature range of -40°C to +85°C. The CLC1201 also features 50ppm maximum nonlinearity. These features make it well suited for use in data acquisition systems.

Functional Block Diagram



Competitive Comparison Plots (continued on page 9)



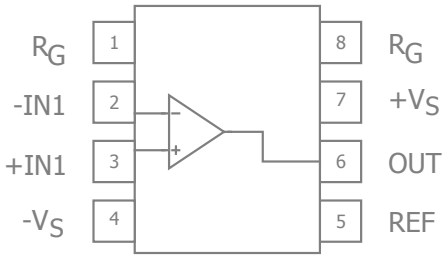
Ordering Information

Part Number	Package	Pb-Free	RoHS Compliant	Operating Temperature Range	Packaging Method
CLC1201ISO8	SOIC-8	Yes	Yes	-40°C to +85°C	Rail
CLC1201ISO8X	SOIC-8	Yes	Yes	-40°C to +85°C	Reel
CLC1201IDP8	DIP-8	Yes	Yes	-40°C to +85°C	Rail

Moisture sensitivity level for all parts is MSL-1.

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Pin Configuration



Pin Assignments

Pin No.	Pin Name	Description
1, 8	R_G	R_G sets gain
2	-IN	Negative input
3	+IN	Positive input
4	$-V_S$	Negative supply
5	REF	Output is referred to the REF pin potential
6	OUT	Output
7	$+V_S$	Positive supply

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Electrical Characteristics

T_A = 25°C, V_S = ±15V, R_L = 2kΩ to GND; unless otherwise noted.

G = 1 + (49.4kΩ / R_G); Total RTI Error = V_{OSI} + (V_{OSO} / G)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Gain						
	Gain Range		1		10,000	
	Gain Error	G = 1, V_{OUT} = ±10V	-0.1		0.1	%
		G = 10, V_{OUT} = ±10V	-0.375		0.375	%
		G = 100, V_{OUT} = ±10V	-0.375		0.375	%
		G = 1,000, V_{OUT} = ±10V	-0.8		0.8	%
	Nonlinearity	G = 1 - 100, V_{OUT} = -10V to 10V, R_L = 10kΩ		10	50	ppm
		G = 1 - 100, V_{OUT} = -10V to 10V, R_L = 2kΩ		10	95	ppm
	Gain vs. Temperature	G = 1		<10		ppm/°C
		G > 1		<-50		ppm/°C
	Reference Gain Error[2]	V_S = ±16.5	-0.03		0.03	%
Voltage Offset						
V_{OSI}	Input Offset Voltage	V_S = ±4.5 to ±16.5	-125		125	µV
		V_S = ±4.5 to ±16.5, -45°C to +85°C	-225		225	µV
	Average Temperature Coefficient	V_S = ±4.5 to ±16.5		0.1		µV/°C
V_{OSO}	Output Offset Voltage	V_S = ±4.5 to ±16.5, G = 1	-1500	200	1500	µV
		V_S = ±4.5 to ±16.5, -45°C to +85°C	-2000		2000	µV
	Average Temperature Coefficient	V_S = ±4.5 to ±16.5		2.5		µV/°C
PSR	Offset Referred to the Input vs. Supply	G = 1, V_S = ±2.3 to ±18V	80	100		dB
		G = 10, V_S = ±2.3 to ±18V	95	120		dB
		G = 100, V_S = ±2.3 to ±18V	110	140		dB
		G = 1,000, V_S = ±2.3 to ±18V	110	140		dB
Input Current						
I_B	Input Bias Current	V_S = ±16.5	-2	0.5	2	nA
		V_S = ±16.5, -45°C to +85°C	-5		5	nA
	Average Temperature Coefficient	V_S = ±16.5		3		pA/°C
I_{OS}	Input Offset Current	V_S = ±16.5	-1		1	nA
		V_S = ±16.5, -45°C to +85°C	-2		2	nA
Input						
	Input Impedance	Differential		10, 2		GΩ, pF
		Common-Mode		10, 2		GΩ, pF
	Input Voltage Range[3]	V_S = ±4.5, G = 1	$-V_S$ +1.9		$+V_S$ -1.2	V
		V_S = ±16.5, G = 1	$-V_S$ +1.9		$+V_S$ -1.4	V
CMRR	Common Mode Rejection Ratio	G = 1, V_S = ±16.5V	70	90		dB
		G = 10, V_S = ±16.5V	90	110		dB
		G = 100, V_S = ±16.5V	108	130		dB
		G = 1,000, V_S = ±16.5V	108	130		dB
Output						
V_{OUT}	Output Swing	V_S = ±2.3V to ±4.5V	$-V_S$ +1.1		$+V_S$ -1.2	V
		V_S = ±4.5, -45°C to +85°C	$-V_S$ +1.6		$+V_S$ -1.3	V
		V_S = ±18, G = 1	$-V_S$ +1.4		$+V_S$ -1.2	V
		V_S = ±16.5, G = 1,-45°C to +85°C	$-V_S$ +1.5		$+V_S$ -2.3	V
I_{SC}	Short Circuit Current			±20		mA

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Symbol	Parameter	Conditions	Min	Typ	Max	Units
Dynamic Performance						
BW_{-3dB}	Small Signal Bandwidth	G = 1		700		kHz
		G = 10		400		kHz
		G = 100		100		kHz
		G = 1,000		12		kHz
SR	Slew Rate	G = 10, V_S = ±15V	0.6	1.2		V/µs
t_S	Settling Time to 0.01%	G = 1 to 100, 5V step		13		µs
		G = 1,000, 5V step		110		µs
e_{ni}	Input Voltage Noise	1kHz, G = 1,000, V_S = ±15V		6.6	13	nV/√Hz
e_{no}	Output Voltage Noise	1kHz, G = 1, V_S = ±15V		70	100	nV/√Hz
RTI	RTI, 0.1Hz to 10Hz	G = 1		5		μV_{pp}
		G = 10, V_S = ±15V			0.8	μV_{pp}
		G = 100, V_S = ±15V		0.2	0.4	μV_{pp}
	Current Noise	f = 1kHz		100		fA/√Hz
		0.1Hz to 10Hz		10		pA_{pp}
Reference Input						
R_{IN}	Input Impedance			20		kΩ
I_{IN}	Input Current	V_S = ±16.5V		50	60	µA
	Voltage Range	V_S = ±15V	$-V_S$ +1.6		$+V_S$ -1.6	V
	Gain to Output			1 ± 0.0001		
Power Supply						
V_S	Operating Range		±2.3		±18	V
I_S	Supply Current	V_S = ±16.5V		1.3	2.2	mA
		V_S = ±15V, -40°C to +85°C			2.5	mA

Notes:

1. 100% tested at 25°C
2. Nominal reference voltage gain is 1.0
3. Input voltage range = CMV + (G V_{DIFF})/2

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Absolute Maximum Ratings

The safety of the device is not guaranteed when it is operated above the "Absolute Maximum Ratings". The device should not be operated at these "absolute" limits. Adhere to the "Recommended Operating Conditions" for proper device function. The information contained in the Electrical Characteristics tables and Typical Performance plots reflect the operating conditions noted on the tables and plots.

Parameter	Min	Max	Unit
Supply Voltage	0	±18	V
Input Voltage Range	$-V_S$	$+V_S$	V
Differential Input Voltage, G = 1 to 10		25	V
Differential Input Voltage, G > 10		≤ 0.05 (R_G + 800) + 1	V
Load Resistance	0.001		kΩ

Reliability Information

Parameter	Min	Typ	Max	Unit
Junction Temperature			150	°C
Storage Temperature Range	-65		150	°C
Lead Temperature (Soldering, 10s)			260	°C
Package Thermal Resistance				
8-Lead SOIC		100		°C/W
8-Lead DIP		TBD		°C/W

Notes:
Package thermal resistance (θ_{JA}), JDEC standard, multi-layer test boards, still air.

ESD Protection

Product	SOIC-8	DIP-8
Human Body Model (HBM)	1.5kV	TBD
Charged Device Model (CDM)	2kV	TBD

Recommended Operating Conditions

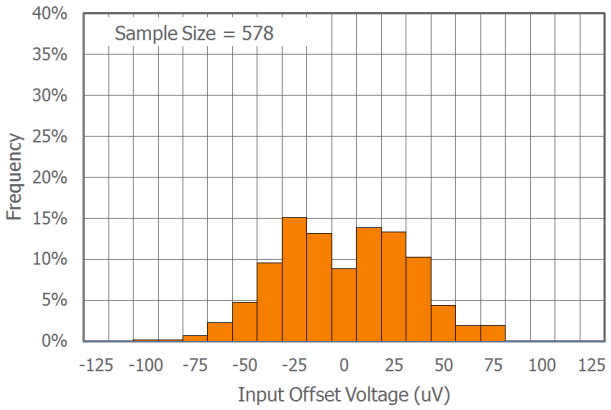
Parameter	Min	Typ	Max	Unit
Operating Temperature Range	-40		+85	°C
Supply Voltage Range	±2.3		±18	V

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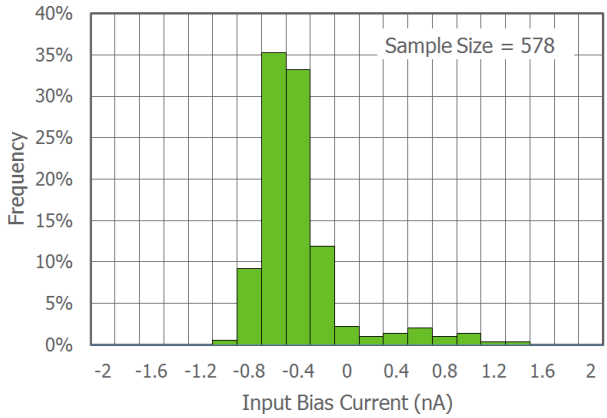
Typical Performance Characteristics

T_A = 25°C, V_S = ±15V, R_L = 2kΩ to GND; unless otherwise noted.

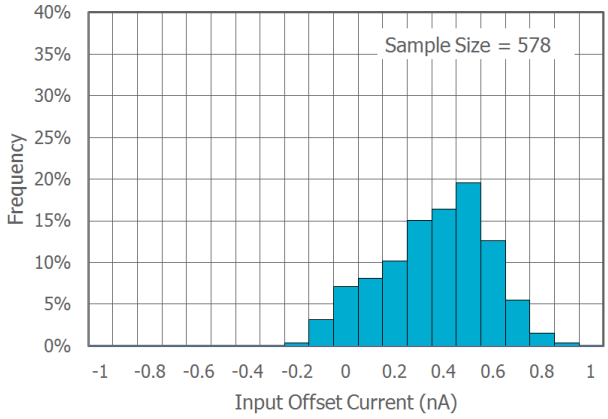
Input Offset Distribution (typical)



Input Bias Current Distribution (typical)



Input Offset Distribution (typical)

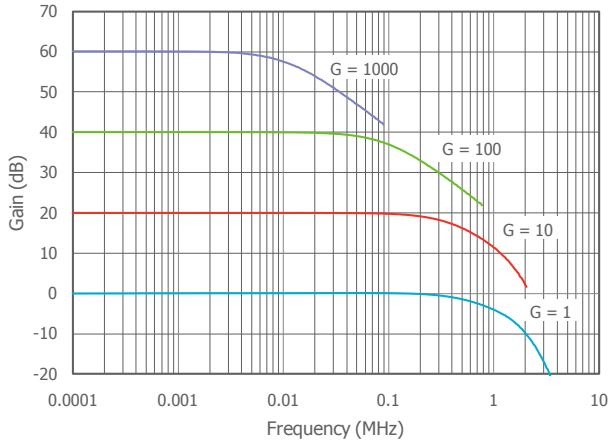


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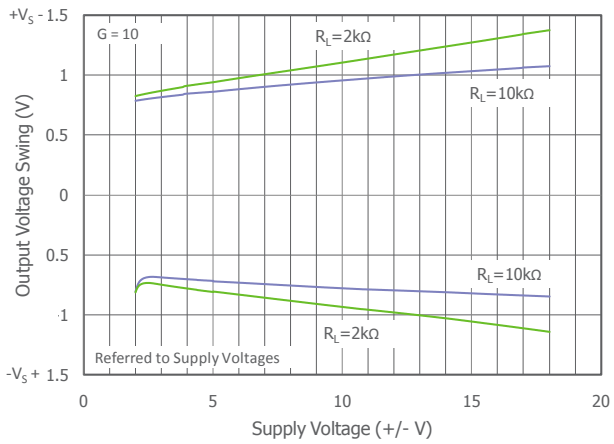
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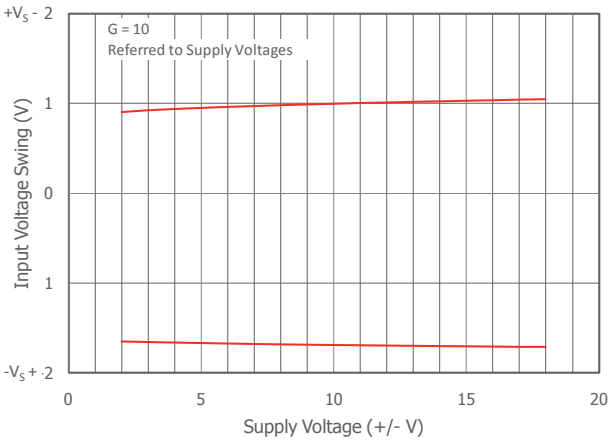
Gain vs. Frequency



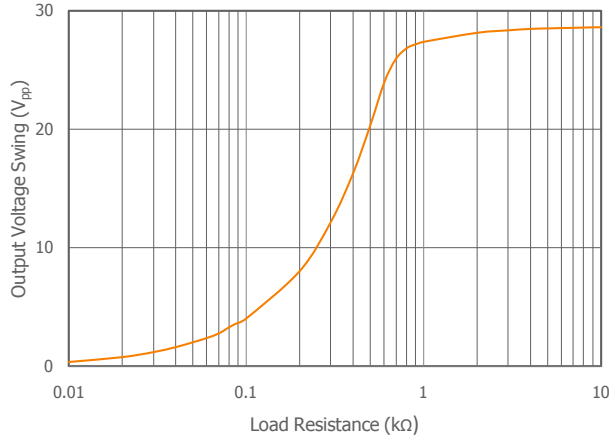
Output Voltage Swing vs. V_S



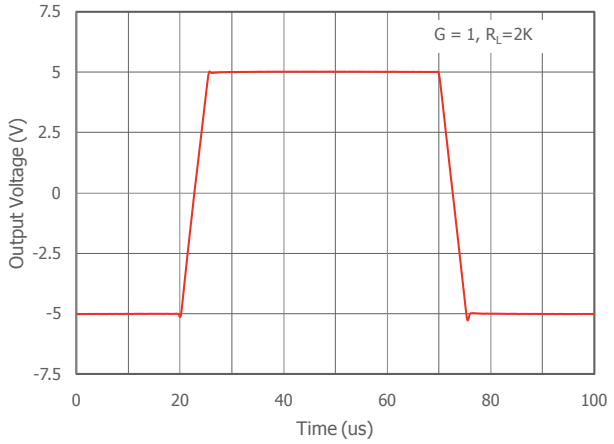
Input Voltage Range vs. V_S



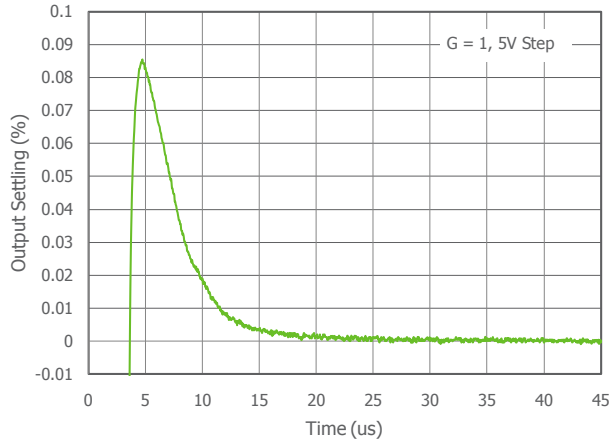
Output Voltage Swing vs. R_L



Large Signal Pulse Response (G = 1)



Large Signal Settling Time (G = 1)

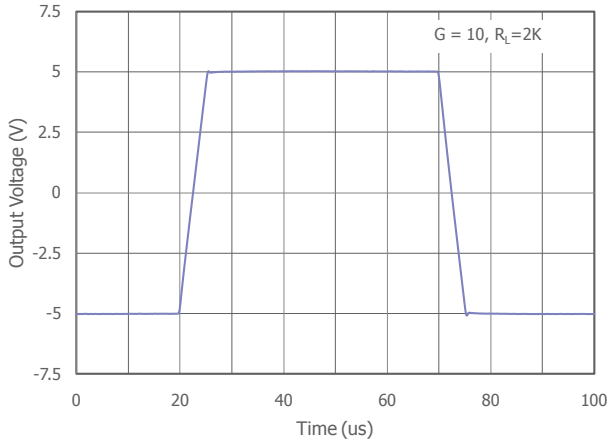


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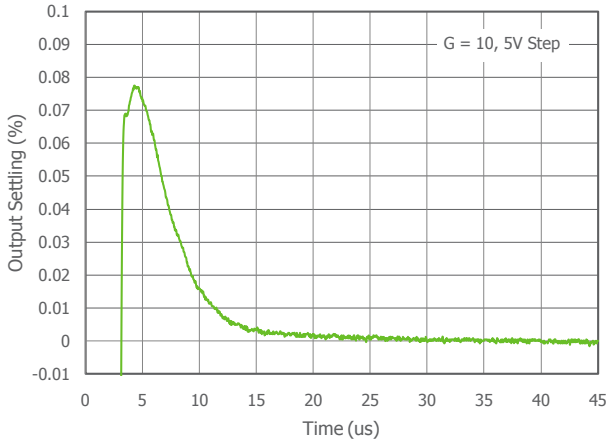
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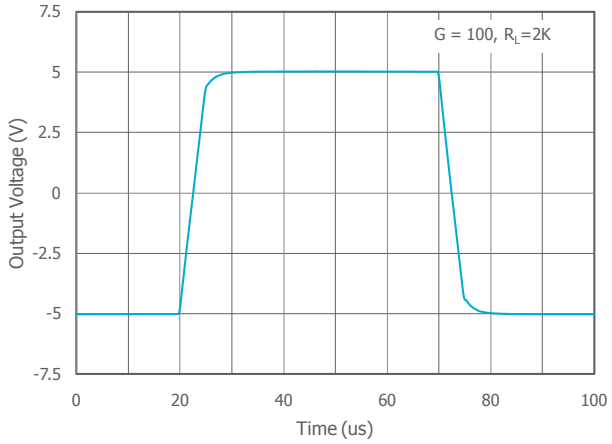
Large Signal Pulse Response (G = 10)



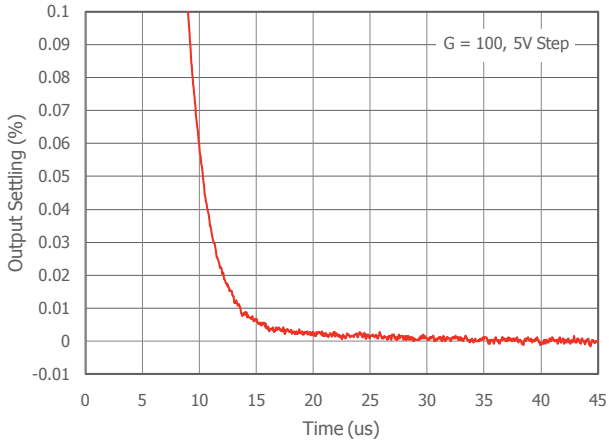
Large Signal Settling Time (G = 10)



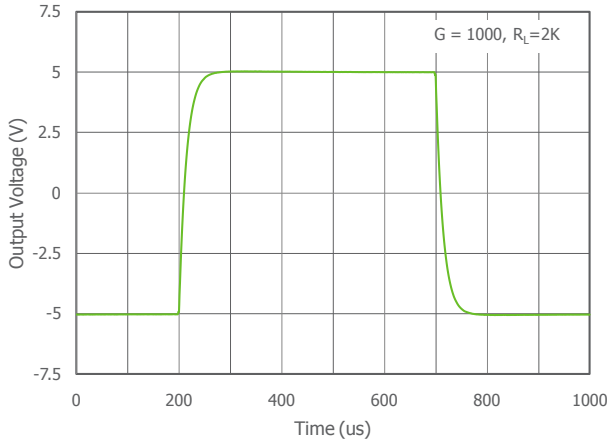
Large Signal Pulse Response (G = 100)



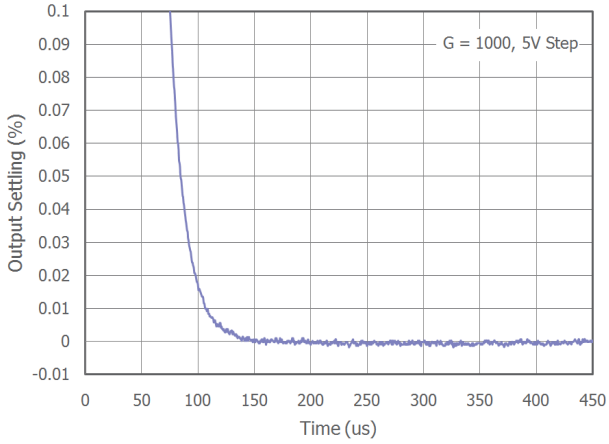
Large Signal Settling Time (G = 100)



Large Signal Pulse Response (G = 1000)



Large Signal Settling Time (G = 1000)

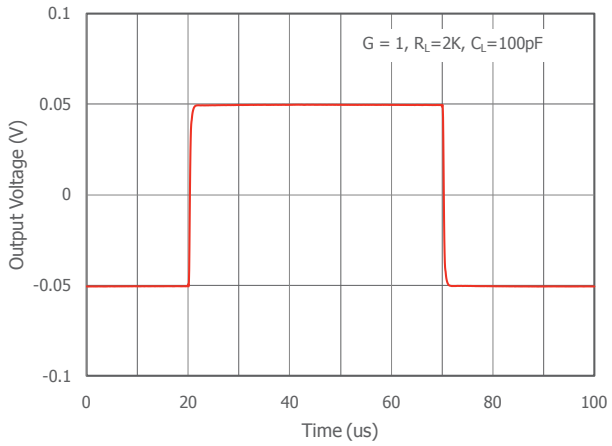


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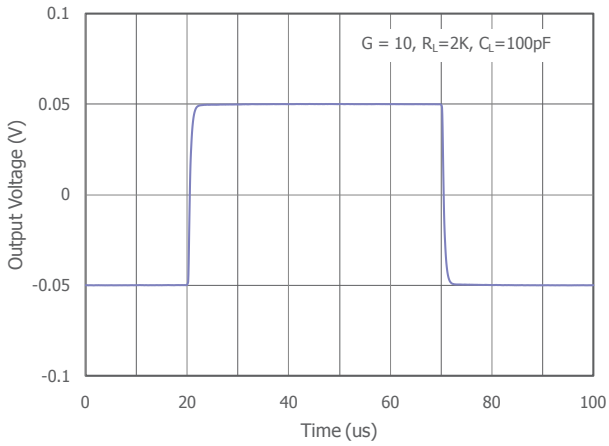
Typical Performance Characteristics

T_A = 25°C, V_S = ±15V, R_L = 2kΩ to GND; unless otherwise noted.

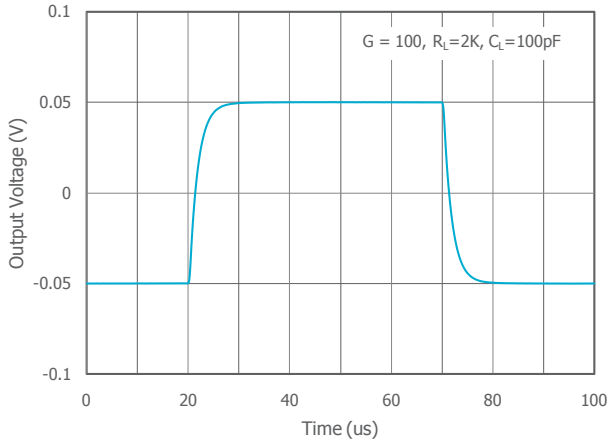
Small Signal Pulse Response (G = 1)



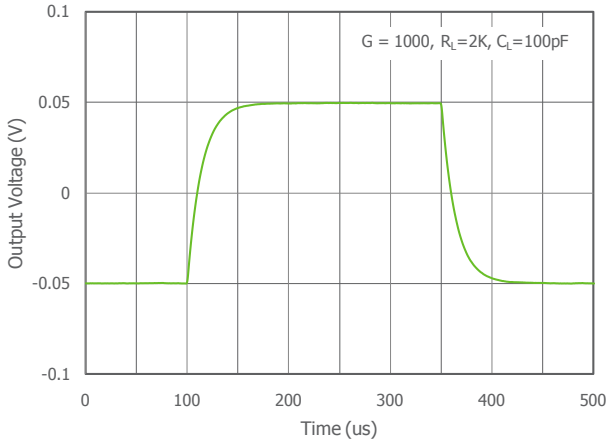
Small Signal Pulse Response (G = 10)



Small Signal Pulse Response (G = 100)



Small Signal Pulse Response (G = 1000)

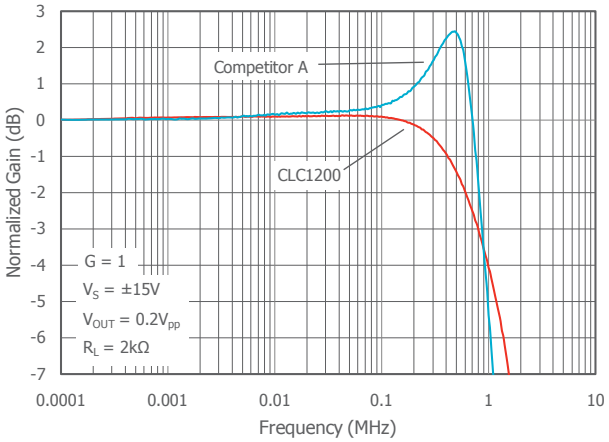


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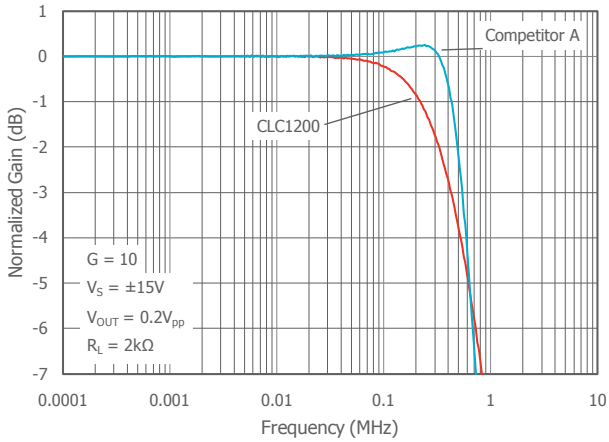
Typical Competitive Comparison Plots

T_A = 25°C, V_S = ±15V, R_L = 2kΩ, CADEKA evaluation board; unless otherwise noted.

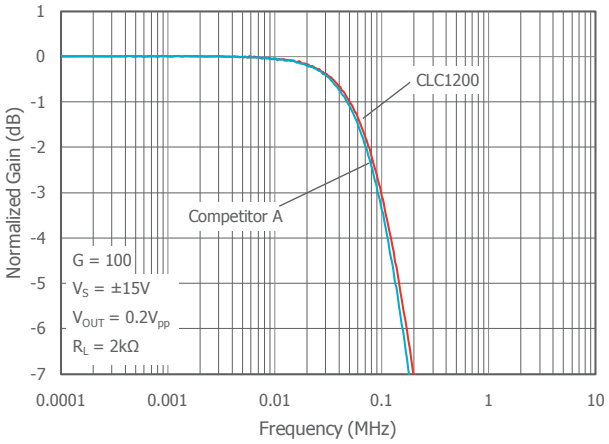
Frequency Response (G = 1)



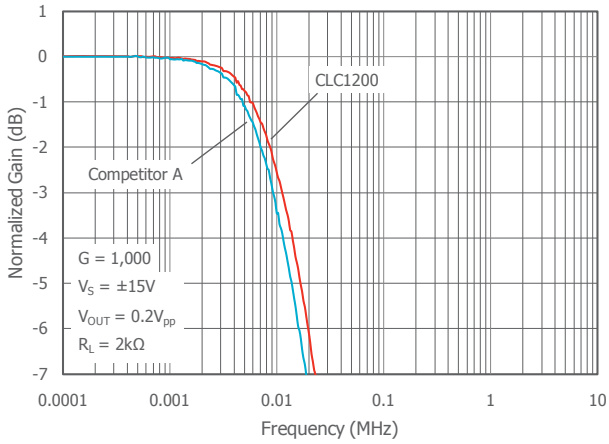
Frequency Response (G = 10)



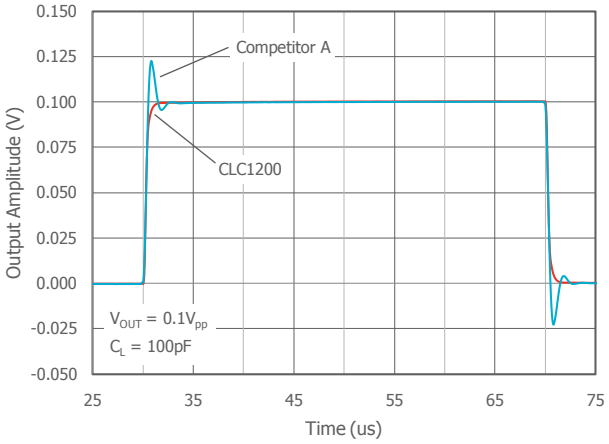
Frequency Response (G = 100)



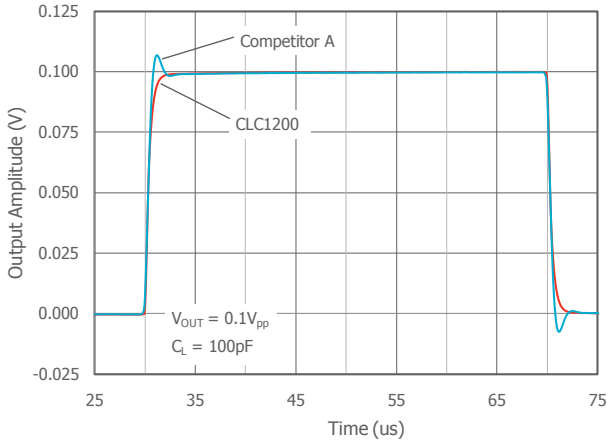
Frequency Response (G = 1,000)



Large Signal Settling Time (G = 1)



Large Signal Settling Time (G = 10)



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Application Information

Basic Operation

The CLC1201 is a monolithic instrumentation amplifier based on the classic three op amp solution, refer to the Functional Block Diagram on page 1. The CLC1201 produces a single-ended output reffered to the REF pin potential.

The internal resistors are trimmed which allows the gain to be accurately adjusted with one external resistor R_G.

$$G = \frac{49.4k}{R_G} + 1; \quad R_G = \frac{49.4k}{G - 1}$$

R_G also determines the transconductance of the preamp stage. As R_G is reduced for larger gains, the transconductance increases to that of the input transistors. Producing the following advantages:

- Open-loop gain increases as the gain is increased, reducing gain releated errors
- Gain-bandwidth increases as the gain is increased, optimizing frequency response
- Reduced input voltage noise which is determined by the collector current and base resistance of the input devices

Gain Selection

The impeadance between pins 1 and 8, R_G, sets the gain of the CLC1201. Table 1 shows the required standard table values of R_G for various calculated gains. For G = 1, $R_G = \infty$.

1% R_G (Ω)	Caclulated Gain	0.1% R_G (Ω)	Calculated Gain
49.9k	1.990	49.3k	2.002
12.4k	4.984	12.4k	4.984
5.49k	9.998	5.49k	9.998
2.61k	19.93	2.61k	19.93
1.00k	50.40	1.01k	49.91
499	100.0	499	100.0
249	199.4	249	199.4
100	495.0	98.8	501.0
49.9	991.0	49.3	1,003.0

Table 1: Recommended R_G Values

Follow these guidelines for improved performance:

- To maintain gain accuracy, use 0.1% to 1% resistors
- To minimize gain error, avoid high parasitic resistance in series with R_G
- To minimize gain drift, use low TC resistors (<10ppm/°C)

Common Mode Rejection

The CLC1201 offers high CMRR. To acheive optimal CMRR performance:

- Connect the reference terminal (pin 5) to a low impedance source
- Minimize capacitive and resistive differences between the inputs

In many applications, shielded cables are used to minimize noise. Properly drive the shield for best CMRR performance over frequency. Figures 1 and 2 show active data guards that are configured to improve AC common-mode rejections. the capacitances of input cable shields are "bootstrapped" to minimize the capacitance mismatch between the inputs.

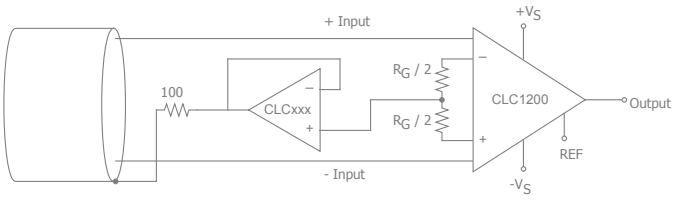


Figure 1: Common-mode Shield Driver

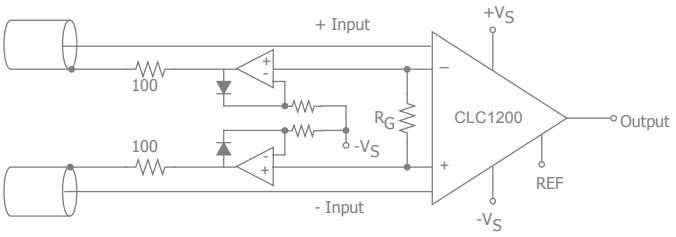


Figure 2: Differential Shield Driver

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Pressure Measurement Applications

The CLC1201 is especially suitable for higher resistance pressure sensors powered at lower voltages where small size and low power become more significant.

Figure 3 shows a 3kΩ pressure transducer bridge powered from 5V. In such a circuit, the bridge consumes only 1.7mA. Adding the CLC1201 and a buffered voltage divider allows the signal to be conditioned for only 3.8mA of total supply current.

Small size and low cost make the CLC1201 especially attractive for voltage output pressure transducers. Since it delivers low noise and drift, it will also serve applications such as diagnostic noninvasive blood pressure measurement.

Medical ECG

The CLC1201 is perfect for ECG monitors because of its low current noise. A typical applicaiton is shown in Figure 4. The CLC1201's low power, low supply voltage requirements, and space-saving 8-lead SOIC package offerings make it an excellent choice for battery-powered data recorders.

Furthermore, the low bias currents and low current noise, coupled with the low voltage noise of the CLC1201, improve the dynamic range for better performance.

The value of capacitor C1 is chosen to maintain stability of the right leg drive loop. Proper safeguards, such as isolation, must be added to this circuit to protect the patient from possible harm.

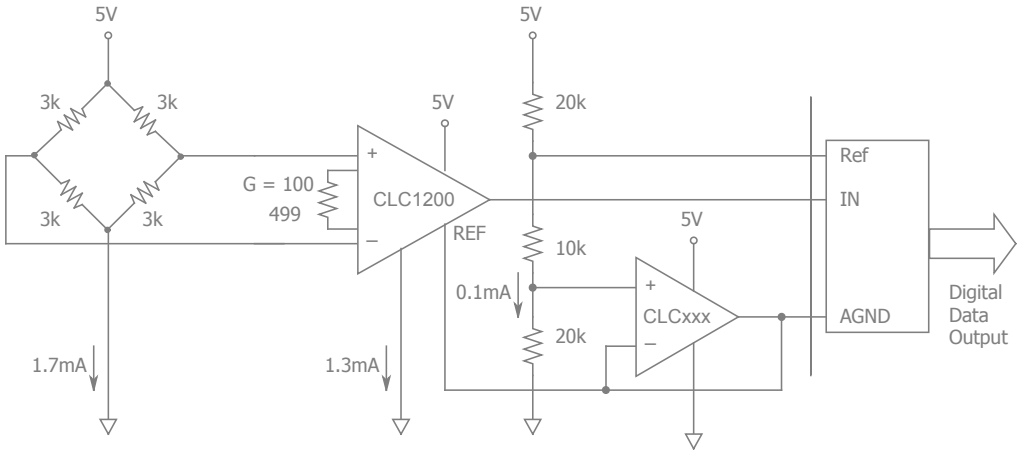


Figure 3: Pressure Monitoring Circuits Operating on a Single 5V Supply

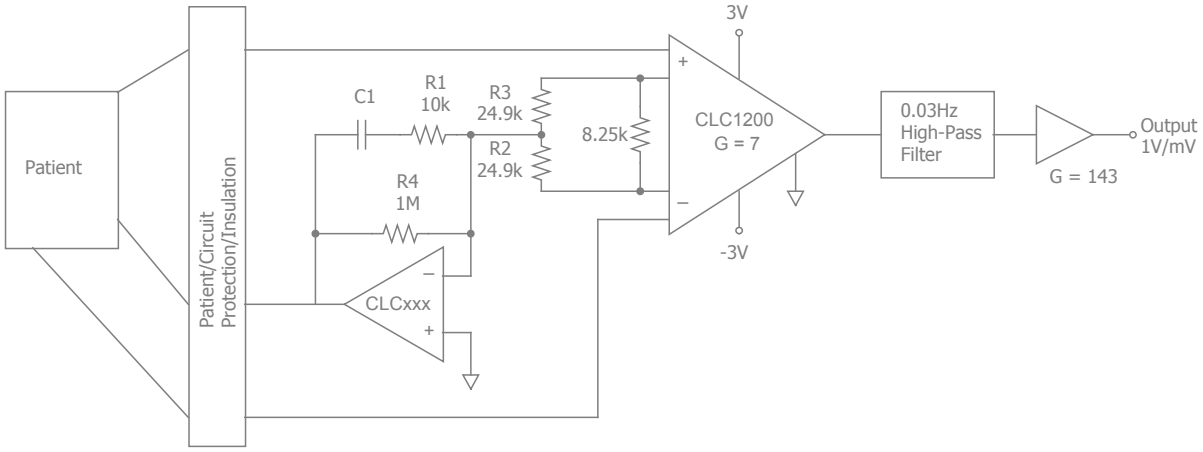


Figure 4: Typical Circuit for ECG Monitor Applications

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Grounding

The output voltage of the CLC1201 is developed with respect to the potential on the reference terminal (pin 8). Simply tie the REF pin to the appropriate "local ground" to resolve many grounding problems.

To isolate low level analog signals from a noisy digital environment, many data-aquisistion components have separate analog and digital ground pins. Use separate ground lines (analog and digital) to minimize current flow from sensitive areas to system ground. These ground returns must be tied together at some point, usually best at the ADC.

Layout Considerations

General layout and supply bypassing play major roles in high frequency performance. CADEKA has evaluation boards to use as a guide for high frequency layout and as an aid in device testing and characterization. Follow the steps below as a basis for high frequency layout:

- Include 6.8µF and 0.1µF ceramic capacitors for power supply decoupling
- Place the 6.8µF capacitor within 0.75 inches of the power pin
- Place the 0.1µF capacitor within 0.1 inches of the power pin
- Remove the ground plane under and around the part, especially near the input and output pins to reduce parasitic capacitance
- Minimize all trace lengths to reduce series inductances

Refer to the evaluation board layouts below for more information.

Evaluation Board Information

The following evaluation boards are available to aid in the testing and layout of these devices:

Evaluation Board	Products
CEB024	CLC1201 in SOIC-8

Evaluation Board Schematics

Evaluation board schematics and layouts are shown in Figures 5-7. These evaluation boards are built for dual-supply operation. Follow these steps to use the board in a single-supply application:

1. Short -Vs to ground.
2. Use C3 and C4, if the $-V_S$ pin of the amplifier is not directly connected to the ground plane.

Figure 5. CEB00x Schematic

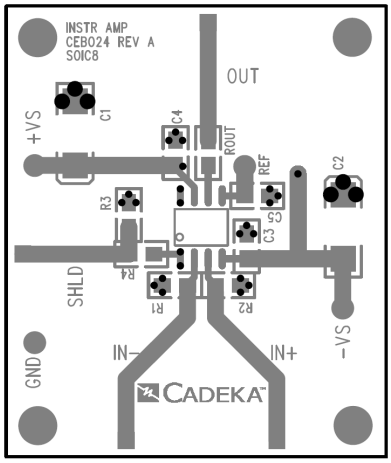


Figure 6. CEB024 Top View

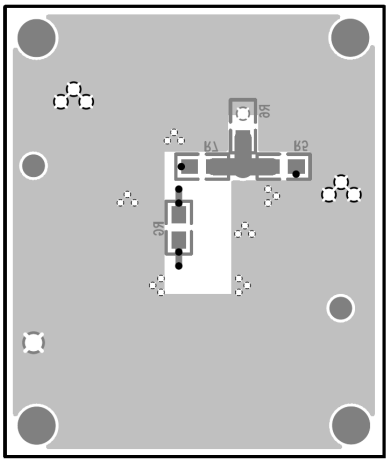


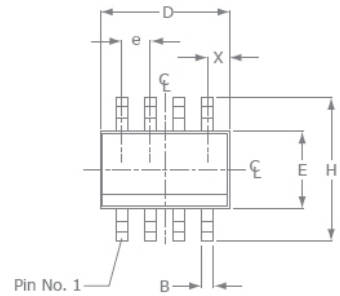
Figure 7. CEB024 Bottom View

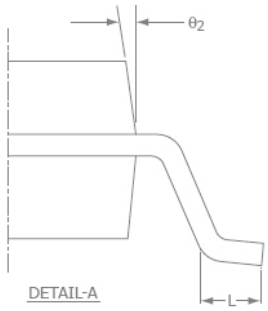
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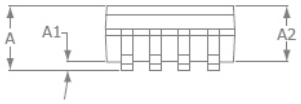
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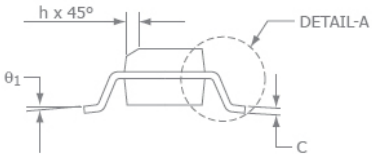
Mechanical Dimensions

SOIC-8 Package









SOIC-8		
SYMBOL	MIN	MAX
A1	0.10	0.25
B	0.36	0.48
C	0.19	0.25
D	4.80	4.98
E	3.81	3.99
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.5
L	0.41	1.27
A	1.37	1.73
θ_1	0°	8°
X	0.55 ref	
θ_2	7° BSC	

NOTE:

1. All dimensions are in millimeters.
2. Lead coplanarity should be 0 to 0.1mm (0.004") max.
3. Package surface finishing: VDI 24~27
4. All dimension excluding mold flashes.
5. The lead width, B to be determined at 0.1905mm from the lead tip.

For additional information regarding our products, please visit CADEKA at: cadeka.com

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