TOSHIBA Bi-CMOS Integrated Circuit Silicon Monolithic

TB62777FNG, TB62777FG

8-Channel Constant-Current LED Driver of the 3.3-V and 5-V Power Supply Voltage Operation

The TB62777FNG/FG is comprised of constant-current drivers designed for LEDs and LED panel displays.

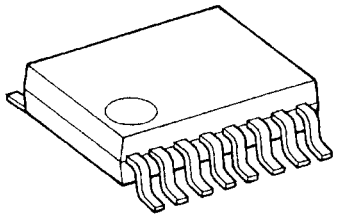
The regulated current sources are designed to provide a constant current, which is adjustable through one external resistor.

The TB62777FNG/FG incorporates eight channels of shift registers, latches, AND gates and constant-current outputs.

Fabricated using the Bi-CMOS process, the TB62777FNG/FG is capable of high-speed data transfers.

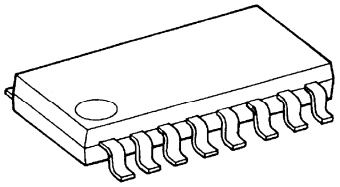
The TB62777FNG/FG is RoHS.

TB62777FNG



SSOP16-P-225-0.65B

TB62777FG



SSOP16-P-225-1.00A

Weight: SSOP16-P-225-0.65B 0.07 g (typ.)
SSOP16-P-225-1.00A 0.14 g (typ.)

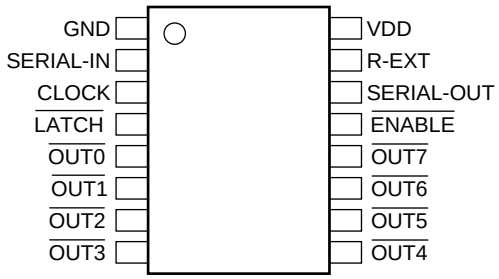
Features

- Power supply voltages: V_{DD} = 3.3 V/5 V
- Output drive capability and output count: 50 mA × 8 channels
- Constant-current output range: 5 to 40 mA
- Voltage applied to constant-current output terminals: 0.4 V (min, I_{OUT} = 5 to 40 mA)
- Designed for common-anode LEDs
- Thermal shutdown (TSD) (min: 150℃)
- Power on reset (POR)
- Logical input signal voltage level: 3.3-V and 5-V CMOS interfaces (Schmitt trigger input)
- Maximum output voltage: 25V
- Serial data transfer rate: 25 MHz (max) @cascade connection
- Operating temperature range: T_{opr} = −40 to 85°C
- Package: SSOP16-P-225-0.65B/ SSOP16-P-225-1.00A
- Constant-current accuracy

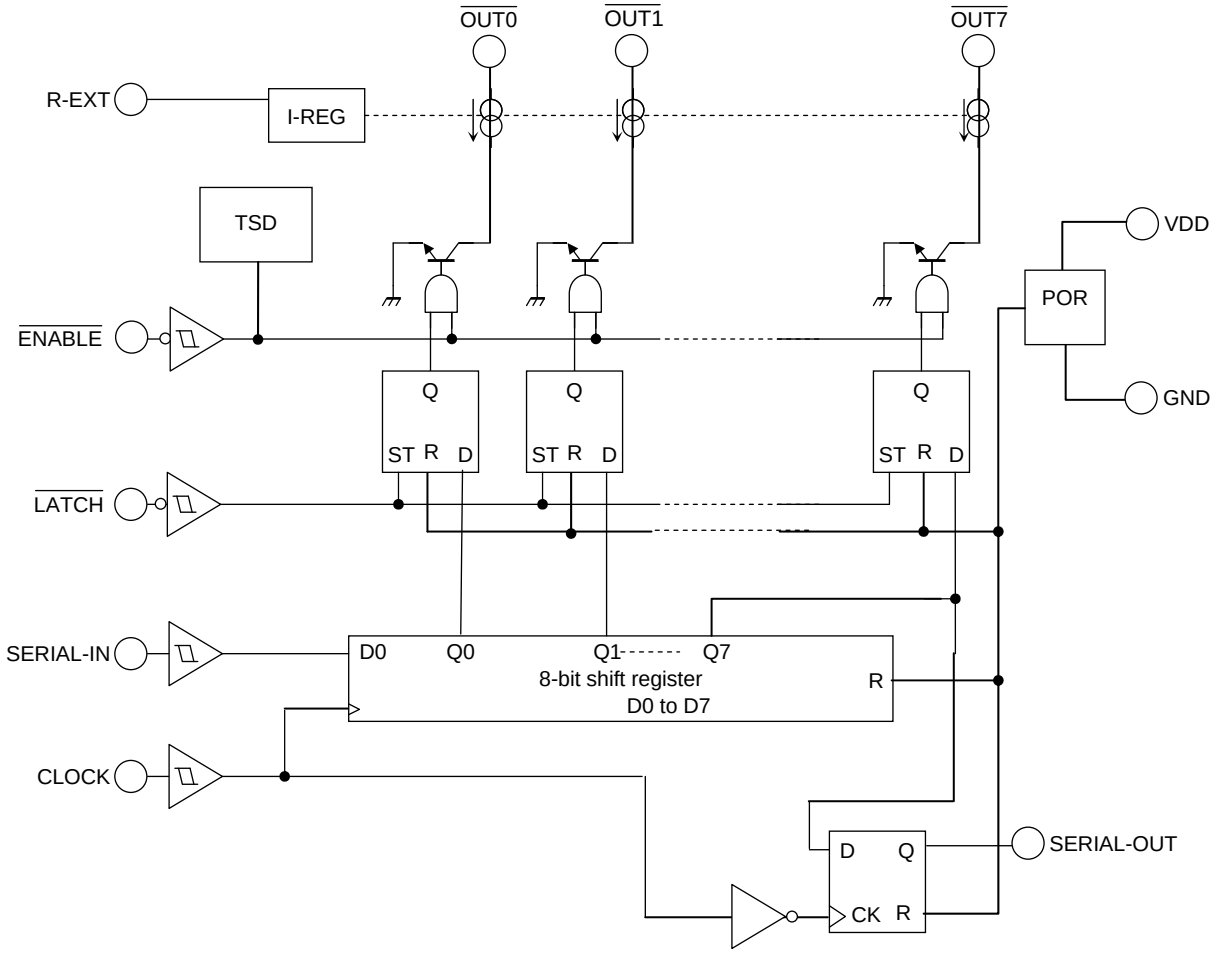
Output Voltage	Current accuracy Between Channels	Current Accuracy Between ICs	Output Current
0.4 V to 4 V	±3%	±6%	15 mA

Marktech Optoelectronics
For part availability and ordering information please call Toll Free: 800.984.5337
Website: www.marktechopto.com | Email: info@marktechopto.com

Pin Assignment (top view)



Block Diagram

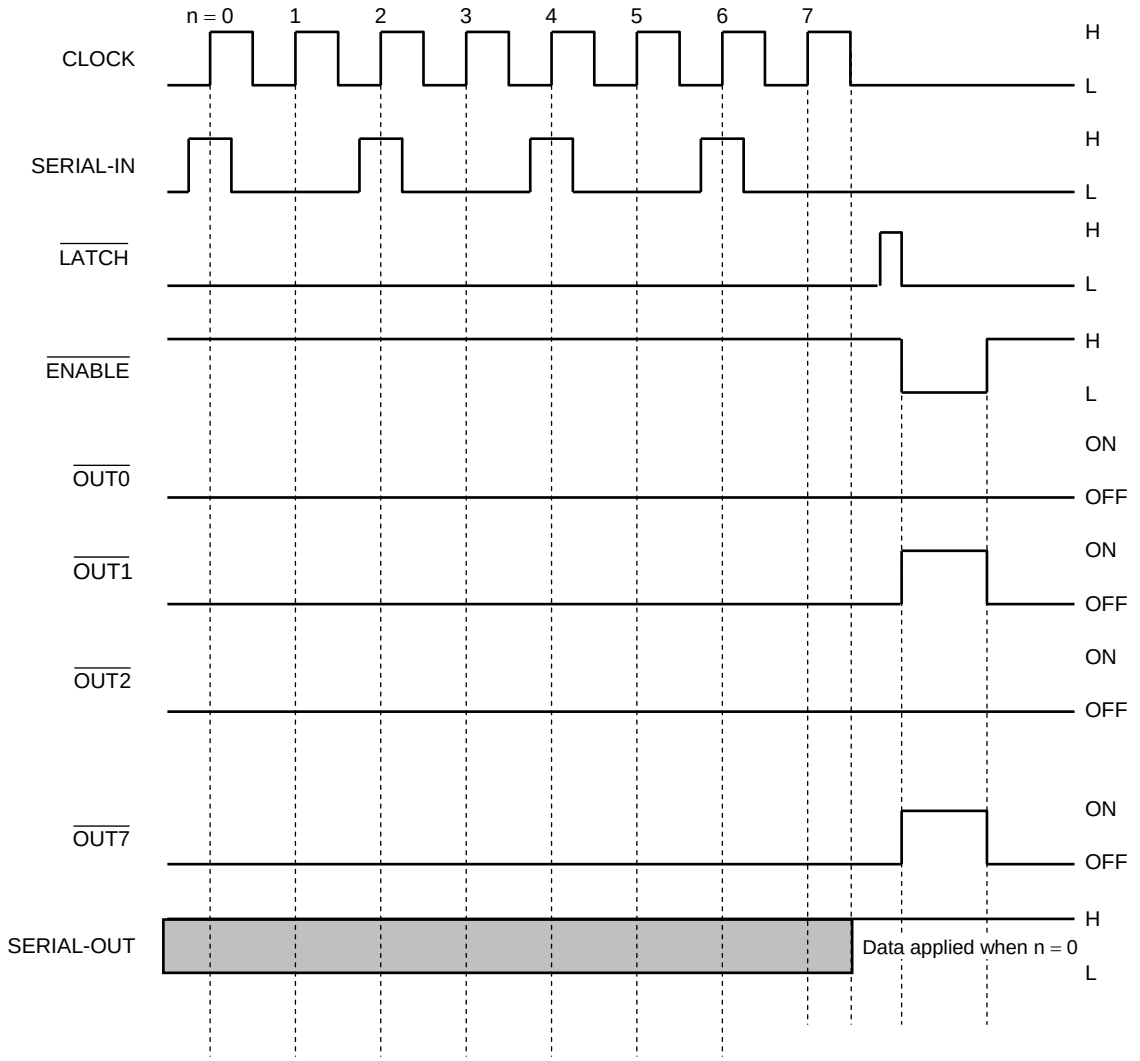


Truth Table

CLOCK	$\overline{\text{LATCH}}$	$\overline{\text{ENABLE}}$	SERIAL-IN	$\overline{\text{OUT0}}$ … $\overline{\text{OUT5}}$ … $\overline{\text{OUT7}}$	SERIAL-OUT
↑	H	L	Dn	Dn … Dn – 5 … Dn – 7	No change
↑	L	L	Dn + 1	No Change	No change
↑	H	L	Dn + 2	Dn + 2 … Dn – 3 … Dn – 5	No change
↑	X	H	Dn + 3	OFF	No change
↓	X	H	Dn + 3	OFF	Dn −4

Note 1: $\overline{\text{OUT0}}$ to $\overline{\text{OUT7}}$ = On when Dn = H; $\overline{\text{OUT0}}$ to $\overline{\text{OUT7}}$ = Off when Dn = L.

Timing Diagram



Note 1: Latches are level-sensitive, not edge-triggered.

Note 2: The TB62777FNG can be used at 3.3 V or 5.0 V. However, the V_{DD} supply voltage must be equal to the input voltage.

Note 3: Serial data is shifted out of SERIAL-OUT on the falling edge of CLOCK.

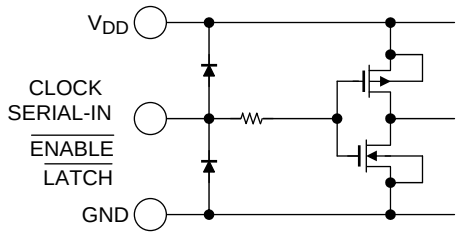
Marks: The latches hold data while the $\overline{\text{LATCH}}$ terminal is held Low. When the $\overline{\text{LATCH}}$ terminal is High, the latches do not hold data and pass it transparently. When the $\overline{\text{ENABLE}}$ terminal is Low, $\overline{\text{OUT0}}$ to $\overline{\text{OUT7}}$ toggle between ON and OFF according to the data. When the $\overline{\text{ENABLE}}$ terminal is High, $\overline{\text{OUT0}}$ to $\overline{\text{OUT7}}$ are forced OFF.

Terminal Description

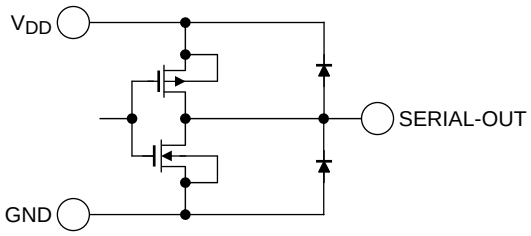
Pin No.	Pin Name	Function
1	GND	GND terminal
2	SERIAL-IN	Serial data input terminal
3	CLOCK	Serial clock input terminal
4	$\overline{\text{LATCH}}$	Latch input terminal
5	$\overline{\text{OUT0}}$	Constant-current output terminal (Open collector)
6	$\overline{\text{OUT1}}$	Constant-current output terminal (Open collector)
7	$\overline{\text{OUT2}}$	Constant-current output terminal (Open collector)
8	$\overline{\text{OUT3}}$	Constant-current output terminal (Open collector)
9	$\overline{\text{OUT4}}$	Constant-current output terminal (Open collector)
10	$\overline{\text{OUT5}}$	Constant-current output terminal (Open collector)
11	$\overline{\text{OUT6}}$	Constant-current output terminal (Open collector)
12	$\overline{\text{OUT7}}$	Constant-current output terminal (Open collector)
13	$\overline{\text{ENABLE}}$	Output enable input terminal All outputs ($\overline{\text{OUT0}}$ to $\overline{\text{OUT7}}$) are disabled when the $\overline{\text{ENABLE}}$ terminal is driven High, and enabled when it is driven Low.
14	SERIAL-OUT	Serial data output terminal. Serial data is clocked out on the falling edge of CLOCK.
15	R-EXT	An external resistor is connected between this terminal and ground. $\overline{\text{OUT0}}$ to $\overline{\text{OUT7}}$ are adjusted to the same current value.
16	V_{DD}	Power supply terminal

Equivalent Circuits for Inputs and Outputs

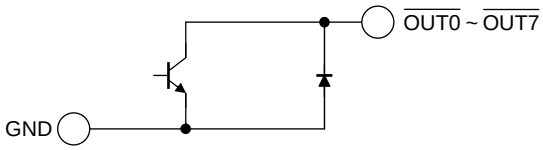
CLOCK, SERIAL-IN, $\overline{\text{ENABLE}}$, $\overline{\text{LATCH}}$ Terminals



SERIAL-OUT Terminal



$\overline{\text{OUT0}}$ to $\overline{\text{OUT7}}$ Constant-current Output Terminals



Absolute Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{DD}	6.0	V
Input voltage	V_{IN}	−0.3 to V_{DD} + 0.3 (Note 1)	V
Output current	I_{OUT}	55	mA/ch
Output voltage	V_{OUT}	−0.3 to 25	V
Power dissipation	P_d	1.19(FG TYPE) / 1.02(FNG TYPE) (Notes 2 and 3)	W
Thermal resistance	$R_{th\ (j\text{-}a)}$	105(FG TYPE) / 122(FNG TYPE) (Note 2)	°C/W
Operating temperature range	T_{opr}	−40 to 85	°C
Storage temperature range	T_{stg}	−55 to 150	°C
Maximum junction temperature	T_j	150	°C

Note 1: However, do not exceed 6.0 V.

Note 2: When mounted on a PCB (76.2 × 114.3 × 1.6 mm; Cu = 30%; 35-μm-thick; SEMI-compliant)

Note 3: Power dissipation is reduced by $1/R_{th\ (j\text{-}a)}$ for each °C above 25°C ambient.

Operating Ranges (unless otherwise specified, Ta = –40°C to 85°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Supply voltage	V_{DD}	—	3	—	5.5	V
Output voltage	V_{OUT}	$\overline{OUT0}$ to $\overline{OUT7}$	0.4	—	4	V
Output current	I_{OUT}	$\overline{OUT0}$ to $\overline{OUT7}$	5	—	40	mA/ch
	I_{OH}	SERIAL-OUT	—	—	–5	mA
	I_{OL}	SERIAL-OUT	—	—	5	
Input voltage	V_{IH}	SERIAL-IN/CLOCK/ $\overline{LATCH}$ / $\overline{ENABLE}$	0.7 × V_{DD}	—	V_{DD}	V
	V_{IL}		GND	—	0.3 × V_{DD}	
Clock frequency	f_{CLK}	Cascade connection	—	—	25	MHz
$\overline{LATCH}$ pulse width	t_{wLAT}	(Note 2)	20	—	—	ns
CLOCK pulse width	t_{wCLK}	(Note 2)	20	—	—	
$\overline{ENABLE}$ pulse width	t_{wENA}	$I_{OUT} \geq$ 20 mA (Note 2)	2	—	—	μs
		5 mA ≤ I_{OUT} ≤ 20 mA (Note 2)	3	—	—	
Setup time	t_{SETUP1}	(Note 2)	5	—	—	ns
	t_{SETUP2}		5	—	—	
Hold time	t_{HOLD1}		5	—	—	
	t_{HOLD2}		5	—	—	
Maximum clock rise time	t_r	Single operation (Notes 1 and 2)	—	—	5	μs
Maximum clock fall time	t_f		—	—	5	

Note 1: For cascade operation, the CLOCK waveform might become ambiguous, causing the t_r and t_f values to be large. Then it may not be possible to meet the timing requirement for data transfer. Please consider the timing carefully.

Note 2: Please see the timing waveform on page 9.

Electrical Characteristics (Unless otherwise specified, Ta = 25°C, V_{DD} = 4.5 to 5.5 V)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output current	I_{OUT1}	5	V_{OUT} = 0.4 V, R-EXT = 1.2 kΩ V_{DD} = 5 V,	—	15	—	mA
Output current error between ICs	ΔI_{OUT1}	5	V_{OUT} = 0.4 V, R-EXT = 1.2 kΩ All channels ON V_{DD} = 5 V,	—	±3	±6	%
Output current error between channels	ΔI_{OUT2}	5	V_{OUT} = 0.4 V, R-EXT = 1.2 kΩ All channels ON V_{DD} = 5 V	—	±1	±3	%
Output leakage current	I_{OZ}	5	V_{OUT} = 25 V	—	—	1	μA
Input voltage	V_{IH}	—	SERIAL-IN/CLOCK/ $\overline{\text{LATCH}}$ / $\overline{\text{ENABLE}}$	0.7 × V_{DD}	—	V_{DD}	V
	V_{IL}	—	SERIAL-IN/CLOCK/ $\overline{\text{LATCH}}$ / $\overline{\text{ENABLE}}$	GND	—	0.3 × V_{DD}	
Input current	I_{IH}	2	V_{IN} = V_{DD} CLOCK/SERIAL-IN / $\overline{\text{LATCH}}$ / $\overline{\text{ENABLE}}$	—	—	1	μA
	I_{IL}	3	V_{IN} = GND CLOCK/SERIAL-IN/ $\overline{\text{LATCH}}$ / $\overline{\text{ENABLE}}$	—	—	−1	
SERIAL-OUT output voltage	V_{OL}	1	I_{OL} = 5.0 mA, V_{DD} = 5 V	—	—	0.3	V
	V_{OH}	1	I_{OH} = −5.0 mA, V_{DD} = 5 V	4.7	—	—	
Changes in constant output current dependent on V_{DD}	%/V_{DD}	5	V_{DD} = 3 V to 5.5 V	—	1	2	%
Supply current	$I_{DD\ (OFF)\ 1}$	4	R-EXT = OPEN, V_{OUT} = 25.0 V	—	—	1	mA
	$I_{DD\ (OFF)\ 2}$	4	R-EXT = 1.2 kΩ, V_{OUT} = 25.0 V, All channels OFF	—	—	5	
	$I_{DD\ (ON)}$	4	R-EXT = 1.2 kΩ, V_{OUT} = 0.4 V, All channels ON	—	—	9	

Switching Characteristics (Unless otherwise specified, Ta = 25°C, V_{DD} = 4.5 to 5.5V)

Characteristics	Symbol	Test Circuit	Test Condition (Note 1)	Min	Typ.	Max	Unit
Propagation delay time	t_{pLH1}	6	CLK- $\overline{\text{OUTn}}$, $\overline{\text{LATCH}}$ = "H", $\overline{\text{ENABLE}}$ = "L"	—	20	300	ns
	t_{pLH2}	6	$\overline{\text{LATCH}}$ – $\overline{\text{OUTn}}$, $\overline{\text{ENABLE}}$ = "L"	—	20	300	
	t_{pLH3}	6	$\overline{\text{ENABLE}}$ – $\overline{\text{OUTn}}$, $\overline{\text{LATCH}}$ = "H"	—	20	300	
	t_{pLH}	6	CLK-SERIAL OUT	2	10	14	
	t_{pHL1}	6	CLK- $\overline{\text{OUTn}}$, $\overline{\text{LATCH}}$ = "H", $\overline{\text{ENABLE}}$ = "L"	—	30	340	
	t_{pHL2}	6	$\overline{\text{LATCH}}$ – $\overline{\text{OUTn}}$, $\overline{\text{ENABLE}}$ = "L"	—	70	340	
	t_{pHL3}	6	$\overline{\text{ENABLE}}$ – $\overline{\text{OUTn}}$, $\overline{\text{LATCH}}$ = "H"	—	70	340	
	t_{pHL}	6	CLK-SERIAL OUT	2	10	14	
Output rise time	t_{or}	6	10% to 90% points of $\overline{\text{OUT0}}$ to $\overline{\text{OUT7}}$ voltage waveforms	—	20	150	
Output fall time	t_{of}	6	90% to 10% points of $\overline{\text{OUT0}}$ to $\overline{\text{OUT7}}$ voltage waveforms	—	125.	300	

Note 1: T_{opr} = 25°C, V_{DD} = V_{IH} = 5 V, V_{IL} = 0 V, R_{EXT} = 1.2 kΩ, I_{OUT} = 15 mA, V_L = 5.0 V,
C_L = 10.5 pF (see test circuit 6.)

Electrical Characteristics (Unless otherwise specified, Ta = 25°C, V_{DD} = 3 to 3.6 V)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output current	I_{OUT1}	5	V_{OUT} = 0.4 V, R-EXT = 1.2 kΩ V_{DD} = 3.3 V	—	15	—	mA
Output current error between ICs	ΔI_{OUT1}	5	V_{OUT} = 0.4 V, R-EXT = 1.2 kΩ All channels ON V_{DD} = 3.3 V	—	±3	±6	%
Output current error between channels	ΔI_{OUT2}	5	V_{OUT} = 0.4 V, R-EXT = 1.2 kΩ All channels ON V_{DD} = 3.3 V	—	±1	±3	%
Output leakage current	I_{OZ}	5	V_{OUT} = 25 V	—	—	1	μA
Input voltage	V_{IH}	—	SERIAL-IN/CLOCK/ $\overline{\text{LATCH}}$ / $\overline{\text{ENABLE}}$	0.7 × V_{DD}	—	V_{DD}	V
	V_{IL}	—	SERIAL-IN/CLOCK/ $\overline{\text{LATCH}}$ / $\overline{\text{ENABLE}}$	GND	—	0.3 × V_{DD}	
Input current	I_{IH}	2	V_{IN} = VDD CLOCK/SERIAL-IN/ $\overline{\text{LATCH}}$ / $\overline{\text{ENABLE}}$	—	—	1	μA
	I_{IL}	3	V_{IN} = GND CLOCK/SERIAL-IN/ $\overline{\text{LATCH}}$ / $\overline{\text{ENABLE}}$	—	—	−1	
SERIAL-OUT output voltage	V_{OL}	1	I_{OL} = 5.0 mA, V_{DD} = 3.3 V	—	—	0.3	V
	V_{OH}	1	I_{OH} = −5.0 mA, V_{DD} = 3.3 V	3.0	—	—	
Changes in constant output current dependent on V_{DD}	%/V_{DD}	5	V_{DD} = 3 V to 5.5 V	—	1	2	%
Supply current	$I_{DD\ (OFF)\ 1}$	4	R-EXT = OPEN, V_{OUT} = 25.0 V	—	—	1	mA
	$I_{DD\ (OFF)\ 2}$	4	R-EXT = 1.2 kΩ, V_{OUT} = 25.0 V, All channels OFF	—	—	5	
	$I_{DD\ (ON)}$	4	R-EXT = 1.2 kΩ, V_{OUT} = 0.4 V, All channels ON	—	—	9	

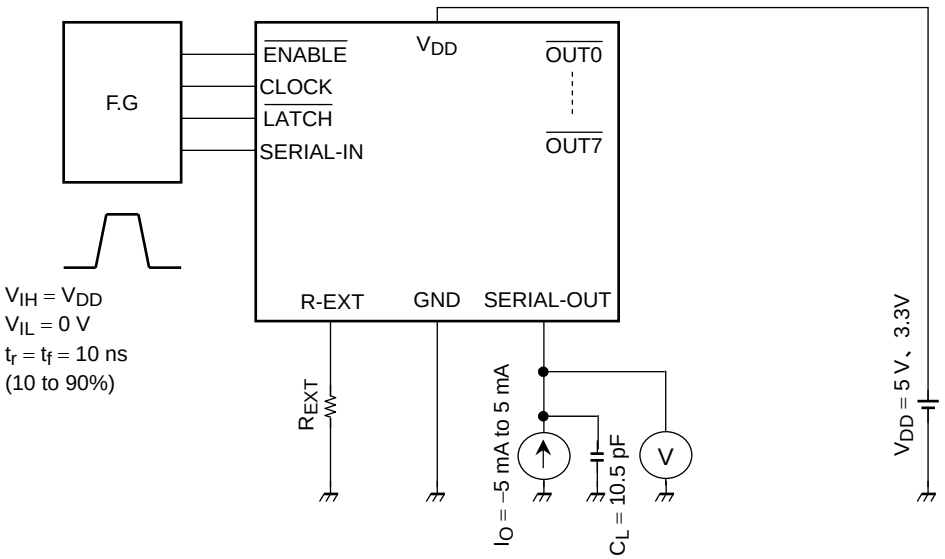
Switching Characteristics (Unless otherwise specified, Ta = 25°C, V_{DD} = 3 to 3.6 V)

Characteristics	Symbol	Test Circuit	Test Condition (Note 1)	Min	Typ.	Max	Unit
Propagation delay time	t_{pLH1}	6	CLK- $\overline{\text{OUTn}}$, $\overline{\text{LATCH}}$ = "H", $\overline{\text{ENABLE}}$ = "L"	—	—	300	ns
	t_{pLH2}	6	$\overline{\text{LATCH}}$ - $\overline{\text{OUTn}}$, $\overline{\text{ENABLE}}$ = "L"	—	—	300	
	t_{pLH3}	6	$\overline{\text{ENABLE}}$ - $\overline{\text{OUTn}}$, $\overline{\text{LATCH}}$ = "H"	—	—	300	
	t_{pLH}	6	CLK-SERIAL OUT	2	—	14	
	t_{pHL1}	6	CLK- $\overline{\text{OUTn}}$, $\overline{\text{LATCH}}$ = "H", $\overline{\text{ENABLE}}$ = "L"	—	—	340	
	t_{pHL2}	6	$\overline{\text{LATCH}}$ - $\overline{\text{OUTn}}$, $\overline{\text{ENABLE}}$ = "L"	—	—	340	
	t_{pHL3}	6	$\overline{\text{ENABLE}}$ - $\overline{\text{OUTn}}$, $\overline{\text{LATCH}}$ = "H"	—	—	340	
	t_{pHL}	6	CLK-SERIAL OUT	2	—	14	
Output rise time	t_{or}	6	10% to 90% points of $\overline{\text{OUT0}}$ to $\overline{\text{OUT7}}$ voltage waveforms	—	—	150	
Output fall time	t_{of}	6	90% to 10% points of $\overline{\text{OUT0}}$ to $\overline{\text{OUT7}}$ voltage waveforms	—	—	300	

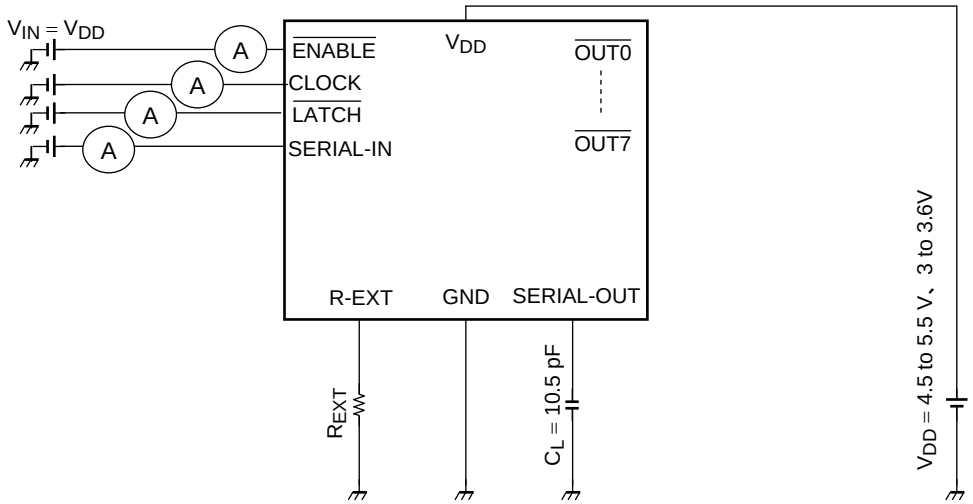
Note 1: T_{opr} = 25°C, V_{DD} = V_{IH} = 3.3 V, V_{IL} = 0 V, R_{EXT} = 1.2 kΩ, I_{OUT} = 15 mA, V_L = 5.0 V,
C_L = 10.5 pF (see test circuit 6.)

Test Circuits

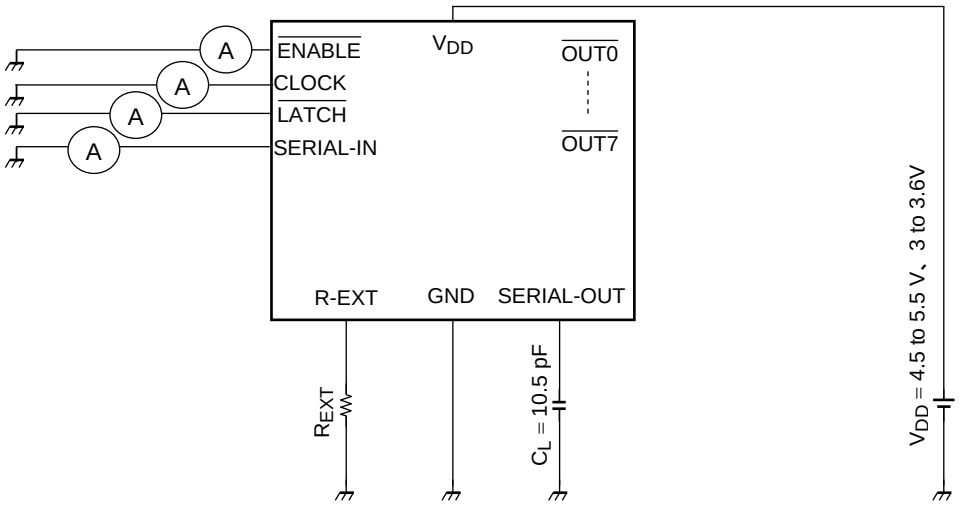
Test Circuit 1: SERIAL-OUT output voltage (V_{OH}/V_{OL})



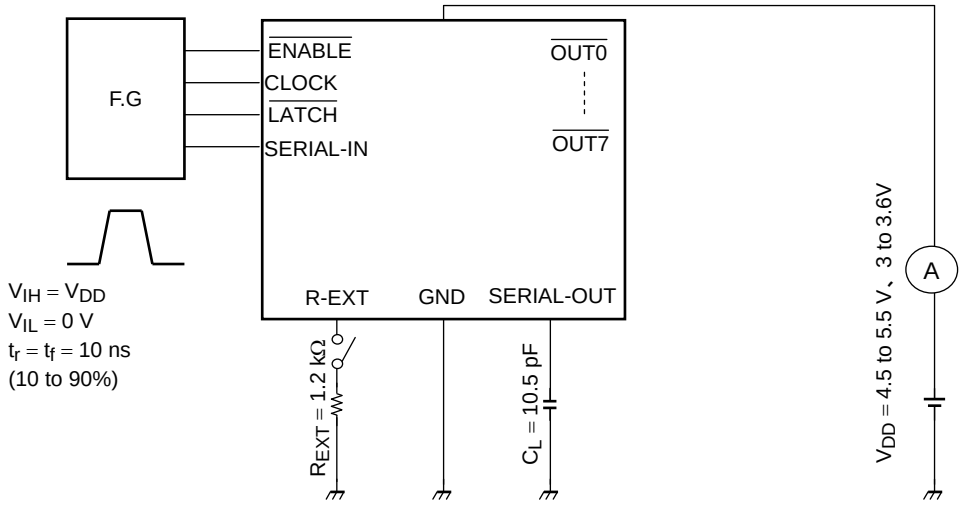
Test Circuit 2: Input Current (I_{IH})



Test Circuit 3: Input Current (I_{IL})

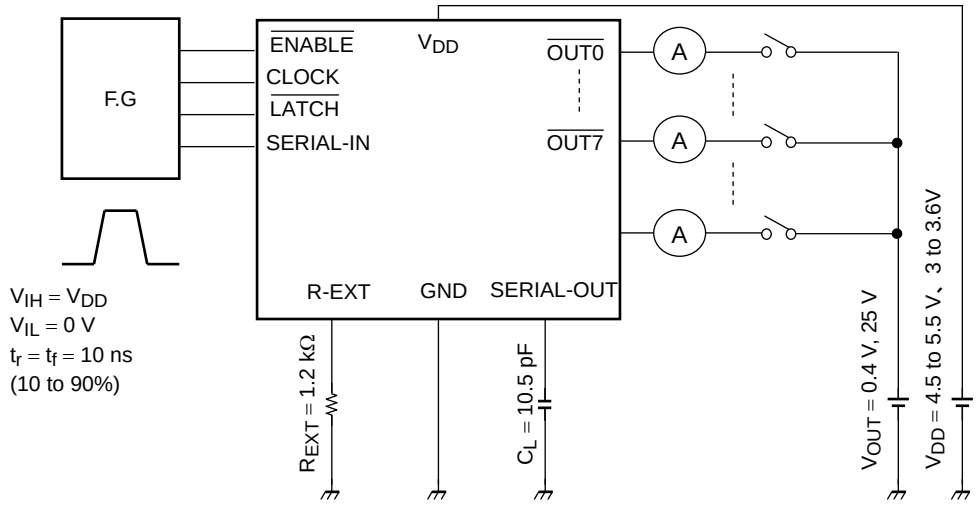


Test Circuit 4: Supply Current



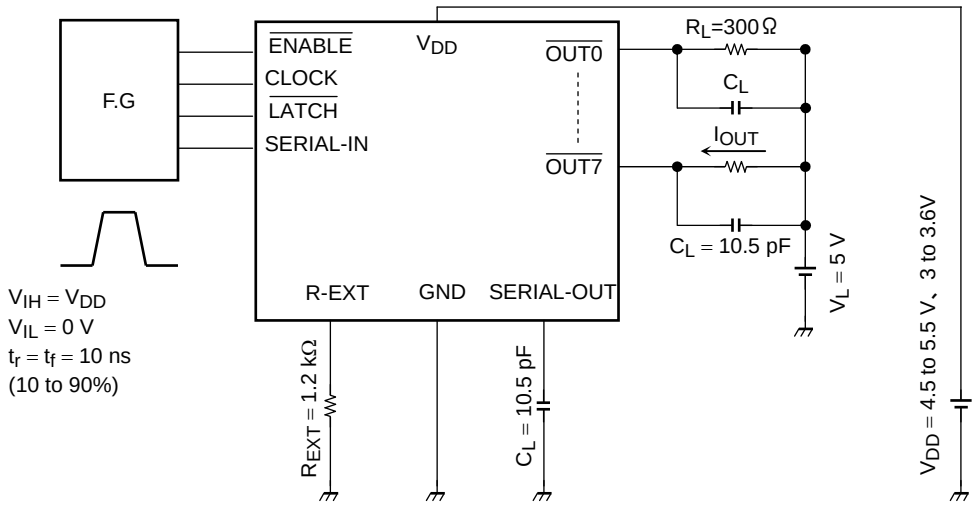
Note: The output terminal is based on the power supply current conditions on page 6 and 7.

Test Circuit 5: Output Current (I_{OUT1}), Output Leakage Current (I_{OZ}), Output Current Error Margin ($\Delta I_{OUT1}/\Delta I_{OUT2}$), Current Variation with V_{DD} (%/V_{DD})



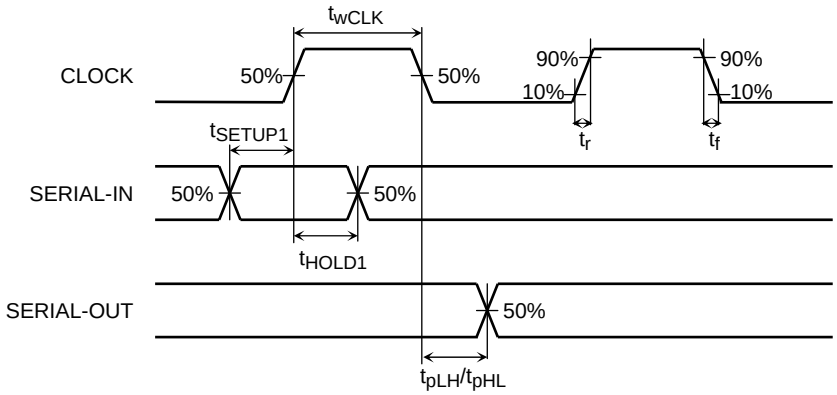
Theoretical output current = 1.13 V/R_{EXT} × 16

Test Circuit 6: Switching Characteristics

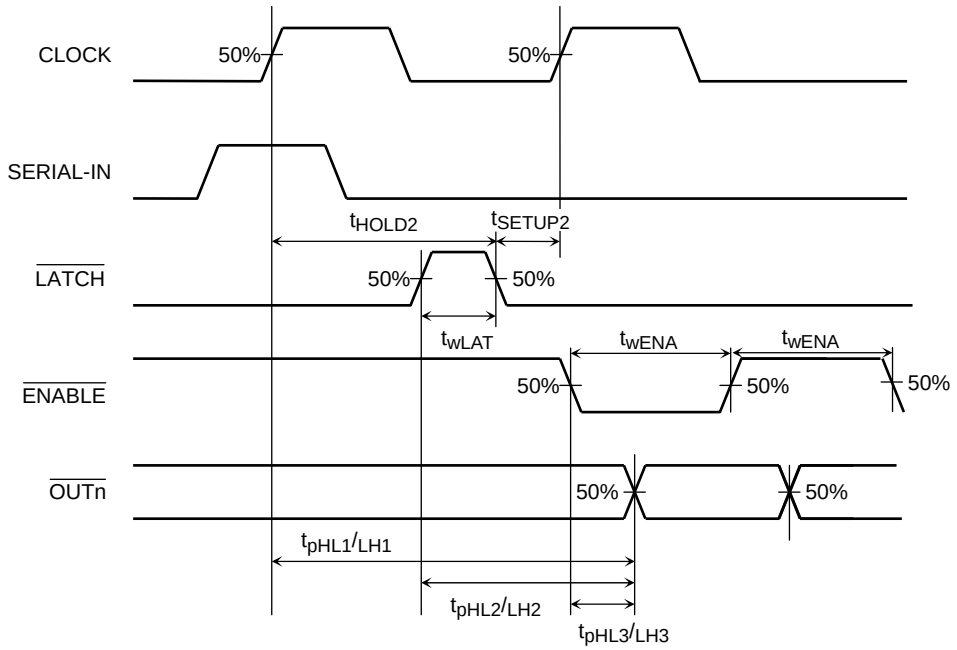


Timing Waveforms

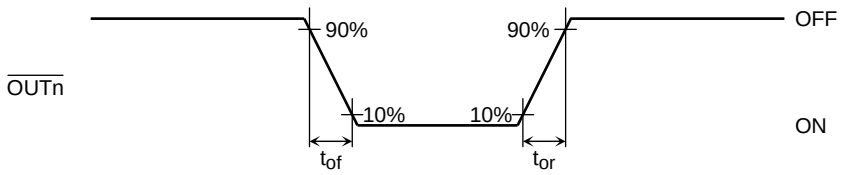
1. CLOCK, SERIAL-IN, SERIAL-OUT



2. CLOCK, SERIAL-IN, $\overline{\text{LATCH}}$, $\overline{\text{ENABLE}}$, $\overline{\text{OUTn}}$



3. $\overline{\text{OUTn}}$

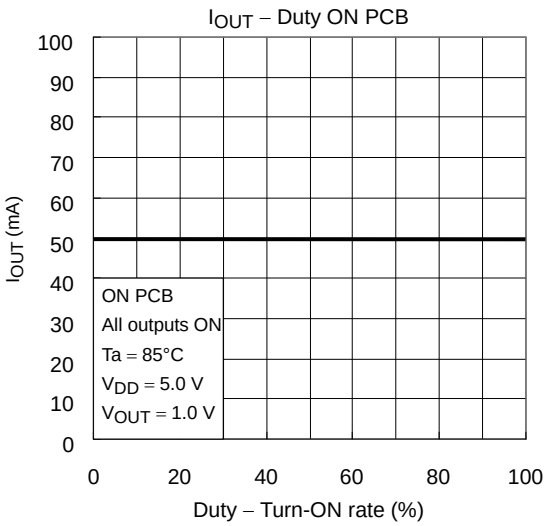


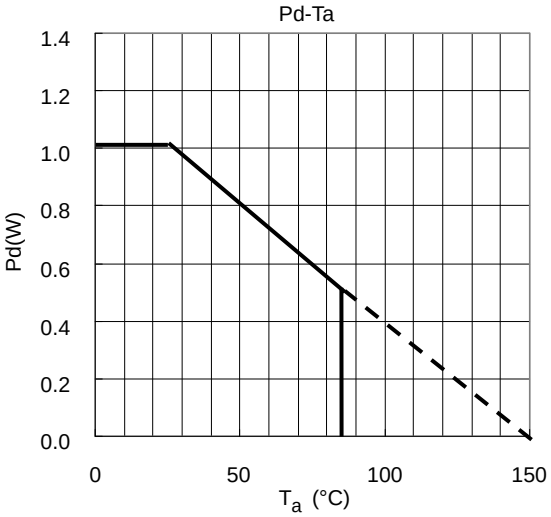
Note: Timing chart waveforms are presented to describe functions and operations and may be simplified. Adequate consideration should be given to timing conditions.

Output Current vs. Derating (lighting rate) Graph

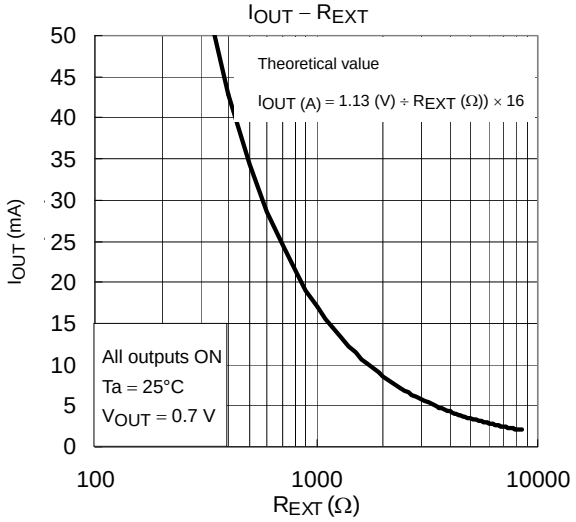
PCB Conditions: 76.2 × 114.3 × 1.6 mm, Cu = 30%, 35-µm Thick, SEMI-Compliant

TB62777FNG





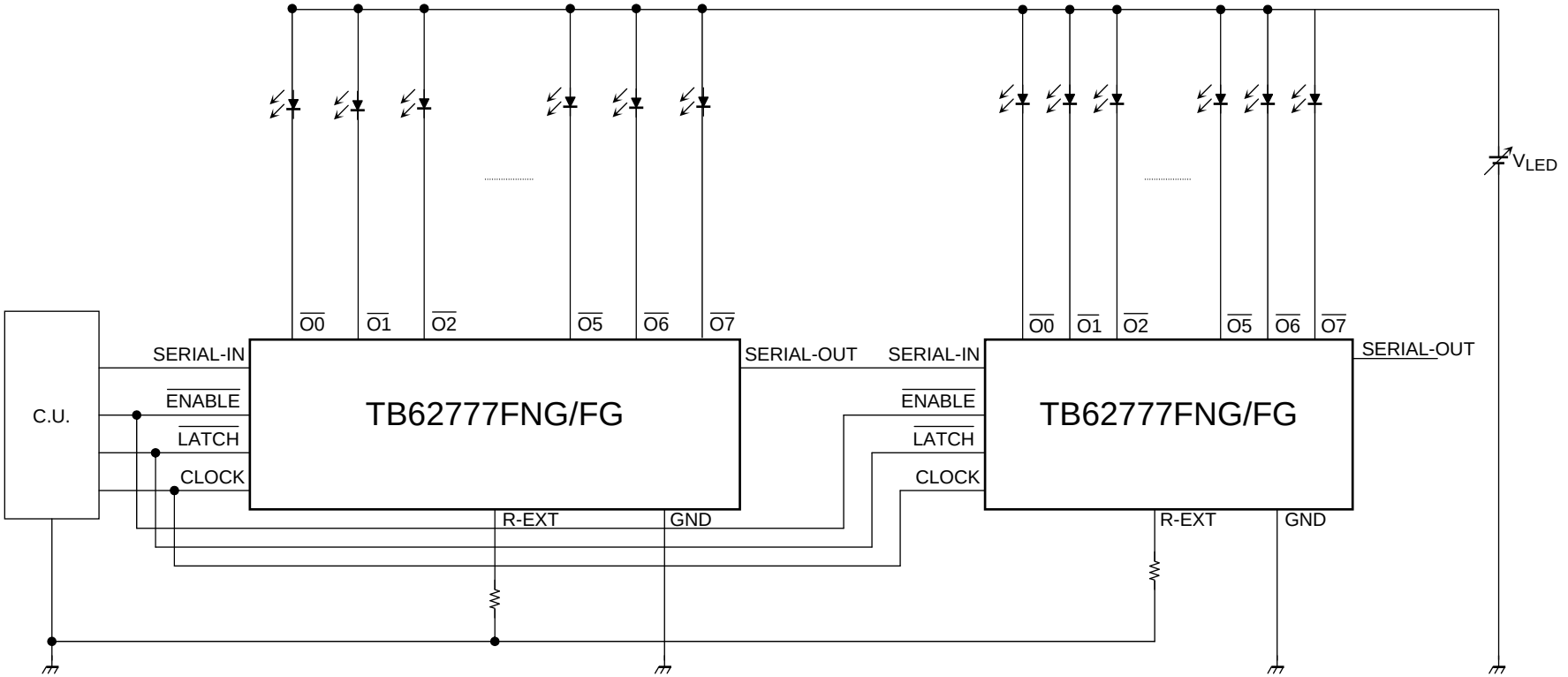
Output Current vs. External Resistor (typ.)



The above graphs are presented merely as a guide and do not constitute any guarantee as to the performance or characteristics of the device. Each product design should be fully evaluated in a real-world environment.

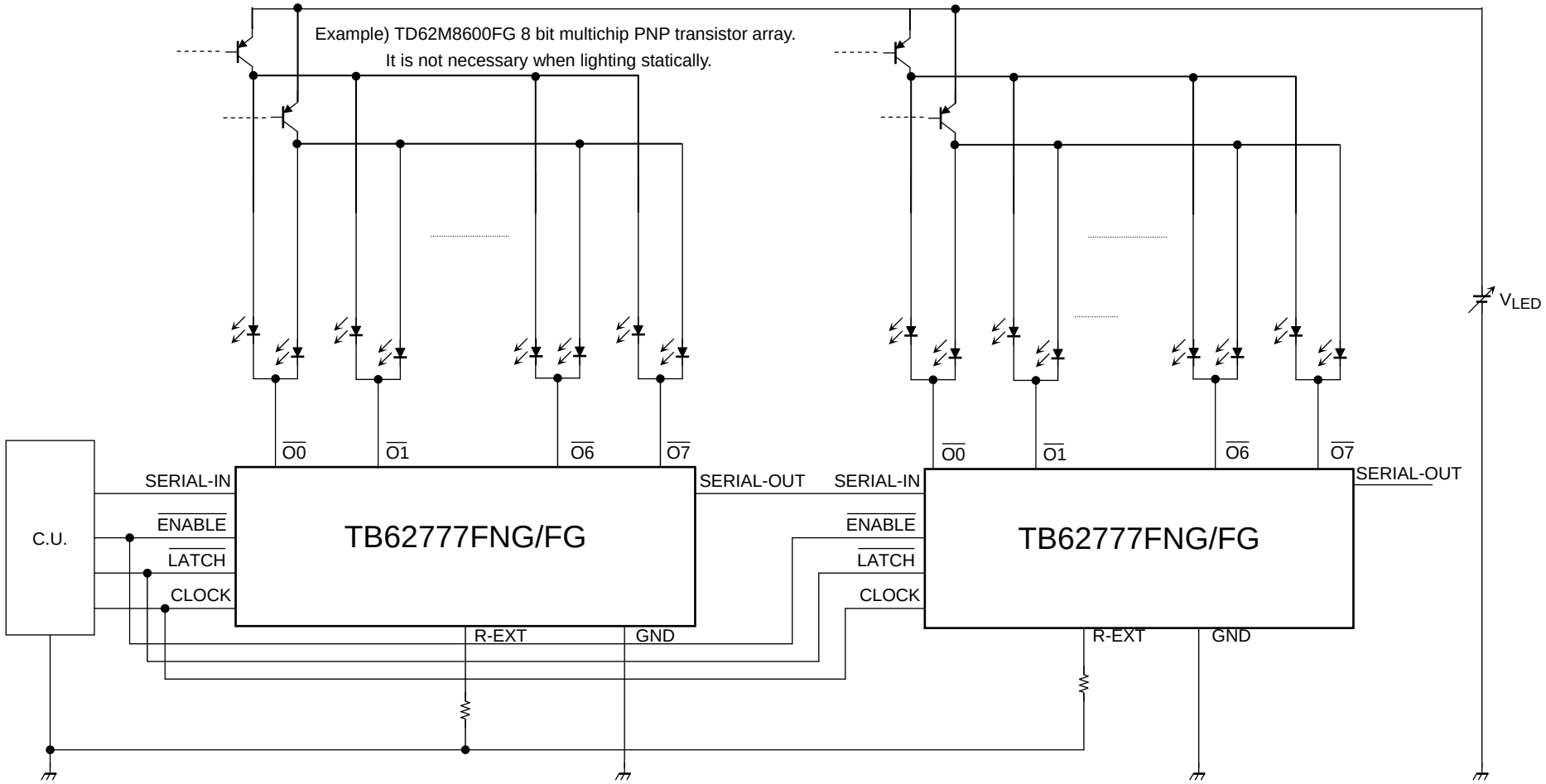
Application Circuit 1: General Composition for Static Lighting of LEDs

In the following diagram, it is recommended that the LED supply voltage (V_{LED}) be equal to or greater than the sum of V_f (max) of all LEDs plus 0.7 V.



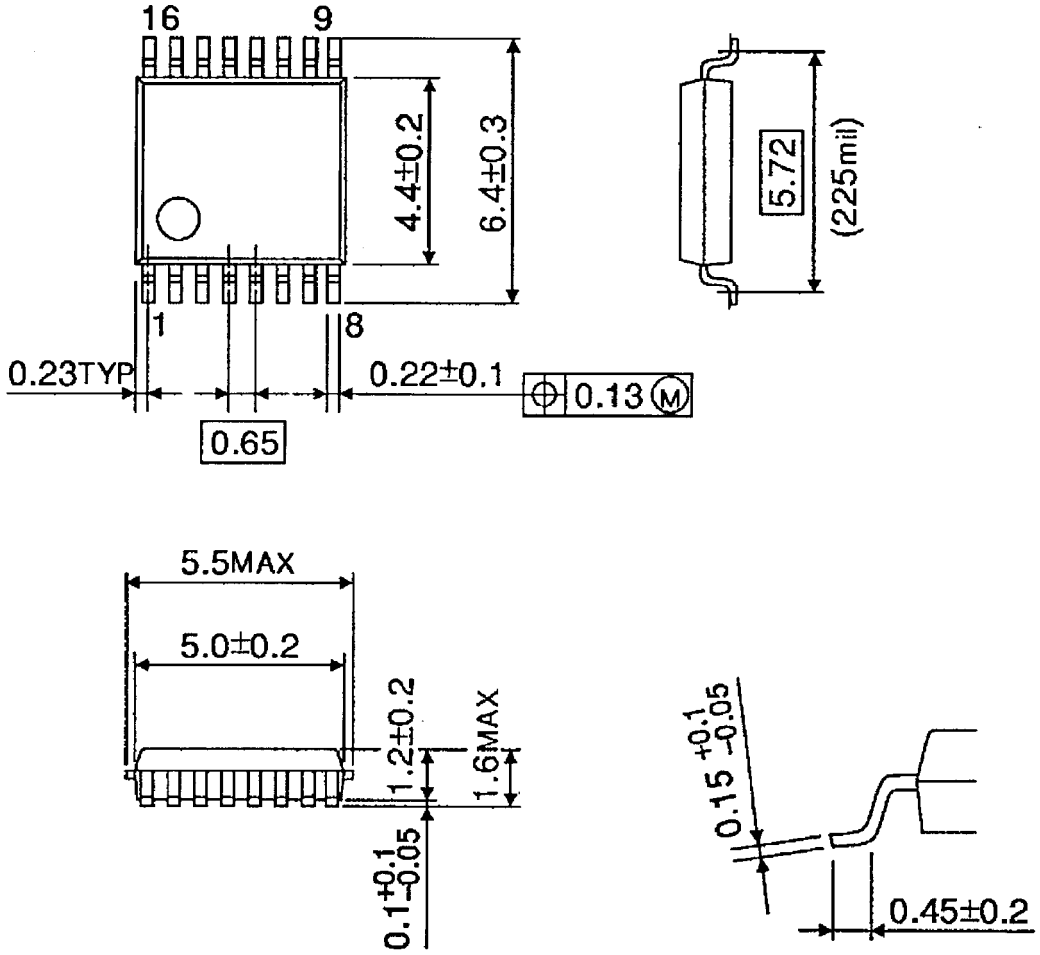
Application Circuit 2: General Composition for Dynamic Lighting of LEDs

In the following diagram, it is recommended that the LED supply voltage (V_{LED}) be equal to or greater than the sum of V_f (max) of all LEDs plus 0.7 V.



Package Dimensions

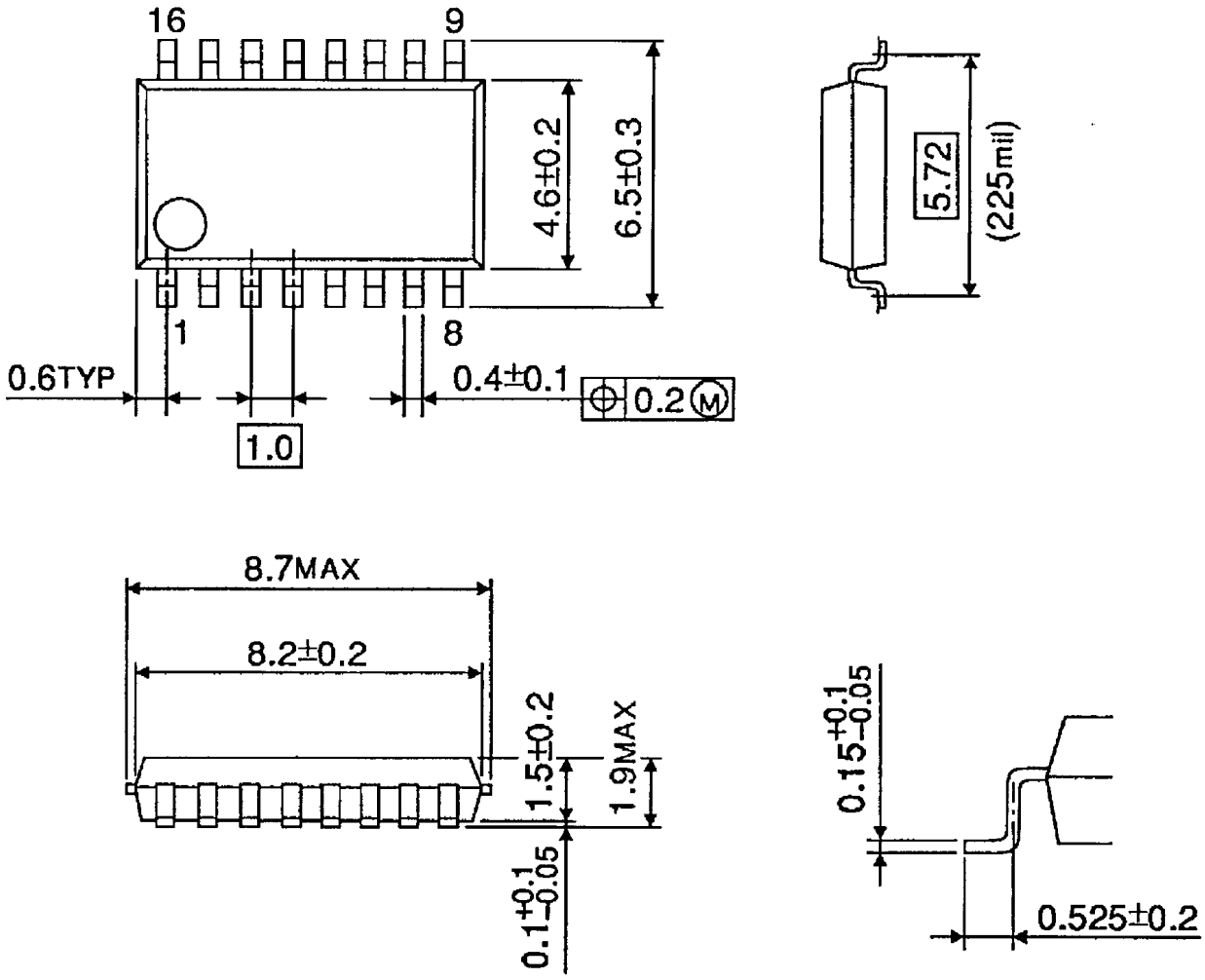
SSOP16-P-225-0.65B Unit : mm



Weight: 0.07 g (typ.)

Package Dimensions

SSOP16-P-225-1.00A Unit : mm



Weight: 0.14 g (typ.)

Notes on Contents

1. Block Diagrams

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2. Equivalent Circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

3. Timing Charts

Timing charts may be simplified for explanatory purposes.

4. Application Circuits

The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass production design stage.
Toshiba does not grant any license to any industrial property rights by providing these examples of application circuits.

5. Test Circuits

Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

IC Usage Considerations

Notes on handling of ICs

(1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause breakdown, damage or deterioration of the device, and may result in injury by explosion or combustion.

(2) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in the event of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow. Such a breakdown can lead to smoke or ignition. To minimize the effects of a large current flow in the event of breakdown, fuse capacity, fusing time, insertion circuit location, and other such suitable settings are required.

(3) If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition.
For ICs with built-in protection functions, use a stable power supply with. An unstable power supply may cause the protection function to not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

(4) Do not insert devices incorrectly or in the wrong orientation. Make sure that the positive and negative terminals of power supplies are connected properly. Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause breakdown, damage or deterioration of the device, which may result in injury by explosion or combustion. In addition, do not use any device that has had current applied to it while inserted incorrectly or in the wrong orientation even once.

(5) Carefully select power amp, regulator, or other external components (such as inputs and negative feedback capacitors) and load components (such as speakers).
If there is a large amount of leakage current such as input or negative feedback capacitors, the IC output DC voltage will increase. If this output voltage is connected to a speaker with low input withstand voltage, overcurrent or IC failure can cause smoke or ignition. (The over current can cause smoke or ignition from the IC itself.) In particular, please pay attention when using a Bridge Tied Load (BTL) connection type IC that inputs output DC voltage to a speaker directly.

Points to remember on handling of ICs

(1) Heat Dissipation Design
In using an IC with large current flow such as a power amp, regulator or driver, please design the device so that heat is appropriately dissipated, not to exceed the specified junction temperature (Tj) at any time or under any condition. These ICs generate heat even during normal use. An inadequate IC heat dissipation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into consideration the effect of IC heat dissipation on peripheral components..

(2) Back-EMF
When a motor rotates in the reverse direction, stops, or slows down abruptly, a current flow back to the motor's power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in your system design.

About solderability, following conditions were confirmed

- Solderability

  (1) Use of Sn-37Pb solder Bath
  - solder bath temperature = 230°C
  - dipping time = 5 seconds
  - the number of times = once
  - use of R-type flux

  (2) Use of Sn-3.0Ag-0.5Cu solder Bath
  - solder bath temperature = 245°C
  - dipping time = 5 seconds
  - the number of times = once
  - use of R-type flux

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