NCS2632

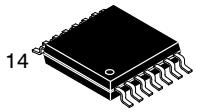
NOCAP™, Pop-Free, 3 V_{RMS} Audio Line Driver with Adjustable Gain

The NCS2632 is a pop−free stereo line driver. It uses ON Semiconductor's patented NOCAP technology which allows the elimination of the external DC−blocking capacitors by providing ground−referenced outputs through the generation of an internal negative supply rail. The device can drive 3 V_{RMS} into a 600 Ω load at 5 V power supply. By eliminating the two external heavy coupling capacitors, the NOCAP approach offers significant space and cost savings compared to similar audio solutions.

The NCS2632 has differential inputs and is available with an external adjustable gain ranging from ±1 V/V to ±10 V/V. The gain is adjusted with external resistors. The device can also be configured as a 2nd order low pass filter to complement DAC's and SOC converters. In addition to the NOCAP architecture, it contains specific circuitry to prevent "Pop & Click" noise from occurring during Enable / Shutdown transitions. The Signal-to-Noise Ratio reaches 105 dB, offering high fidelity audio sound. The NCS2632 exhibits a high power supply rejection with a typical value of 90 dB. This device also features an Under−Voltage Protection (UVP) function which can be adjusted using an external resistor bridge. The device is available in a TSSOP−14 package.

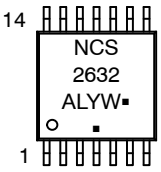
ON Semiconductor®

http://onsemi.com



TSSOP−14
CASE 948G

MARKING DIAGRAM



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(*Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8473/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 13 of this data sheet.

Features

- NOCAP
  - Eliminates Pop/Clicks
  - Eliminates Output DC−Blocking Capacitors – Provides Flat Frequency Response 20 Hz – 20 kHz
- Supply Voltage from 2.2 V to 5.5 V
- Low Noise and THD
  - SNR = 105 dB
  - Typical V_n at 8 μVrms, A−Weighted
  - THD+N < 0.001% at 1 kHz
- Output Voltage into 600 Ω Load
  - 2 V_{RMS} with 3.3 V Supply Voltage
  - 3 V_{RMS} with 5 V Supply Voltage
- Adjustable Gain from ± 1 V/V to ± 10 V/V
- Differential Input
- High PSRR: 90 dB
- External Under−Voltage Detection Function
- Enhanced Pop & Click Suppression Function
- Offset Voltage ≤ ±400 μV
- Outputs pass ±8 kV contact discharge according to IEC61000−4−2 under application conditions
- Available in a TSSOP−14 package
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Set−Top Boxes
- PDP / LCD TV
- Blu−ray™ Player, DVD Players
- Home Theater in a Box
- Laptops, Notebook PCs

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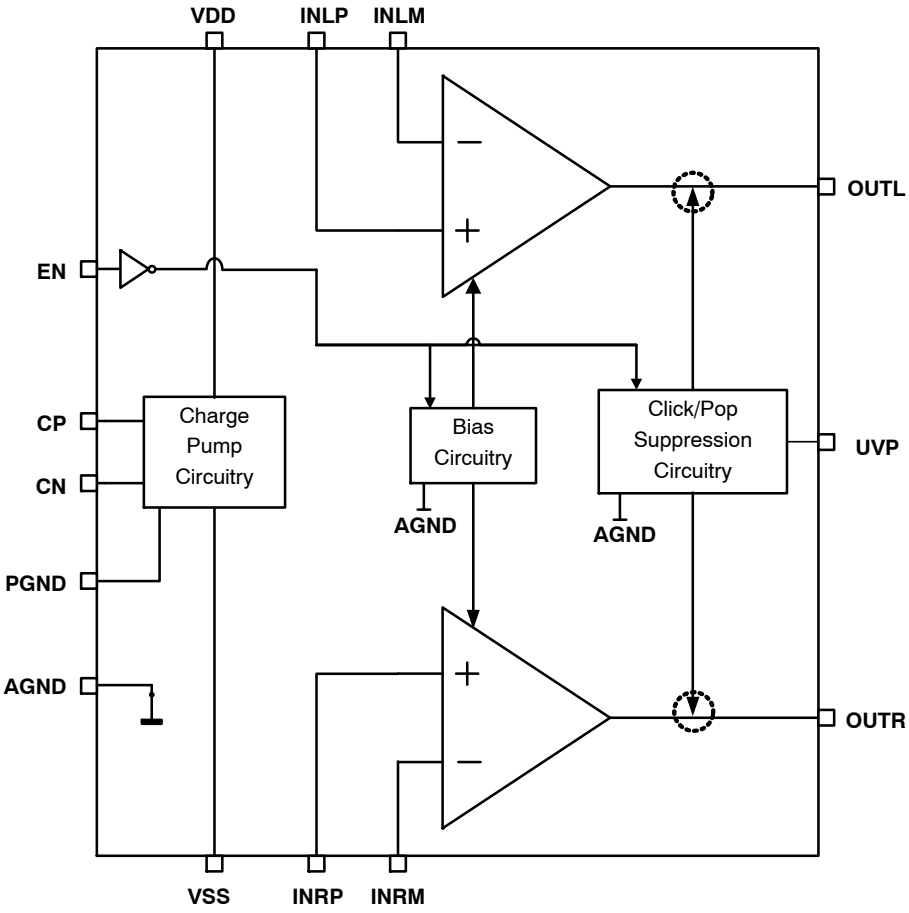


Figure 1. NCS2632, Simplified Block Diagram

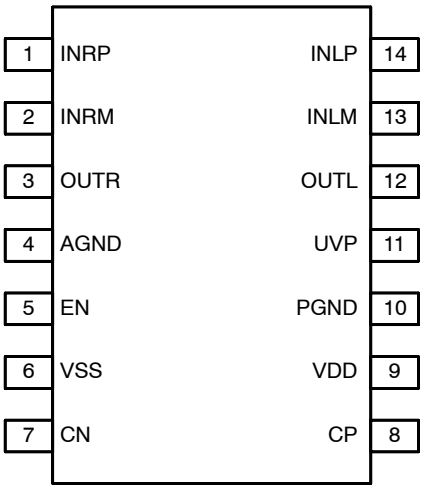


Figure 2. NCS2632, Pinout

PIN FUNCTION AND DESCRIPTION

Pin	Name	Type	Description
1	INRP	Input	Right channel positive input
2	INRM	Input	Right channel negative input
3	OUTR	Output	Right channel output
4	AGND	Ground	Analog ground. Connect to PGND
5	EN	Input	Enable pin. Active High
6	VSS	Power	Negative rail output. Connected to ground through 1 μF low ESR ceramic reservoir capacitor.
7	CN	–	Flying capacitor Negative terminal. Connected to CP through 1 μF low ESR ceramic capacitor.
8	CP	–	Flying capacitor Positive terminal. Connected to CN through 1 μF low ESR ceramic capacitor.
9	VDD	Power	Power Supply Input
10	PGND	Ground	Power ground
11	UVP	Input	Under−voltage detection pin.
12	OUTL	Output	Left Channel Output
13	INLM	Input	Left channel negative input
14	INLP	Input	Left channel positive input

ABSOLUTE MAXIMUM RATINGS (Note 1)

Parameter		Symbol	Value	Unit
Supply Voltage, VDD to GND		V_{DD}	−0.3 to 5.5	V
Input Voltage		V_I	V_{SS} − 0.3 to V_{DD} + 0.3	V
Minimum Load Impedance		R_L	>600	Ω
Logic Pin Voltage (EN)			−0.3 to V_{DD} +0.3	V
Maximum Junction Temperature		$T_{J(max)}$	−40 to 150	°C
Storage Temperature Range		T_{STG}	−40 to 150	°C
ESD Capability (Note 2)	Human Body Model Machine Model	ESD_{HBM} ESD_{MM}	2000 200	V
Latch−up Current (Note 3)		I_{LU}	100	mA
Moisture Sensitivity Level (Note 4)		MSL	Level 1	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (JEDEC standard: JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (JEDEC standard: JESD22−A115)
3. Latch−up Current tested per JEDEC standard: JESD78
4. Moisture Sensitivity Level tested per IPC/JEDEC standard: J−STD−020A

THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Junction−to−Ambient Thermal Resistance, TSSOP−14 (Note 5)	θ_{JA}	115	°C/W

5. Values based on copper area of 645 mm^2 (or 1 in^2) of 1 oz copper thickness and FR4 PCB substrate.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage with UVP connected to Ground	V_{DD}	2.2	3.3	5.5	V
High−Level Input Voltage	V_{IH} (EN)	1.2			V
Low−Level Input Voltage	V_{IL} (EN)			0.4	V
Ambient Temperature	T_A	−40		85	°C

ELECTRICAL CHARACTERISTICS, T_A = 25°C (unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Offset Voltage	$\|V_{OS}\|$	V_{DD} = 2.5 V to 5 V, Voltage follower − gain = 1		100	400	μV
High−Level Input Current (EN)	$\|I_{IH}\|$	V_{DD} = 5 V, V_I = V_{DD}			100	nA
Low−Level Input Current (EN)	$\|I_{IL}\|$	V_{DD} = 5 V, V_I = 0 V			100	nA
Supply Current	I_{DD}	V_{DD} = 2.2 V, No load, EN = V_{DD}		7	11	mA
		V_{DD} = 5.5 V, No load, EN = V_{DD}		8	11	mA
		Shutdown mode, V_{DD} = 2.2 V to 5.5 V		60	500	nA
Under−Voltage Protection (UVP) Threshold	V_{UVP}			1.25		V
UVP Internal Hysteresis Current Source	I_{HYS}			5		μA
Charge Pump Frequency	f_{cp}			400		kHz

OPERATING CHARACTERISTICS

V_{DD} = 3.3 V, T_A = 25°C, R_L = 2.5 kΩ, C_{VSS} = 1 μF, C_{IN} = 10 μF, R_{IN} = 10 kΩ, R_{fb} = 20 kΩ (unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage (Outputs In Phase)	V_O	THD = 1%, V_{DD} = 3.3 V, f = 1 kHz	2.05			Vrms
		THD = 1%, V_{DD} = 5 V, f = 1 kHz	3.05			
		THD = 1%, V_{DD} = 5 V, f = 1 kHz, R_L = 100 kΩ	3.1			
Total Harmonic Distortion plus Noise	THD+N	V_O = 2 Vrms, f = 1 kHz		0.001		%
		V_O = 2 Vrms, f = 10 kHz		0.001		%
Power Supply Rejection	PSRR	V_{DD} = 2.5 V to 5 V		90		dB
Crosstalk	XTALK	V_O = 2 Vrms, f = 1 kHz		−120		dB
Output Current Limit	I_O	V_{DD} = 3.3 V		21		mA
Input Resistor Range (Note 6)	R_{IN}		1	10	47	kΩ
Feedback Resistor Range (Note 6)	R_{fb}		4.7	20	100	kΩ
Maximum Capacitive Load (Note 6)	C_{OUT}			220		pF
Noise Output Voltage	V_N	A−weighted		8		μVrms
Signal to Noise Ratio	SNR	V_O = 2 Vrms, THD + N = 0.1% A−weighted filter		105		dB

6. Guaranteed by design.

TYPICAL CHARACTERISTICS

V_{DD} = 3.3 V, T_A = 25°C, R_L = 2.5 kΩ, C_{VSS} = 1 μF, C_{IN} = 10 μF, R_{IN} = 10 kΩ, R_{fb} = 20 kΩ (unless otherwise noted)

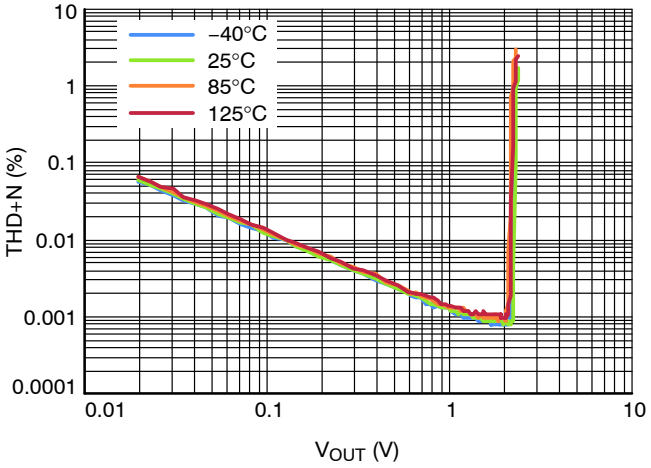


Figure 3. THD+N vs. Output Voltage over Temperature, R_L = 2.5 kΩ, V_{DD} = 3.3 V, f = 1 kHz

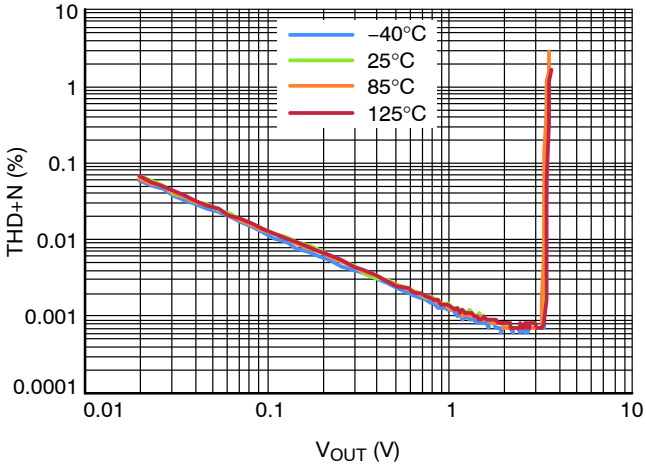


Figure 4. THD+N vs. Output Voltage over Temperature, R_L = 2.5 kΩ, V_{DD} = 5 V, f = 1 kHz

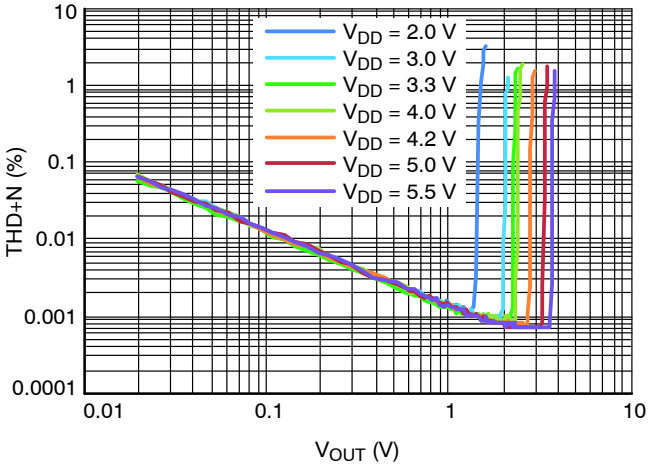


Figure 5. THD+N vs. Output Voltage over Supply, R_L = 2.5 kΩ, f = 1 kHz

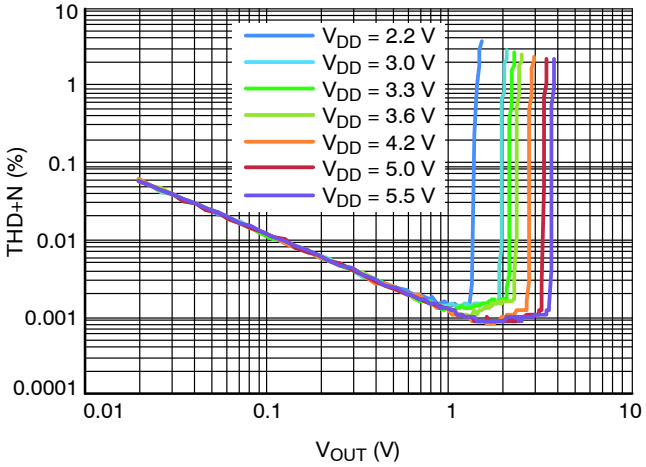


Figure 6. THD+N vs. Output Voltage over Supply, R_L = 600 Ω, f = 1 kHz

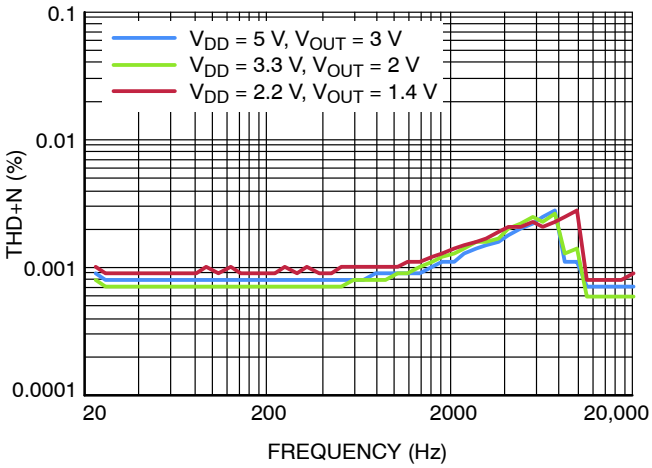


Figure 7. THD+N vs. Frequency, R_L = 2.5 kΩ

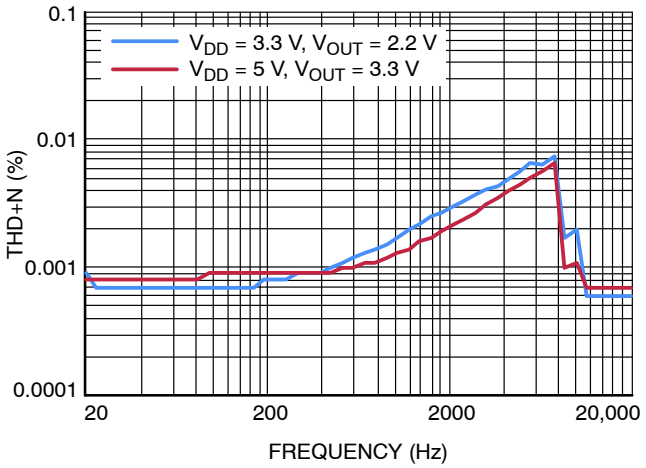


Figure 8. THD+N vs. Frequency, R_L = 600 Ω

TYPICAL CHARACTERISTICS

V_{DD} = 3.3 V, T_A = 25°C, R_L = 2.5 kΩ, C_{VSS} = 1 μF, C_{IN} = 10 μF, R_{IN} = 10 kΩ, R_{fb} = 20 kΩ (unless otherwise noted)

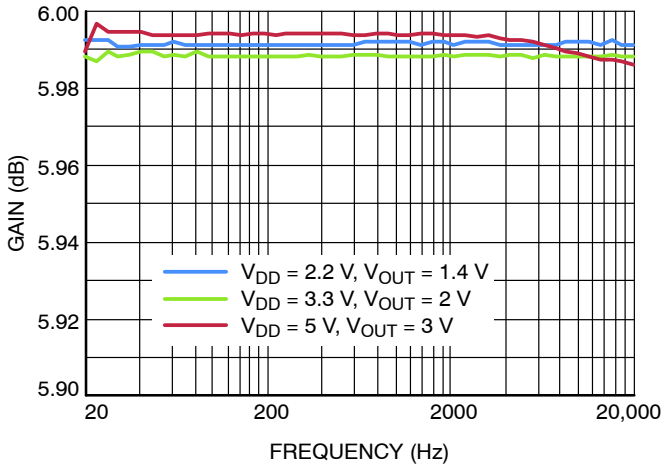


Figure 9. Gain vs. Frequency, R_L = 2.5 kΩ

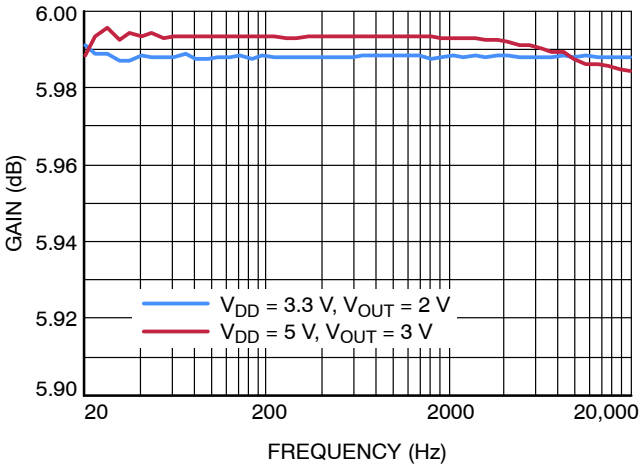


Figure 10. Gain vs. Frequency, R_L = 600 Ω

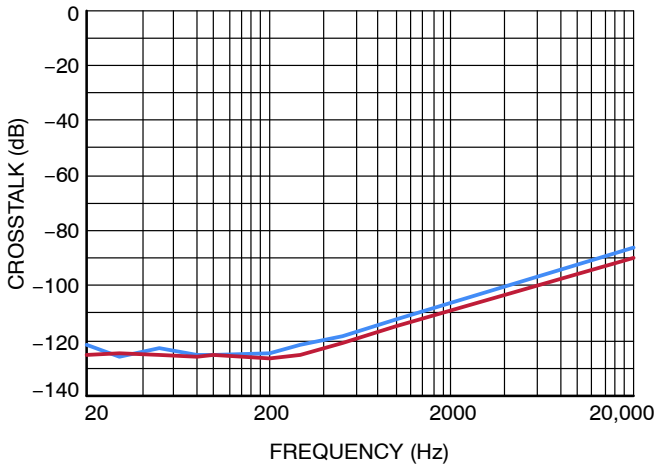


Figure 11. Crosstalk vs. Frequency, R_L = 2.5 kΩ, V_{DD} = 3.3 V, V_O = 2 Vrms

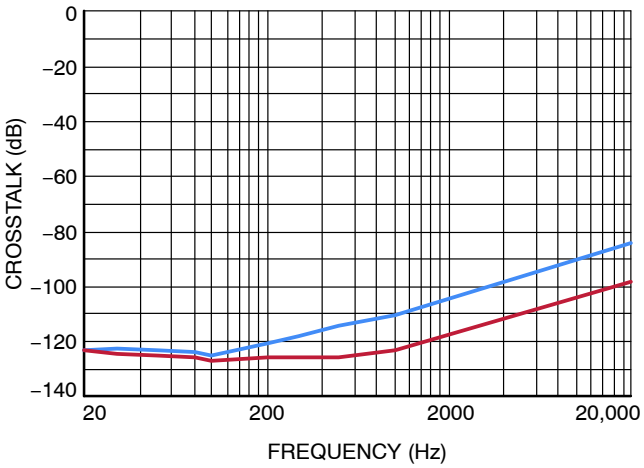


Figure 12. Crosstalk vs. Frequency, R_L = 2.5 kΩ, V_{DD} = 5 V, V_O = 2 Vrms

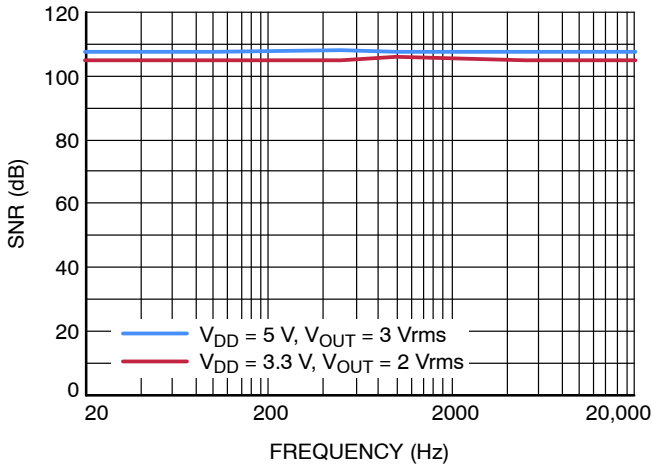


Figure 13. Signal−to−Noise Ratio vs. Frequency, R_L = 2.5 kΩ

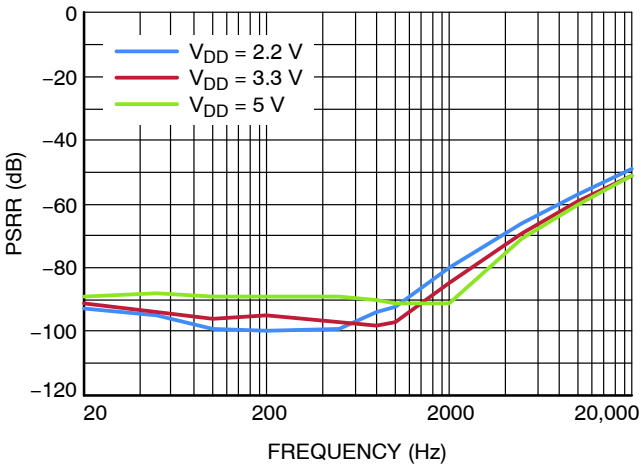


Figure 14. Power Supply Rejection Ratio vs. Frequency, R_L = 2.5 kΩ

TYPICAL CHARACTERISTICS

V_{DD} = 3.3 V, T_A = 25°C, R_L = 2.5 kΩ, C_{VSS} = 1 μF, C_{IN} = 10 μF, R_{IN} = 10 kΩ, R_{fb} = 20 kΩ (unless otherwise noted)

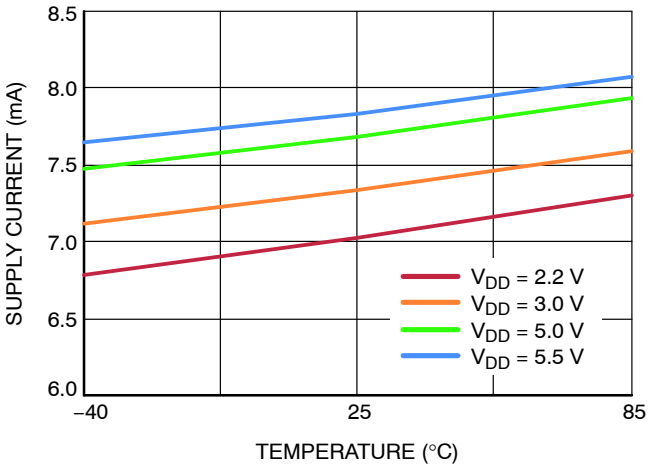


Figure 15. Quiescent Current vs. Temperature, No Load, V_I = 0 V, EN = High

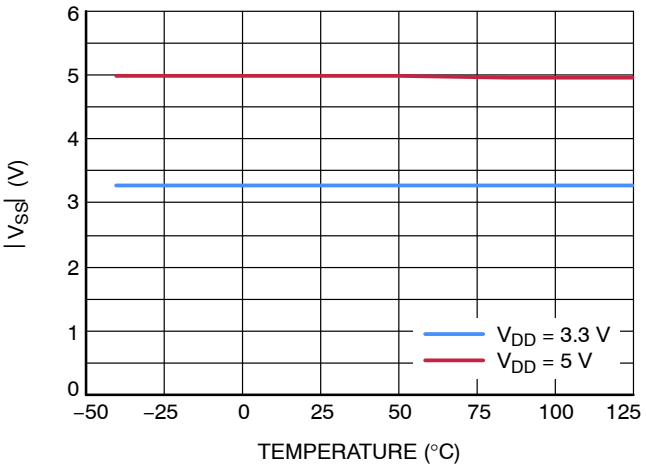


Figure 16. V_{SS} vs. Temperature

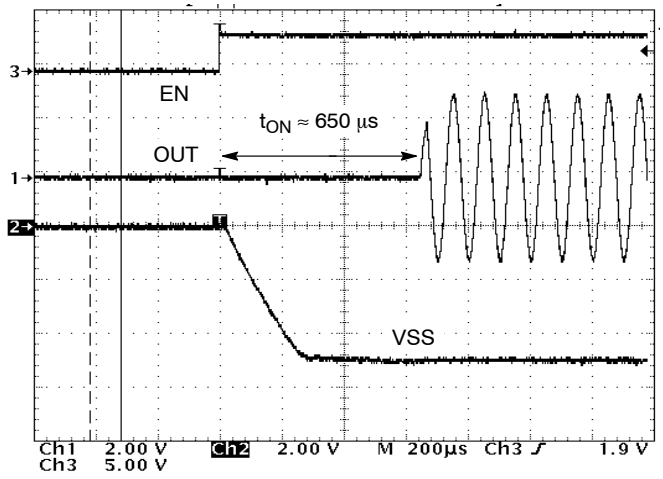


Figure 17. Startup Turn−On Time, R_L = 2.5 kΩ, V_{DD} = 5 V

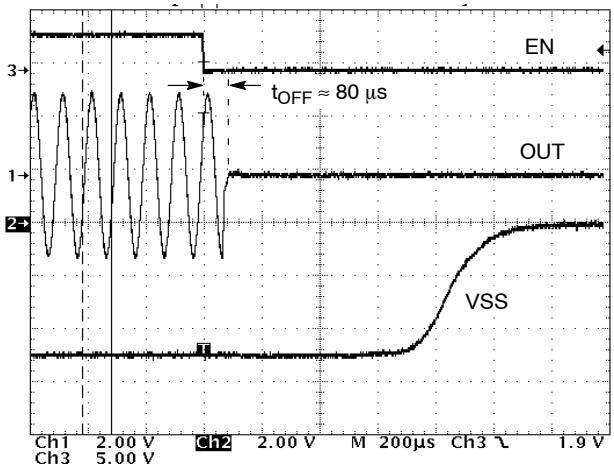


Figure 18. Shutdown Turn−Off Time, R_L = 2.5 kΩ, V_{DD} = 5 V

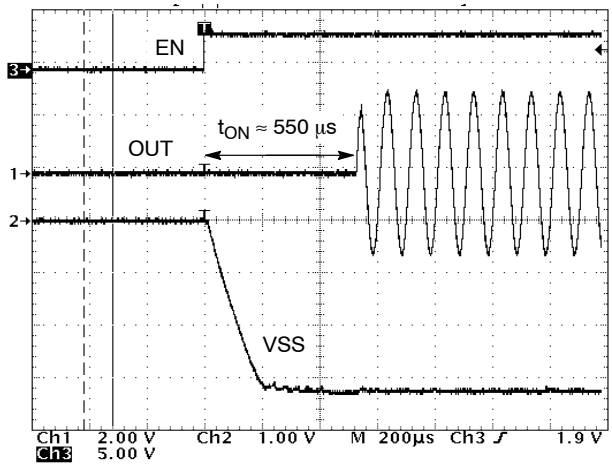


Figure 19. Startup Turn−On Time, R_L = 2.5 kΩ, V_{DD} = 3.3 V

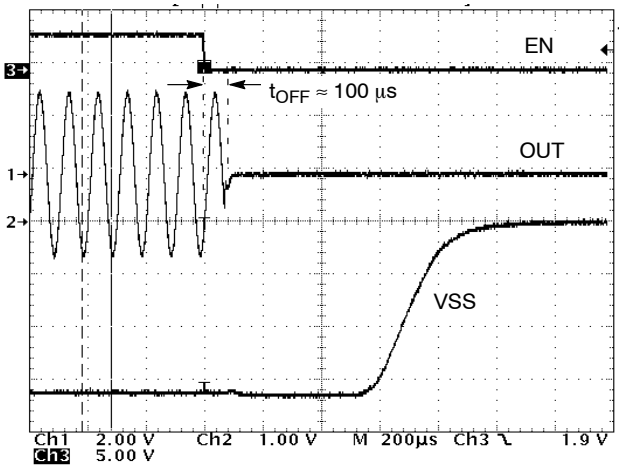


Figure 20. Shutdown Turn−Off Time, R_L = 2.5 kΩ, V_{DD} = 3.3 V

APPLICATION INFORMATION

DESCRIPTION

The NCS2632 is a stereo line driver with a NOCAP architecture. This architecture eliminates the need to use two large, external capacitors required by conventional audio line driver applications. The NCS2632 is basically composed of two true ground amplifiers with internal power supply rail, one UVP−circuit block, and short−circuit protection. The gain of the NCS2632 can be adjusted with two external resistors.

The NOCAP approach is a patented architecture that requires only two 1 μF low ESR ceramic capacitors (fly capacitor and reservoir capacitor). It generates a symmetrical positive and negative voltage and it allows the output of the amplifiers to be biased around the ground (True Ground).

The NCS2632 includes a special circuitry for eliminating any pop and click noise during turn on and turn off time. This circuitry combined with the true ground output architecture and a trimmed output offset voltage makes the elimination of pop and click particularly efficient.

UNDER−VOLTAGE PROTECTION (UVP) PIN MANAGEMENT

The UVP pin can be used to shut down the audio line driver by monitoring the board's main power supply. Then the line driver can be shut down before upstream devices disable, contributing this way to eliminate potential source of pop noise.

The device shuts down when the UVP voltage goes below 1.25 V typically. To monitor the lower main power supply limit, an external voltage divider constituted with three resistors, RUP, RDW and RHYS is used (Figure 21). Resistors values have to be chosen based on the requested power supply shutdown threshold and hysteresis for a given application. It is recommended to have RHYS >> RDW // RUP. RHYS is optional in the case where hysteresis is not necessary.

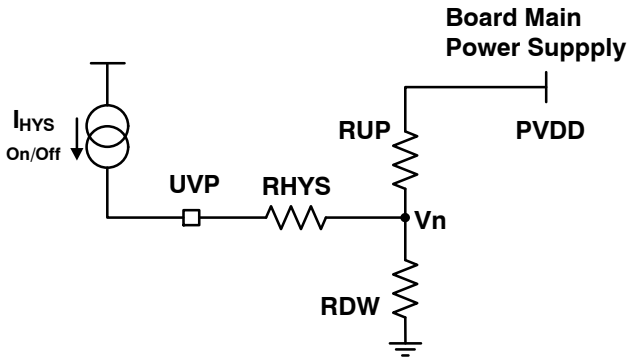


Figure 21. Voltage Divider Connected to UVP for Power Supply Monitoring

When the resistor divider is connected to the pin UVP as shown in Figure 21, the UVP pin voltage is a function of PVDD and I_{HYS} according to the below equation:

$$V_{UVP} = PVDD \times \frac{RDW}{RDW + RUP} + \left(RHYS \times \frac{RDW \times RUP}{RDW + RUP}\right) \times I_{HYS} \quad \text{(eq. 1)}$$

With V_{UVPth} = 1.25 V and I_{HYS} = 5 μA

This gives a PVDD Shutdown threshold.
PVDD Shutdown Threshold:

$$PVDD_{SD} = V_{UVPth} \times \frac{RDW + RUP}{RDW} - I_{HYS} \times \left(RHYS + \frac{RDW \times RUP}{RDW + RUP}\right) \times \frac{RDW + RUP}{RDW} \quad \text{(eq. 2)}$$

Simplified PVDD Shutdown threshold assuming RHYS >> RDW // RUP:

$$PVDD_{SD} = \left(V_{UVPth} - I_{HYS} \times RHYS\right) \times \frac{RDW + RUP}{RDW} \quad \text{(eq. 3)}$$

The PVDD Startup threshold is given by the below equation.
PVDD Hysteresis:

$$PVDD_{UP} = V_{UVPth} \times \frac{RDW + RUP}{RDW} \quad \text{(eq. 4)}$$

The hysteresis component is:
PVDD Hysteresis:

$$\Delta PVDD = V_{HYS} = I_{HYS} \times \left(RHYS + \frac{RDW \times RUP}{RDW + RUP}\right) \times \frac{RDW + RUP}{RDW}$$

$$= I_{HYS} \times \left(RHYS + \frac{RDW \times RUP}{RDW} + RUP\right) \times \frac{PVDD_{UP}}{V_{UVPth}} \quad \text{(eq. 5)}$$

Simplified PVDD Hysteresis assuming RYS >> RDW // RUP:

$$\Delta PVDD = V_{HYS} = I_{HYS} \times RHYS \times \frac{RDW + RUP}{RDW} = I_{HYS} \times RYS \times \frac{PVDD_{UP}}{V_{UVPth}} \quad \text{(eq. 6)}$$

For a given PVDD threshold RUP will be a function of RDW.
RUP and RDW:

$$RUP = \left(\frac{PVDD_{UP}}{V_{UVPth}} - 1\right) \times RDW \quad \text{(eq. 7)}$$

According to Equation 6, assuming RHYS >> RDW // RUP, and for a given hysteresis V_{HYS} and PVDD threshold, RHYS is:
RHYS

$$RHYS = \frac{V_{HYS} \times V_{UVPth}}{I_{HYS} \times PVDD_{UP}} = \frac{1.25 \times V_{HYS}}{5\ \mu A \times PVDD_{UP}} \quad \text{(eq. 8)}$$

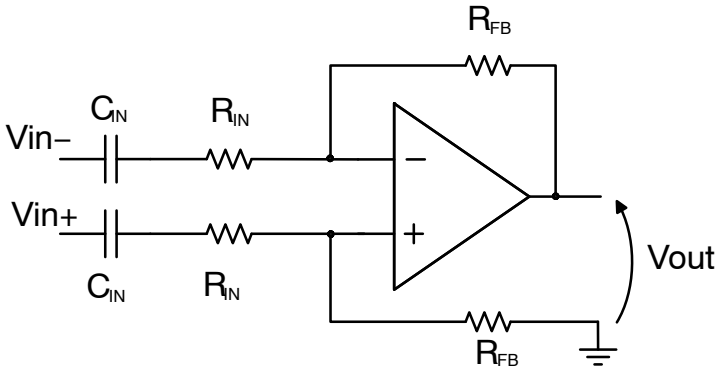
For example, to get $PVDD_{SD}$ = 2.5 V and 0.625 V hysteresis,
Power Divider Resistors have to be: RUP = 1.5 kΩ, RDW = 1 kΩ and RHYS = 51 kΩ

GAIN SETTING RESISTOR SELECTION (R_{IN} and R_{FB})

R_{IN} and R_{FB} set the closed−loop gain of the amplifier. The resistor values have to be chosen so that amplifier stability is preserved. A low gain configuration (close to 1) minimizes the THD + noise values and maximizes the signal to noise ratio.

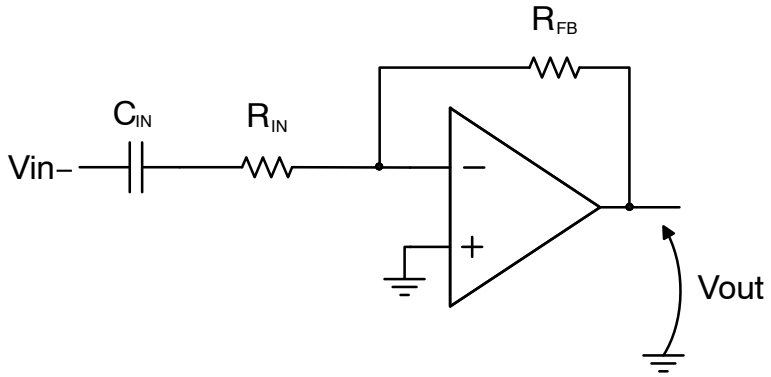
A closed−loop gain in the range of 1 to 10 is recommended to optimize overall system performance.

Selecting values that are too low requires a relatively large input ac-coupling capacitor, C_{IN}. Selecting values that are too high increases the overall noise of the amplifier.



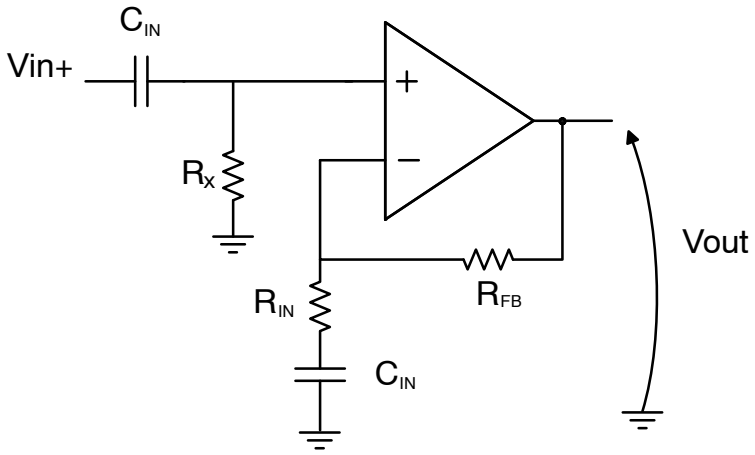
$$Av = \frac{Vout}{Vin+ - Vin-} = \frac{R_{FB}}{R_{in}} \quad \text{(eq. 9)}$$

Figure 22. Differential Input Gain Configuration



$$Av = \frac{Vout}{Vin-} = \frac{-R_{FB}}{R_{IN}} \quad \text{(eq. 10)}$$

Figure 23. Inverting Gain Configuration



$$Av = \frac{V_{out}}{Vin+} = 1 + \frac{R_{FB}}{R_{IN}} \quad \text{(eq. 11)}$$

Figure 24. Non−Inverting Gain Configuration

Table 1. RECOMMENDED RESISTOR VALUES

Input Resistor Value, R_{IN}	Feedback Resistor Value, R_{FB}	Differential Input Gain	Inverting Input Gain	Non Inverting Input Gain
22 kΩ	22 kΩ	1.0 V/V	−1.0 V/V	2.0 V/V
22 kΩ	33 kΩ	1.5 V/V	−1.5 V/V	2.5 V/V
33 kΩ	68 kΩ	2.06 V/V	−2.06 V/V	3.1 V/V
10 kΩ	100 kΩ	10.0 V/V	−10.0 V/V	11.0 V/V

INPUT CAPACITOR

The input coupling capacitor blocks the DC voltage at the amplifier input terminal. This capacitor creates a high−pass filter with R_{IN}. The size of the capacitor must be large enough to couple at low frequencies without severe attenuation in the audio bandwidth (20 Hz − 20 kHz).

The cut off frequency for the input high−pass filter is:

$$f_c = \frac{1}{2\pi R_{in} C_{in}} \quad \text{(eq. 12)}$$

A f_c < 20 Hz is recommended.

CHARGE PUMP CAPACITOR SELECTION

It is recommended to use ceramic capacitors with low ESR for better performances. X5R or X7R capacitors are recommended. The flying capacitor C_{fly} (1 μF) serves to transfer charge during the generation of the negative voltage. The VSS reservoir capacitor C_{VSS} must be equal at least to the C_{fly} capacitor to allow maximum charge transfer. The 1 μF capacitors have to be connected as close as possible to the corresponding pins.

Lower value capacitors can be used but the device may not operate to specifications.

POWER SUPPLY DECOUPLING CAPACITORS

The NCS2632 is a True Ground amplifier that requires an adequate decoupling capacitor on VDD to reduce noise and THD+N. Use a X5R / X7R ceramic capacitor and place it close to the VDD pin. A value of 1μF is recommended. For filtering lower frequency noise signals, a 10 μF or greater capacitor placed near the audio power amplifier would also help.

SHUTDOWN FUNCTION

The device enters shutdown mode when Enable signal is low. During the shutdown mode, the internal charge pump is shut down, and the DC quiescent current of the circuit does not exceed 500 nA. The output is pulled to ground through a low output impedance of about 40 ohms.

USING THE NCS2632 AS A 2nd ORDER FILTER

Audio DACs can require an external low-pass filter to remove out-of-band noise. This is possible with the NCS2632, which can be used as a standard Operational Amplifier with the advantage of better performances including “pop & click” noise behavior.

Single-ended and differential topologies can be implemented. In Figures 25 and 26, a Multiple-FeedBack (MFB) topoplogy, with differential inputs and single-ended inputs is shown. The two topologies use AC-Coupling capacitors (C_{IN}) to block the DC-signal component coming from the source; they contribute to reducing the output offset voltage.

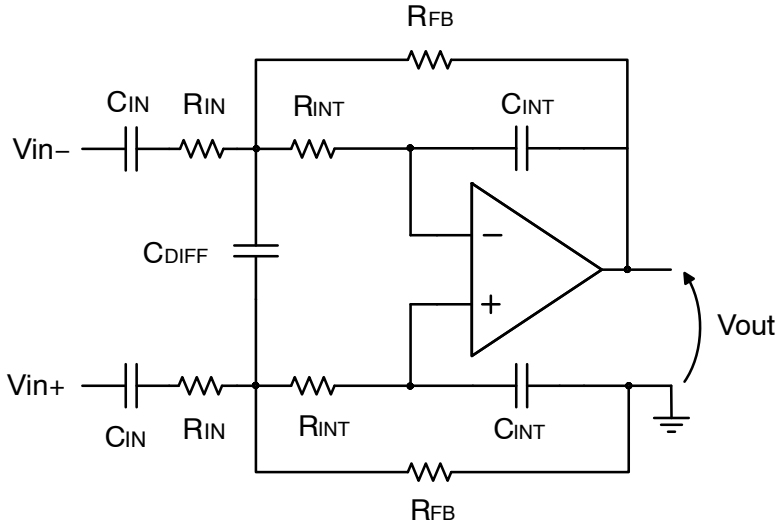


Figure 25. 2nd Order Active Low Pass Filter − Differential Input

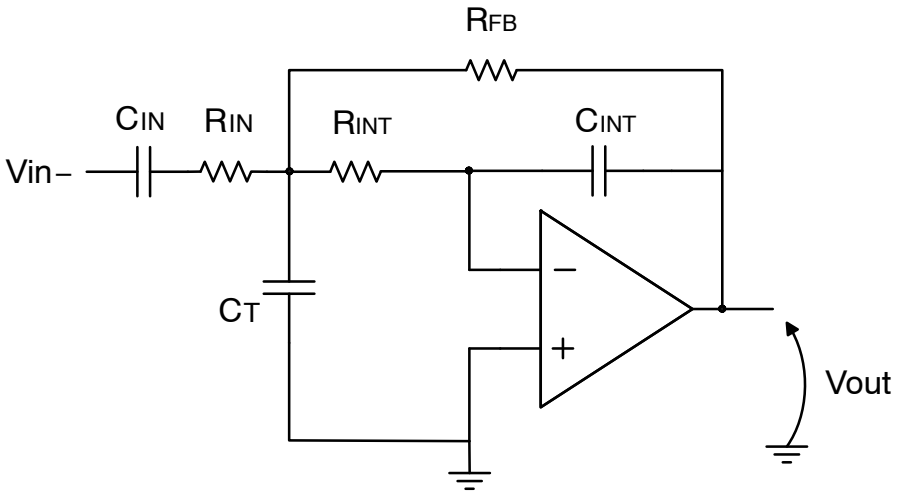


Figure 26. 2nd Order Active Low Pass Filter − Inverting Input

INITIALIZATION AND POP−FREE POWER UP/DOWN

For an on/off/on power sequence, VDD is required to be ramped down to 0 V before ramping back up for power on (shown in Figure 27). This ensures that the NCS2632 internal circuits are properly initialized to guarantee an optimal output.

Pop−free power−up/−down is ensured by keeping EN (Enable pin) low during power supply ramp−up or ramp−down. The EN pin should be kept low until the input ac−coupling capacitors are fully charged before asserting the EN pin high; this way, proper pre−charge of the ac−coupling is performed, and pop−free power−up is achieved. Figure 27 illustrates the preferred sequence.

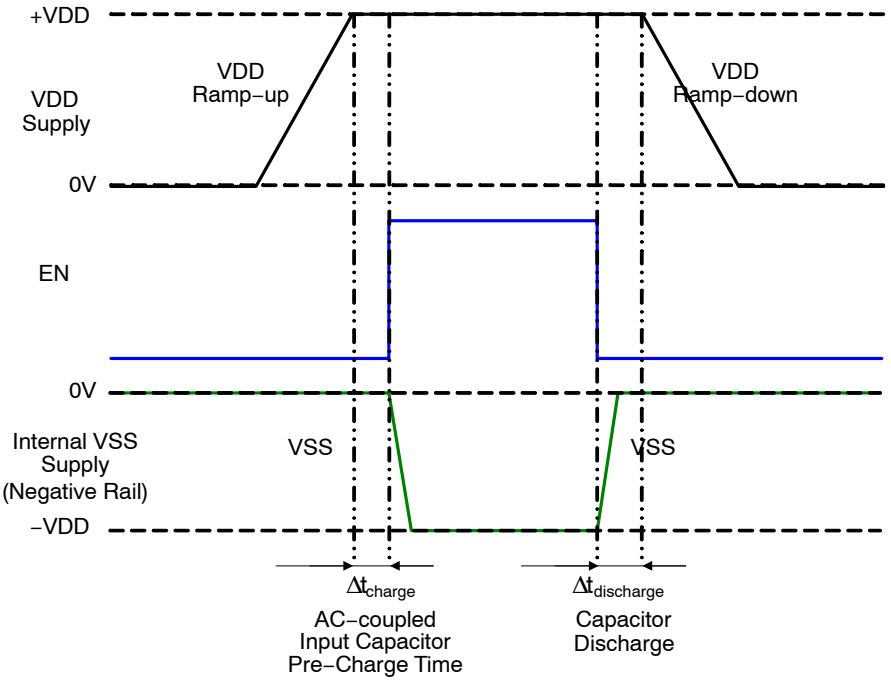


Figure 27. Initialization and Power Up/Down Sequence

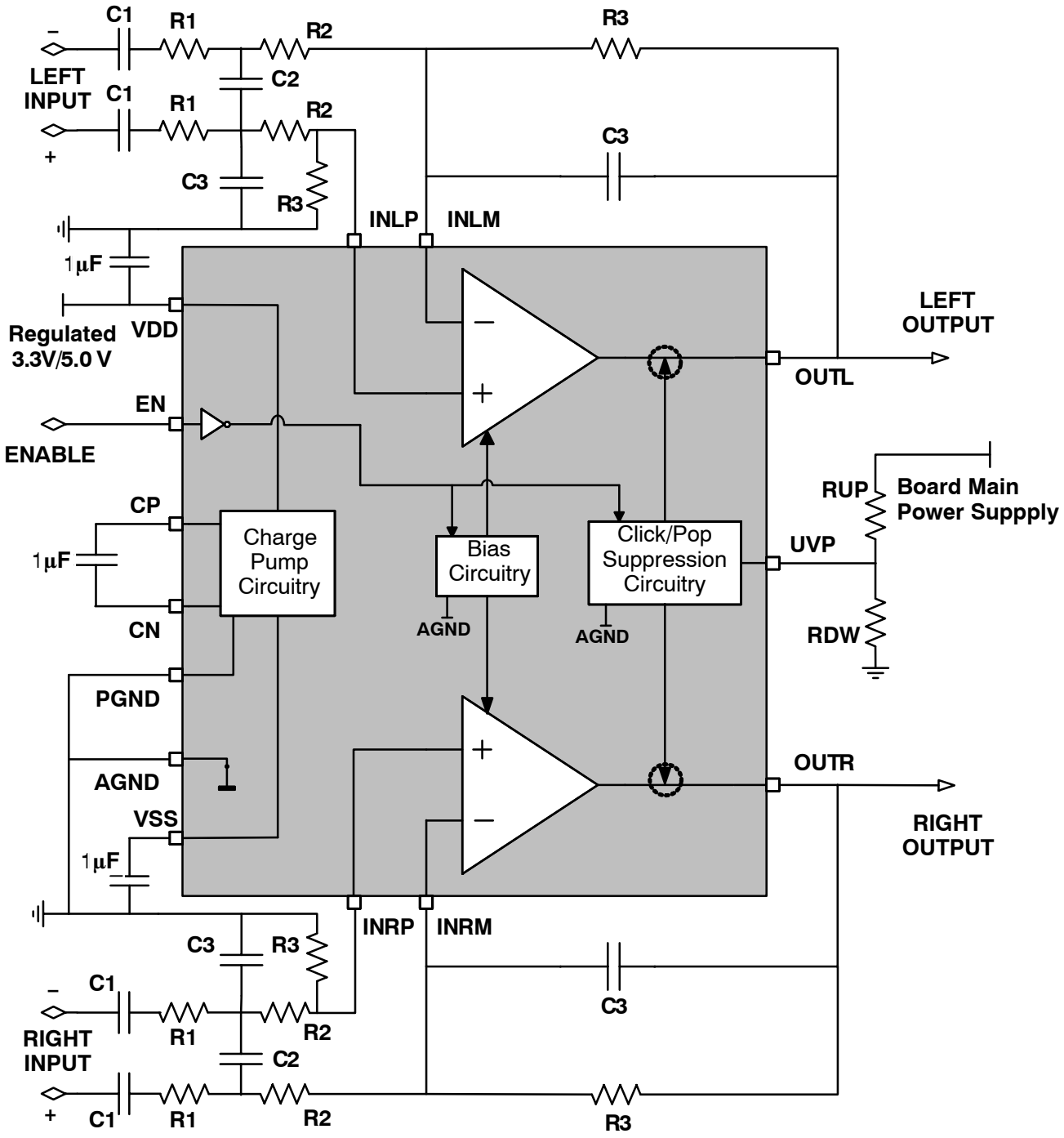
CAPACITIVE LOAD

The NCS2632 has the ability to drive a high capacitive load up to 220 pF directly. Higher capacitive loads can be accepted by adding a series resistor of 10 Ω or larger.

ESD PERFORMANCE

From the system level perspective, the outputs of the NCS2632 are rated to Level 4 of the IEC61000−4−2 ESD standard. Using the contact discharge method, the outputs pass a ±8 kV discharge with an RC network of R = 33 ohms and C = 1 nF at each output to simulate the application environment.

APPLICATION SCHEMATIC



R1 = R2 = R3 = 5.6 kΩ, C1 = 100 nF, C2 = 470 pF, C3 = 220 pF

Figure 28. Application Schematic

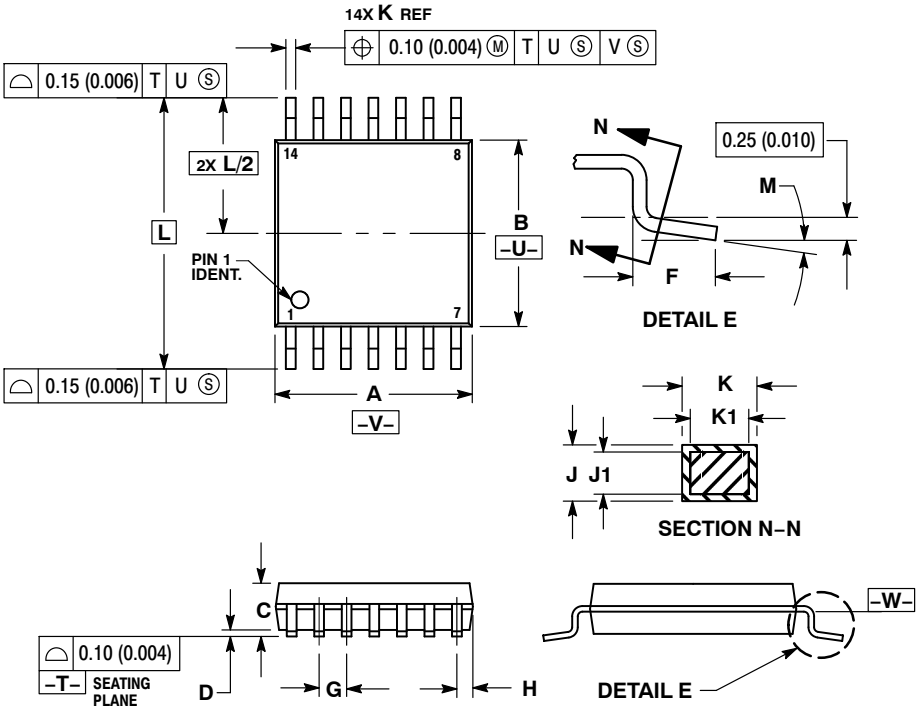
ORDERING INFORMATION

Device	Package	Shipping†
NCS2632DTBR2G	TSSOP−14 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

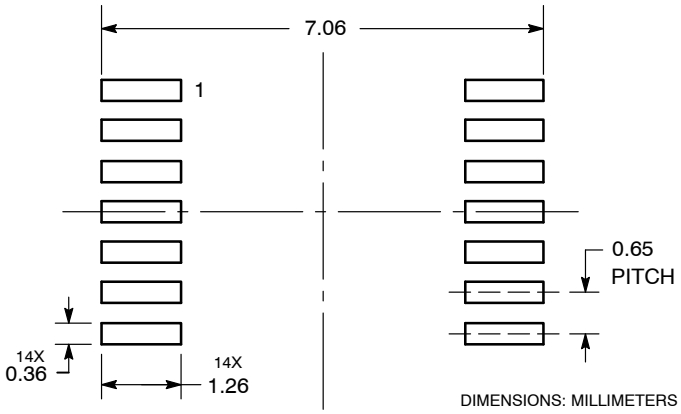
TSSOP−14
CASE 948G
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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