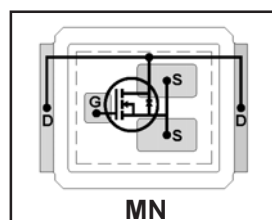


IRF6644PbF IRF6644TRPbF

DirectFET™ Power MOSFET ②

Typical values (unless otherwise specified)

V_{DS}	V_{GS}	$R_{DS(on)}$
100V max	$\pm 20V$ max	10.3m Ω @ 10V
Q_g tot	Q_{gd}	$V_{gs(th)}$
35nC	11.5nC	3.7V



- RoHS Compliant ①
- Lead-Free (Qualified up to 260°C Reflow)
- Application Specific MOSFETs
- Ideal for High Performance Isolated Converter Primary Switch Socket
- Optimized for Synchronous Rectification
- Low Conduction Losses
- High $C_{dv/dt}$ Immunity
- Low Profile (<0.7mm)
- Dual Sided Cooling Compatible ①
- Compatible with existing Surface Mount Techniques ①

Applicable DirectFET Outline and Substrate Outline (see p.7,8 for details)①

SH	SJ	SP	MZ	MN					
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Description

The IRF6644PbF combines the latest HEXFET® Power MOSFET Silicon technology with the advanced DirectFET™ packaging to achieve the lowest on-state resistance in a package that has the footprint of an SO-8 and only 0.7 mm profile. The DirectFET package is compatible with existing layout geometries used in power applications, PCB assembly equipment and vapor phase, infra-red or convection soldering techniques, when application note AN-1035 is followed regarding the manufacturing methods and processes. The DirectFET package allows dual sided cooling to maximize thermal transfer in power systems, improving previous best thermal resistance by 80%.

The IRF6644PbF is optimized for primary side bridge topologies in isolated DC-DC applications, for wide range universal input Telecom applications (36V - 75V), and for secondary side synchronous rectification in regulated DC-DC topologies. The reduced total losses in the device coupled with the high level of thermal performance enables high efficiency and low temperatures, which are key for system reliability improvements, and makes this device ideal for high performance isolated DC-DC converters.

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{DS}	Drain-to-Source Voltage	100	V
V_{GS}	Gate-to-Source Voltage	± 20	
I_D @ $T_A = 25^\circ C$	Continuous Drain Current, V_{GS} @ 10V ③	10.3	A
I_D @ $T_A = 70^\circ C$	Continuous Drain Current, V_{GS} @ 10V ③	8.3	
I_D @ $T_C = 25^\circ C$	Continuous Drain Current, V_{GS} @ 10V ④	60	
I_{DM}	Pulsed Drain Current ⑤	82	
E_{AS}	Single Pulse Avalanche Energy ⑥	220	mJ
I_{AR}	Avalanche Current ⑤	6.2	A

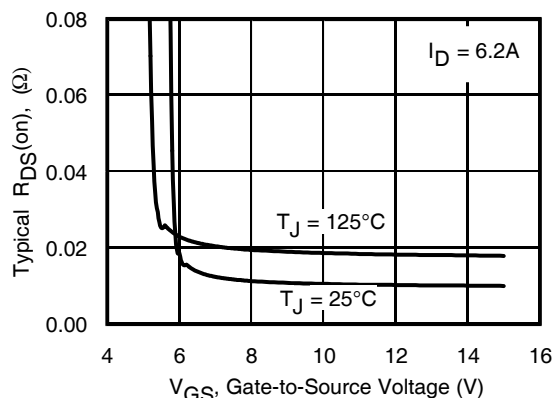


Fig 1. Typical On-Resistance Vs. Gate Voltage

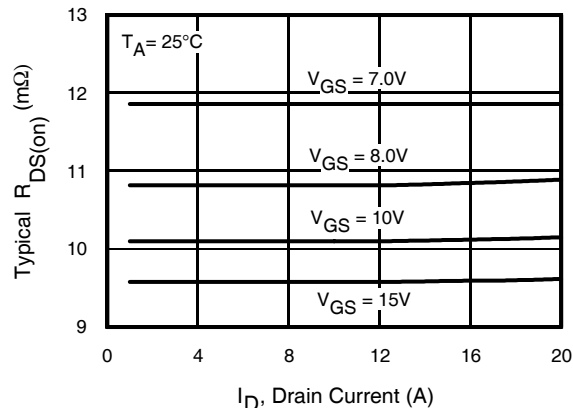


Fig 2. Typical On-Resistance Vs. Drain Current

Notes:

① Click on this section to link to the appropriate technical paper.

② Click on this section to link to the DirectFET Website.

③ Surface mounted on 1 in. square Cu board, steady state.

www.irf.com

④ T_C measured with thermocouple mounted to top (Drain) of part.

⑤ Repetitive rating; pulse width limited by max. junction temperature.

⑥ Starting $T_J = 25^\circ C$, $L = 12mH$, $R_G = 25\Omega$, $I_{AS} = 6.2A$.

Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	100	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.11	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	10.3	13	m Ω	$V_{GS} = 10V, I_D = 10.3A$ ①
$V_{GS(th)}$	Gate Threshold Voltage	2.8	—	4.8	V	$V_{DS} = V_{GS}, I_D = 150\mu A$
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-10	—	mV/ $^\circ\text{C}$	
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	$V_{DS} = 100V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 80V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$
g_{fs}	Forward Transconductance	15	—	—	S	$V_{DS} = 10V, I_D = 6.2A$
Q_g	Total Gate Charge	—	35	47	nC	$V_{DS} = 50V$ $V_{GS} = 10V$ $I_D = 6.2A$ See Fig. 15
Q_{gs1}	Pre-V _{th} Gate-to-Source Charge	—	8.0	—		
Q_{gs2}	Post-V _{th} Gate-to-Source Charge	—	1.6	—		
Q_{gd}	Gate-to-Drain Charge	—	11.5	17.3		
Q_{godr}	Gate Charge Overdrive	—	13	—		
Q_{sw}	Switch Charge ($Q_{gs2} + Q_{gd}$)	—	13.1	—		
Q_{oss}	Output Charge	—	17	—	nC	$V_{DS} = 16V, V_{GS} = 0V$
R_G	Gate Resistance	—	1.0	2.0	Ω	
$t_{d(on)}$	Turn-On Delay Time	—	17	—	ns	$V_{DD} = 50V, V_{GS} = 10V$ ① $I_D = 6.2A$ $R_G = 6.2\Omega$
t_r	Rise Time	—	26	—		
$t_{d(off)}$	Turn-Off Delay Time	—	34	—		
t_f	Fall Time	—	16	—		
C_{iss}	Input Capacitance	—	2210	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	420	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	100	—		$f = 1.0\text{MHz}$
C_{oss}	Output Capacitance	—	2120	—		$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0\text{MHz}$
C_{oss}	Output Capacitance	—	240	—		$V_{GS} = 0V, V_{DS} = 80V, f = 1.0\text{MHz}$

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	10	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ②	—	—	82		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 6.2A, V_{GS} = 0V$ ①
t_{rr}	Reverse Recovery Time	—	42	63	ns	$T_J = 25^\circ\text{C}, I_F = 6.2A, V_{DD} = 50V$
Q_{rr}	Reverse Recovery Charge	—	69	100	nC	$di/dt = 100A/\mu s$ ①

Notes:

⑤ Repetitive rating; pulse width limited by max. junction temperature.

⑦ Pulse width $\leq 400\mu s$; duty cycle $\leq 2\%$.

Absolute Maximum Ratings

	Parameter	Max.	Units
P _D @T _A = 25°C	Power Dissipation ①	2.8	W
P _D @T _A = 70°C	Power Dissipation ①	1.8	
P _D @T _C = 25°C	Power Dissipation ④	89	
T _P	Peak Soldering Temperature	270	°C
T _J	Operating Junction and	-40 to + 150	
T _{STG}	Storage Temperature Range		

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient ①⑤	—	45	$^\circ\text{C/W}$
$R_{\theta JA}$	Junction-to-Ambient ②⑤	12.5	—	
$R_{\theta JA}$	Junction-to-Ambient ③⑤	20	—	
$R_{\theta JC}$	Junction-to-Case ④⑤	—	1.4	
$R_{\theta J-PCB}$	Junction-to-PCB Mounted	1.0	—	

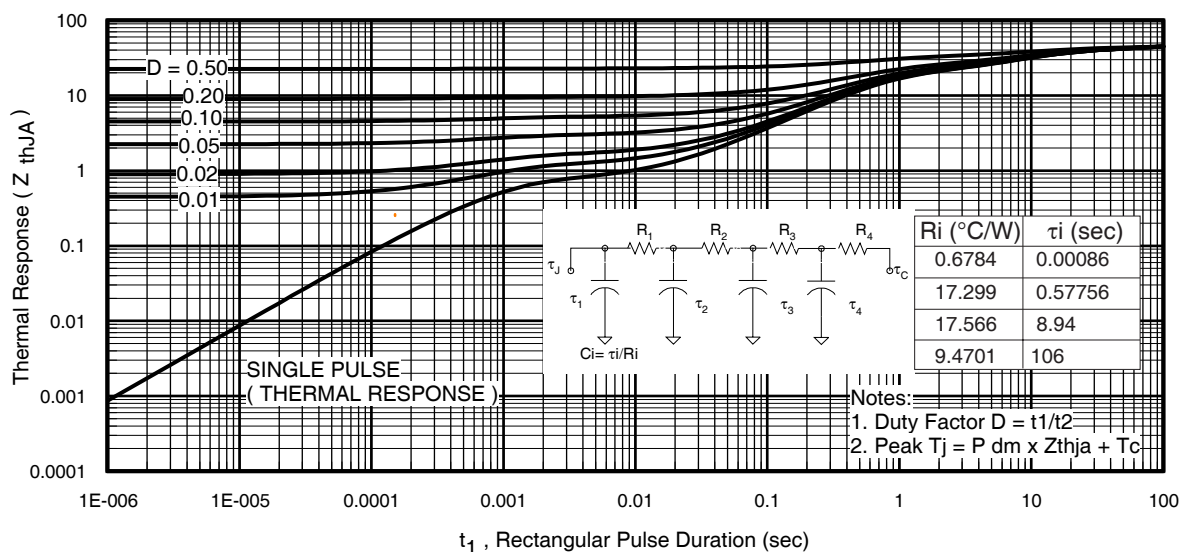
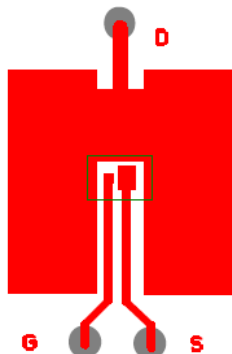


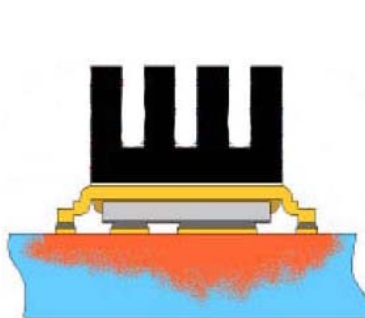
Fig 3. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient ①

Notes:

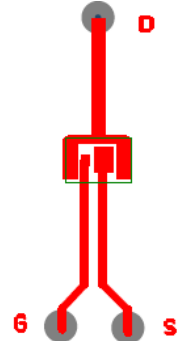
- ③ Surface mounted on 1 in. square Cu board, steady state.
- ④ T_C measured with thermocouple incontact with top (Drain) of part.
- ⑤ Mounted on minimum footprint full size board with metalized back and with small clip heatsink.
- ⑥ Used double sided cooling, mounting pad with large heatsink.
- ⑦ R_{θ} is measured at T_J of approximately 90°C .



③ Surface mounted on 1 in. square Cu board (still air).



⑥ Mounted to a PCB with small clip heatsink (still air)



⑤ Mounted on minimum footprint full size board with metalized back and with small clip heatsink (still air)

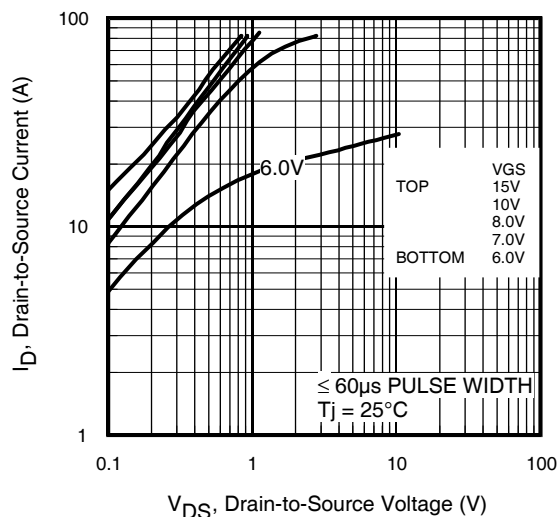


Fig 4. Typical Output Characteristics

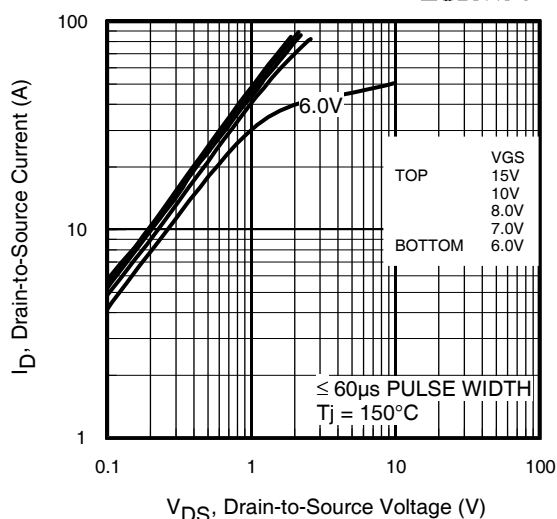


Fig 5. Typical Output Characteristics

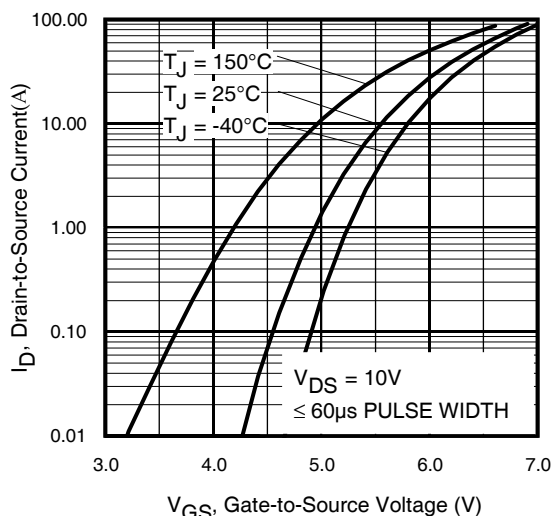


Fig 6. Typical Transfer Characteristics

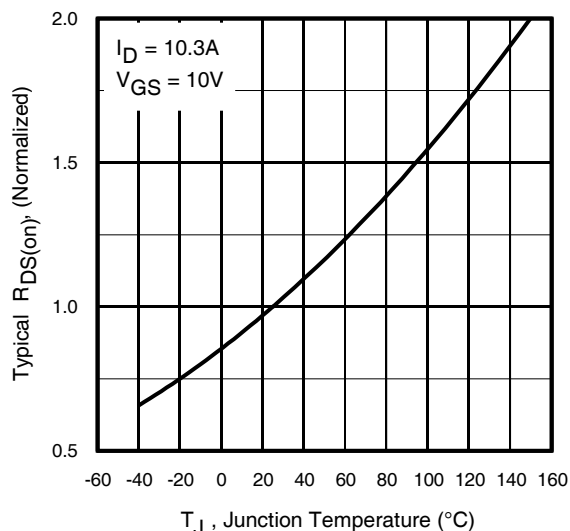


Fig 7. Normalized On-Resistance vs. Temperature

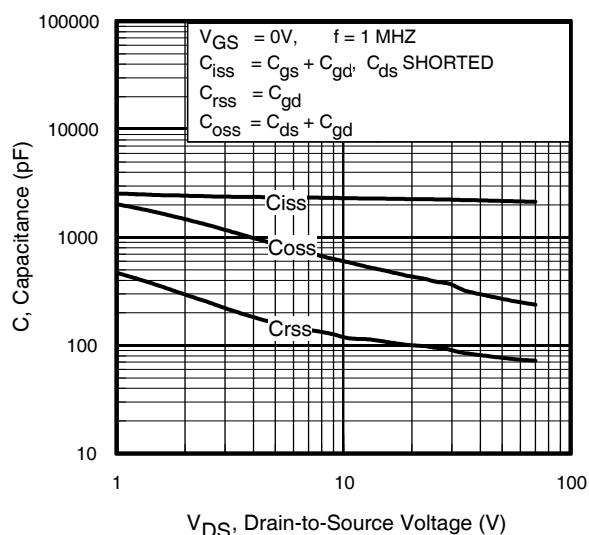


Fig 8. Typical Capacitance vs. Drain-to-Source Voltage

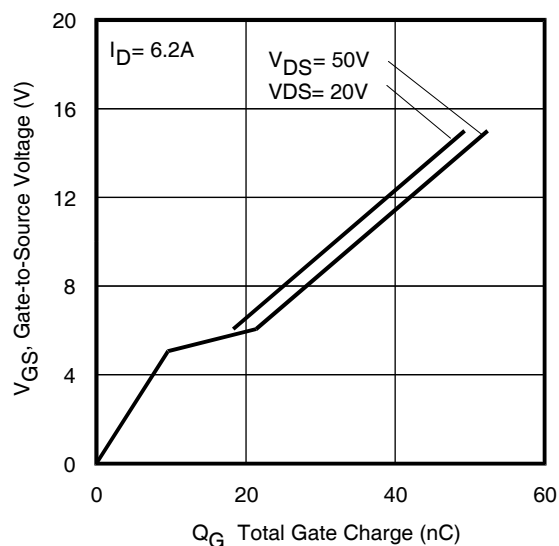


Fig 9. Typical Total Gate Charge vs. Gate-to-Source Voltage

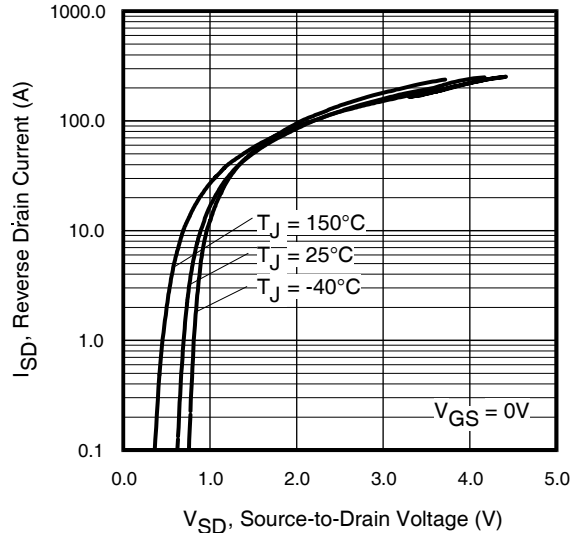


Fig 10. Typical Source-Drain Diode Forward Voltage

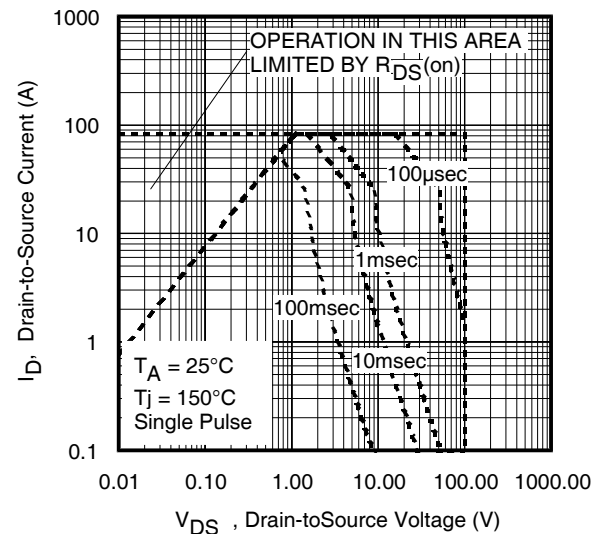


Fig11. Maximum Safe Operating Area

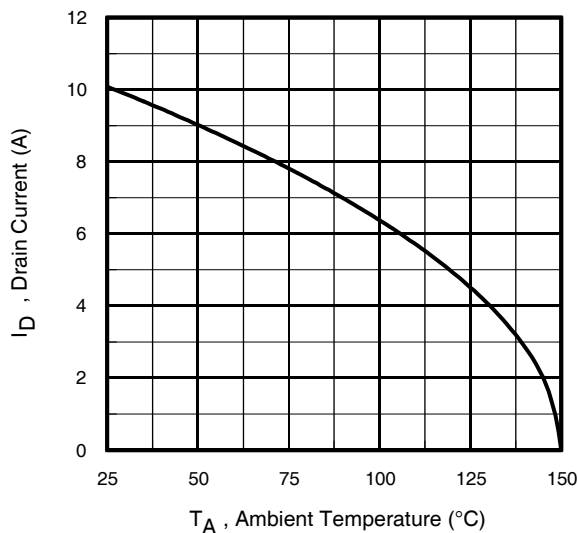


Fig 12. Maximum Drain Current vs. Ambient Temperature

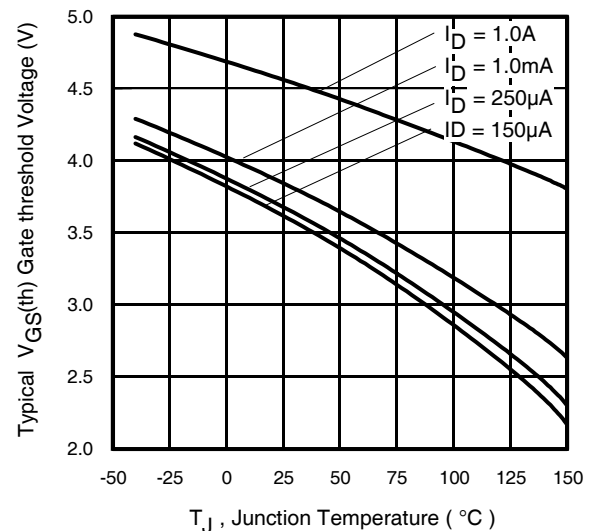


Fig 13. Typical Threshold Voltage vs. Junction Temperature

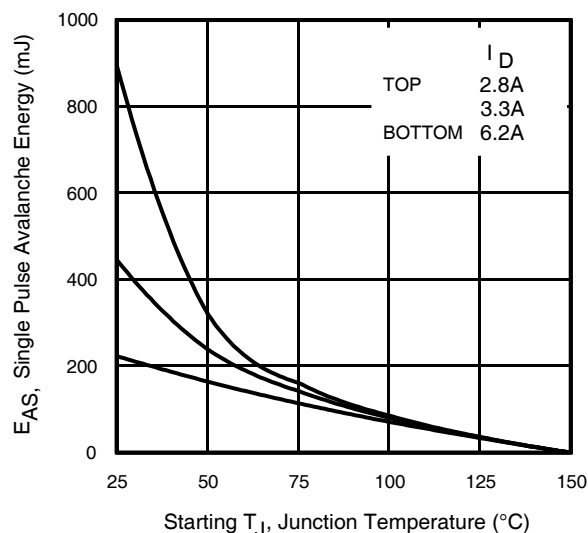


Fig 14. Maximum Avalanche Energy Vs. Drain Current

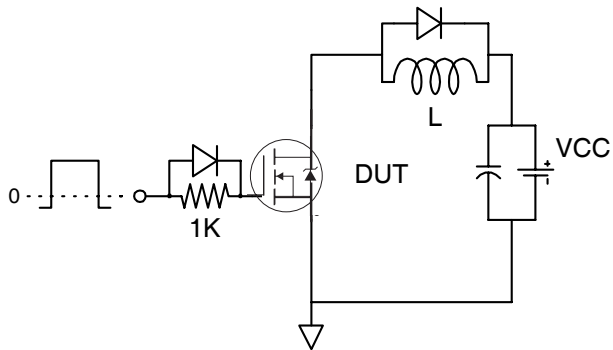


Fig 15a. Gate Charge Test Circuit

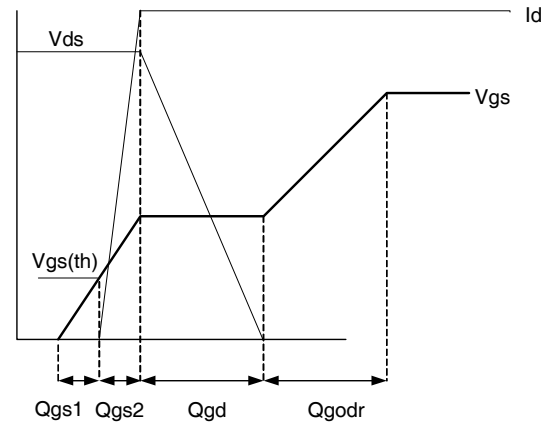


Fig 15b. Gate Charge Waveform

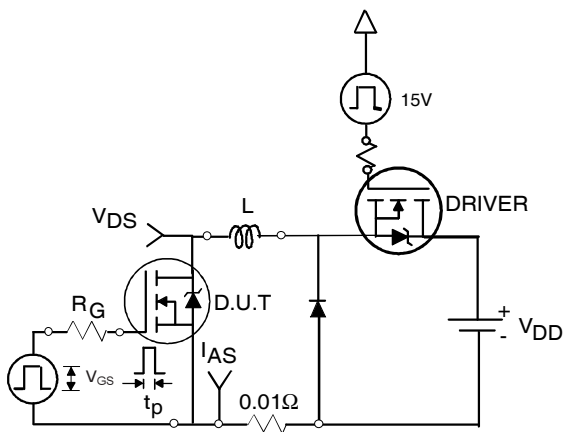


Fig 16b. Unclamped Inductive Test Circuit

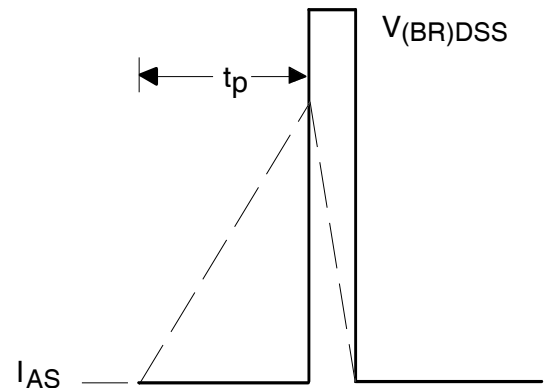


Fig 16c. Unclamped Inductive Waveforms

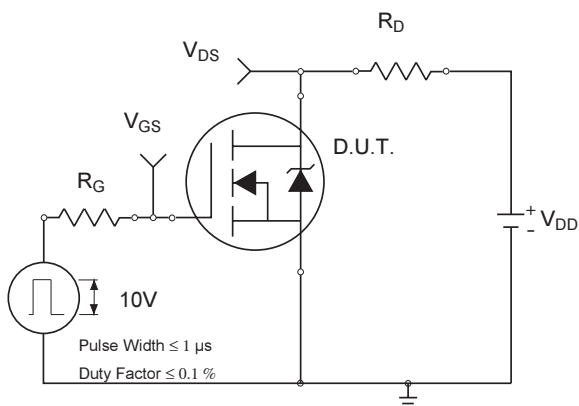


Fig 17a. Switching Time Test Circuit

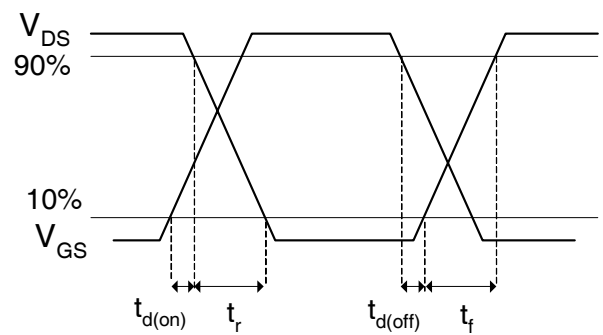


Fig 17b. Switching Time Waveforms

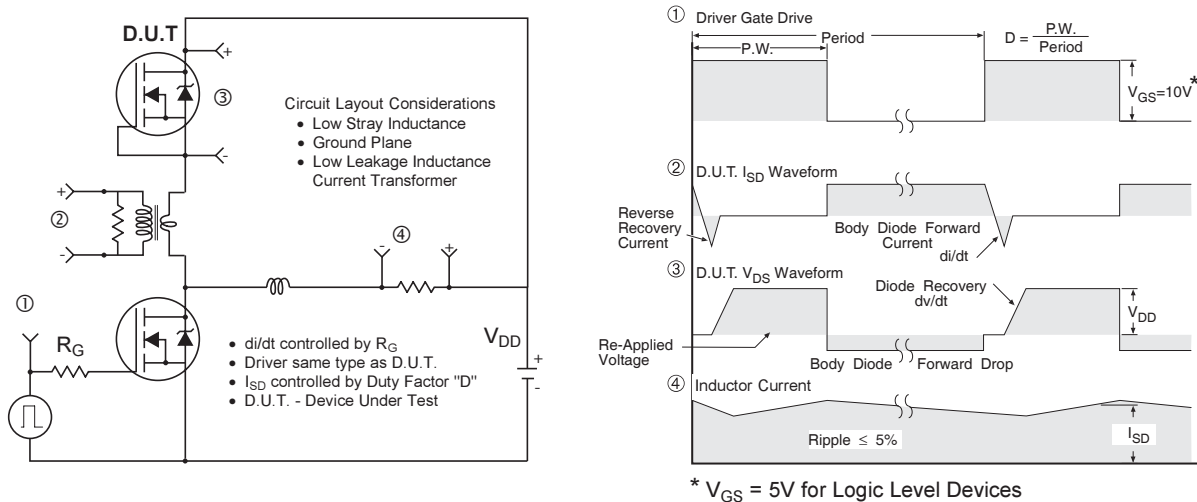
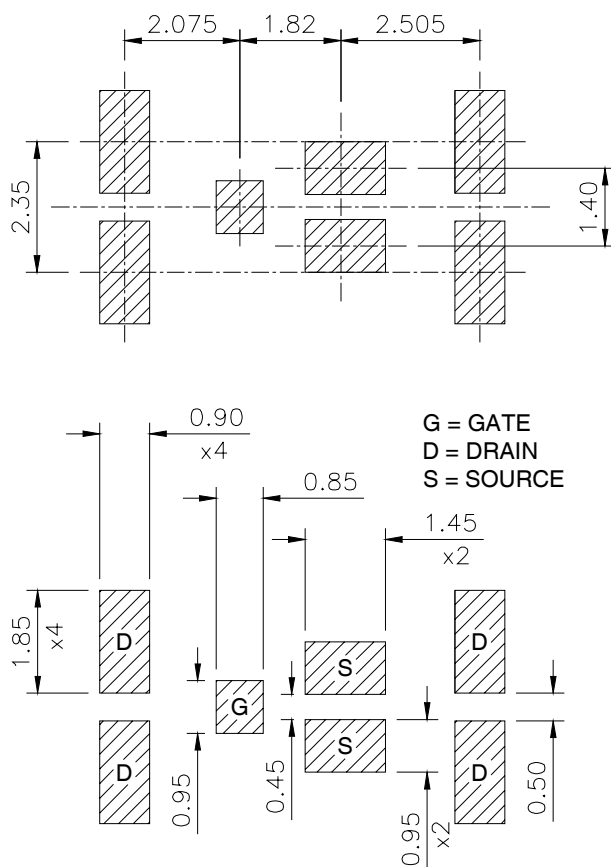


Fig 18. Diode Reverse Recovery Test Circuit for N-Channel HEXFET® Power MOSFETs

DirectFET™ Substrate and PCB Layout, MN Outline (Medium Size Can, N-Designation).

Please see DirectFET application note AN-1035 for all details regarding the assembly of DirectFET.

This includes all recommendations for stencil and substrate designs.

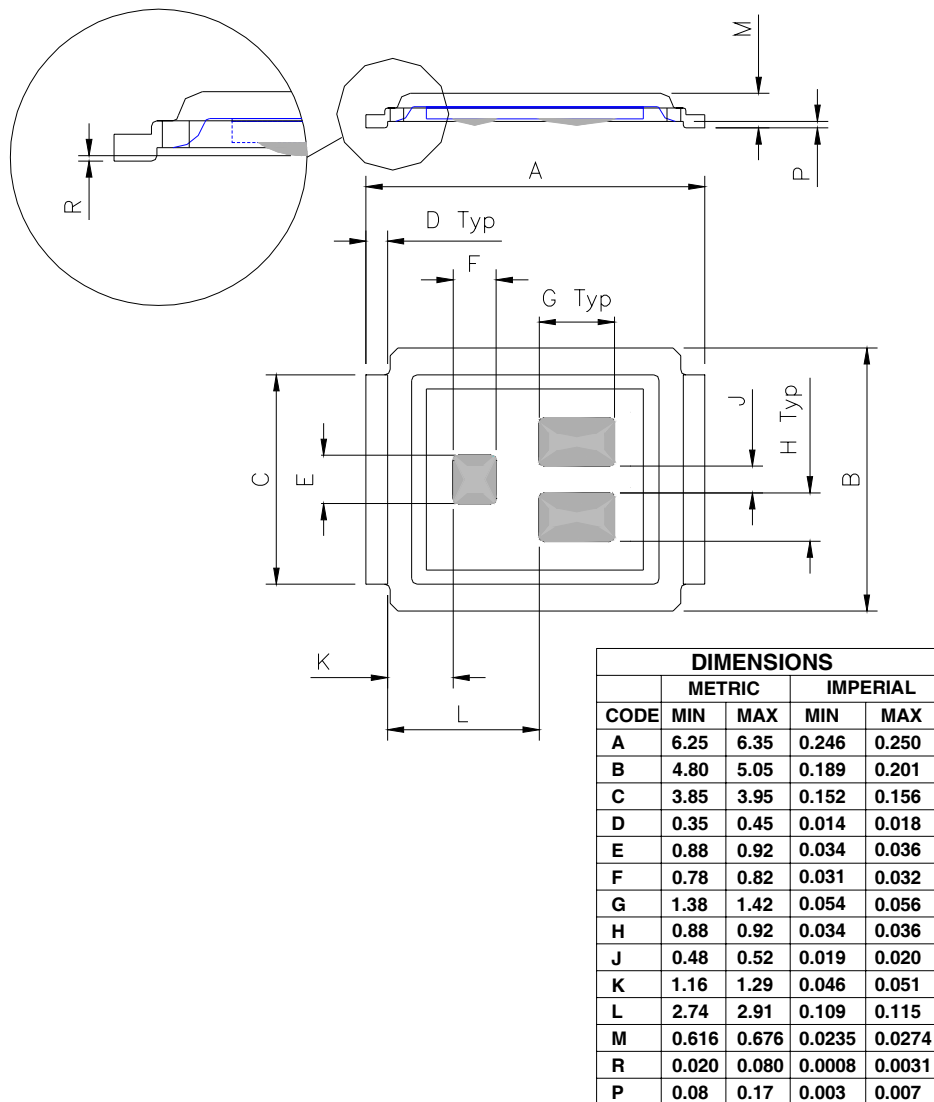


IRF6644PbF

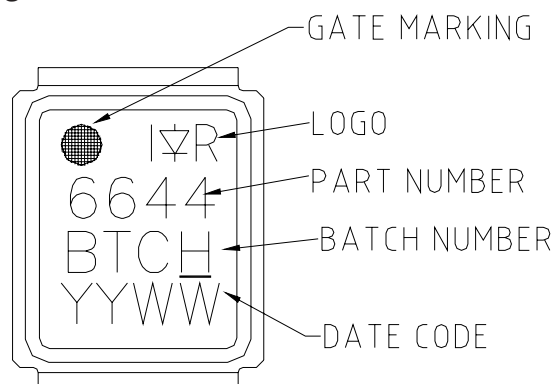
DirectFET™ Outline Dimension, MN Outline (Medium Size Can, N-Designation).

Please see DirectFET application note AN-1035 for all details regarding the assembly of DirectFET.

This includes all recommendations for stencil and substrate designs.

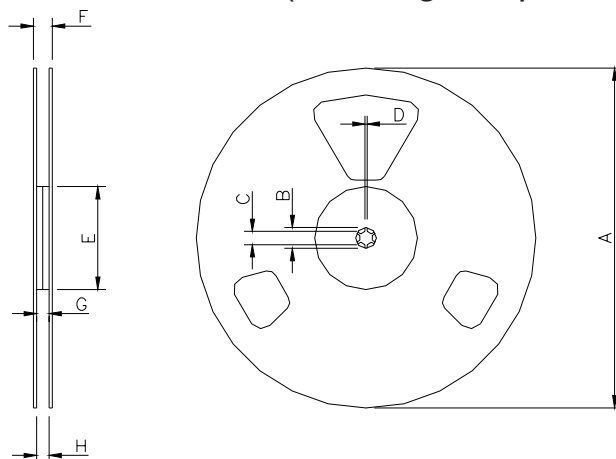


DirectFET™ Part Marking



Note: Line above the last character of the date-code indicates "Lead-Free".

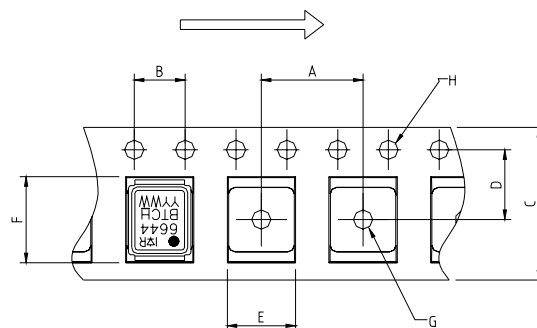
DirectFET™ Tape & Reel Dimension (Showing component orientation).



NOTE: Controlling dimensions in mm
Std reel quantity is 4800 parts. (ordered as IRF6644TRPBF). For 1000 parts on 7" reel, order IRF6644TR1PBF

REEL DIMENSIONS									
STANDARD OPTION (QTY 4800)					TR1 OPTION (QTY 1000)				
CODE	METRIC		IMPERIAL		METRIC		IMPERIAL		
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
A	330.0	N.C	12.992	N.C	177.77	N.C	6.9	N.C	
B	20.2	N.C	0.795	N.C	19.06	N.C	0.75	N.C	
C	12.8	13.2	0.504	0.520	13.5	12.8	0.53	0.50	
D	1.5	N.C	0.059	N.C	1.5	N.C	0.059	N.C	
E	100.0	N.C	3.937	N.C	58.72	N.C	2.31	N.C	
F	N.C	18.4	N.C	0.724	N.C	13.50	N.C	0.53	
G	12.4	14.4	0.488	0.567	11.9	12.01	0.47	N.C	
H	11.9	15.4	0.469	0.606	11.9	12.01	0.47	N.C	

LOADED TAPE FEED DIRECTION



DIMENSIONS					
CODE	METRIC		IMPERIAL		
	MIN	MAX	MIN	MAX	
A	7.90	8.10	0.311	0.319	
B	3.90	4.10	0.154	0.161	
C	11.90	12.30	0.469	0.484	
D	5.45	5.55	0.215	0.219	
E	5.10	5.30	0.201	0.209	
F	6.50	6.70	0.256	0.264	
G	1.50	N.C	0.059	N.C	
H	1.50	1.60	0.059	0.063	

Data and specifications subject to change without notice.

This product has been designed and qualified for the Consumer market.

Qualification Standards can be found on IR's Web site.

International
IR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105

TAC Fax: (310) 252-7903

Visit us at www.irf.com for sales contact information.08/06

Note: For the most current drawings please refer to the IR website at:
<http://www.irf.com/package/>