4.5-V TO 20-V SYNCHRONOUS BUCK CONTROLLER WITH SYNCHRONIZATION AND POWER GOOD

Check for Samples: TPS40195

FEATURES

- **Input Operating Voltage Range: 4.5 V to 20 V**
- **Output Voltage as Low as 0.591 V ±0.5%**
- **180° Bi-Directional Out-of-Phase Synchronization**
- **Internal 5-V Regulator**
- **High and Low MOSFET Sense Overcurrent**
- **100 kHz to 600 kHz Switching Frequency**
- **Enable and Power Good**
- **Programmable UVLO and Hysteresis**
- **Thermal Shutdown at 150°C**
- **Selectable Soft-Start**
- **Pre-Bias Output Safe**

APPLICATIONS

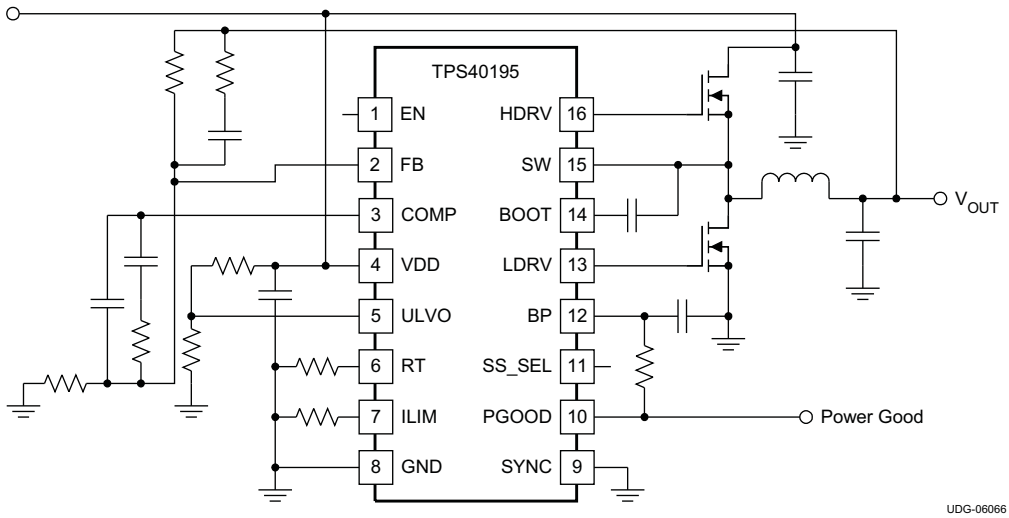
- **Digital TV**
- **Entry-Level and Midrange Servers**
- **Networking Equipment**
- **Non-Isolated DC-DC modules**

CONTENTS

DESCRIPTION

The TPS40195 is a flexible synchronous buck controller that operates from a nominal 4.5 V to 20 V supply. This controller implements voltage mode control with the switching frequency adjustable from 100 kHz to 600 kHz. Flexible features found on this device include selectable soft-start time, programmable short circuit limit, programmable undervoltage lockout (UVLO) and synchronization capability. An adaptive anti-cross conduction scheme is used to prevent shoot through current in the power FETs. Over-current detection is done by sensing the voltage drop across the low-side MOSFET when it is on, and comparing it with a user programmable threshold.

SIMPLIFIED APPLICATION DIAGRAM



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

The threshold is set with a single external resistor connected from ILIM to GND. Pulse-by-pulse limiting (to prevent current runaway) is provided by sensing the voltage across the high-side MOSFET when it is on and terminating the cycle when the voltage drop rises above a fixed threshold of 550 mV. When the controller senses an output short circuit, both MOSFETs are turned off and a timeout period is observed before attempting to restart. This provides limited power dissipation in the event of a sustained fault. Synchronization on this device is bi-directional. Devices can be synchronized 180° out of phase to a chosen master TPS40195 running at a fixed 250 kHz or 500 kHz, or can be synchronized to an outside clock source anywhere in the 100 kHz to 600 kHz range.

ORDERING INFORMATION

T_J	PACKAGE	QUANTITY	PACKAGING(1)	PART NUMBER
-40°C to 85°C	Plastic 16-Pin TSSOP (PW)	90	Tube	TPS40195PW
		2000	Reel	TPS40195PWR
	Plastic 16-Pin QFN (RGY)	250	Tape	TPS40195RGYT
		3000	Reel	TPS40195RGYR

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

DEVICE RATINGS

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

		TPS40195	UNIT
Input voltage range	VDD	–0.3 to 22	V
	SW	–5 to 25	
	BOOT	–0.3 to 30	
	HDRV	–5 to 30	
	BOOT–SW, HDRV–SW (Differential from BOOT or HDRV to SW)	–0.3 to 6	
	EN, FB, BP, LDRV, PGOOD, ILIM, SYNC, UVLO, SS_SEL, RT	–0.3 to 6	
	COMP	–0.3 to 3	
T_J	Operating junction temperature range	–40 to 150	°C
T_{stg}	Storage temperature	–55 to 150	

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{VDD}	Input voltage	4.5		20	V
T_J	Operating junction temperature	-40		125	°C

PACKAGE DISSIPATION RATINGS

PACKAGE	AIRFLOW (LFM)	$R_{\theta JA}$ High-K Board(1) (°C/W)	Power Rating (W) T_A = 25°C	Power Rating (W) T_A = 85°C
PW	0 (Natural Convection)	110	0.90	0.36
RGY	0 (Natural Convection)	49.2	2.0	0.81
	200	41.2	2.4	0.97
	400	37.7	2.6	1.0

(1) Ratings based on JEDEC High Thermal Conductivity (High K) Board. For more information on the test method, see TI Technical Brief SZZA017.

ELECTROSTATIC DISCHARGE (ESD) PROTECTION

	MIN	TYP	MAX	UNIT
Human Body Model (HBM)		2500		V
Charged Device Model (CDM)		1500		

ELECTRICAL CHARACTERISTICS

T_J = –40°C to 85°C, V_{VDD}= 12 V_{dc}, all parameters at zero power dissipation (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
REFERENCE						
V_{FB}	Feedback voltage range	0°C ≤ T_J ≤ 85°C	588	591	594	mV
		-40°C ≤ T_J ≤ 85°C	585	591	594	
INPUT SUPPLY						
V_{VDD}	Input voltage range		4.5		20.0	V
I_{VDD}	Operating current	V_{EN} = 3 V			4	mA
		V_{EN} < 0.6 V, V_{VDD} = 12 V		165	250	µA
		V_{EN} < 0.6 V, V_{VDD} = 20 V		230	330	
ON BOARD REGULATOR						
V_{BP}	Output voltage	V_{VDD} > 6 V, I_{BP} ≤ 10 mA	5.1	5.3	5.5	V
V_{DO}	Regulator dropout voltage, V_{VDD} - V_{BP}	V_{VDD} = 5 V, I_{BP} ≤ 25 mA		350	550	mV
I_{SC}	Regulator current limit threshold		75			mA
I_{BP}	Average current				75	
OSCILLATOR						
f_{SW}	Switching frequency	V_{RT} = V_{BP}	400	500	580	kHz
		V_{RT} = 0 V	200	250	290	
		R_{RT} = 100 kΩ		250		
V_{RMP}	Ramp amplitude(1)			1		V
SYNCHRONIZATION						
V_{INH}	High-level input voltage		2.5			V
V_{INL}	Low-level input voltage				0.5	
$T_{F(max)}$	Maximum input fall time(1)				100	ns
V_{OH}	High-level output voltage	I_{SYNC} = 100 µA, sourcing	3.5			V
V_{OL}	Low-level output voltage	I_{SYNC} = 100 µA, sinking			0.3	
T_F	Output fall time(1)	C_{SYNC} =25 pF		10	25	ns
T_R	Output rise time(1)			100	300	

(1) Specified by design. Not production tested.

ELECTRICAL CHARACTERISTICS (continued)

T_J = –40°C to 85°C, V_{VDD}= 12 V_{dc}, all parameters at zero power dissipation (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PWM						
D_{MAX}	Maximum duty cycle (2)		85%			
$t_{ON(min)}$	Minimum controlled pulse (2)				130	ns
t_{DEAD}	Output driver dead time	HDRV off to LDRV on		50		ns
		LDRV off to HDRV on		25		
SOFT-START						
t_{SS}	Soft-start time	V_{SS_SEL} = 0 V, f_{SW} = 250 kHz		4.8		ms
		V_{SS_SEL} = 0 V, f_{SW} = 500 kHz		2.4		
		V_{SS_SEL} = Floating, f_{SW} = 250 kHz		2.4		
		V_{SS_SEL} = Floating, f_{SW} = 500 kHz		1.2		
		V_{SS_SEL} = V_{BP}, f_{SW} = 250 kHz		1.2		
		V_{SS_SEL} = V_{BP}, f_{SW} = 500 kHz		0.6		
ERROR AMPLIFIER						
GBWP	Gain bandwidth product (2)		7	10		MHz
A_{OL}	DC gain (2)		60			dB
I_{FB}	Input bias current (current out of FB pin)				100	nA
I_{EAOP}	Output source current	V_{FB} = 0 V	1			mA
I_{EAOM}	Output sink current	V_{FB} = 2 V	1			
SHORT CIRCUIT PROTECTION						
$t_{PSS(min)}$	Minimum pulse during short circuit (2)			250		ns
t_{BLNK}	Blanking time (2)		60	90	120	
t_{OFF}	Off-time between restart attempts			40		ms
I_{ILIM}	ILIM pin bias current	T_J = 25°C	7	9	11	µA
$V_{ILIMOFST}$	Low side comparator offset voltage		-20	0	20	mV
V_{ILIMH}	Short circuit threshold voltage on high-side MOSFET	T_J = 25°C	400	550	650	mV
OUTPUT DRIVERS						
R_{HDHI}	High-side driver pull-up resistance	V_{BOOT} - V_{SW} = 4.5 V, I_{HDRV} = -100 mA		3	6	Ω
R_{HDLO}	High-side driver pull-down resistance	V_{BOOT} - V_{SW} = 4.5 V, I_{HDRV} = 100 mA		1.5	3.0	
R_{LDHI}	Low-side driver pull-up resistance	I_{LDRV} = -100 mA		2.5	5.0	
R_{LDLO}	Low-side driver pull-down resistance	I_{LDRV} = 100 mA		0.8	1.5	
t_{HRISE}	High-side driver rise time (2)	C_{LOAD} = 1 nF		15	35	ns
t_{HFALL}	High-side driver fall time (2)			10	25	
t_{LRISE}	Low-side driver rise time (2)			15	35	
t_{LFALL}	Low-side driver fall time (2)			10	25	
UVLO						
V_{UVLOBP}	BP5 UVLO threshold voltage		3.9	4.1	4.3	V
$V_{UVLOBPH}$	BP5 UVLO hysteresis voltage			800		mV
V_{UVLO}	Turn-on voltage		1.125	1.26	1.375	V
I_{UVLO}	UVLO pin hysteresis current	V_{UVLO} = 1.375 V		5.2		µA
SHUTDOWN						
V_{IH}	High-level input voltage, EN			1.9	3	V
V_{IL}	Low-level input voltage, EN		0.6			
POWER GOOD						

(2) Specified by design. Not production tested.

ELECTRICAL CHARACTERISTICS (continued)

T_J = –40°C to 85°C, V_{VDD}= 12 V_{dc}, all parameters at zero power dissipation (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OV}	Feedback voltage limit for power good			650		mV
V_{UV}	Feedback voltage limit for power good			530		
V_{PG_HYST}	Powergood hysteresis voltage at FB pin			30		
R_{PGD}	Pulldown resistance of PGD pin	V_{FB} < 530 mV or V_{FB} > 650 mV		7	20	Ω
I_{PDGLK}	Leakage current	530 mV ≤ V_{FB} ≤ 650 mV V_{PGOOD} = 5V		7	12	µA
BOOT DIODE						
V_{DFWD}	Bootstrap diode forward voltage	I_{BOOT} = 5 mA	0.5	0.8	1.2	V
THERMAL SHUTDOWN						
T_{JSD}	Junction shutdown temperature (3)			150		°C
T_{JSDH}	Hysteresis(3)			20		

(3) Specified by design. Not production tested.

TYPICAL CHARACTERISTICS

INPUT CURRENT vs JUNCTION TEMPERATURE

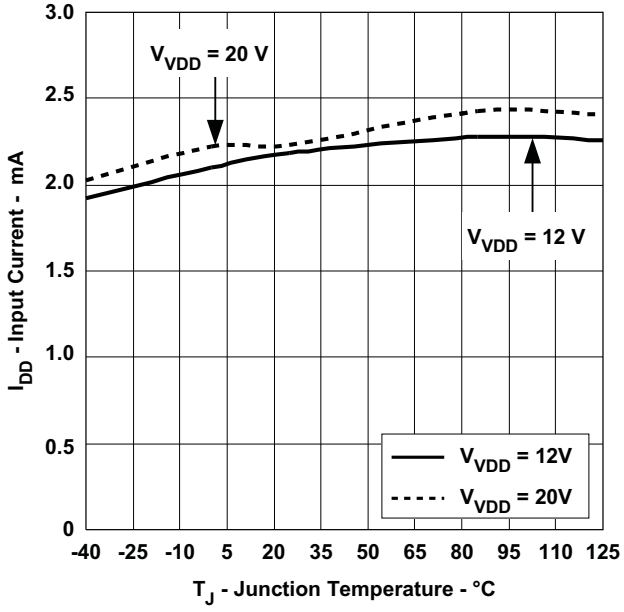


Figure 1.

OPERATING CURRENT IN SHUTDOWN vs JUNCTION TEMPERATURE

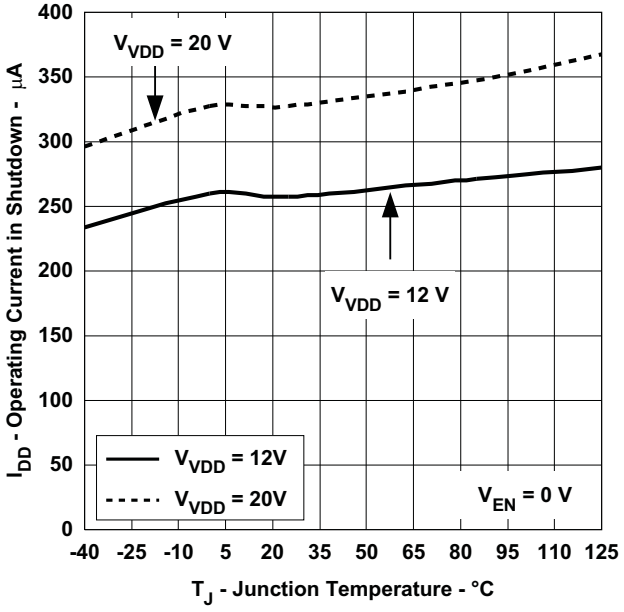


Figure 2.

POWERGOOD LEAKAGE CURRENT vs JUNCTION TEMPERATURE

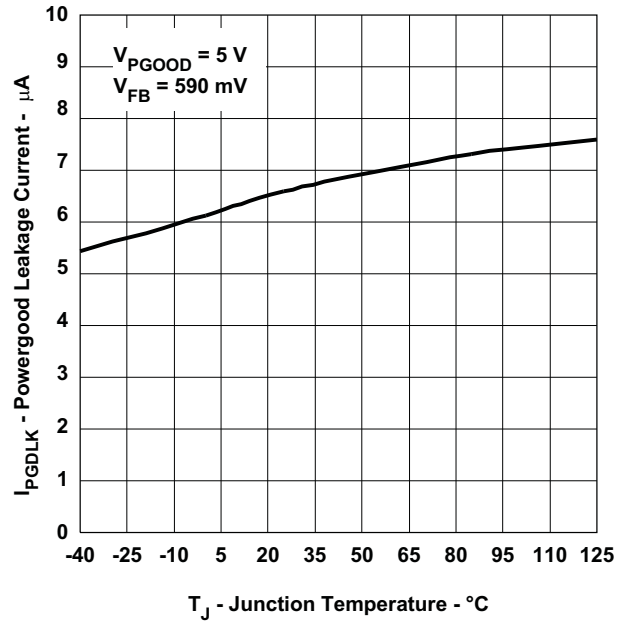


Figure 3.

CURRENT LIMIT OFFSET VOLTAGE vs JUNCTION TEMPERATURE

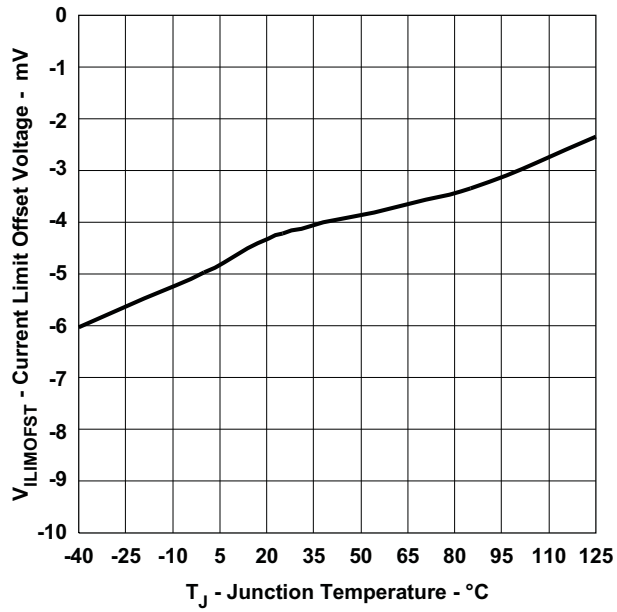


Figure 4.

TYPICAL CHARACTERISTICS (continued)

RELATIVE OVERCURRENT TRIP POINT vs FREEWHEEL TIME

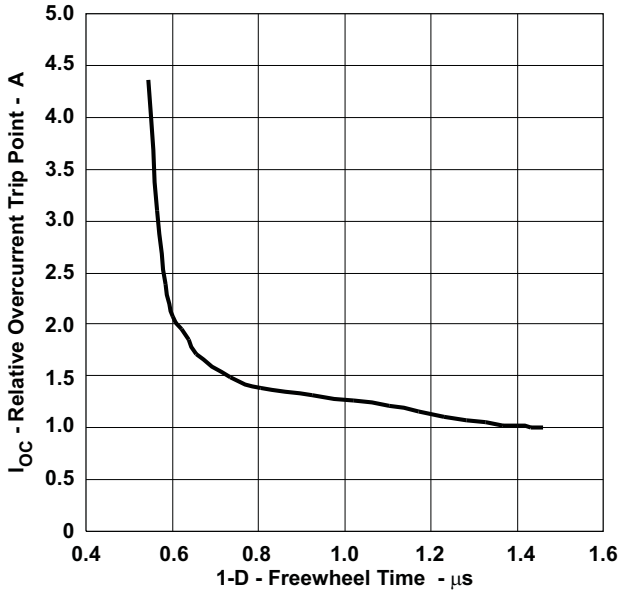


Figure 5.

EN THRESHOLD VOLTAGES vs JUNCTION TEMPERATURE

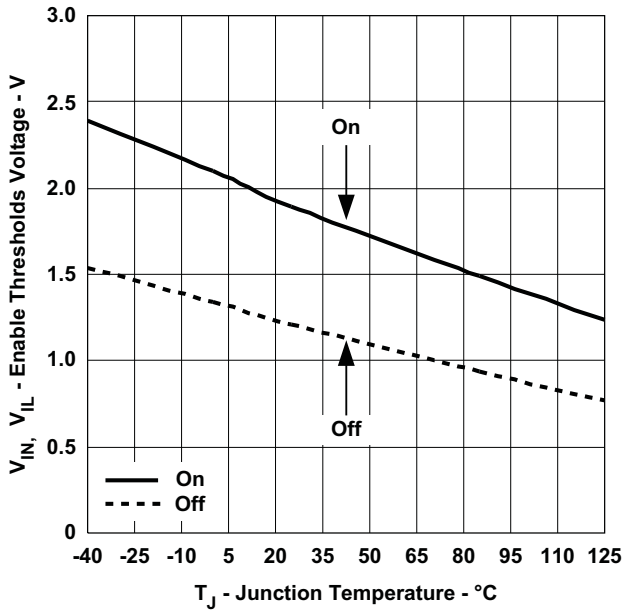


Figure 6.

SWITCHING FREQUENCY CHANGE vs JUNCTION TEMPERATURE

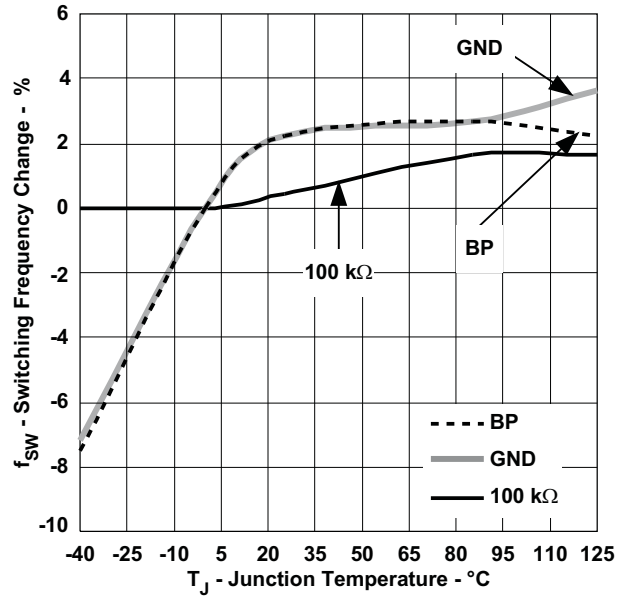


Figure 7.

BP SHORT CIRCUIT CURRENT vs JUNCTION TEMPERATURE

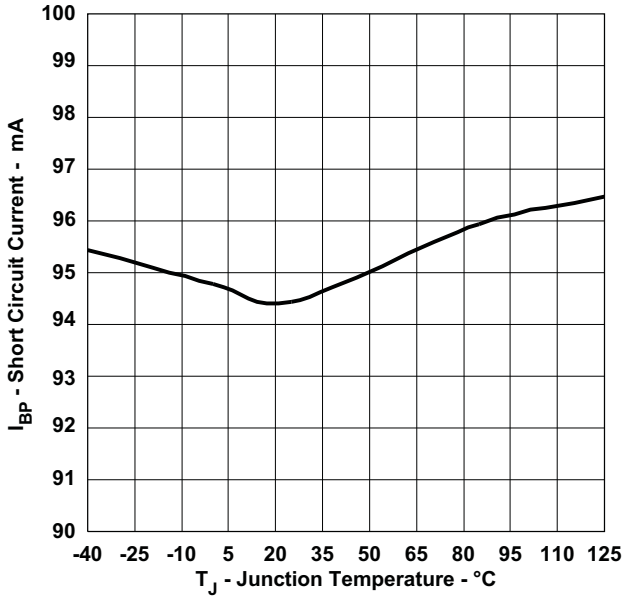


Figure 8.

TYPICAL CHARACTERISTICS (continued)

BP DROPOUT VOLTAGE vs JUNCTION TEMPERATURE

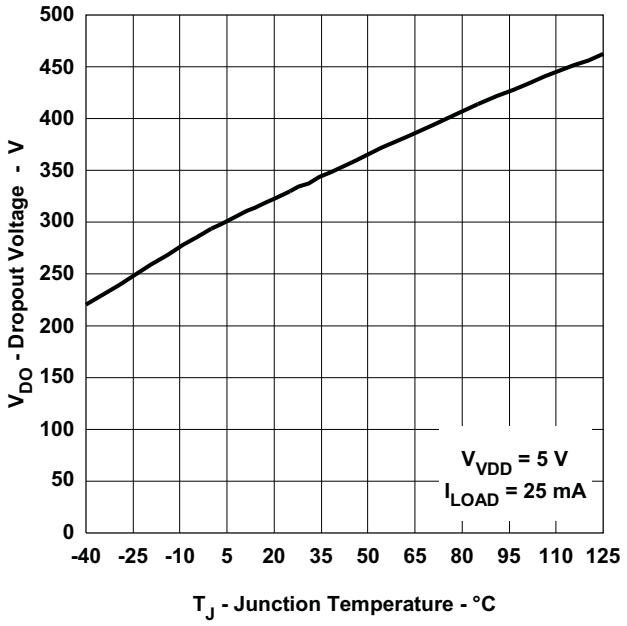


Figure 9.

UNDERVOLTAGE LOCKOUT THRESHOLD vs JUNCTION TEMPERATURE

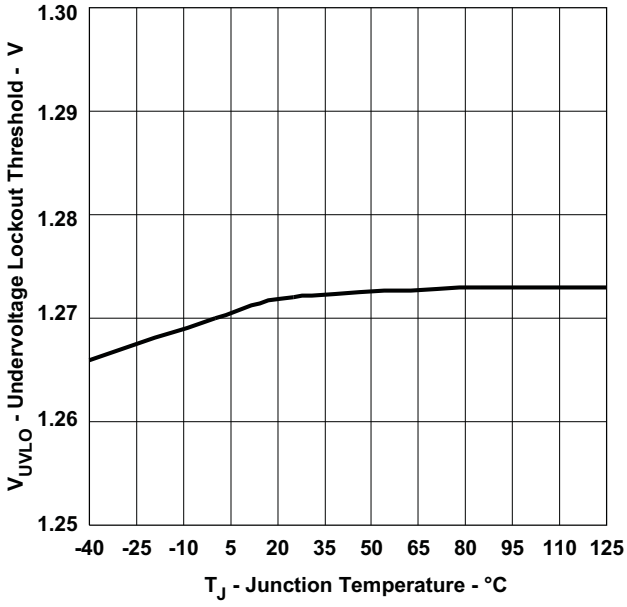


Figure 10.

UNDERVOLTAGE LOCKOUT HYSTERESIS vs JUNCTION TEMPERATURE

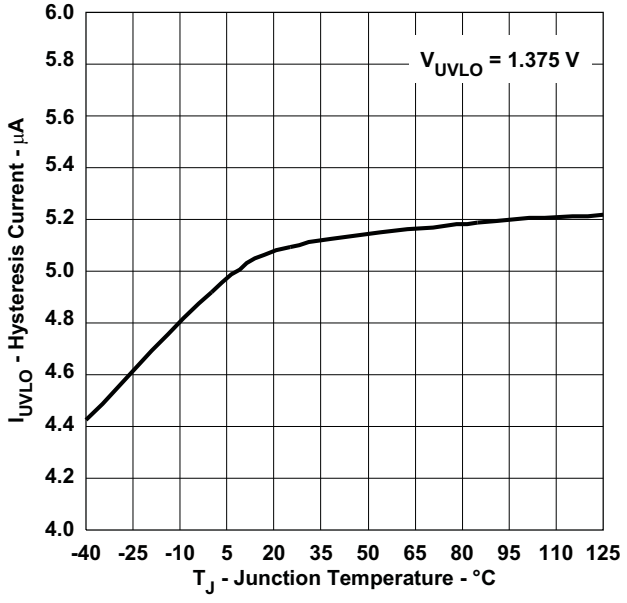


Figure 11.

BP UNDERVOLTAGE LOCKOUT VOLTAGE vs JUNCTION TEMPERATURE

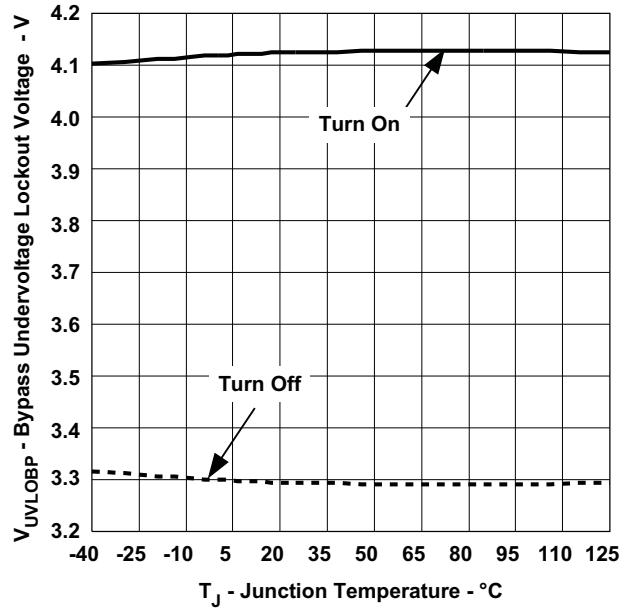


Figure 12.

TYPICAL CHARACTERISTICS (continued)

FEEDBACK BIAS CURRENT vs JUNCTION TEMPERATURE

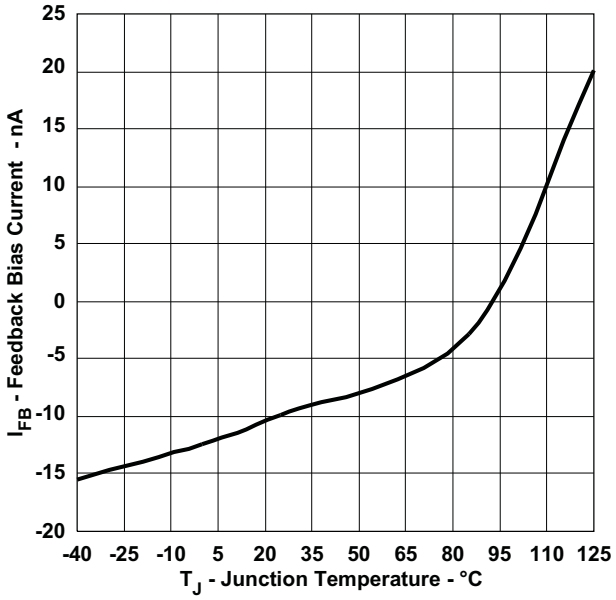


Figure 13.

RELATIVE FEEDBACK VOLTAGE CHANGE vs JUNCTION TEMPERATURE

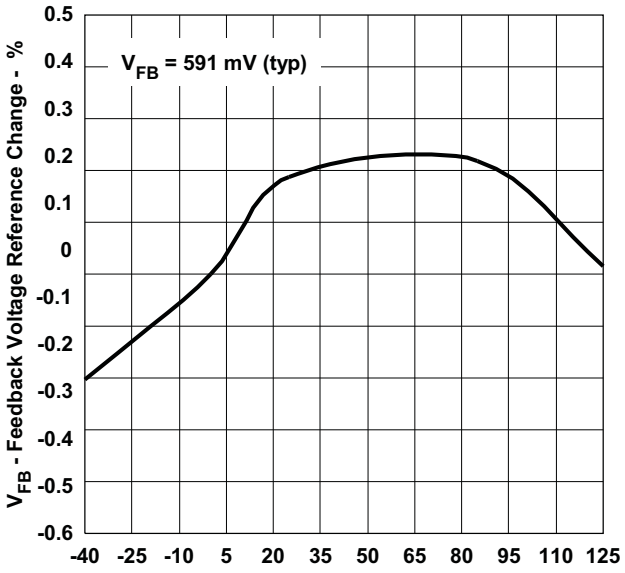


Figure 14.

OSCILLATOR FREQUENCY vs TIMING RESISTANCE

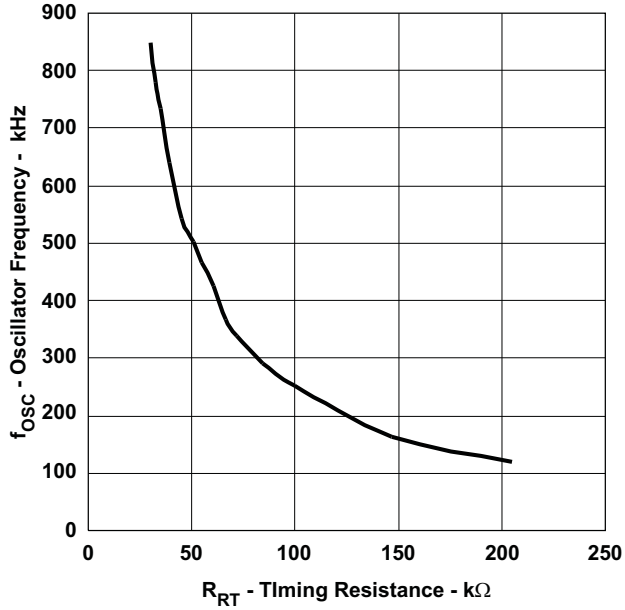


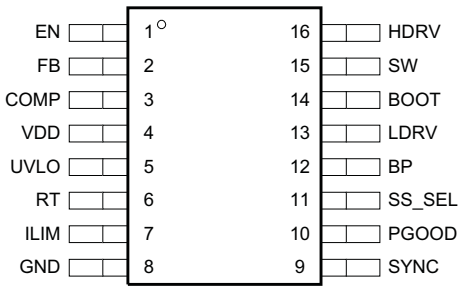
Figure 15.

DEVICE INFORMATION

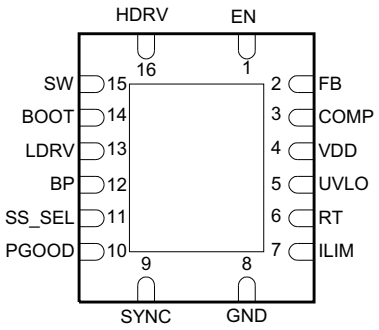
TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
BOOT	14	I	Gate drive voltage for the high-side N-channel MOSFET. A 100-nF capacitor (typical) must be connected between this pin and SW.
BP	12	O	Output bypass for the internal regulator. Connect a capacitor of 1-µF (or greater) from this pin to GND. Larger capacitors, up to 4.7µF will improve noise performance with a low side FET Qg over 25nC. Do not connect to VDD or drive externally. This regulator is turned off when ENABLE is pulled low
COMP	3	O	Output of the error amplifier.
EN	1	I	Logic level input which starts or stops the controller from an external user command. A high-level turns the controller on. A weak internal pull-up holds this pin high so that the pin may be left floating if this function is not used. Observe interface cautions in applications information.
FB	2	I	Inverting input to the error amplifier. In normal operation the voltage on this pin is equal to the internal reference voltage (591 mV typical)
GND	8	-	Common reference for the device
HDRV	16	O	Gate drive output to the high-side N-channel FET.
ILIM	7	I	Current limit. Sets short circuit protection threshold for low-side MOSFET sensing. Connect a resistor to GND to set the threshold
LDRV	13	O	Gate drive output for the low side N-channel FET.
PGOOD	10	O	Open drain power good output. Pulls low under any fault condition, soft start is active or if the FB pin voltage is outside the specified voltage window.
RT	6	I	Switching frequency programming pin. Also determines function of SYNC pin. Connected to GND for 250 kHz operation and using SYNC as an output. Connect to BP for 500-kHz operation and using SYNC as an output. Connect a resistor to GND to program a frequency and allow SYNC to accept synchronization pulses. If RT is used to program a switching frequency and SYNC is not to be used to synchronize the converter to an external clock, connect SYNC to GND.
SS_SEL	11	I	Soft-start timing selection. Can be connected to GND, BP or left floating to select a soft start time that is proportional to the switching frequency.
SW	15	I	Sense line for the adaptive anti-cross conduction circuitry. Serves as common connection for the flying high-side MOSFET driver
SYNC	9	I/O	Bidirectional synchronization I/O pin. SYNC is an output when the RT pin is connected to BP or GND. The output is a falling edge signal 180° out-of-phase with the rising edge of HDRV. In this mode SYNC can be used to drive the SYNC pin of an additional TPS40195 device whose RT pin is tied to GND through a resistor, providing two converters that operate 180° out-of-phase to one another. SYNC may be used as an input to synchronize to an external system clock if RT is connected to GND through a resistor as well. The device synchronizes to the falling edge of the external clock signal. If RT is used to program a switching frequency and SYNC is not to be used to synchronize the converter to an external clock, connect SYNC to GND.
UVLO	5	I	Programmable UVLO pin for the controller. A resistor divider on this pin to VDD sets the converter turn on voltage and the hysteresis for turn-off.
VDD	4	I	Power input to the controller. A 100 nF bypass capacitor should be connected closely from this pin to GND.

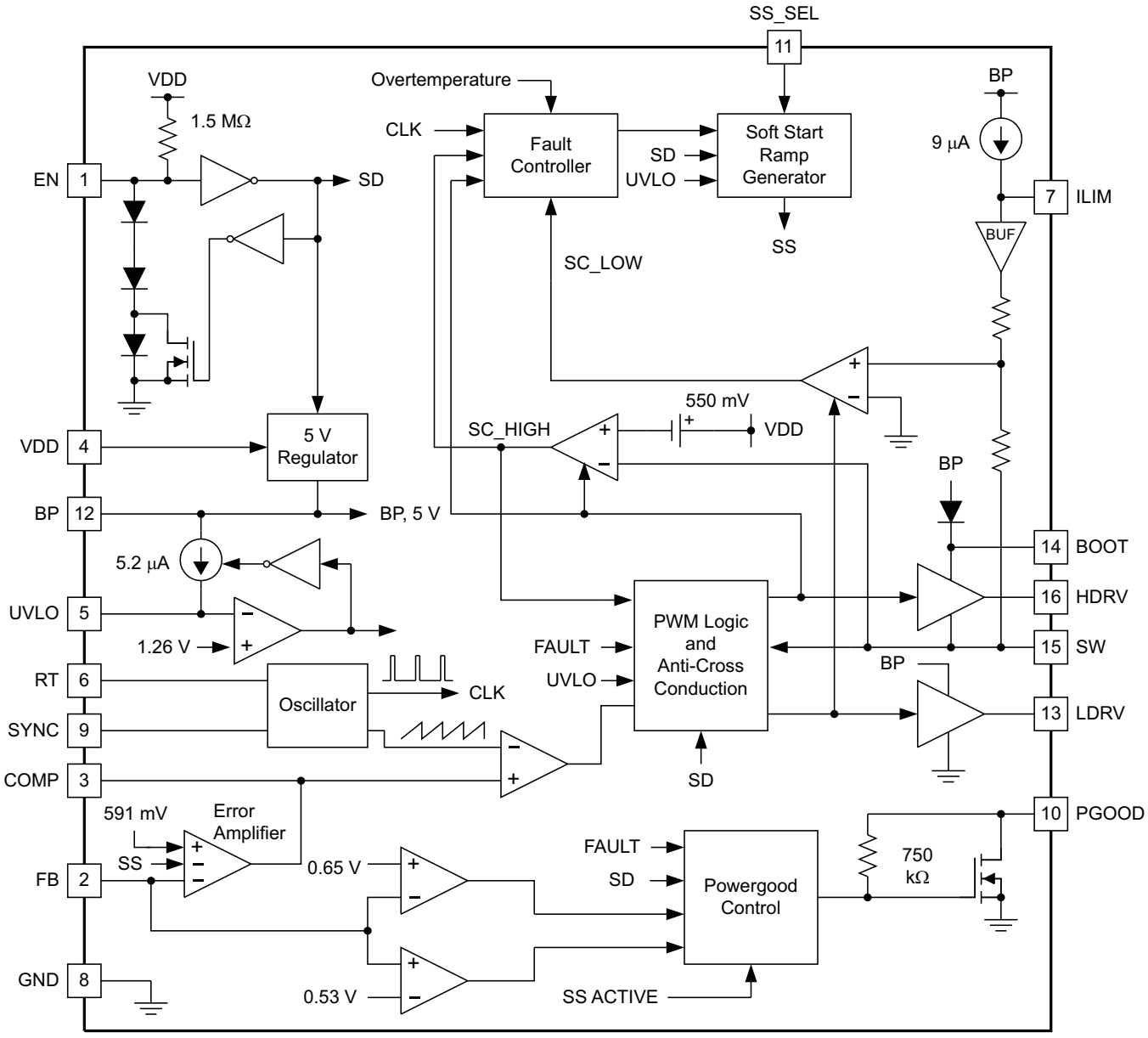
PW Package
(Top View)



RGY Package
(Bottom View)



BLOCK DIAGRAM



APPLICATION INFORMATION

Introduction

The TPS40195 is a flexible controller providing all the necessary features to construct a high performance DC-DC converter while keeping costs to a minimum. Support for pre-biased outputs eliminates concerns about damaging sensitive loads during startup. Strong gate drivers for the high side and rectifier N channel FETs decrease switching losses for increased efficiency. Adaptive gate drive timing minimizes body diode conduction in the rectifier FET, also increasing efficiency. Selectable short circuit protection thresholds and hiccup recovery from a short circuit increase design flexibility and minimize power dissipation in the event of a prolonged output fault. A dedicated enable pin (EN) allows the converter to be placed in a low quiescent current shutdown mode.

Enable Functionality

The TPS40195 has a dedicated device enable (EN) pin. This simplifies user level interface design since no multiplexed functions exist. Another benefit is a true low power shutdown mode of operation. When the EN pin is pulled to GND, all unnecessary functions inside the IC, including the BP regulator, are turned off and the TPS40195 consumes a typical 165-µA of current. A functionally equivalent circuit to the enable circuitry on the TPS40195 is shown in Figure 16.

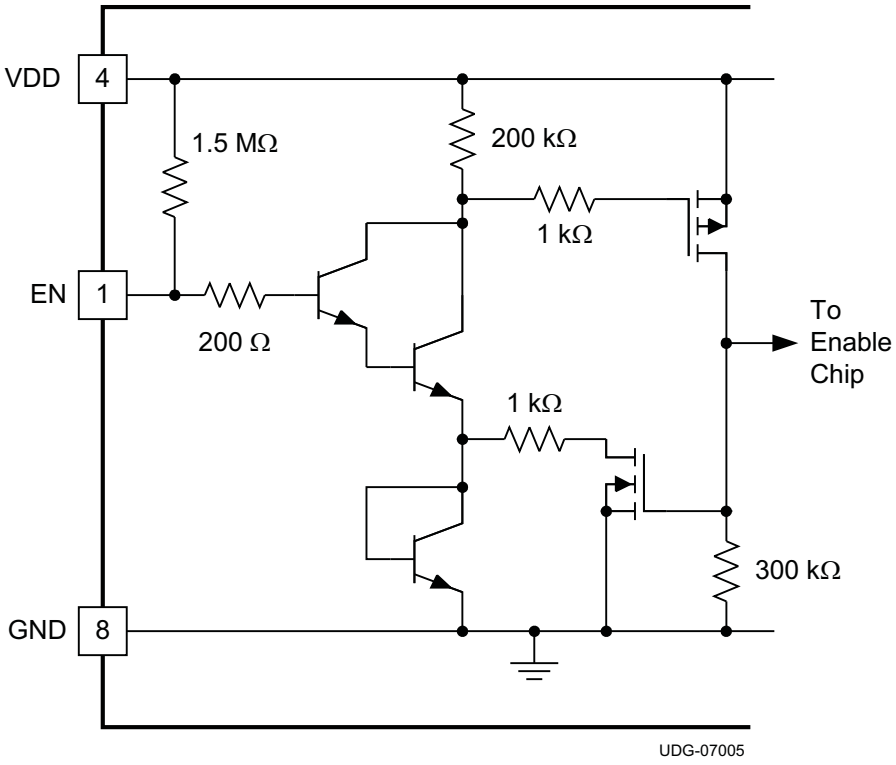


Figure 16. TPS40195 EN Pin Internal Circuitry

If the EN pin is left floating, the chip starts automatically. The pin must be pulled to less than 600 mV for the TPS40195 to be in shutdown mode. Note that the EN pin is relatively high impedance. In some situations, there could be enough noise nearby to cause the EN pin to swing below the 600 mV threshold and give erroneous shutdown commands to the rest of the device. There are two solutions to this problem should it arise.

1. Place a capacitor from EN to GND. A side effect of this is to delay the start of the converter while the capacitor charges past the enable threshold
2. Place a resistor from VDD to EN. This causes more current to flow in the shutdown mode, but does not delay converter startup. If a resistor is used, the total current into the EN pin should be limited to no more than 500 µA.

The ENABLE pin is self-clamping. The clamp voltage can be as low as 1 V with a 1-kΩ ground impedance. Due to this self-clamping feature, the pull-up impedance on the ENABLE pin should be selected to limit the sink current to less than 500 µA. Driving the ENABLE pin with a low-impedance source voltage can result in damage to the device. Because of the self-clamping feature, it requires care when connecting multiple ENABLE pins together. For enabling multiple TPS4019x devices (TPS40190, TPS40192, TPS40193, TPS40195, TPS40197), see the Application Report SLVA509.

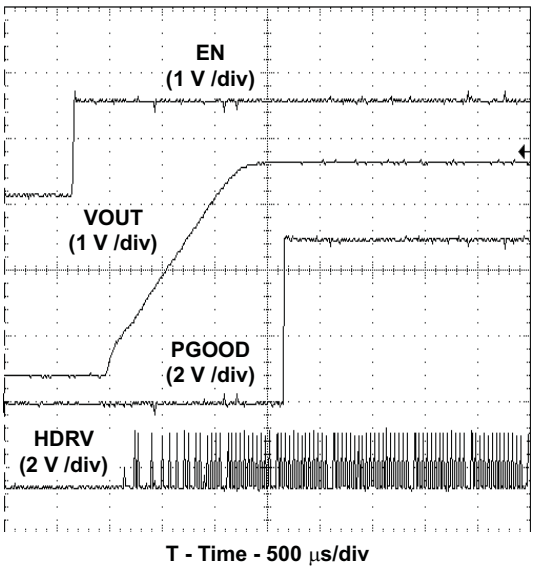


Figure 17. TPS40195 EN Pin Startup

Voltage Reference

The band gap cell is designed with a trimmed 0.591-V output. The 0.5% tolerance on the reference voltage allows the user to design a very accurate power supply.

Oscillator and Synchronization

The TPS40195 has a programmable switching frequency of 100 kHz to 600 kHz using a resistor connected from the RT pin to GND. The relationship between switching frequency and the resistor from RT to GND is given in Equation 1.

$$f_{SW} = \frac{2.5 \times (10)^4}{R_{RT}} \quad (1)$$

where

- f_{SW} is the switching frequency in kHz
- R_{RT} is the resistor connected from RT to GND in kΩ

When the oscillator is programmed using this method, the SYNC pin is configured as an input. The device may be synchronized to a higher frequency than the free running frequency by applying a pulse train to the SYNC pin. For best results, limit the frequency of the pulse train applied to SYNC to 20% more than the free running frequency. The TPS40195 will synchronize to the falling edge of the pulse train applied to the SYNC pin.

The SYNC pin can also function as an output. To get this functionality, the RT pin must be connected to either GND or to BP. When this is done the oscillator will run at either 250 kHz or 500 kHz. SYNC can then be connected to other TPS40195 controllers (with their SYNC pins configured as an input) and the two or more controllers will synchronize to the same switching frequency. The output waveform on SYNC will be approximately a 50% duty cycle pulse train. The pull up is relatively weak, but the pull down is strong to insure that a good clean signal is presented to any devices that are to be synchronized. A summary is shown in Table 1.

Table 1. R_T Connection and SYNC Pin Function

R_T Connection	SYNC Pin Function	Switching Frequency
Resistor to GND	Input	See Equation 1
GND	Output	250 kHz
BP	Output	500 kHz

Using the TPS40195 with its RT pin connected to BP or to GND as a master clock source for another TPS40195 with a resistor connected from its RT pin to GND will result in the two controllers operating at the same frequency but 180° out of phase.

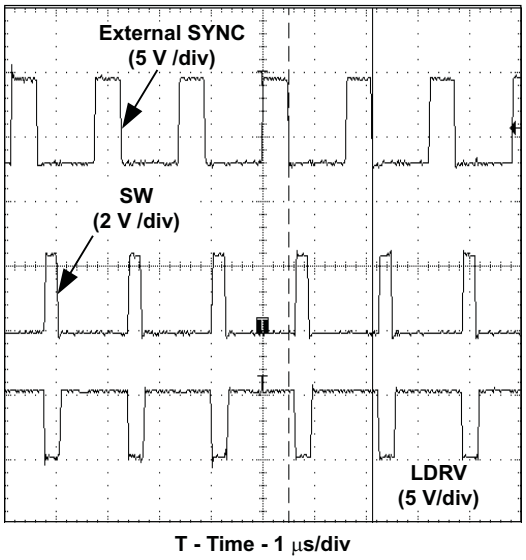


Figure 18. TPS40195 Synchronized to External SYNC Pin Pulse (Negative Edge Triggered)

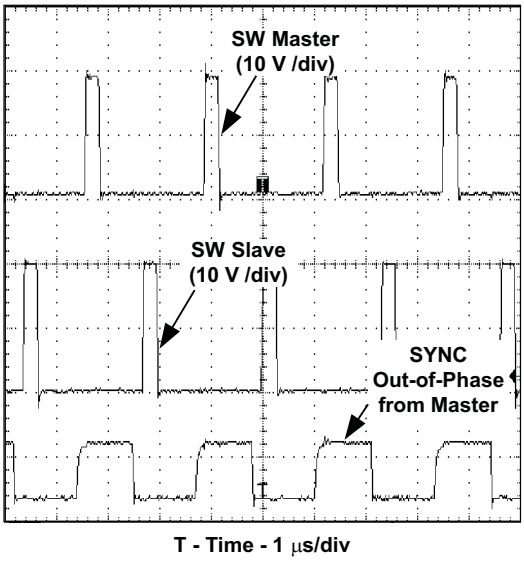


Figure 19. TPS40195 SYNC Pin Master/Slave Configuration. 180° Out-of-Phase Operation

Undervoltage Lockout (UVLO)

There are two separate UVLO circuits in the TPS40195. Both must be satisfied before the controller starts. One circuit detects the BP voltage and the other circuit detects voltage on the UVLO pin. The voltage on the BP pin (V_{BP}) must be above 4.3 V in order for the device to start up.

The UVLO pin is generally used to provide a higher UVLO voltage than that which the BP UVLO circuit provides. This level is programmed using a resistor divider from V_{IN} to GND with the tap connected to the UVLO pin of the TPS40195. Hysteresis is provided by a 5.2-µA current source that is turned on when the UVLO pin reaches the 1.26 V turn on threshold. The turn on level is determined by the divider ratio, and the hysteresis level is determined by the divider equivalent impedance.

To determine the resistor values for the UVLO circuit, a turn on voltage and turn off voltage must be known. Once these are known the resistors can be calculated in Equation 2 and Equation 3. The functional schematic is shown in Figure 20.

$$R1 = \frac{V_{ON} - V_{OFF}}{I_{UVLO}} \quad (2)$$

$$R2 = R1 \times \frac{V_{UVLO}}{V_{ON} - V_{UVLO}}$$

where

- V_{ON} is the desired turn on voltage of the converter
- V_{OFF} is the desired turn off voltage for the converter, must be less than V_{ON}
- I_{UVLO} is the hysteresis current generated by the device, 5.2 µA (typ)
- V_{UVLO} is the UVLO pin threshold voltage, 1.26 V (typ) (3)

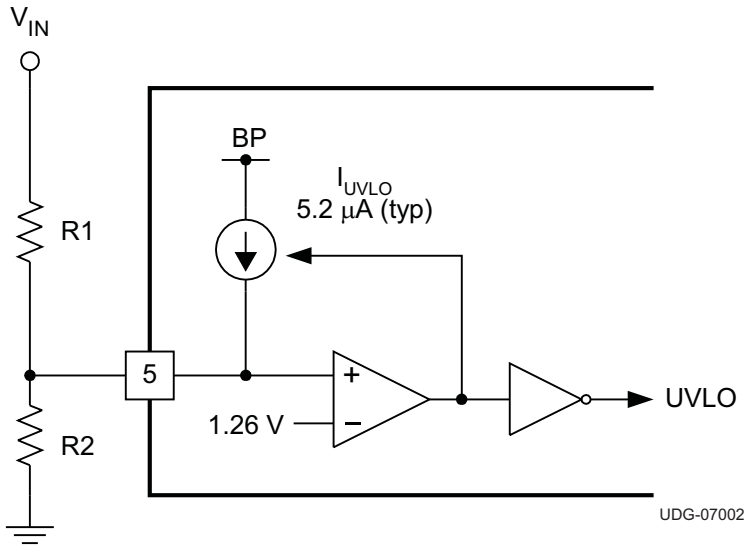


Figure 20. Undervoltage Lockout

Soft Start

The TPS40195 uses a digital closed loop soft start system. The soft start ramp is generated internally by a counter and digital-to-analog converter (DAC) that ramps up the effective reference voltage to the error amplifier. The DAC supplies a voltage to the error amp that is used as the reference until that supplied voltage becomes greater than the 591-mV reference voltage. At that point soft-start is complete and the 591-mV reference controls the output voltage. The ramp rate is dependent on the oscillator frequency as each step in the DAC takes one clock cycle from the oscillator. The user can choose from three ramp rates, or DAC counter widths depending on viewpoint, for any given switching frequency by connecting the SS_SEL pin to GND, BP pin or letting the pin float. The possibilities are summarized in Table 2.

Table 2. Soft Start Clock Cycles

SS_SEL Connection	Clock Cycles in 1-V Ramp (N_{DAC})
GND	2048
Floating	1024
BP	512

The ramp output from the soft start DAC is 1 V in amplitude. Since the soft start is closed loop and reference voltage of the device is actually 591 mV, the actual ramp time is less than the time it takes for the SS ramp to finish and reach 1 V. The actual soft-start time is the amount of time that it takes for the internal soft-start ramp to reach the 591-mV reference level. The soft-start time can be found using Equation 4.

$$t_{SS} = 0.591 \times \frac{N_{DAC}}{f_{SW}}$$

where

- N_{DAC} is the number of 1-V DAC ramp cycles from Table 2
- f_{SW} is the switching frequency in Hz (4)

Selecting the Short Circuit Threshold

An over current is detected by sensing a voltage drop across the low-side FET when it is on, and across the high-side FET when it is on. If the voltage drop across either FET exceeds the short circuit threshold in any given switching cycle, a counter increments one count. If the voltage across the high-side FET was higher that the short circuit threshold, that FET is turned off early. If the voltage drop across either FET does not exceed the short circuit threshold during a cycle, the counter is decremented for that cycle. If the counter fills up (a count of 7) a fault condition is declared and the drivers turn off both MOSFETs. After a timeout of approximately 40 ms, the controller attempts to restart. If a short circuit remains present at the output, the current quickly ramps up to the short circuit threshold and another fault condition is declared and the process of waiting for the 40 ms and attempting to restart repeats.

The current limit threshold for the low-side FET is programmable by the user. To set the threshold a resistor is connected from the ILIM pin to GND. A current source inside the IC connected to the ILIM pin and this resistor set a voltage that is the threshold used for the overcurrent detection threshold. The low side threshold will increase as the low side on time decreases due to blanking time and comparator response time. See Figure 5 for changes in the threshold as the low-side FET conduction time decreases. Refer to Figure 21 for details on the functional equivalent schematic.

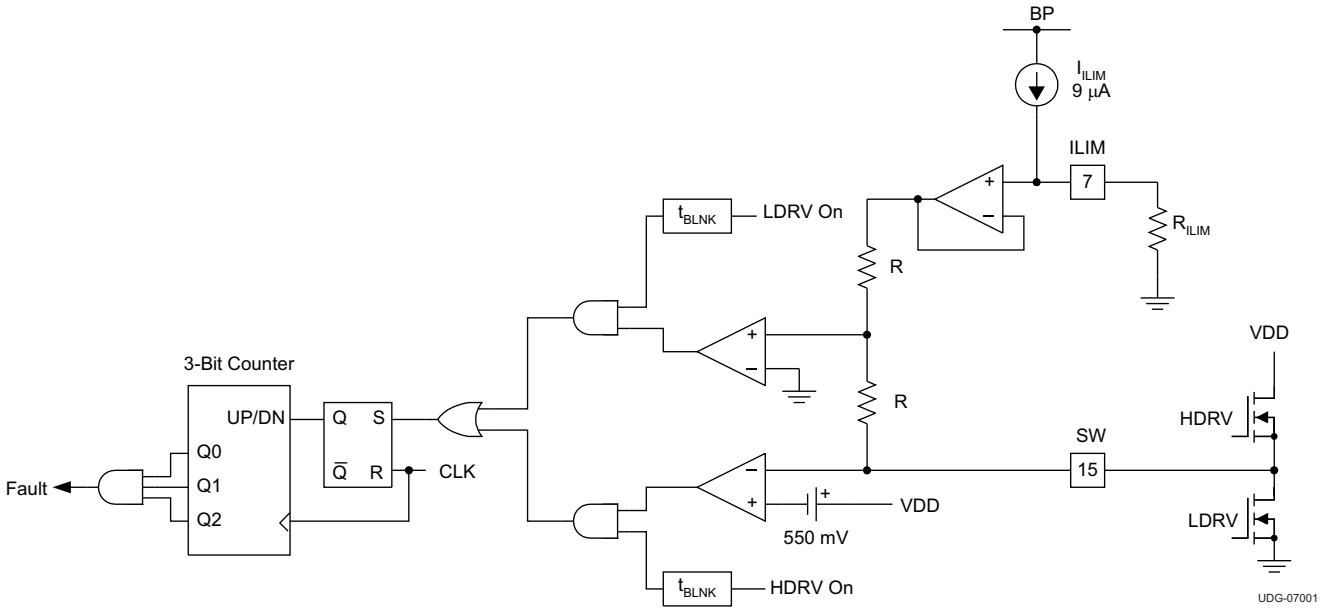


Figure 21. Overcurrent

$$I_{SCP(min)} = \frac{I_{ILIM(min)} \times R_{ILIM(min)} + V_{ILIMOFST(min)}}{R_{DS(on)(max)}}$$

$$I_{SCP(max)} = \frac{I_{ILIM(max)} \times R_{ILIM(max)} + V_{ILIMOFST(max)}}{R_{DS(on)(min)}} \quad (5)$$

where

- $I_{S.P.}$ is the short circuit current
- I_{ILIM} is ILIM pin bias current, 9.0µA (typ)
- R_{ILIM} is the resistance connected from ILIM to GND

- $V_{ILIMOFST}$ is the offset voltage of the low side current sense comparator, ±20 mV
- $R_{DS(on)}$ is the channel resistance of the low-side MOSFET (6)

The short circuit protection threshold for the high-side MOSFET is fixed at 550-mV typical, 400-mV minimum with a 4000 ppm/°C temperature coefficient to help compensate for changes in the high side FET channel resistance as temperature increases. This threshold is in place to provide a maximum current output in the case of a fault. The maximum amount of current that can be sourced from a converter can be found by Equation 7.

$$I_{OUT(max)} = \frac{V_{ILIMH(min)}}{R_{DS(on)(max)}}$$

where

- $I_{OUT(max)}$ is the maximum current that the converter is specified to source
- $V_{ILIMH(min)}$ is the short circuit threshold for the high-side MOSFET (400 mV)
- $R_{DS(on)max}$ is the maximum resistance of the high-side MOSFET (7)

If the required current from the converter is greater than the calculated $I_{OUT(max)}$, a lower resistance high-side MOSFET must be chosen.

The length of time between restart attmepts after an output fault can be found from Equation 8.

$$t_{OFF} = \frac{7 \times N_{DAC}}{f_{SC}}$$

where

- N_{DAC} is the number of 1-V DAC ramp cycles from Table 2.
- f_{SW} is the switching frequency in Hz (8)

5-V Regulator

This device has an on board 5-V regulator that allows the parts to operate from a single voltage feed. No separate 5-V feed to the part is required. This regulator requires a minimum of 1 µF of capacitance on the BP pin for stability. A ceramic capacitor is suggested for this purpose. Noise performance can be improved by increasing this capacitance to 4.7 µF when driving FETs with more than 25nC gate charge requirements.

This regulator can also be used to supply power to nearby circuitry, eliminating the need for a separate LDO in some cases. If this pin is used for external loads, be aware that this is the power supply for the internals of the TPS40195. While efforts have been made to reduce sensitivity, any noise induced on this line has an adverse effect on the overall performance of the internal circuitry and shows up as increased pulse jitter, or skewed reference voltage. Note that when the EN pin is pulled low, the BP regulator will be turned off and not available to supply power to external loads.

The amount of power available from this pin varies with the size of the power MOSFETs that the drivers must operate. Larger MOSFETs require more gate drive current and reduces the amount of power available on this pin for other tasks.

Pre-Bias Startup

The TPS40195 contains a unique circuit to prevent current from being pulled from the output during startup in the condition the output is pre-biased. When the soft-start commands a voltage higher than the pre-bias level (internal soft-start becomes greater than feedback voltage [V_{FB}]), the controller slowly activates synchronous rectification by starting the first LDRV pulses with a narrow on-time. It then increments that on-time on a cycle-by-cycle basis until it coincides with the time dictated by (1-D), where D is the duty cycle of the converter. This scheme prevents the initial sinking of the pre-bias output, and ensures that the out voltage (V_{OUT}) starts and ramps up smoothly into regulation and the control loop is given time to transition from pre-biased startup to normal mode operation with minimal disturbance to the output voltage. The amount of time from the start of switching until the low-side MOSFET is turned on for the full 1-D interval is defined by 32 clock cycles.

Drivers

The drivers for the external HDRV and LDRV MOSFETs are capable of driving a gate-to-source voltage of 5 V. The LDRV driver switches between VDD and GND, while HDRV driver is referenced to SW and switches between BOOT and SW. The drivers have non-overlapping timing that is governed by an adaptive delay circuit to minimize body diode conduction in the synchronous rectifier. The drivers are capable of driving MOSFETS that are appropriate for a 15-A converter if power dissipation requirements are met. See *Package Dissipation Ratings* Table.

Power Good

The TPS40195 provides an indication that output power is good for the converter. This is an open drain signal and pulls low when any condition exists that would indicate that the output of the supply might be out of regulation. These conditions include:

- V_{FB} > ±10% from nominal
- soft-start is active
- a undervoltage condition exists for the device
- a short circuit condition has been detected
- die temperature is over (150°C)

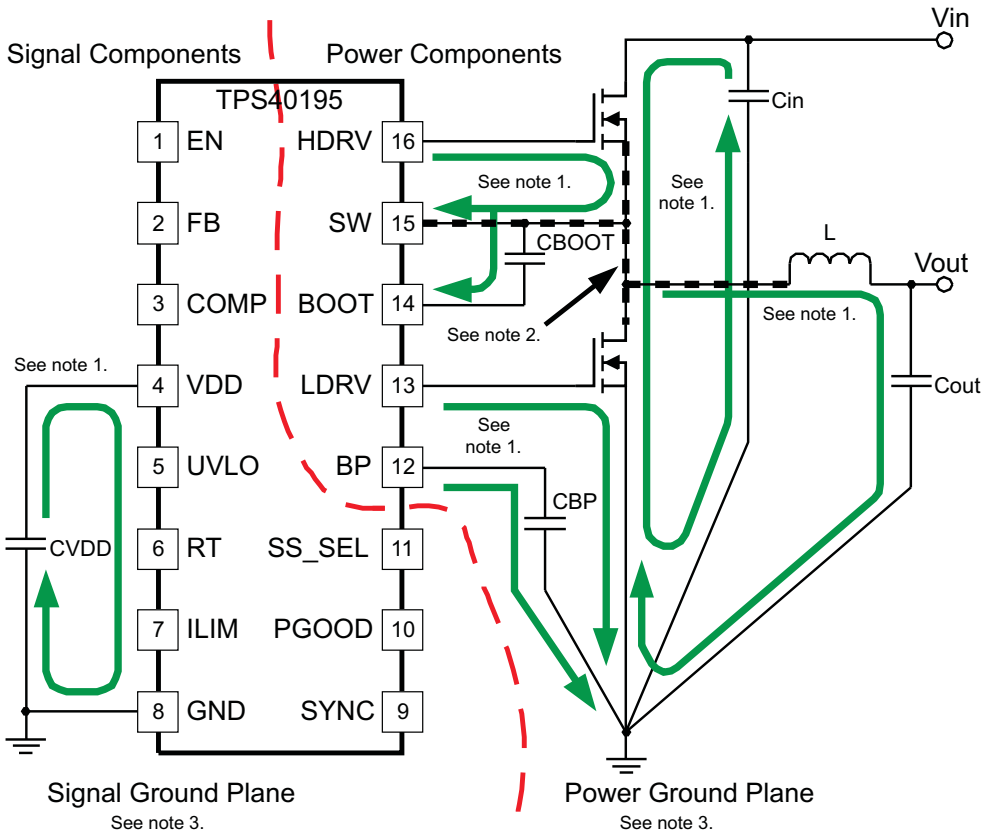
NOTE

When there is no power to the device, PGOOD is not able to pull close to GND if an auxiliary supply is used for the power good indication. In this case, a built in resistor connected from drain to gate on the PGOOD pull down device makes the PGOOD pin look approximately like a diode to GND.

Thermal Shutdown

Thermal shutdown If the junction temperature of the device reaches the thermal shutdown limit of 150°C, the PWM and the oscillator is turned off and HDRV and LDRV are driven low, turning off both FETs. When the junction cools to the required level (130°C nominal), the PWM initiates soft start as during a normal power up cycle.

Layout Suggestions



1. Keep these loops as short as possible. Run out and return lines close together.
2. Keep the switch node area as small as possible
3. Keep Signal and Power Grounds separate. Connect into a general power plane on one layer.

Figure 22. Layout Suggestion

- Keep the input switching current loop as small as possible.
- Place the input capacitor (C_{IN}) close to the top switching FET The output loop current loop should also be kept as small as possible.
- Keep the SW node as physically small as possible to minimize parasitic capacitance and to minimize radiated emissions Kelvin connections should be brought from the output to the feedback pin (FB) of the device.
- Keep analog and non-switching components away from switching components.
- The gate drive trace should be as close to the power FET's gate as possible.
- Make a single point connection from the signal ground to power ground.
- Do not allow switching current to flow under the device.

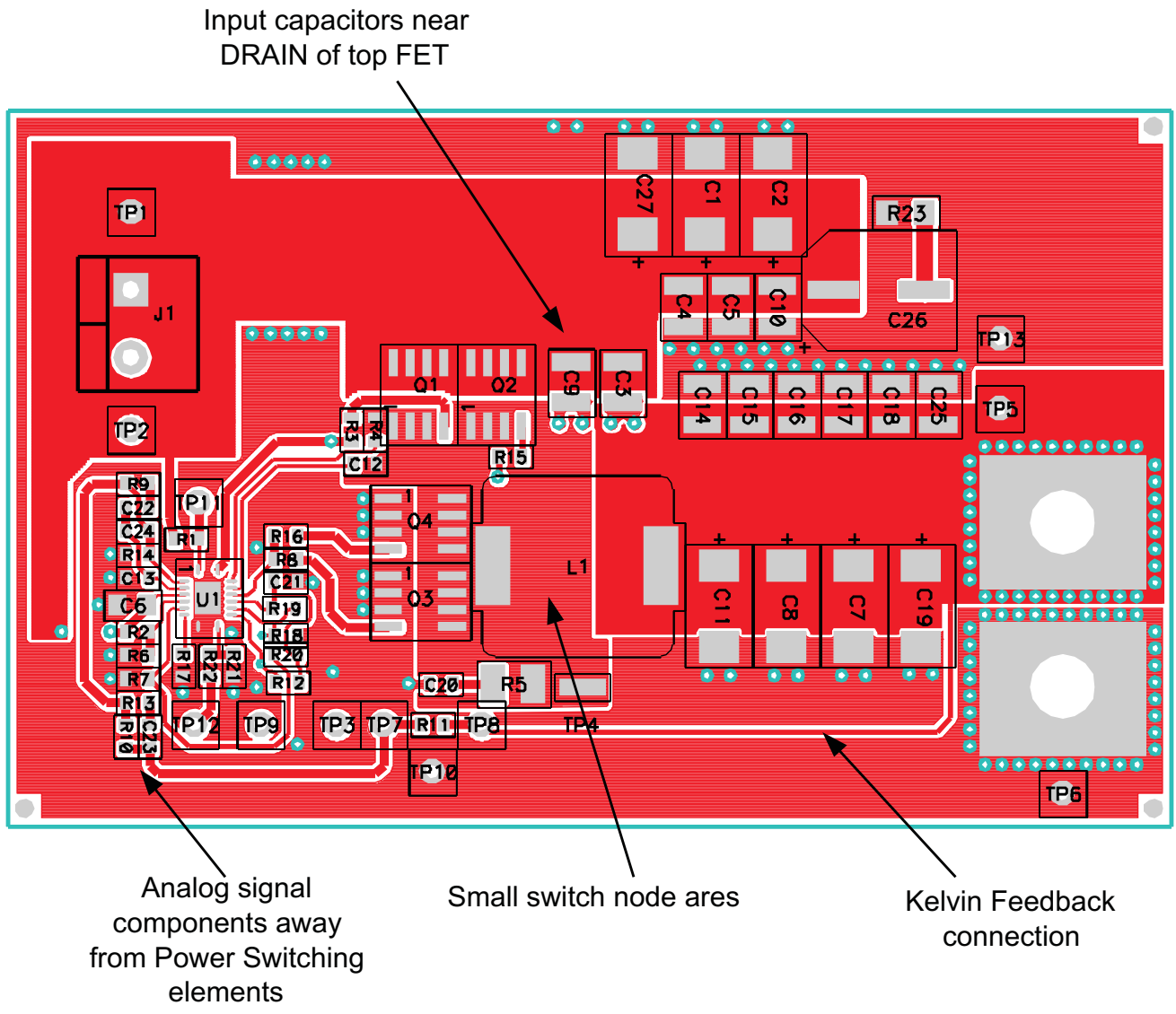


Figure 23. Board Layout

DESIGN EXAMPLES

Design Example 1

Table 3. Design Example Electrical Specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
V_{IN}	Input voltage		10.8	12.0	13.2	V
I_{IN}	Input current	V_{IN} = 12 V, I_{OUT}= 10 A		1.7	1.8	A
		No load, V_{IN} = 12 V, I_{OUT}= 0 A			5	mA
VIN_ UVLO_OFF	Undervoltage lockout turn off threshold	0 A ≤ I_{OUT} ≤ 10 A	5.4	6.0	6.6	V
VIN_UVLO _ON	Undervoltage lockout turn on threshold	0 A ≤ I_{OUT} ≤ 10 A	6.6	7.0	7.6	
OUTPUT						
V_{OUT}	Input voltage range	V_{IN} = 12 V, I_{OUT}= 5	1.75	1.80	1.85	V
	Line regulation	10.8 ≤ V_{IN} ≤ 13.2 V			0.5%	
	Load regulation	0 A ≤ I_{OUT} ≤ 10 A			0.5%	
$V_{OUT(ripple)}$	Output voltage ripple	V_{IN} = 12 V, I_{OUT}= 10 A			100	mV_{P-P}
I_{OUT}	Output current	10.8 ≤ V_{IN} ≤ 13.2 V	0	5	10	A
I_{OCP}	Output overcurrent inception point	V_{IN} = 12 V, V_{OUT}= (V_{OUT}- 5)	14	20	43	
ΔI	Transient response load step	10 A ≤ $I_{OUT(max)}$ ≤ 0.2 × ($I_{OUT(max)}$)		8		A
	Transient response load slew rate			5		A/µs
	Transient response overshoot			200		mV
	Transient response settling time			1		ms
SYSTEM						
f_{SW}	Switching frequency		240	300	360	kHz
η_{PK}	Peak efficiency	V_{IN} = 12 V, 0 A ≤ I_{OUT} ≤ 10 A		90%		
η	Efficiency at full load	V_{IN} = 12 V, I_{OUT} = 10 A		87%		
T_{OP}	Operating temperature range	10.8 ≤ V_{IN} ≤ 13.2 V, 0 A ≤ I_{OUT} ≤ 10 A	-40	25	85	°C
MECHANICAL						
W	Width			1.6		in
L	Length			3.5		
h	Height			0.26		

Schematic

This section discusses basic buck converter design. Designers already familiar with the design of buck converters can skip to the next section *Component Selection* of this design example.

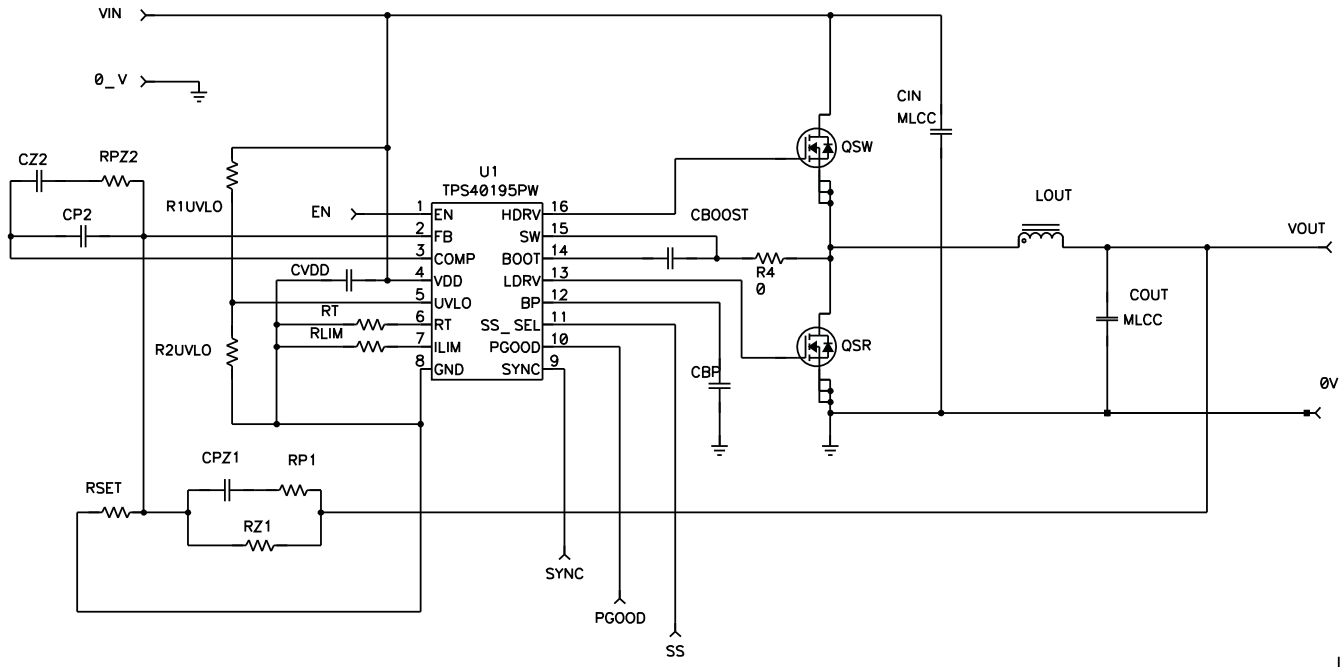


Figure 24. TPS40195 Design Example Schematic

Output Inductor, L_{OUT}

Equation 9 can be used to calculate L_{OUT}.

$$L_{OUT} = \frac{V_{OUT}}{V_{IN(max)}} \times \frac{(V_{IN(max)} - V_{OUT})}{f_{SW} \times I_{RIPPLE}} = \frac{1.8\,V}{13.2\,V} \times \frac{(13.2\,V - 1.8\,V)}{300\,kHz \times 2.0} = 2.59\,\mu H \quad (9)$$

where

- I_{RIPPLE} = the allowable ripple current in the inductor, 20% of maximum I_{OUT}

For this design a 2.5-µH inductor from Coilcraft is used. I_{RIPPLE} is recalculated using Equation 10 and a 2.5-µH inductor value to give a new estimate of I_{RIPPLE} of 2.1 A .

$$I_{RIPPLE} = \frac{V_{OUT}}{V_{IN(max)}} \times \frac{(V_{IN(max)} - V_{OUT})}{f_{SW} \times L_{OUT}} = \frac{1.83\,V}{13.2\,V} \times \frac{(13.2\,V - 1.83\,V)}{300\,kHz \times 2.5\,\mu H} = 2.10\,A \quad (10)$$

With this I_{RIPPLE} value, the RMS and peak current flowing in L_{OUT}can be calculated.

$$I_{LOUT\_RMS} = \sqrt{(I_{OUT})^2 + \frac{(I_{RIPPLE})^2}{12}} = \sqrt{(10)^2 + \frac{(2.10)^2}{12}} = 10.02\,A \quad (11)$$

$$I_{PK} = I_{OUT} + \frac{I_{RIPPLE}}{2} = 10 + \frac{2.10}{2} = 11.05\,A \quad (12)$$

Output Capacitor, C_{OUT}

The capacitance value is selected to be greater than the largest value calculated from Equation 13 and Equation 14.

$$C_{OUT} = \frac{L_{OUT} \times (I_{STEP})^2}{2 \times V_{UNDER} \times D_{MAX} \times (V_{IN(min)} - V_{OUT})} = \frac{2.5\,\mu H \times (8)^2}{2 \times 200\,mV \times 90\% \times (10.8\,V - 1.8\,V)} = 71.68\,\mu F \quad (13)$$

$$C_{OUT} = \frac{L_{OUT} \times (I_{STEP})^2}{2 \times V_{OVER} \times V_{OUT}} = \frac{2.5\,\mu H \times 8^2}{2 \times 200\,mV \times 1.8\,V} = 222.2\,\mu F \quad (14)$$

$$ESR = \frac{V_{RIPPLE}}{I_{RIPPLE}} = \frac{100\,mV}{2.1A} = 47\,m\Omega \quad (15)$$

From Equation 13, Equation 14 and Equation 15, the capacitance for C_{OUT} should be greater than 223 µF and its ESR should be less than 47 mΩ. Three 100-µF, 6.3-V, X5R ceramic capacitors are chosen. Each capacitor has an ESR of 5 mΩ .

Input Capacitor, C_{IN}

The input capacitor is selected to handle the ripple current of the buck stage. A relatively large capacitance is used to keep the ripple voltage on the supply line low. This is especially important were the supply line has a high impedance. It is recommended that the supply line impedance be kept low. The input capacitor RMS current can be calculated using Equation 16.

$$I_{CAP(RMS)} = \sqrt{\left[\left(I_{OUT} - \frac{V_{OUT}}{V_{IN}} \times I_{OUT}\right)^2 + \frac{(I_{RIPPLE})^2}{12}\right] \times \frac{V_{OUT}}{V_{IN}} + \left(\frac{V_{OUT}}{V_{IN}} \times I_{OUT}\right)^2 \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (16)$$

The RMS current in the input capacitor is 3.56 A. Two 22-µF, size 1206 capacitors using X7R material has a typical dissipation factor of 5%. For a 22-µF capacitor at 300 kHz the ESR is approximately 5 mΩ. Two of these capacitors are used in parallel. The power dissipation in each capacitor is less than 16 mW. A 470-µF, 25-V electrolytic is added to maintain the voltage on the input rail.

Switching MOSFET, Q_{SW}

The following key parameters must be met by the selected MOSFET.

- Drain-to-source voltage, V_{DS}, must be able to withstand the input voltage plus spikes that may be on the switching node. For this design a V_{DS} rating of between 25 V and 30 V is recommended.

$$I_{QSW(rms)} = \sqrt{\frac{V_{OUT}}{V_{IN(min)}} \times \left((I_{OUT(max)})^2 + \frac{(I_{RIPPLE})^2}{12}\right)} \quad (17)$$

  For this design I_{DD} should be greater than 4.1 A
- Gate source voltage, V_{gs}, must be able to withstand the gate voltage from the control device. For the TPS40195 this is 5 V.

Target efficiency for this design is 90%. Based on 1.8-V output and 10-A operating current this equates to a power loss in the module of 1.8 W. The design allocates this power budget equally between the two power FETS and the inductor The equations below are used to calculate the power loss, P_{QSW}, in the switching MOSFET.

$$P_{GATE} = Q_{g(TOT)} \times V_g \times f_{SW} \quad (18)$$

$$P_{QSW} = P_{CON} + P_{SW} + P_{GATE} \quad (19)$$

$$P_{CON} = R_{DS(on)} \times \left(I_{QSW(rms)}\right)^2 = R_{DS(on)} \times \frac{V_{OUT}}{V_{IN}} \times \left(\left(I_{OUT}\right)^2 + \frac{\left(I_{RIPPLE}\right)^2}{12} \right) \quad (20)$$

$$P_{SW} = V_{IN} \times f_S \times \left[\frac{\left(I_{OUT} + \frac{I_{RIPPLE}}{2} \right) \times \left(Q_{gs1} + Q_{gd}\right)}{I_g} \right]$$

where

- P_{CON} is conduction losses
- P_{SW} is switching losses
- P_{GATE} is gate drive losses
- Q_{gd} is drain source charge or miller charge
- Q_{gs1} is gate source post threshold charge
- I_g is gate drive current
- $Q_{g(TOT)}$ is total gate charge from 0 V to the gate voltage
- V_g is gate voltage (21)

Equation 22 and Equation 23 describe the preliminary values for $R_{DS(on)}$ and (Q_{gs1} + Q_{gd}). Note output losses due to Q_{OSS} and gate losses have been ignored here. Once a MOSFET is selected these parameters can be added. The switching MOSFET for this design should have an $R_{DS\ (on)}$ of less than 20 mΩ . The sum of Q_{gd} and Q_{gs1} should be approximately 14.8 nC. . The Vishay SI7860ADP was selected for this design. This device has an $R_{DS(on)}$ of 9 mΩ and a (Q_{gs1}+Q_{gd}) of 13 nC. The estimated conduction losses are 0.135 W and the switching losses are 0.297 W. This gives a total estimated power loss of 0.432 W versus 0.6 W for our initial boundary condition. Note this does not include gate losses of approximately 10 mW.

Rectifier MOSFET, Q_{SR}

Similar criteria as used above apply to the rectifier MOSFET. One significant difference however, is that the rectifier MOSFET switches with nearly zero voltage across its drain and source so its switching losses are nearly zero. There are losses from the source to drain body diode that occur as it conducts during the delay before the FET turns on. The equations used to calculate the losses in the rectifier MOSFET are shown below.

$$P_{QSR} = P_{CON} + P_{BD} + P_{GATE} \quad (22)$$

$$P_{CON} = R_{DS(on)} \times \left(I_{QSW(rms)}\right)^2 = R_{DS(on)} \times \frac{V_{OUT}}{V_{IN}} \times \left(\left(I_{OUT}\right)^2 + \frac{\left(I_{RIPPLE}\right)^2}{12} \right) \quad (23)$$

$$P_{GATE} = Q_{g(TOT)} \times V_g \times f_{SW} \quad (24)$$

$$P_{BD} = V_f \times I_{OUT} \times \left(t_1 + t_2\right) \times f_S$$

where

- P_{BD} is the body diode loss
- t_1 is the body diode conduction prior to turn-on of channel (57nS)
- t_2 is the body diode conduction after turn-off of channel (14nS)
- V_f is the body diode forward voltage (25)

Estimating the body diode losses based on a forward voltage of 1.0 V yields 0.162 W. The gate losses are unknown at this time so assume 0.1 W gate losses. This leaves 0.338 W for conduction losses. Using this figure a target $R_{DS(on)}$ of 4.0 mΩ was calculated. The SI7886ADP has an $R_{DS(on)}$ maximum of 4.8 mΩ and was used for this design.

Using the parameters from its data sheet the actual expected power losses were calculated. Conduction loss is 0.394 W, body diode loss is 0.210 W and the gate loss was 0.063 W. This totals 0.667 W associated with the rectifier MOSFET.

The ratio between C_{gs} and C_{gd} should be greater than one. The Si7886 capacitor meets this criterion and helps reduce the risk of dv/dt induced turn on of the rectifier MOSFET. If this is likely to be a problem a small resistor may be added in series with the boost capacitor, C_{BOOST}. to slow the turn on speed of Q_{SW} at the expense of increased switching losses in that device.

Component Selection for the TPS40195

Timing Resistor, R_T

The timing resistor is calculated using the following equation.

$$R_T = \frac{2.5 \times (10)^7}{f_S} = \frac{2.5 \times (10)^7}{300} = 83.3\,k\Omega \tag{26}$$

A standard value resistor of 82.5 kΩ is used.

Setting UVLO

The equations below are used to set the UVLO voltages.

$$R_{UVLO1} = \frac{V_{ON} - V_{OFF}}{I_{UVLO}} = \frac{7 - 6}{5.2 \times (10)^{-6}} = 192.3\,k\Omega \tag{27}$$

$$R_{UVLO2} = R_{UVLO1} \times \frac{V_{UVLO}}{(V_{ON} - V_{UVLO})} = 192.3\,k\Omega \times \frac{1.26}{7 - 1.26} = 42.2\,k\Omega \tag{28}$$

The UVLO threshold voltage (V_{UVLO}) is 1.26 V. The module has a turn on voltage of 7 V and a turn off voltage of 6 V. This sets $R_{UVLO1}$to 191 kΩ, the nearest standard value. The second resistor R_{UVLO2} is 42.2 kΩ.

Setting the Soft-Start Time

The selection of the soft start time should be greater than the time constant of the output filter, L_{OUT} and C_{OUT}. This time is given in Equation 29 and Equation 30.

$$t_{START} \geq 2\pi \times \sqrt{L_{OUT} \times C_{OUT}} \tag{29}$$

$$t_{START} \geq 6.28 \times \sqrt{2.5 \times (10)^{-6} \times 300 \times (10)^{-6}} = 0.172\,ms \tag{30}$$

The soft-start time is determined using Equation 31 . The TPS40195 uses a counter operating at the clock frequency that increments an internal DAC until it reaches the turn on threshold voltage of 0.591 V. The number of counts required to reach this threshold is determined by one of three settings on the SS pin. In this case, the pin is floating (with a small bypass capacitor) which sets the clock count (N_{DAC}) to 1024 and the soft-start time is 2.0 ms

$$t_{SS} = 0.591 \times \frac{N_{DAC}}{f_{SW}} = 0.591 \times \frac{1024}{300} = 2.0\,ms \tag{31}$$

Short Circuit Protection, R_{ILIM}

Short circuit protection is programmed using the R_{ILIM} resistor. Selection of this resistor depends on the $R_{DS(on)}$ of the switching MOSFET and the required short circuit current trip point, I_{SCP}. The minimum I_{SCP} must exceed the sum of the output current, the peak ripple current, and the output capacitor charging current during start up. Equation 30 gives this minimum.

$$I_{SCP} \geq \frac{C_{OUT} \times V_{OUT}}{t_{START}} + I_{PK} = \frac{300 \times (10)^{-6} \times 1.8}{2 \times (10)^{-3}} + 11.05 = 11.32\,A \tag{32}$$

The minimum short circuit current trip point for this design is set to 14 A. Equation 33 is then used to calculate the minimum R_{ILIM} value.

$$R_{ILIM(min)} = \frac{R_{DS(on)(max)} \times I_{SCP(min)} - V_{ILIMOFSET(min)}}{I_{LIM(min)}} = \frac{(4.88 \times (10)^{-3} \times 14) + 20mV}{7.0 \times (10)^{-6}} = 12.6k\Omega \tag{33}$$

R_{ILIM} is calculated to be 12.6 kΩ . The closest standard value of 12.7 kΩ is used. The minimum and maximum short circuit current can be calculated using Equation 34 and Equation 35 .

$$I_{SCP(min)} = \frac{I_{ILIM(min)} \times R_{ILIM(min)} + V_{ILIMOFST(min)}}{R_{DS(on)(max)}} \tag{34}$$

$$I_{SCP(max)} = \frac{I_{ILIM(max)} \times R_{ILIM(max)} + V_{ILIMOFST(max)}}{R_{DS(on)(min)}} \tag{35}$$

The minimum I_{SCP} is 14 A and the maximum is 46 A.

Voltage Decoupling Capacitors, C_{BP}, and C_{VDD}

Two pins on the TPS40195 have DC voltages. It is recommended to add small decoupling capacitors to these pins. Below are the recommended values.

- C_{BP} = 4.7 µF
- C_{VDD} = 0.1 µF

Boost Voltage, C_{BOOST} and D_{BOOST} (optional)

Selection of the boost capacitor is based on the total gate charge of the switching MOSFET and the allowable ripple on the boost voltage, V_{BOOST}. A ripple of 0.2 V is assumed for this design. Using these two parameter and equation (26) the minimum value for C_{BOOST} can be calculated.

$$C_{BOOST} > \frac{Q_{g(TOT)}}{\Delta V_{BOOST}} \tag{36}$$

The total gate charge of the switching MOSFET is 13.3 nC. A minimum C_{BOOST} of 0.066-µF is required. A 0.1-µF capacitor was chosen. This capacitor must be able to withstand the maximum input voltage plus the maximum voltage on BP. This is 16 V plus 5.4 V which is 21.4 V. A 50-V capacitor is used.

To reduce losses in the TPS40195 and to increase the available gate voltage for the switching MOSFET an external diode can be added between the BP pin and the BOOST pin of the device. A small signal schottky should be used here, such as the BAT54.

Closing the Feedback Loop R_{Z1}, R_{P1}, R_{PZ2}, R_{SET1}, R_{SET2}, C_{Z2}, C_{P2} AND C_{PZ1}

A graphical method is used to select the compensation components. This is a standard feedforward buck converter. Its PWM gain is given by the following equation.

$$K_{PWM} \cong \frac{V_{IN}}{V_{RAMP}} \tag{37}$$

The gain of the output LC filter is given in Equation 38.

$$K_{LC} = \frac{(1 + s \times ESR \times C_{OUT})}{1 + s \times \left(\frac{L_{OUT}}{R_{OUT}}\right) + (s)^2 \times L_{OUT} \times C_{OUT}} \quad (38)$$

The equation for the PWM and LC gain is:

$$G_e(s) = K_{PWM} \times K_{LC} = \frac{V_{IN}}{V_{RAMP}} \times \frac{(1 + s \times ESR \times C_{OUT})}{1 + s \times \left(\frac{L_{OUT}}{R_{OUT}}\right) + (s)^2 \times L_{OUT} \times C_{OUT}} \quad (39)$$

To plot this on a Bode plot the DC gain must be expressed in dB. The DC gain is equal to K_{PWM}. To express this in dB we take its LOG and multiple by 20. For this converter the DC gain is:

$$DC\,gain = 20 \times LOG\left(\frac{V_{IN}}{V_{RAMP}}\right) = 20 \times LOG(12) = 21.6\,dB \quad (40)$$

Also the pole and zero frequencies should be calculated. A double pole is associated with the LC and a zero is associated with the ESR of the output capacitance. The frequency at where these occur can be calculated using Equation 41.

$$f_{LC\_Pole} = \frac{1}{2\pi \times \sqrt{L_{OUT} \times C_{OUT}}} = 5.8\,kHz \quad (41)$$

$$f_{ESR\_Zero} = \frac{1}{2\pi \times ESR \times C_{OUT}} = 318\,kHz \quad (42)$$

A Bode plot of the PWM and LC filter is shown in Figure 25.

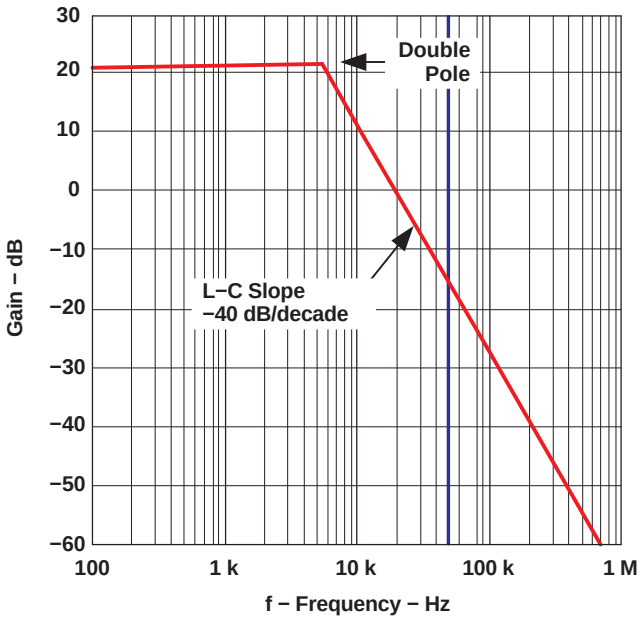


Figure 25. PWM and L-C Filter Gain

A Type-III compensation network, shown in Figure 26, is used for this design. A typical bode plot of a Type-III compensation network is shown below in Figure 27.

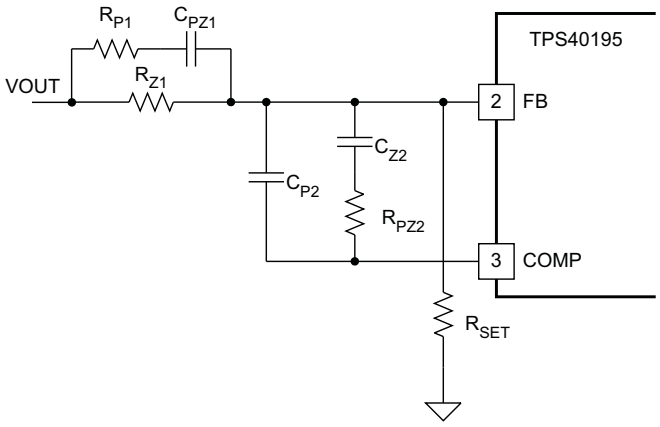


Figure 26. Type III Compensation Schematic

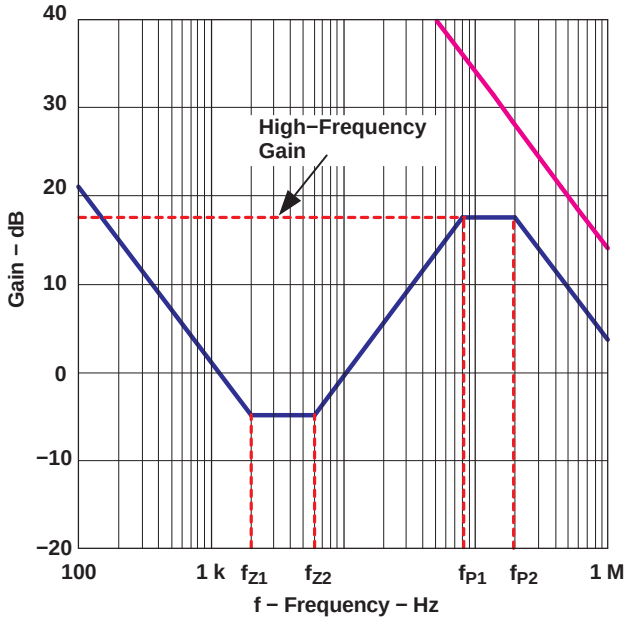


Figure 27. Type-III Compensation Network Typical Bode Plot

The output voltage, the high-frequency gain and the break (pole and zero) frequencies are calculated using the following equations.

$$R_{SET} = \frac{(V_{REGF} \times R_{Z1})}{(V_{OUT} - V_{REF})} \quad (43)$$

$$R_{SET} = \frac{0.591 \times 51k\Omega}{1.8 - 0.591} = 24.9k\Omega \quad (44)$$

$$Gain = \frac{R_{PZ2} \times \left(R_{Z1} + R_{P1} + \left(\frac{1}{2\pi f_c \times C_{PZ1}} \right) \right)}{R_{Z1} \left(R_{P1} + \frac{1}{2\pi f_C \times C_{PZ1}} \right)} \quad (45)$$

$$f_{P1} = \frac{1}{2\pi \times R_{P1} \times C_{PZ1}} \quad (46)$$

$$f_{P2} = \frac{C_{P2} + C_{Z2}}{2\pi \times R_{PZ2} \times C_{P2} \times C_{Z2}} \approx \frac{1}{2\pi \times R_{PZ2} \times C_{P2}} \quad (47)$$

$$f_{Z1} = \frac{1}{2\pi \times R_{Z1} \times C_{PZ1}} \quad (48)$$

$$f_{Z2} = \frac{1}{2\pi \times (R_{PZ2} + R_{P1}) \times C_{Z2}} \approx \frac{1}{2\pi \times R_{PZ2} \times C_{Z2}} \quad (49)$$

Steps in closing the feedback loop.

1. Place one zero well below the L-C double pole at 5.8 kHz (f_{Z1}=2.1 kHz)
2. Place the second zero near the double pole f_{Z2} at 5.8 kHz.
3. Place one pole well above the desired cross over frequency, selected as one sixth the switching frequency, f_{CO1} = 50 kHz, f_{P1} = 300 kHz

4. Place the second pole near the ESR zero of the output capacitors of 318 kHz. f_{P2} = 318 kHz
5. The high frequency gain must be such that the over all system has 0 dB at the required crossover frequency. This gain is -1 times the sum of the modulator gain and the gain of the output stage at the crossover frequency of 50 kHz.

Using these values and the above equations calculate the set point and the Rs and Cs around the compensation network using the following procedure.

1. Set R_{Z1} = 51 kΩ
2. Calculate R_{SET} using Equation 43. For this module R_{SET} = a standard 1% value = 24.9 kΩ.
3. Using Equation 48 and f_{Z1} = 1.8 kHz, C_{PZ1} can be calculated to be 1500 pF, F_{P1} and Equation 46 yields R_{P1} to be 363 Ω and the standard value 357 Ω is used.
4. From Figure 25, the required gain is calculated at 15.8 dB. Equation 45 sets the value for R_{PZ2}. A resistor for R_{PZ2} with value of 12.7 kΩ is used. C_{Z2} is calculated using Equation 49 and the desired frequency for the second zero, C_{Z2} = 1475 pF. A 2200 pF capacitor is used.
5. C_{P2} is calculated using the second pole frequency and Equation 47, C_{P2} = 37 pF. A 33-pf capacitor is used.

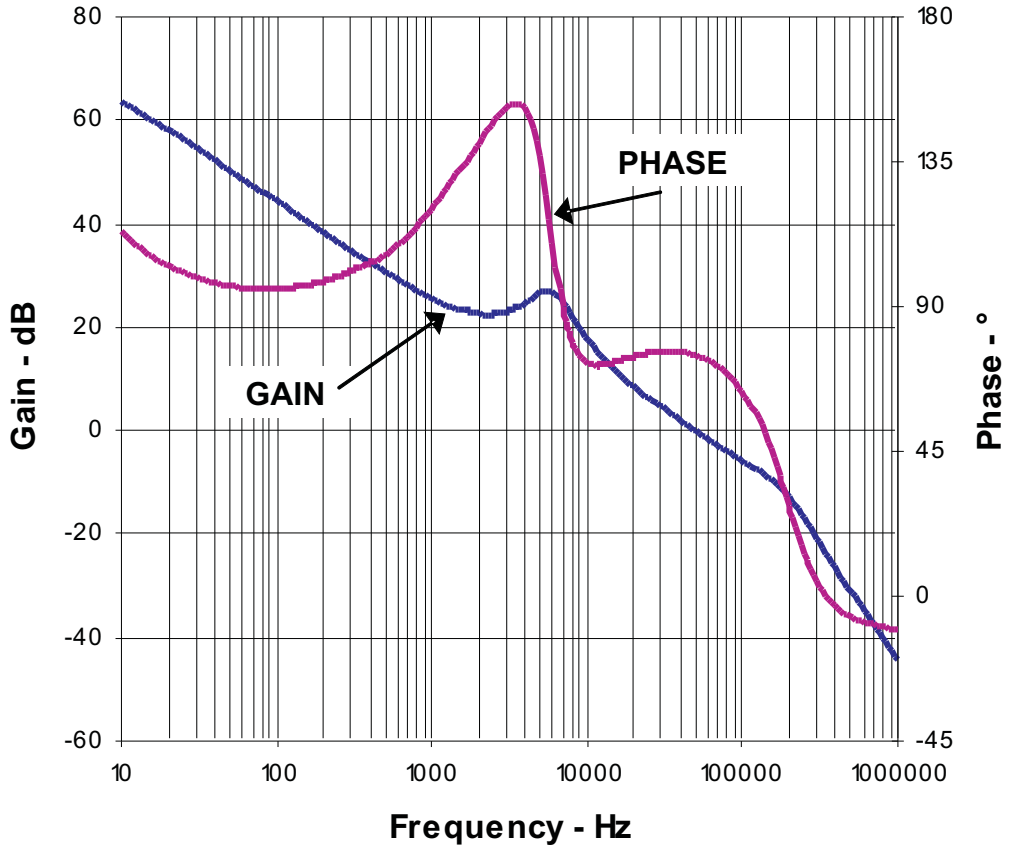


Figure 28. Final Bode Plot

Design Example 2

This example demonstrates the performance of the TPS40195 in a design that produces 5 A of output current at a voltage of 3.3 V. The input for this design is 12 V ±10%.

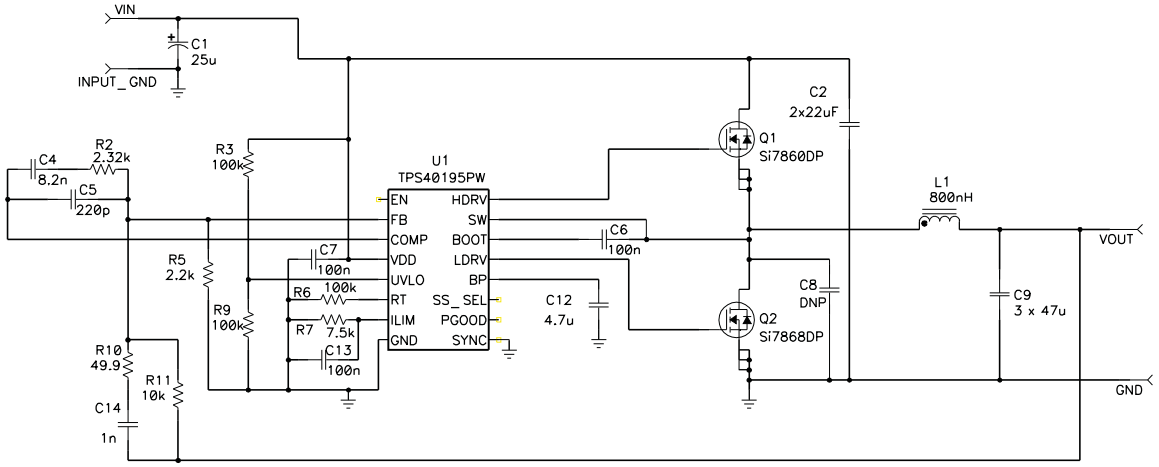


Figure 29. Design Example 2 Schematic

EFFICIENCY vs LOAD CURRENT

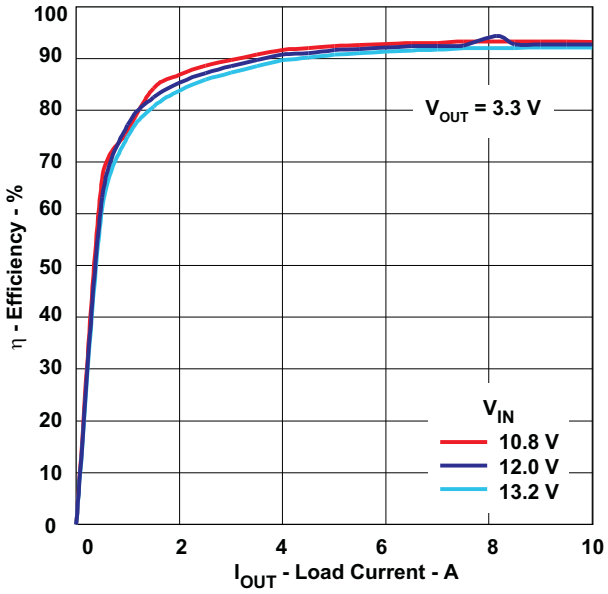


Figure 30.

OUTPUT VOLTAGE vs LOAD CURRENT

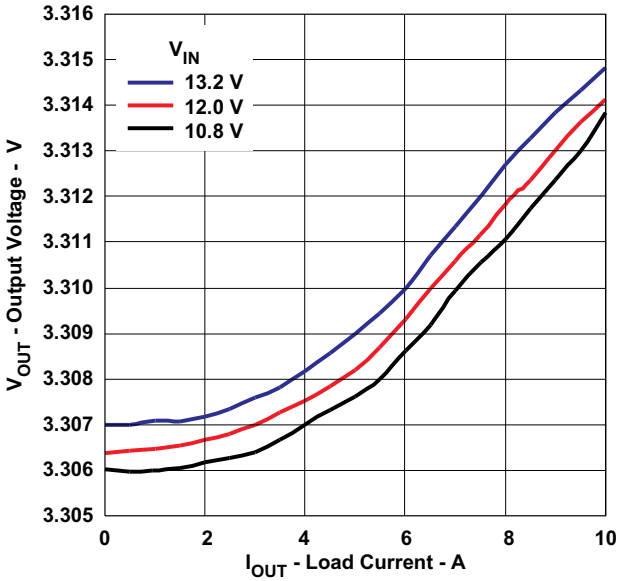


Figure 31.

Table 4. Design Example 2 Bill of Materials

QTY	RefDes	Value	Description	Size	Part Number	MFR
1	C1	25 µF	Capacitor, Aluminun, 25V, SM ±20%	0.406 in × 0.457 in	EEVFK1E471P	Panasonic
2	C2	22 µF	Capacitor, Ceramic, 16V, XR5, 20%	0603	Std	Std
1	C4	8.2 nF	Capacitor, Ceramic, 16V, X7R, 10%	0603	Std	Std
1	C5	220 pF	Capacitor, Ceramic, 16V, X7R, 10%	0603	Std	Std
3	C6, C7, C13	100 nF	Capacitor, Ceramic, 16V, X7R, 10%	0603	Std	Std
1	C8	1 nF	Capacitor, Ceramic, 50V, X7R,10%	0805	Std	Std
1	C9	47 µF	Capacitor, Ceramic, 6.3V, X5R, 20%	1210	C3225X5R0J476M	TDK
1	C12	4.7 µF	Capacitor, Ceramic, 10V, X5R, 10%		Std	Std
1	C14	1 nF	Capacitor, Ceramic, 16V, X7R, 10%	0603	Std	Std
1	L1	800 nH	Inductor, SMT, 31A	0.512 × 0.571 inch	PG0077.801	Pulse
1-	Q1	Si7860DP	MOSFET, N-Ch, 30V, 15A, 11mΩ	SOT-8 PWRPAK	Si7860DP	Vishay
1	Q2	Si7868DP	MOSFET, N-Ch, 20V, 2.75 mΩ, 25 A	SOT-8 PWRPAK	Si7868DP	Vishay
3	R2, R3, R6	2.32 kΩ	Resistor, Chip, 1/16W, 5%	0603	Std	Std
1	R5	2.2 kΩ	Resistor, Chip, 1/16W, 5%	0603	Std	Std
1	R7	7.5 kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R9	100 kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R10	49.9 kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R11	10 kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	U1	TPS40195PW	4.5-V to 20-V Synchronous Buck Controller	TSSOP-16	TPS40195PW	TI

Design Example 3

This design delivers 1 A to 3 A from a 10 V supply. The output voltage may be adjusted from 1 V to 5 V with a single resistor. The part has 57° of phase margin at a crossover frequency of 59 kHz. The design is built on a double sided PC board with an active area of 1.5 cm × 3 cm.

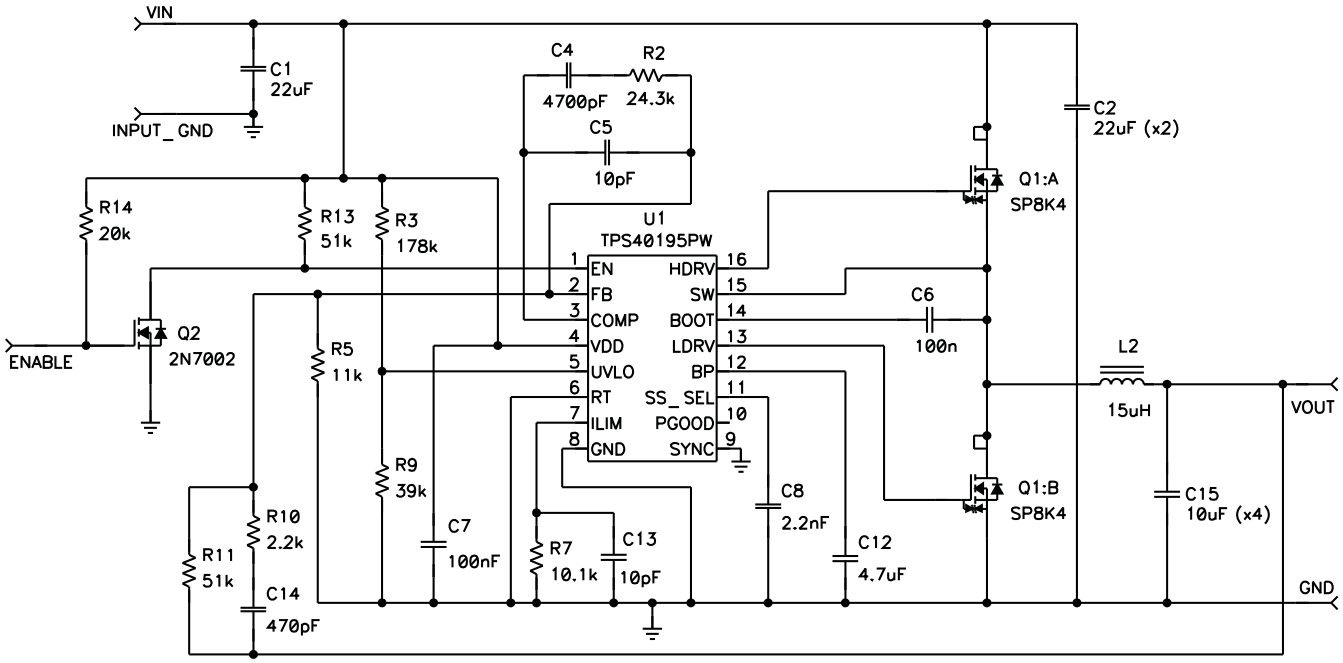


Figure 32. Design Example 3 Schematic

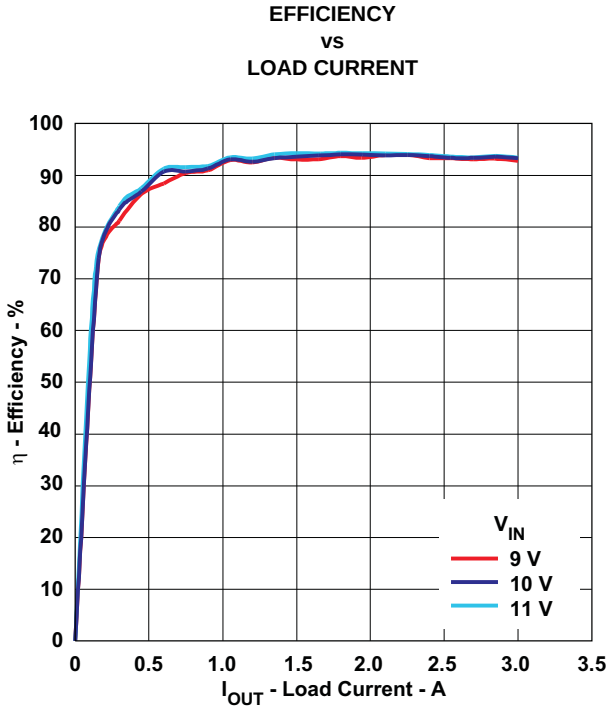


Figure 33.

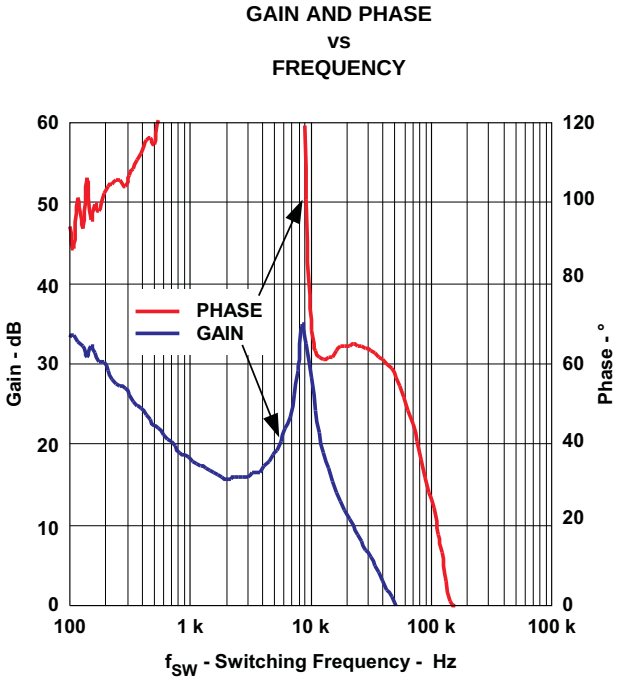


Figure 34.

Table 5. Example 3 Bill of Materials

QTY	RefDes	Value	Description	Size	Part Number	MFR
1	C1	22 µF	Capacitor, Aluminun, 16V, X7R, 20%	1210	Std	TDK
2	C2	22 µF	Capacitor, Ceramic, 16V, XR5, 20%	1210	Std	TDK
1	C4	4700 pF	Capacitor, Ceramic, 25V, X7R, 20%	0402	Std	Std
1	C5	10 pF	Capacitor, Ceramic, 25V, X7R, 20%	0402	Std	Std
2	C6, C7	100 nF	Capacitor, Ceramic, 25V, X7R, 20%	0603	Std	Std
1	C8	2.2 nF	Capacitor, Ceramic, 25V, X7R, 20%	0402	Std	Std
1	C12	4.7 µF	Capacitor, Ceramic, 6.3V, X5R, 20%	0603	Std	Std
1	C13	10 pF	Capacitor, Ceramic, 25V, X7R, 20%	0603	Std	Std
1	C14	470 pF	Capacitor, Ceramic, 25V, X7R, 20%	0402	Std	Std
4	C15	10 µF	Capacitor, Ceramic, 6.3V, X5R, 20%	0805	C2012X5R0J106M	TDK
1	L2	15 µH	Inductor, SMT, 4.2A, 24 mΩ,	0.394 × 0.3941 inch	SLF120565T-150M4R2-PF	TDK
1	Q1	SP8K4	XSTR, MOSFET, Dual N-Ch,30V, 9A	SOP-8	SP8K4	Rohm
1	Q2	2N7002DICT	MOSFET, N-Ch, 60V, 115mA, 1.2Ω	SOT-23	2N7002DICT	Vishay
1	R2	24.3 kΩ	Resistor, Chip, 1/16W, x%	0402	Std	Std
1	R3	178 kΩ	Resistor, Chip, 1/16W, x%	0402	Std	Std
1	R5	11 kΩ	Resistor, Chip, 1/16W, x%	0402	Std	Std
1	R7	10.1 kΩ	Resistor, Chip, 1/16W, x%	0402	Std	Std
1	R9	39 kΩ	Resistor, Chip, 1/16W, x%	0402	Std	Std
1	R10	2.2 kΩ	Resistor, Chip, 1/16W, x%	0402	Std	Std
2	R11, R13	51 kΩ	Resistor, Chip, 1/16W, x%	0402	Std	Std
1	R14	20 kΩ	Resistor, Chip, 1/16W, x%	0402	Std	Std
1	U1	TPS40195PW	4.5-V to 20-V Synchronous Buck Controller	TSSOP-16	TPS40195PW	TI

ADDITIONAL REFERENCES

Related Parts

The following parts have characteristics similar to the TPS40195 and may be of interest.

Table 6. Related Parts

DEVICE	DESCRIPTION
TPS40100	Midrange Input Synchronous Controller with Advanced Sequencing and Output Margining
TPS40075	Wide Input Synchronous Controller with Voltage Feed Forward
TPS40190	Low Pin Count Synchronous Buck Controller
TPS40192/3	4.5V to 18V Input, Low Pin Count, Synchronous Buck Controller with Power Good

References

These references may be found on the web at www.power.ti.com under Technical Documents. Many design tools and links to additional references, including design software, may also be found at www.power.ti.com

1. *Under The Hood Of Low Voltage DC/DC Converters*, SEM 1500 Topdevice 5, 2002 Seminar Series
2. *Understanding Buck Power Stages in Switchmode Power Supplies*, SLVA057, March 1999
3. *Design and Application Guide for High Speed MOSFET Gate Drive Circuits*, SEM 1400, 2001 Seminar Series
4. *Designing Stable Control Loops*, SEM 1400, 2001 Seminar Series
5. Additional PowerPAD™ information may be found in Applications Briefs SLMA002 and SLMA004
6. QFN/SON PCB Attachment, Texas Instruments Literature Number SLUA271, June 2002

REVISION HISTORY

Changes from Revision D (November 2008) to Revision E **Page**

- Added a new paragraph to the end of the Enable Functionality section 13

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS40195PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	40195	Samples
TPS40195PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	40195	Samples
TPS40195PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	40195	Samples
TPS40195PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	40195	Samples
TPS40195RGYR	ACTIVE	VQFN	RGY	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-2-260C-1 YEAR	-40 to 85	40195	Samples
TPS40195RGYRG4	ACTIVE	VQFN	RGY	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	40195	Samples
TPS40195RGYT	ACTIVE	VQFN	RGY	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-2-260C-1 YEAR	-40 to 85	40195	Samples
TPS40195RGYTG4	ACTIVE	VQFN	RGY	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	40195	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

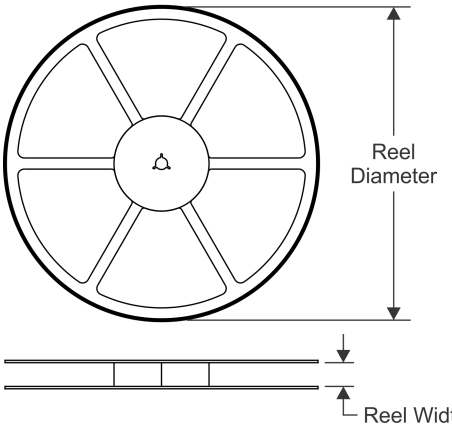
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

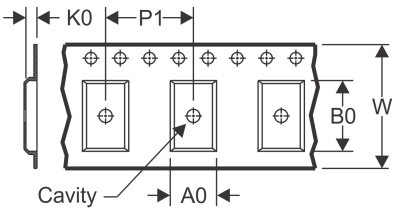
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

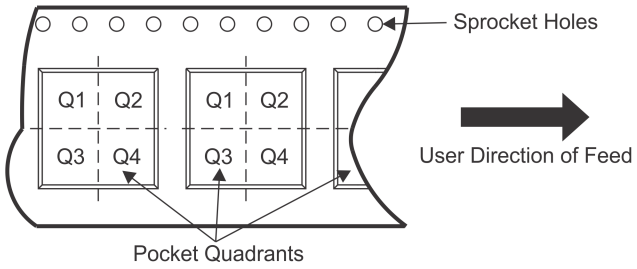


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

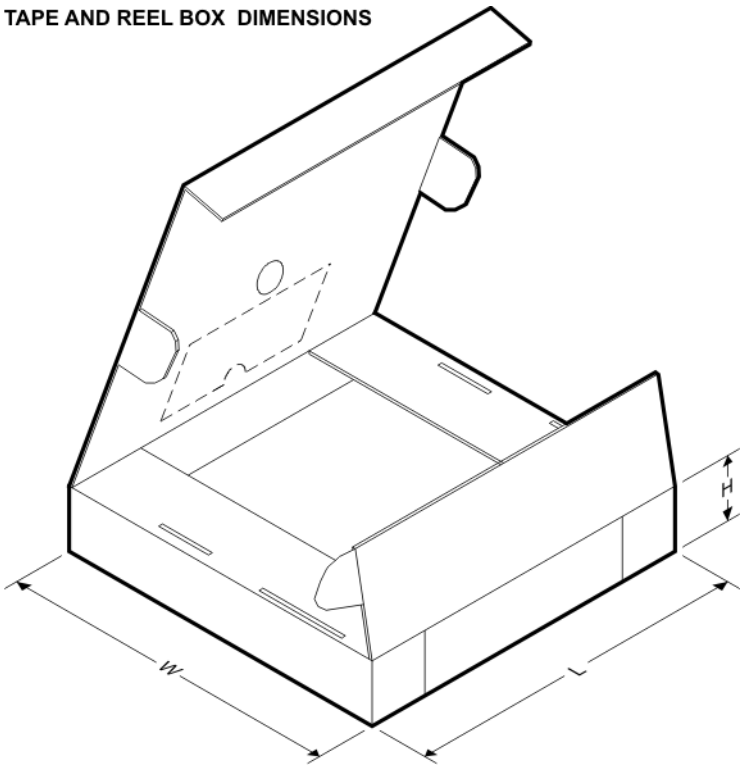
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS40195PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS40195RGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
TPS40195RGYR	VQFN	RGY	16	3000	330.0	12.4	3.71	4.21	1.11	8.0	12.0	Q1
TPS40195RGYT	VQFN	RGY	16	250	180.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
TPS40195RGYT	VQFN	RGY	16	250	330.0	12.4	3.71	4.21	1.11	8.0	12.0	Q2

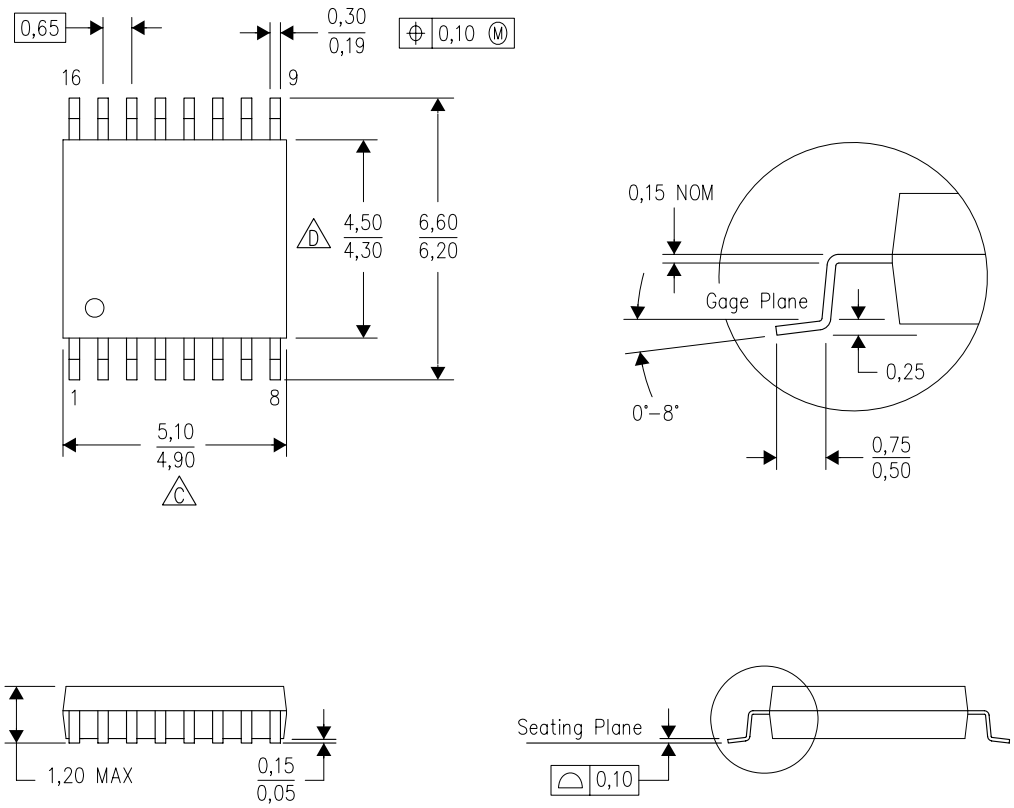
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS40195PWR	TSSOP	PW	16	2000	367.0	367.0	35.0
TPS40195RGYR	VQFN	RGY	16	3000	367.0	367.0	35.0
TPS40195RGYR	VQFN	RGY	16	3000	338.0	355.0	50.0
TPS40195RGYT	VQFN	RGY	16	250	210.0	185.0	35.0
TPS40195RGYT	VQFN	RGY	16	250	338.0	355.0	50.0

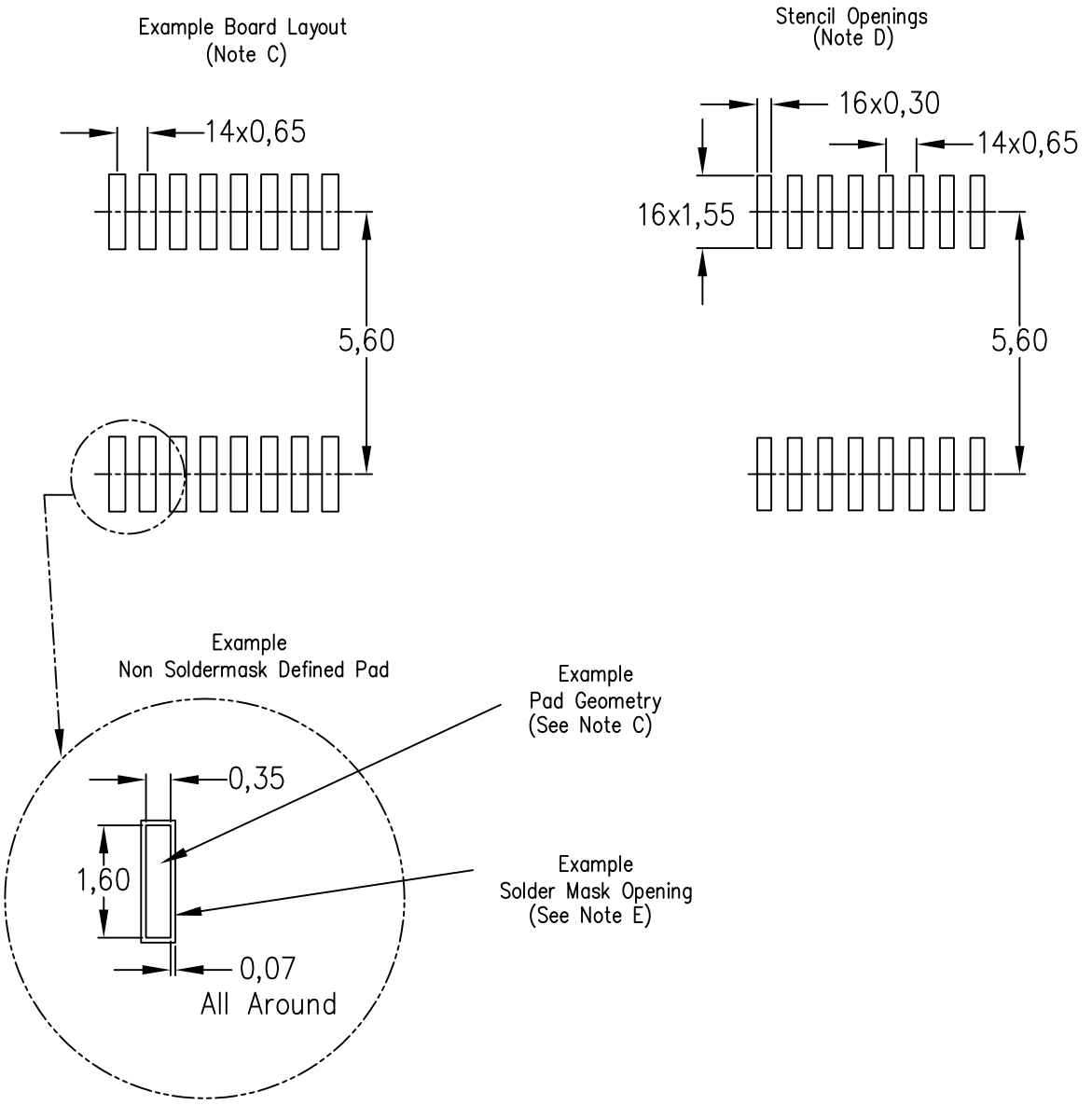
PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



4040064–4/G 02/11

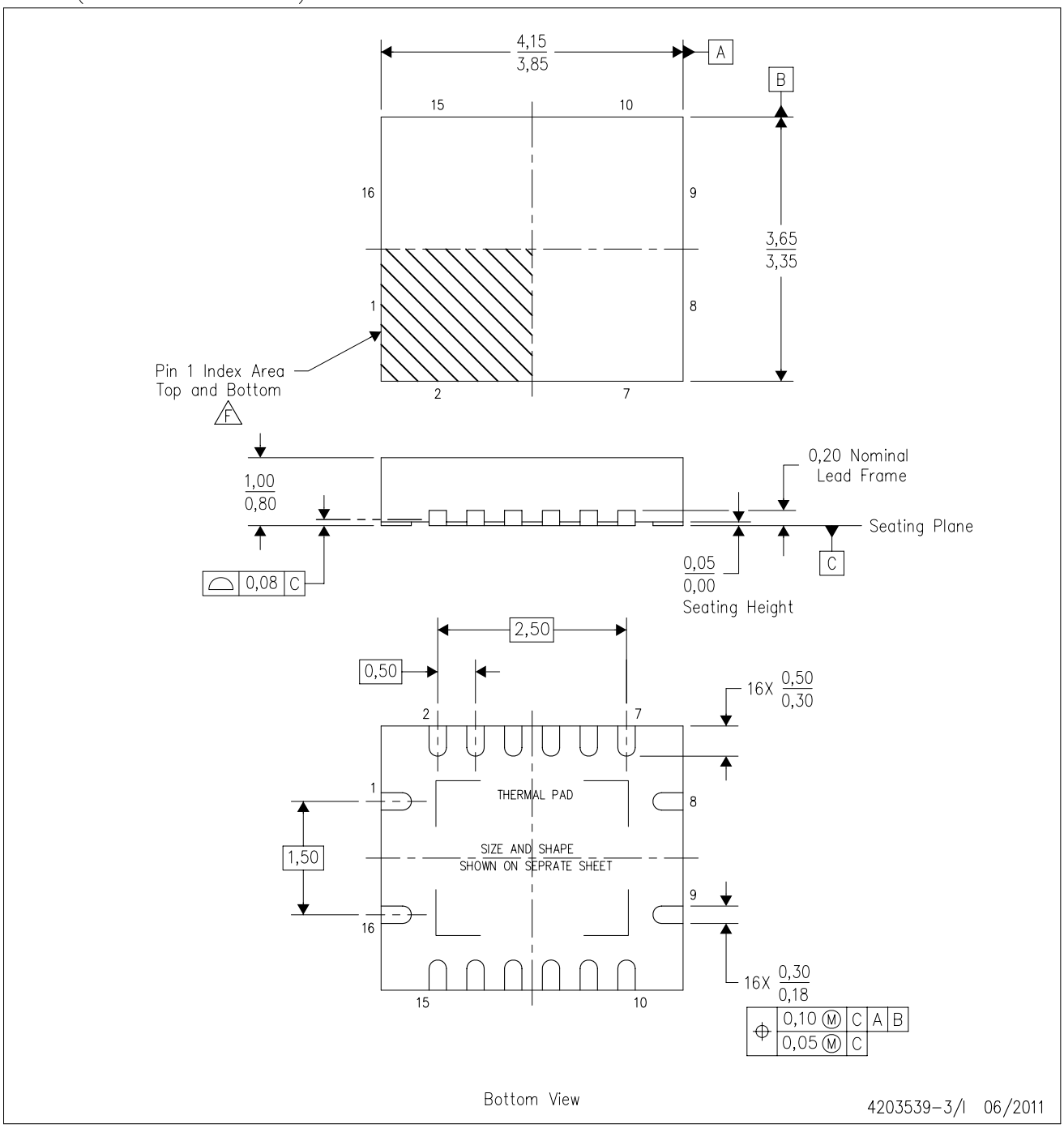
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
G. Package complies to JEDEC MO–241 variation BA.

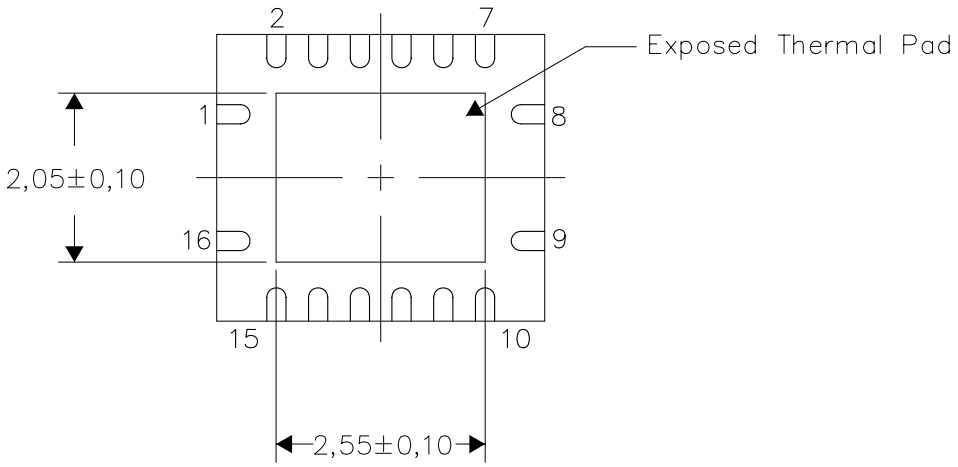
RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



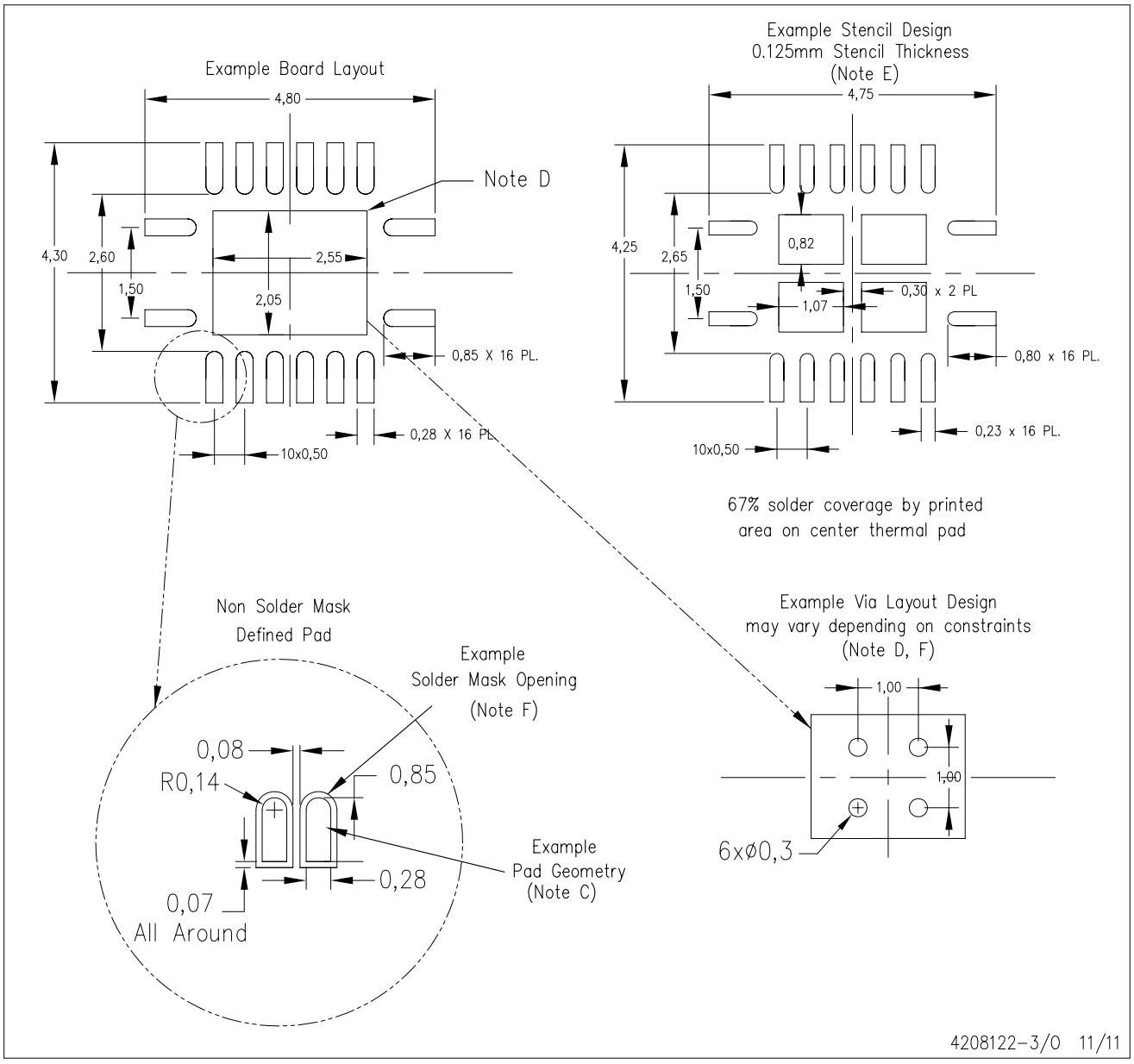
Bottom View

Exposed Thermal Pad Dimensions

4206353–3/0 11/11

NOTE: All linear dimensions are in millimeters

RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265