GS1524A HD-LINX®II Adaptive Cable Equalizer

Features

- SMPTE 292M, SMPTE 344M and SMPTE 259M compliant
- Automatic cable equalization
- Multi-standard operation from 143Mb/s to 1.485Gb/s
- Supports DVB-ASI at 270Mb/s
- Pb-free and RoHS Compliant
- Pin compatible with the GS9064 Cable Equalizer
- Manual bypass (useful for low data rates with slow rise/fall times)
- Performance optimized for 270Mb/s and 1.485Gb/s
- Typical maximum equalized length of Belden 1694A cable: 140m at 1.485Gb/s, 350m at 270Mb/s
- 50Ω differential output (with internal 50Ω pull-ups)
- Manual output mute or programmable mute based on max cable length adjust
- Cable length indicator for SMPTE 259M inputs
- Single 3.3V power supply operation
- Operating temperature range: 0°C to +70°C

Applications

- SMPTE 292M, SMPTE 344M and SMPTE 259M Coaxial Cable Serial Digital Interfaces.

Description

The GS1524A is a second-generation high-speed bipolar integrated circuit designed to equalize and restore signals received over 75Ω co-axial cable.

The GS1524A is designed to support SMPTE 292M, SMPTE 344M and SMPTE 259M, and is optimized for performance at 270Mb/s and 1.485Gb/s.

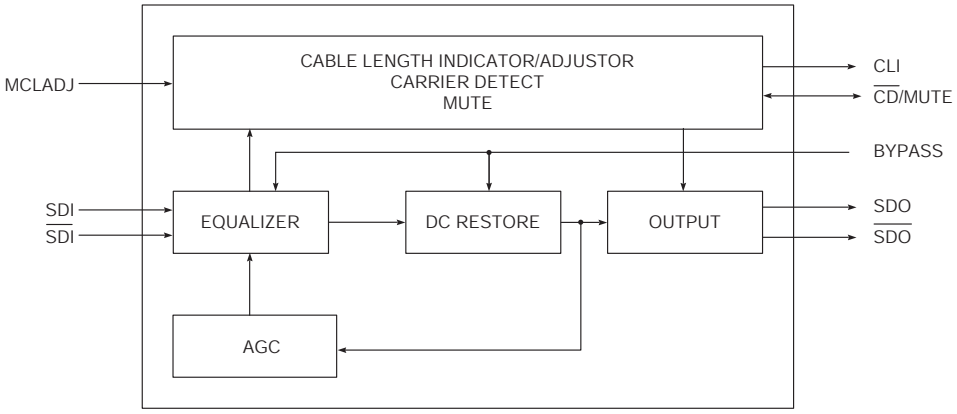
The GS1524A features DC restoration to compensate for the DC content of SMPTE pathological test patterns. The device also incorporates a Cable Length Indicator (CLI) that provides an indication of the amount of cable being equalized for data rates up to 360Mb/s.

A voltage programmable mute threshold (MCLADJ) is included to allow muting of the GS1524A output when an approximate selected cable length is reached for SMPTE 259M signals. This feature allows the GS1524A to distinguish between low amplitude SD-SDI signals and noise at the input of the device.

The bidirectional $\overline{CD}$/MUTE pin indicates the presence of a valid signal at the input of the GS1524A in addition to functioning as a mute control input. The outputs of the GS1524A will be forced to a mute state when an invalid input reference signal is applied to the input of the device or the application layer sets the $\overline{CD}$/MUTE pin HIGH. If the application layer forces $\overline{CD}$/MUTE LOW, the serial digital output of the device will always be active.

Power consumption is typically 265mW using a 3.3V power supply.

The GS1524A is Pb-free, and the encapsulation compound does not contain halogenated flame retardant (RoHS Compliant).



GS1524A Functional Block Diagram

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1. Pin Out

1.1 GS1524A Pin Assignment

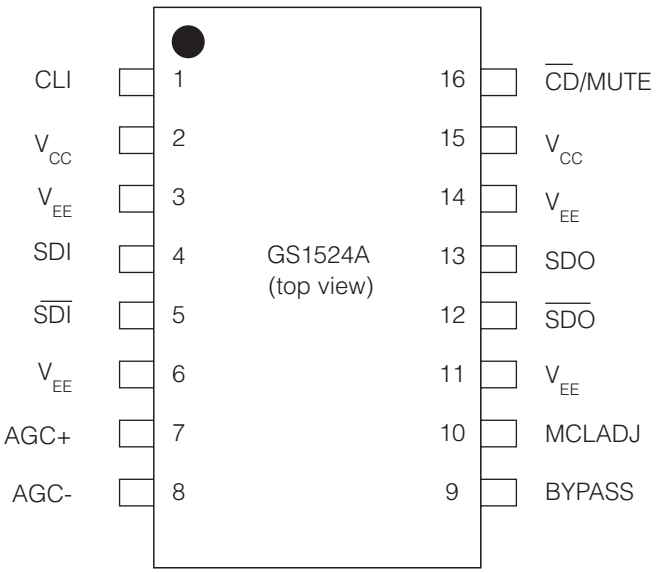


Figure 1-1: 16-Pin SOIC

1.2 GS1524A Pin Descriptions

Table 1-1: GS1524A Pin Descriptions

Pin Number	Name	Timing	Type	Description
1	CLI	Analog	Output	Cable Length Indicator. An analog voltage will be output proportional to the cable length connected to the serial digital input. NOTE: CLI is recommended for data rates up the 360Mb/s only.
2, 15	V_{CC}	Analog	Power	Most positive power supply connection. Connect to +3.3V DC.
3, 6, 11, 14	V_{EE}	Analog	Power	Most negative power supply connection. Connect to GND.
4, 5	SDI, $\overline{SDI}$	Analog	Input	Serial digital differential input.
7, 8	AGC+, AGC-	Analog	–	External AGC capacitor. Connect pin 7 and pin 8 together through a 1uF capacitor.
9	BYPASS	Not Synchronous	Input	Forces the Equalizing and DC RESTORE stages into bypass mode when HIGH. No equalization occurs in this mode.
10	MCLADJ	Analog	Input	Maximum cable length adjust. Adjusts the approximate maximum amount of cable to be equalized (from 0m to the maximum cable length). The output is muted (latched to the last state) when the maximum cable length is achieved. NOTE: MCLADJ is only recommended for data rates up to 360Mb/s.
12, 13	$\overline{SDO}$, SDO	Analog	Output	Equalized serial digital differential output.
16	$\overline{CD}$/MUTE	Not Synchronous	Bidirectional	STATUS SIGNAL OUTPUT / CONTROL SIGNAL INPUT levels are LVCMOS/LVTTL compatible. OUTPUT ($\overline{CD}$): Indicates the presence of a valid input signal. When the $\overline{CD}$ pin is LOW, a valid input signal has been detected. When this pin is HIGH, the input signal is invalid. If $\overline{CD}$ is set HIGH, the serial digital output of the device will be forced to a steady state (latched to the last state). NOTE: This pin will indicate loss of carrier for data rates > 19Mb/s. INPUT (MUTE): When the MUTE pin is set HIGH by the application interface, the serial digital output of the device will be forced to a steady state (latched to the last state). When the MUTE pin is set LOW, the serial digital output of the device will be active. NOTE: The $\overline{CD}$/MUTE pin is not functional when BYPASS is set HIGH.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Parameter	Value
Supply Voltage	-0.5V to +3.6 V_{DC}
Input ESD Voltage	2kV
Storage Temperature Range	-50°C < T_s < 125°C
Input Voltage Range (any input)	-0.3 to (V_{CC} +0.3)V
Operating Temperature Range	0°C to 70°C
Solder Reflow Temperature	260°C

2.2 DC Electrical Characteristics

Table 2-1: DC Electrical Characteristics

V_{DD} = 3.3V, T_A = 0°C to 70°C, unless otherwise shown

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Supply Voltage	V_{CC}	–	3.135	3.3	3.465	V	±5%
Power Consumption	P_D	T_A = 25°C	–	265	–	mW	–
Supply Current	I_s	T_A = 25°C	–	80	–	mA	–
Output Common Mode Voltage	V_{CMOUT}	T_A = 25°C	–	V_{CC} - ΔV_{SDO}/2	–	V	–
Input Common Mode Voltage	V_{CMIN}	T_A = 25°C	–	1.75	–	V	–
CLI DC Voltage (0m)	–	T_A = 25°C	–	2.5	–	V	–
CLI DC Voltage (no signal)	–	T_A = 25°C	–	1.9	–	V	–
MCLADJ DC Voltage (to mute signal)	–	0m, T_A = 25°C	–	1.3	–	V	–
MCLADJ Range	–	T_A = 25°C	–	0.69	–	V	–
$\overline{CD}$/MUTE Output Voltage	$V_{\overline{CD}/MUTE(OH)}$	Carrier not present	2.4	–	–	V	–
	$V_{\overline{CD}/MUTE(OL)}$	Carrier present	–	–	0.4	V	–

Table 2-1: DC Electrical Characteristics

V_{DD} = 3.3V, T_A = 0°C to 70°C, unless otherwise shown

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
$\overline{CD}$/MUTE Input Voltage Required to Force Outputs to Mute	$V_{\overline{CD}/MUTE}$	Mute	2.0	–	–	V	–
$\overline{CD}$/MUTE Input Voltage Required to Force Outputs Active	$V_{\overline{CD}/MUTE}$	Activate	–	–	0.8	V	–

2.3 AC Electrical Characteristics

V_{DD} = 3.3V, T_A = 0°C to 70°C, unless otherwise shown

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Serial input data rate	DR_{SDO}	GS1524A	143	–	1485	Mb/s	–
Input Voltage Swing	ΔV_{SDI}	T_A =25°C, at transmitter	720	800	950	mV_{p-p}	–
Output Voltage Swing	ΔV_{SDO}	50Ω load, T_A =25°C, differential	–	750	–	mV_{p-p}	–
Output Jitter	–	270Mb/s, Belden 1694A, 350m equalized cable	–	0.2	–	UI	1
	–	270Mb/s, Belden 8281, 280m equalized cable	–	0.2	–	UI	1
	–	1.485Gb/s, Belden 1694A, 140m equalized cable	–	0.25	–	UI	1
	–	1.485Gb/s, Belden 8281, 100m equalized cable	–	0.25	–	UI	1
Output Rise/Fall time	–	20% - 80%	–	80	220	ps	–
Mismatch in rise/fall time	–	–	–	–	30	ps	–
Duty cycle distortion	–	–	–	–	30	ps	–
Overshoot	–	–	–	–	10	%	–
Input Return Loss	–	–	15	–	–	dB	2
Input Resistance	–	single ended	–	1.64	–	kΩ	–
Input Capacitance	–	single ended	–	1	–	pF	–
Output Resistance	–	single ended	–	50	–	Ω	–

NOTES:

1. Equalizer Pathological.
2. Tested on CB1524 board from 5MHz to 2GHz.

2.4 Solder Reflow Profiles

The device is manufactured with Matte-Sn terminations and is compatible with both standard eutectic and Pb-free solder reflow profiles. MSL qualification was performed using the maximum Pb-free reflow profile shown in Figure 2-1. The recommended standard Pb reflow profile is shown in Figure 2-2.

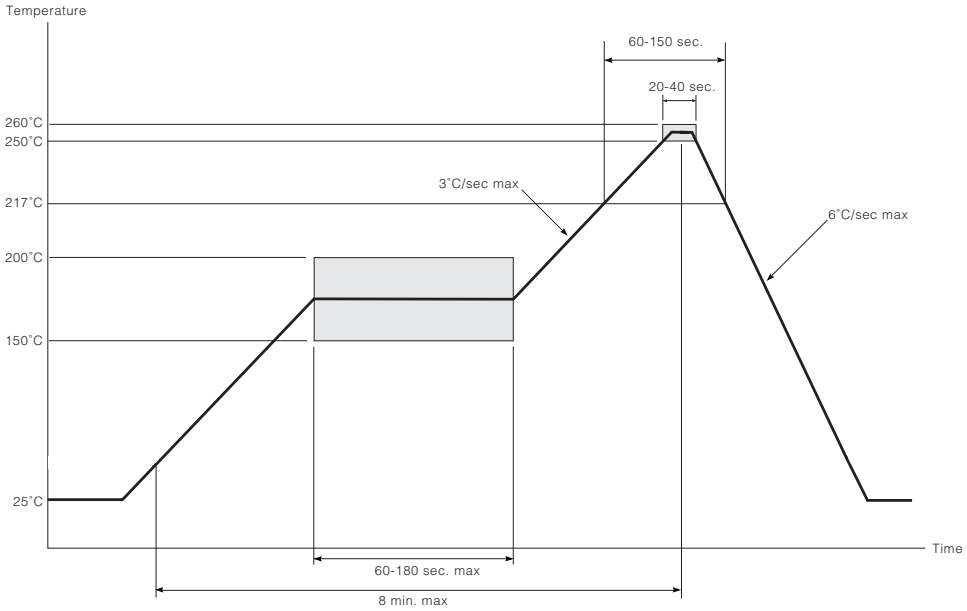


Figure 2-1: Maximum Pb-free Solder Reflow Profile (Preferred)

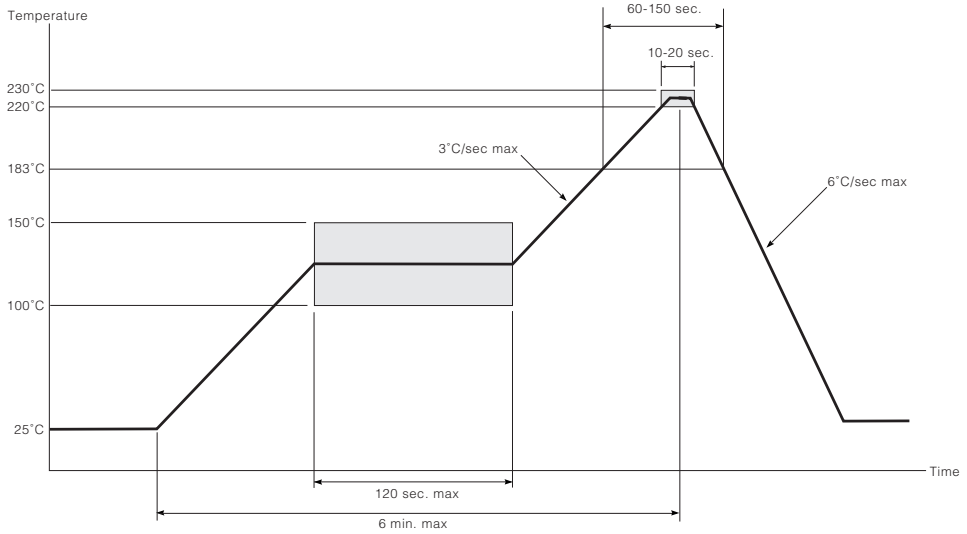


Figure 2-2: Standard Pb Solder Reflow Profile (Pb-free package)

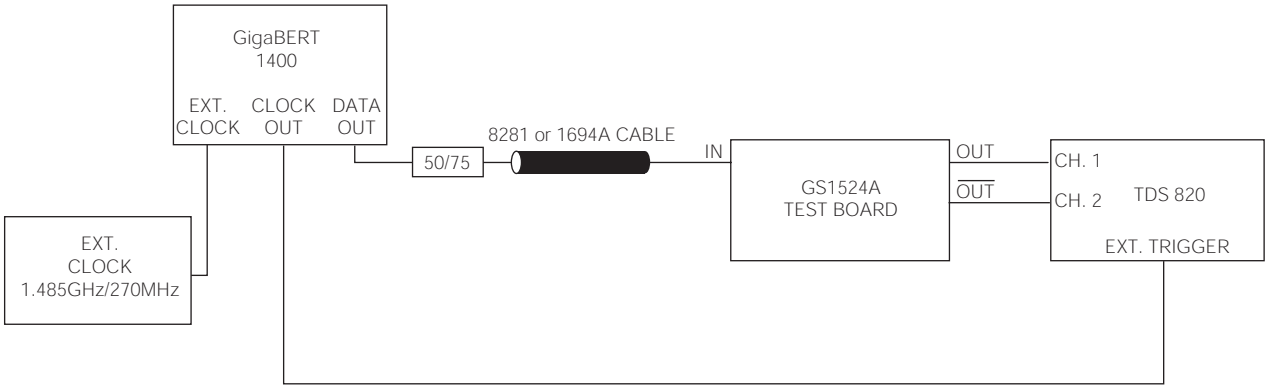


Figure 2-3: Test Circuit

3. Input / Output Circuits

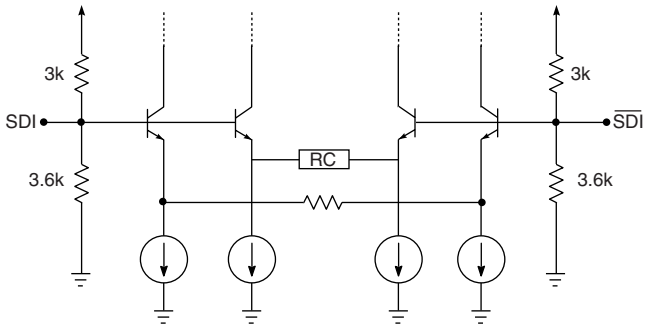


Figure 3-1: Input Equivalent Circuit

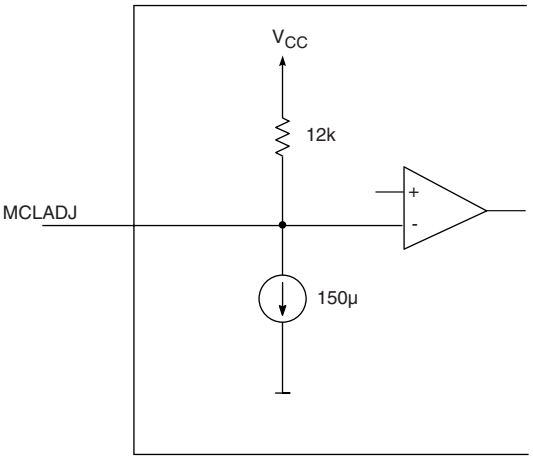


Figure 3-2: MCLADJ Equivalent Circuit

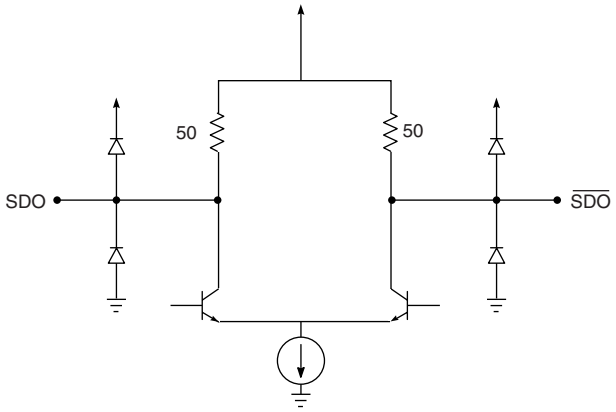


Figure 3-3: Output Circuit

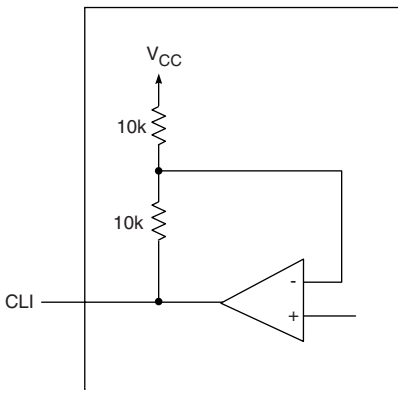


Figure 3-4: CLI Output Circuit

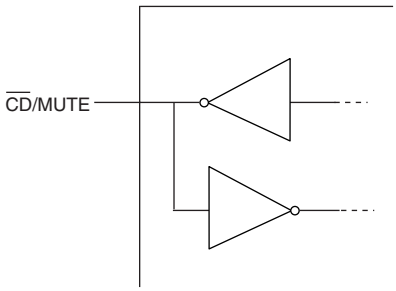


Figure 3-5: $\overline{CD}$/MUTE Circuit

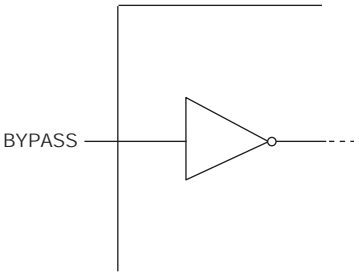


Figure 3-6: Bypass Circuit

4. Detailed Description

The GS1524A is a high speed bipolar IC designed to equalize serial digital signals.

The GS1524A can equalize both HD and SD serial digital signals, and will typically equalize greater than 140m of Belden 1694A cable at 1.485Gb/s and 350m at 270Mb/s.

The GS1524A/ is powered from a single +3.3V power supply and consumes approximately 265mW of power.

4.1 Serial Digital Inputs

The serial data signal may be connected to the input pins (SDI/$\overline{\text{SDI}}$) in either a differential or single ended configuration. AC coupling of the inputs is recommended, as the SDI and $\overline{\text{SDI}}$ inputs are internally biased at approximately 1.8V.

4.2 Cable Equalization

The input signal passes through a variable gain equalizing stage whose frequency response closely matches the inverse of the cable loss characteristic. In addition, the variation of the frequency response with control voltage imitates the variation of the inverse cable loss characteristic with cable length.

The edge energy of the equalized signal is monitored by a detector circuit which produces an error signal corresponding to the difference between the desired edge energy and the actual edge energy. This error signal is integrated by both an internal and an external AGC filter capacitor providing a steady control voltage for the gain stage. As the frequency response of the gain stage is automatically varied by the application of negative feedback, the edge energy of the equalized signal is kept at a constant level which is representative of the original edge energy at the transmitter. The equalized signal is also DC restored, effectively restoring the logic threshold of the equalized signal to its correct level independent of shifts due to AC coupling. The digital output signals have a nominal voltage of 750mV$_{pp}$ differential, or 375mV$_{pp}$ single ended when terminated with 50Ω as shown in Figure 4-1.

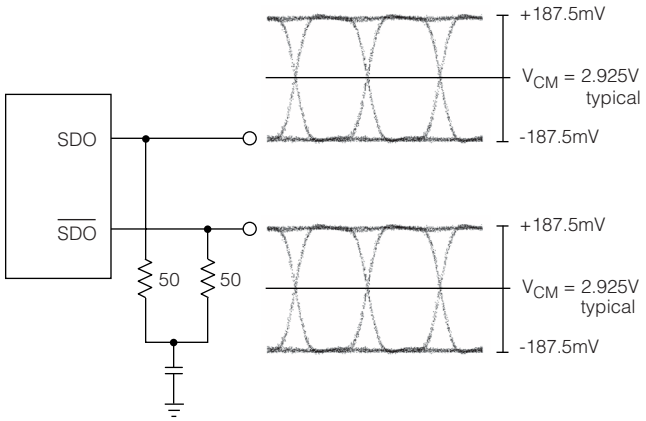


Figure 4-1: Typical Output Voltage Levels

4.3 Programmable Mute Output and Cable Length Indicator

For SMPTE 259M inputs, the GS1524A incorporates a programmable threshold output mute (MCLADJ) and an analog cable length indicator (CLI).

MCLADJ

In applications where there are multiple input channels using the GS1524A, it is advantageous to have a programmable mute output to avoid signal crosstalk.

The output of the GS1524A can be muted when the input signal decreases below a certain input level. This threshold is determined using the input voltage applied to the MCLADJ pin. The MCLADJ pin may be left unconnected for applications where output muting is not required.

This feature has been designed for use in applications such as routers where signal crosstalk and circuit noise cause the equalizer to output erroneous data when no input signal is present. The use of a Carrier Detect function with a fixed internal reference does not solve this problem since the signal to noise ratio on the circuit board could be significantly less than the default signal detection level set by the on chip reference.

NOTE: MCLADJ is only recommended for data rates up to 360Mb/s.

CLI

The output voltage of the CLI pin is an approximation of the amount of cable present at the GS1524A input. With 0m of cable, 800mV input signal levels, and a data rate of 270Mb/s, the CLI output voltage is approximately 2.5V. As the cable length increases, the CLI voltage decreases providing an approximate correlation between the CLI voltage and cable length.

NOTE: CLI is only recommended for data rates up to 360Mb/s.

4.4 Mute and Carrier Detect

In addition to the programmable mute output and cable length indicator, the GS1524A includes a multi-function $\overline{CD}$/MUTE bidirectional pin that provides the following functions:

INPUT (MUTE)

Applying a HIGH INPUT to the $\overline{CD}$/MUTE pin forces the GS1524A outputs to a muted condition. The minimum voltage required to force the outputs to a muted condition is listed in the DC electrical characteristics table. In this condition the outputs will be latched to the last logic level present at the output to avoid signal crosstalk.

Applying a LOW INPUT to the $\overline{CD}$/MUTE pin will force the GS1524A outputs to remain active regardless of the length of input cable and the voltage applied to the MCLADJ pin. See the DC electrical characteristics table for voltage levels.

OUTPUT ($\overline{CD}$)

When used as an OUTPUT, the $\overline{CD}$/MUTE pin will indicate the presence of a valid input signal. When $\overline{CD}$/MUTE is LOW, a valid input signal has been detected at the input of the device. When $\overline{CD}$/MUTE is HIGH, the input signal is invalid. This pin will indicate loss of carrier for data rates greater than 19Mb/s.

NOTE: The $\overline{CD}$/MUTE pin is not functional in BYPASS mode.

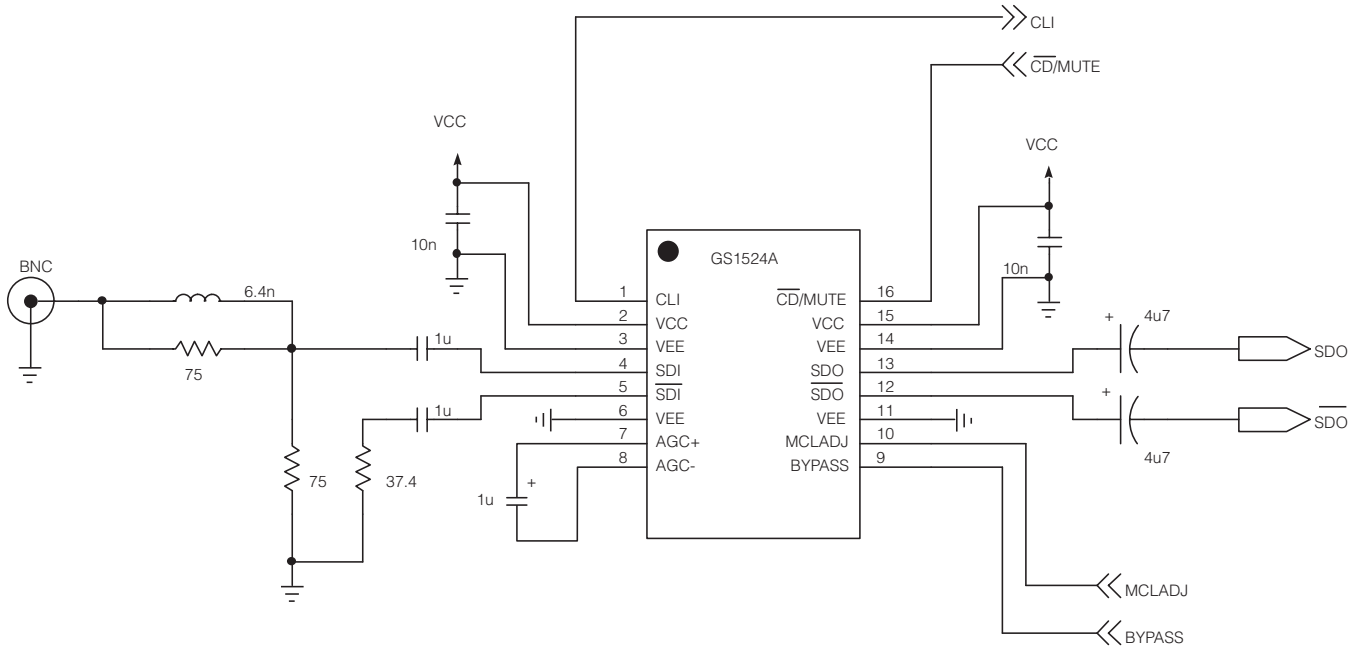
5. Application Information

5.1 PCB Layout

Special attention must be paid to component layout when designing serial digital interfaces for HDTV. An FR-4 dielectric can be used, however, controlled impedance transmission lines are required for PCB traces longer than approximately 1cm. Note the following PCB artwork features used to optimize performance:

- PCB trace width for HD rate signals is closely matched to SMT component width to minimize reflections due to change in trace impedance.
- The PCB ground plane is removed under the GS1524A input components to minimize parasitic capacitance.
- The PCB ground plane is removed under the GS1524A output components to minimize parasitic capacitance.
- High speed traces are curved to minimize impedance changes.

5.2 Typical Application Circuits

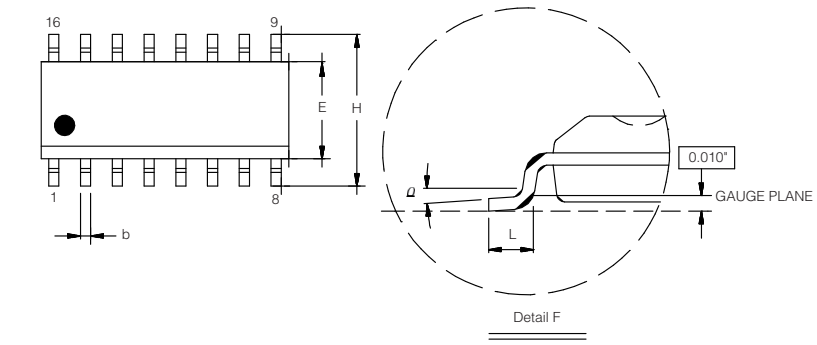


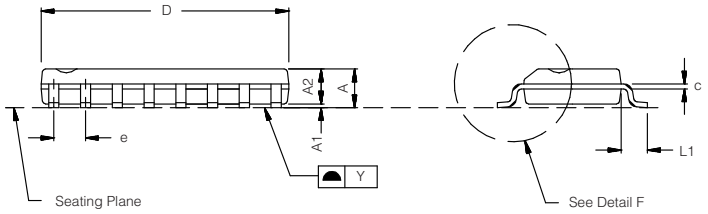
NOTE: All resistors in Ohms, capacitors in Farads, and inductors in Henrys, unless otherwise noted.

Figure 5-1: GS1524A Typical Application Circuit

6. Package & Ordering Information

6.1 Package Dimensions





* CONTROLLING DIMENSION: MM

Symbol	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.35	1.63	1.75	0.053	0.064	0.069
A1	0.10	0.15	0.25	0.004	0.006	0.010
A2	1.30	1.40	1.50	0.051	0.055	0.059
b	0.33	0.41	0.51	0.013	0.016	0.020
c	0.19		0.25	0.007		0.010
D	9.80	9.91	10.01	0.386	0.390	0.394
E	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.50	
H	5.80	6.00	6.20	0.228	0.236	0.244
L	0.40	0.64	1.27	0.016	0.025	0.050
L1		1.07			0.042	
Y			0.10			0.004
Ω	0°		8°	0°		8°

6.2 Packaging Data

Parameter	Value
Package Type	SOIC 16L
Package Drawing Reference	JEDEC MS012
Moisture Sensitivity Level	2
Junction to Air Thermal Resistance, θ_{j-a} (at zero airflow)	94.1°C/W
Pb-free and RoHS Compliant	Yes

6.3 Ordering Information

	Part Number	Package	Temperature Range
GS1524A	GS1524ACKDE3	Pb-free 16-Pin SOIC	0°C to 70°C

7. Revision History

Version	ECR	Date	Changes and/or Modifications
A	131284	March 2004	New document.
0	135247	December 2004	Changed to Preliminary Data Sheet. Removed references to GS9064A. Updated AC, DC and Absolute Maximum Ratings tables. Added solder reflow profiles. Added Packaging Data information. Corrected minor typing errors.
1	136832	May 2005	Updated document status to Data Sheet. Updated all 'Green' references to say 'RoHS Compliant'. Clarified naming of solder reflow profiles and re-ordered profiles to show preference for Pb-free profile. Removed 'Proprietary and Confidential' footer. Corrected minor typing errors.

CAUTION
ELECTROSTATIC SENSITIVE DEVICES
DO NOT OPEN PACKAGES OR HANDLE
EXCEPT AT A STATIC-FREE WORKSTATION



DOCUMENT IDENTIFICATION
DATA SHEET
The product is in production. Gennum reserves the right to make changes to the product at any time without notice to improve reliability, function or design, in order to provide the best product possible.

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