

SCM-i.MX 6SX Data Sheet for Industrial Products

1. Introduction

NXP Single Chip System Modules (SCMs) are a suite of highly integrated products in an ultra-small form factor. The member of this portfolio, the NXP SCM-i.MX 6SoloX, drastically reduces time to market by providing a solution that minimizes design time. We've integrated and validated the i.MX 6SoloX applications processor with the power management system and LPDDR2 memory into a 13x13mm package. It is a small yet powerful solution intended for use in a wide variety of industrial applications.

The SCM-i.MX 6SoloX speeds and eases development time by addressing technology challenges such as design of DDR and power management. Our single chip module consists of the i.MX 6SoloX applications processor, MMPF0100 (PMIC) for power management, along with a mix of discrete components, and is enabled for LPDDR2 memory through a PoP package assembly.

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1.1. Ordering information

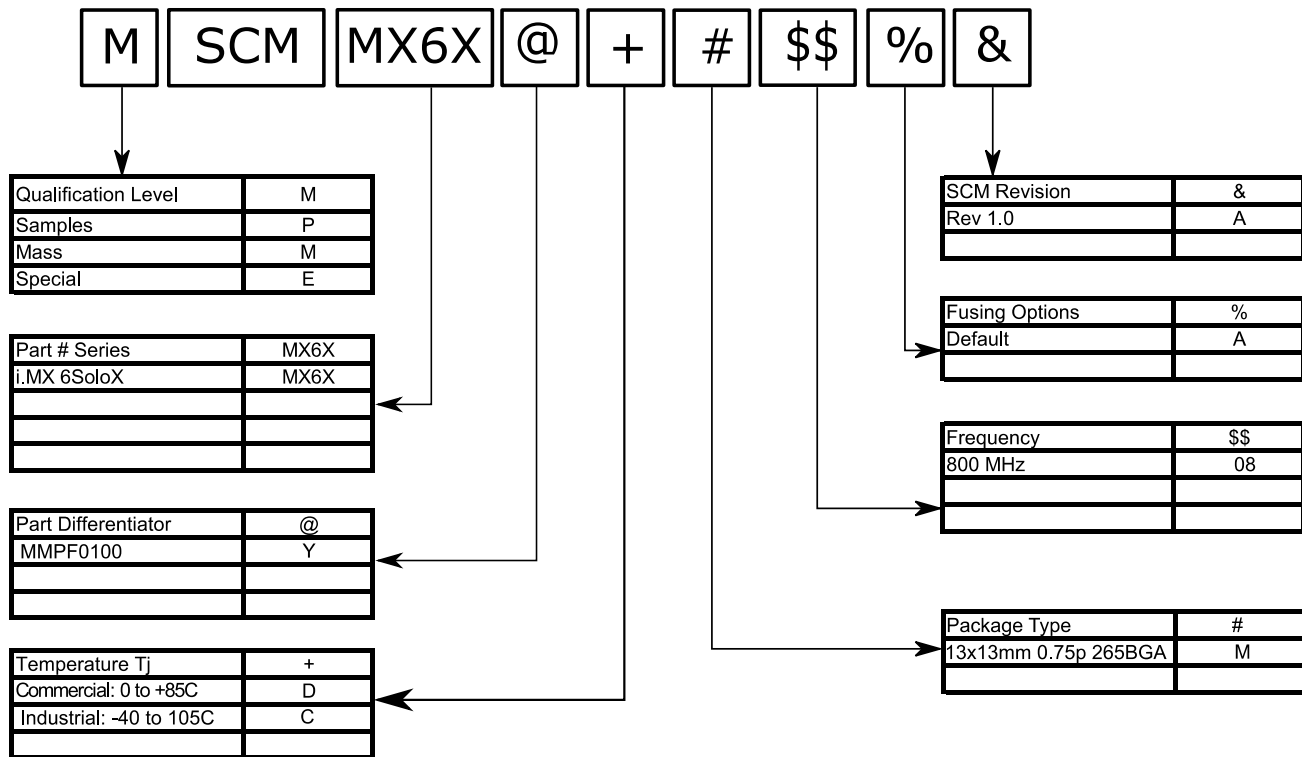


Figure 1. Part number nomenclature

The table below shows examples of orderable part numbers.

Table 1. Orderable part numbers

Part Number	Cortex A9 Speed ¹	Junction Temperature Range	Package Type
MSCMMX6XYCM08AA	800 MHz	Industrial: -40 to 105°C	265 pin BGA

- If a 24 MHz input clock is used (required for USB), the maximum Cortex-A9 speed for 800 MHz speed grade is limited to 792 MHz.

1.2. Features

The SCM-i.MX 6SoloX integrates the i.MX6SoloX processor with the MMPF0100 PMIC inside a 13x13mm BGA package that supports a variety of LPDDR2 memory configurations through a 168ball PoP interface. This part is packaged in a 265 pin BGA which uses a diagonal ball array and a 0.75mm pitch to allow for all pins to be brought out on a 4-layer PCB.

1.2.1. i.MX 6SoloX features

The i.MX 6SoloX processor features NXP's advanced implementation of the single ARM® Cortex®-A9 core in addition to the ARM Cortex-M4 core. This type of heterogeneous multicore architecture provides greater levels of system integration, smart low-power system awareness, and fast real-time

responsiveness. The i.MX 6SoloX includes a GPU processor capable of supporting 2D and 3D operations, a wide range of display and connectivity options, and integrated power management.

For a full list of module features see [Table 3](#).

1.2.2. MMPF0100 Features in this Package

- Three buck converters.
- Boost regulator to 5.0 V output for USB OTG support.
- Three general purpose linear regulators
- Programmable output voltage, sequence, and timing
- OTP (One Time Programmable) memory for device configuration
- Coin cell charger and RTC supply
- Power control logic with processor interface and event detection
- I2C control
- Individually programmable ON, OFF, and Standby modes

1.3. References

This document is intended to be a companion to the data sheets of the following integrated parts:

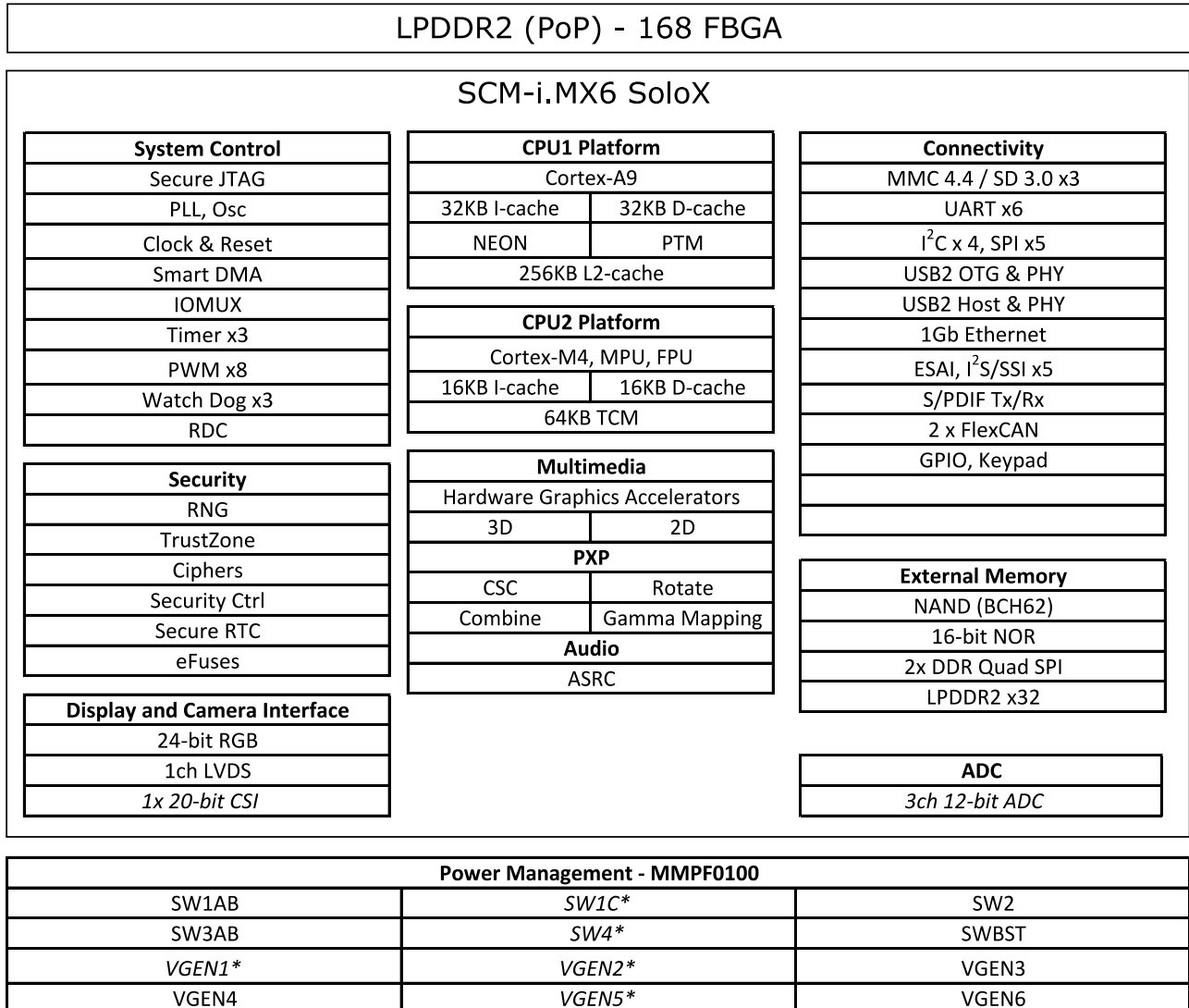
- *NXP i.MX SoloX Data Sheet for Industrial Products* (document [IMX6SXIEC](#))
- *NXP MMPF0100* (document [MMPF0100Z](#))

2. Architectural overview

The following subsections provide an architectural overview of the SCM-i.MX 6SoloX system.

2.1. Block diagram

The following figure shows the main functional relationship between the i.MX6SX, PMIC, Memory and PCB in the SCM-i.MX 6SoloX. It purposely does not show all of the functional modules in the part – that is found in [Section 3](#), “[Modules list](#)”.



* These features are either unavailable or reduced in functionality.

Figure 2. SCM-i.MX6SX block diagram

3. Modules list

Table 2. SCM modules overview

Block Name	Description/Notes
i.MX6SoloX	Freescale i.MX6SoloX Applications Processor. Defeatured from the standard discrete part. See Table 3 for details on feature availability and/or deratings.
MMPF0100	Power management IC requires only a single supply and can provide power and voltage references to entire SCM. See Section 4, "Electrical characteristics" for electrical details.
LPDDR2 PoP Interface	Interface to support LPDDR2 in PoP configuration using a 12mm x 12mm FBGA168 footprint.

The SCM-i.MX 6SoloX processors contain a variety of digital and analog modules. This table describes these modules in alphabetical order:

Table 3. SCM-i.MX 6SoloX modules list

Block Mnemonic	Block Name	Subsystem	Brief Description	Availability
ADC1	Analog to Digital Converter	—	The ADC is a 12-bit general purpose analog to digital converter.	Only 3 channels of ADC1
ARM	ARM Platform	ARM	The ARM Core Platform includes 1xCortex-A9 and 1xCortex-M4 cores. It also includes associated sub-blocks, such as the Level 2 Cache Controller, SCU (Snoop Control Unit), GIC (General Interrupt Controller), private timers, watchdog, and CoreSight debug modules.	Full Feature
ASRC	Asynchronous Sample Rate Converter	Multimedia Peripherals	The Asynchronous Sample Rate Converter (ASRC) converts the sampling rate of a signal associated to an input clock into a signal associated to a different output clock. The ASRC supports concurrent sample rate conversion of up to 10 channels of about -120dB THD+N. The sample rate conversion of each channel is associated to a pair of incoming and outgoing sampling rates. The ASRC supports up to three sampling rate pairs.	Full Feature
AUDMUX	Digital Audio Mux	Multimedia Peripherals	The AUDMUX is a programmable interconnect for voice, audio, and synchronous data routing between host serial interfaces (for example, SSI1, SSI2, and SSI3) and peripheral serial interfaces (audio and voice codecs). The AUDMUX has seven ports with identical functionality and programming models. A desired connectivity is achieved by configuring two or more AUDMUX ports.	Full Feature
BCH	Binary-BCH ECC Processor	System Control Peripherals	The BCH module provides up to 62-bit ECC encryption/decryption for NAND Flash controller (GPMI)	Full Feature
CAAM	Cryptographic accelerator and assurance module	Security	CAAM is a cryptographic accelerator and assurance module. CAAM implements several encryption and hashing functions, a run-time integrity checker, and a Pseudo Random Number Generator (PRNG). The pseudo random number generator is certified by Cryptographic Algorithm Validation Program (CAVP) of National Institute of Standards and Technology (NIST). Its DRBG validation number is 94 and its SHS validation number is 1455. CAAM also implements a Secure Memory mechanism. In i.MX 6SoloX processors, the security memory provided is 32 KB.	Full Feature
CCM GPC SRC	Clock Control Module, General Power Controller,	Clocks, Resets, and Power Control	These modules are responsible for clock and reset distribution in the system, and also for the system power management.	Full Feature

Table 3. SCM-i.MX 6SoloX modules list

Block Mnemonic	Block Name	Subsystem	Brief Description	Availability
	System Reset Controller			
CSI	Parallel CSI	Multimedia Peripherals	The CSI IP provides parallel CSI standard camera interface port. The CSI parallel data ports are up to 24 bits. It is designed to support 24-bit RGB888/YUV444, CCIR656 video interface, 8-bit YCbCr, YUV or RGB, and 8-bit/10-bit/26-bit Bayer data input.	Full Feature
CSU	Central Security Unit	Security	The Central Security Unit (CSU) is responsible for setting comprehensive security policy within the i.MX 6SoloX platform.	Full Feature
CTI	Cross Trigger Interfaces	Debug/Trace	Cross Trigger Interfaces allows cross-triggering based on inputs from masters attached to CTIs. The CTI module is internal to the Cortex-A9 Core Platform.	Full Feature
DAP	Debug Access Port	System Control Peripherals	The DAP provides real-time access for the debugger without halting the core to: System memory and peripheral registers All debug configuration registers The DAP also provides debugger access to JTAG scan chains. The DAP module is internal to the Cortex-A9 Core Platform.	Full Feature
DBGMON	Debug Monitor	Debug	DBGMON is a real-time debug monitor to record last AXI transaction before system reset.	Full Feature
eCSPI1 eCSPI2 eCSPI3 eCSPI4 eCSPI5	Configurable SPI	Connectivity Peripherals	Full-duplex enhanced Synchronous Serial Interface, with data rate up to 52 Mbit/s. It is configurable to support Master/Slave modes, four chip selects to support multiple peripherals.	Full Feature
EIM	NOR-Flash /PSRAM interface	Connectivity Peripherals	The EIM NOR-FLASH / PSRAM provides: Support 16-bit (in muxed IO mode only) PSRAM memories (sync and async operating modes), at slow frequency Support 16-bit (in muxed IO mode only) NOR-Flash memories, at slow frequency Multiple chip selects	Full Feature
ENET1 ENET2	Ethernet Controller	Connectivity Peripherals	The Ethernet Media Access Controller (MAC) is designed to support 10/100/1000 Mbps Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media. The module has dedicated hardware to support the IEEE 1588 standard. See the ENET chapter of the <i>i.MX 6SoloX Applications Processor Reference Manual</i> (document IMX6SXR M) for details.	Only RGMII1 available
EPIT1 EPIT2	Enhanced Periodic Interrupt Timer	Timer Peripherals	Each EPIT is a 32-bit “set and forget” timer that starts counting after the EPIT is enabled by software. It is capable of providing precise interrupts at regular intervals with minimal processor intervention. It has a 12-bit prescaler for division of input clock frequency to get the required time setting for the interrupts to occur, and counter value can be programmed on the fly.	Not available
ESAI	Enhanced Serial	Connectivity	The Enhanced Serial Audio Interface (ESAI)	Full Feature

Table 3. SCM-i.MX 6SoloX modules list

Block Mnemonic	Block Name	Subsystem	Brief Description	Availability
	Audio Interface	Peripherals	provides a full-duplex serial port for serial communication with a variety of serial devices, including industry-standard codecs, SPDIF transceivers, and other processors. The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator. All serial transfers are synchronized to a clock. Additional synchronization signals are used to delineate the word frames. The normal mode of operation is used to transfer data at a periodic rate, one word per period. The network mode is also intended for periodic transfers; however, it supports up to 32 words (time slots) per period. This mode can be used to build time division multiplexed (TDM) networks. In contrast, the on-demand mode is intended for non-periodic transfers of data and to transfer data serially at high speed when the data becomes available. The ESAI has 12 pins for data and clocking connection to external devices.	
FLEXCAN1 FLEXCAN2	Flexible Controller Area Network	Connectivity Peripherals	The CAN protocol was primarily, but not only, designed to be used as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the Electromagnetic interference (EMI) environment of a vehicle, cost-effectiveness and required bandwidth. The FlexCAN module is a full implementation of the CAN protocol specification, Version 2.0 B, which supports both standard and extended message frames.	Full Feature
Fuse Box	Electrical Fuse Array	Security	Electrical Fuse Array. Enables setup of boot modes, security levels, security keys, and many other system parameters. The fuses are accessible through OCOTP_CTRL interface.	Full Feature
GC400T	Graphics Engine	Multimedia Peripherals	The GC400T is a graphics engine with separate 2D and 3D pipelines to provide both 2D and 3D acceleration. It supports DirectFB and GAL APIs. It supports OpenGL ES1.1/2.0 and OpenVG 1.1 APIs.	Full Feature
GIC	Global Interrupt Controller	ARM/Control	The Global Interrupt Controller (GIC) collects interrupt requests from all i.MX 6SoloX sources and routes them to the ARM MPCore(s). Each interrupt can be configured as a normal or a secure interrupt. Software Force Registers and software Priority Masking are also supported. This IP is part of the ARM Core complex.	Full Feature
GIS	General Interrupt Service module	Camera, Display, & Graphics	GIS can be used to automate the flow of data from the camera to the display.	Full Feature
GPIO1 GPIO2 GPIO3 GPIO4 GPIO5 GPIO6 GPIO7	General Purpose I/O Modules	System Control Peripherals	Used for general purpose input/output to external ICs. Each GPIO module supports 32 bits of I/O.	Reduced GPIO's.

Table 3. SCM-i.MX 6SoloX modules list

Block Mnemonic	Block Name	Subsystem	Brief Description	Availability
GPMI	General Purpose Memory Interface	Connectivity Peripherals	The GPMI module supports up to 8x NAND devices and 60-bit ECC encryption/decryption for NAND Flash Controller (GPMI2). GPMI supports separate DMA channels for each NAND device.	Full Feature
GPT	General Purpose Timer	Timer Peripherals	Each GPT is a 32-bit “free-running” or “set and forget” mode timer with programmable prescaler and compare and capture register. A timer counter value can be captured using an external event and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in “set and forget” mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either with an external clock or an internal clock.	Not available.
I2C-1 I2C-2 I2C-3 I2C-4	I2C Interface	Connectivity Peripherals	I2C provide serial interface for external devices. Data rates of up to 400 kbps are supported.	Full Feature
IOMUXC	IOMUX Control	System Control Peripherals	This module enables flexible IO multiplexing. Each IO pad has default and several alternate functions. The alternate functions are software configurable.	Full Feature
KPP	Key Pad Port	Connectivity Peripherals	KPP Supports 8x8 external key pad matrix. KPP features are: <ul style="list-style-type: none"> • Open drain design • Glitch suppression circuit design • Multiple keys detection • Standby key press detection 	Reduced KPP pins.
LCDIF	LCD Interface	Multimedia Peripherals	The LCDIF provides display data for external LCD panels from simple text-only displays to WVGA, 16/18/24 bpp color TFT panels. The LCDIF supports all of these different interfaces by providing fully programmable functionality and sharing register space, FIFOs, and ALU resources at the same time. The LCDIF supports RGB (DOTCLK) modes as well as system mode including both VSYNC and WSYNC modes.	Full Feature
LVDS (LDB)	LVDS Display Bridge	Connectivity Peripherals	LVDS Display Bridge is used to connect an external LVDS display interface. LDB supports the following signals: <ul style="list-style-type: none"> • One clock pair • Four data pairs 	Full Feature
MLB	MediaLB	Connectivity/ Multimedia Peripherals	The MLB interface module provides a link to a MOST® data network, using the standardized MediaLB protocol (MOST25, MOST 50).	Full Feature
MMDC	Multi-Mode DDR Controller	Connectivity Peripherals	DDR Controller supports 32-bit LP-DDR2-800	PoP memory on Full Feature
MU	Messaging Unit	Interprocessor	The MU module supports interprocessor	Full Feature

Table 3. SCM-i.MX 6SoloX modules list

Block Mnemonic	Block Name	Subsystem	Brief Description	Availability
		Comm. & Synch.	communication between the Cortex-A9 and Cortex-M4 cores.	
OCOTP_CTRL	OTP Controller	Security	The On-Chip OTP controller (OCOTP_CTRL) provides an interface for reading, programming, and/or overriding identification and control information stored in on-chip fuse elements. The module supports electrically-programmable (eFUSE) polyfuses. The OCOTP_CTRL also provides a set of volatile software-accessible signals that can be used for software control of hardware elements, not requiring non-volatility. The OCOTP_CTRL provides the primary user-visible mechanism for interfacing with on-chip fuse elements. Among the uses for the fuses are unique chip identifiers, mask revision numbers, cryptographic keys, JTAG secure mode, boot characteristics, and various control signals, requiring permanent non-volatility.	Full Feature
OCRAM	On-Chip Memory Controller	Data Path	The On-Chip Memory controller (OCRAM) module is designed as an interface between system's AXI bus and internal (on-chip) SRAM memory module.	Full Feature
OCRAM 128 KB	Internal RAM	Internal Memory	Internal RAM, which is accessed through OCRAM memory controller.	Full Feature
OCRAM_S 16KB	Secure/nonsecure RAM	Secured Internal Memory	Secure/nonsecure internal RAM, interfaced through the CAAM. OCRAM_S can be used by software for state retention of the CPU and other hardware blocks.	Full Feature
OSC32KHz	OSC32KHz	Clocking	Generates 32.768 KHz clock from external crystal.	Full Feature
PCIe	PCI Express 2.0	Connectivity Peripherals	The PCIe IP provides PCI Express Gen 2.0 functionality.	Not available
PMU	Power-Mgmt.	Data Path	Integrated power management unit. Used to provide power to various SoC domains.	Full Feature
PWM-1 PWM-2 PWM-3 PWM-4 PWM-5 PWM-6 PWM-7 PWM-8	Pulse Width Modulation	Connectivity Peripherals	The pulse-width modulator (PWM) has a 16-bit counter and is optimized to generate sound from stored sample audio images and it can also generate tones. It uses 16-bit resolution and a 4x16 data FIFO to generate sound.	Full Feature
PXP	PiXel Processing Pipeline	Display Peripherals	A high-performance pixel processor capable of 1 pixel/clock performance for combined operations, such as color-space conversion, alpha blending, gamma-mapping, and rotation. The PXP is enhanced with features specifically for gray scale applications.	Full Feature
QSPI	Quad Serial Peripheral Interface	Connectivity Peripherals	The Quad Serial Peripheral Interface (QuadSPI) block acts as an interface to one or two external serial flash devices, each with up to four bidirectional data lines.	Full Feature
ROM 96KB	Boot ROM	Internal Memory	Supports secure and regular boot modes	Full Feature
RDC	Resource Domain Controller	Multicore Isolation/Sharing	RDC module supports domain-based access control to shared resources.	Full Feature
SEMA4	Semaphore	Multicore/Isolation/	Supports hardware-enforced semaphores.	Full Feature

Table 3. SCM-i.MX 6SoloX modules list

Block Mnemonic	Block Name	Subsystem	Brief Description	Availability
		Sharing		
SEMA42	Semaphore	Multicore/Isolation/ Sharing	SEMA42 is similar to SEMA4 with the following key differences: <ul style="list-style-type: none"> SEMA42 increases the number of access domains from 2 to 15 SEMA42 does not have interrupt to indicate semaphore release RDC programming model supports the option to require hardware semaphore for peripherals shared between domains. Signaling between the SEMA42 and RDC binds peripherals to semaphore gates within SEMA42. 	Full Feature
SAI1 SAI2			The SAI module provides a synchronous audio interface (SAI) that supports full duplex serial interfaces with frame synchronization, such as I2S, AC97, TDM, and codec/DSP interfaces.	Full Feature
SDMA	Smart Direct Memory Access	System Control Peripherals	The SDMA is multi-channel flexible DMA engine. It helps in maximizing system performance by off-loading the various cores in dynamic data routing. It has the following features: <ul style="list-style-type: none"> Powered by a 16-bit Instruction-Set micro-RISC engine Multi-channel DMA supporting up to 32 time-division multiplexed DMA channels. 48 events with total flexibility to trigger any combination of channels. Memory accesses including linear, FIFO, and 2D addressing. Shared peripherals between ARM and SDMA Very fast Context-Switching with 2-level priority based preemptive multi-tasking. DMA units with auto-flush and prefetch capability Flexible address management for DMA transfers (increment, decrement, and no address changes on source and destination address). DMA ports can handle unit-directional and bi-directional flows (copy mode). Up to 8-word buffer for configurable burst transfers for EMIv2.5. Support of byte-swapping and CRC calculations. Library of Scripts and API is available 	Full Feature
SJC	System JTAG Controller	System Control Peripherals	The SJC provides JTAG interface, which complies with JTAG TAP standards, to internal logic. The i.MX 6SoloX processors use JTAG port for production, testing, and system debugging. In addition, the SJC provides BSR (Boundary Scan Register) standard support, which complies with IEEE1149.1 and IEEE1149.6 standards. The JTAG port must be accessible during platform initial laboratory bring-up, for manufacturing tests and	Full Feature

Table 3. SCM-i.MX 6SoloX modules list

Block Mnemonic	Block Name	Subsystem	Brief Description	Availability
			troubleshooting, as well as for software debugging by authorized entities. The i.MX 6SoloX SJC incorporates three security modes for protecting against unauthorized accesses. Modes are selected through eFUSE configuration.	
SNVS	Secure Non-Volatile Storage	Security	Secure Non-Volatile Storage, including Secure Real Time Clock, Security State Machine, Master Key Control, and Violation/Tamper Detection and reporting.	Full Feature
SPDIF	Sony Philips Digital Interconnect Format	Multimedia Peripherals	A standard audio file transfer format, developed jointly by the Sony and Phillips corporations. Has transmitter and receiver functionality.	Full Feature
SSI1 SSI2 SSI3	I2S/SSI/AC97 Interface	Connectivity Peripherals	The SSI is a full-duplex synchronous interface, which is used on the AP to provide connectivity with off-chip audio peripherals. The SSI supports a wide variety of protocols (SSI normal, SSI network, I2S, and AC-97), bit depths (up to 24 bits per word), and clock / frame sync options. The SSI has two pairs of 8x24 FIFOs and hardware support for an external DMA controller in order to minimize its impact on system performance. The second pair of FIFOs provides hardware interleaving of a second audio stream that reduces CPU overhead in use cases where two time slots are being used simultaneously.	Full Feature
TEMPMON	Temperature Monitor	System Control Peripherals	The Temperature sensor IP is used for detecting die temperature. The temperature read out does not reflect case or ambient temperature. It reflects the temperature in proximity of the sensor location on the die. Temperature distribution may not be uniformly distributed, therefore the read out value may not be the reflection of the temperature value of the entire die.	Full Feature
TVDECODE	TV Decoder (via VADC)	Connectivity Peripherals	The TVDEC decodes NTSC/PAL input from VADC analog front end and provides YUV888 data CSI.	Not available
TZASC	Trust-Zone Address Space Controller	Security	The TZASC (TZC-380 by ARM) provides security address region control functions required for intended application. It is used on the path to the DRAM controller.	Full Feature
UART1 UART2 UART3 UART4 UART5 UART6	UART Interface	Connectivity Peripherals	Each of the UARTv2 modules support the following serial data transmit/receive protocols and configurations: <ul style="list-style-type: none"> 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd or none) Programmable baud rates up to 5 Mbps. 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud Option to operate as 8-pins full UART, DCE, or DTE UART1/6 support 8-pin, UART2/3/4/5 support 4-pin 	Reduced functionality for UART1 and UART2.
uSDHC1	SD/MMC and	Connectivity	i.MX 6SoloX specific SoC characteristics: All	uSDHC1 is not

Table 3. SCM-i.MX 6SoloX modules list

Block Mnemonic	Block Name	Subsystem	Brief Description	Availability
uSDHC2 uSDHC3 uSDHC4	SDXC Enhanced Multi-Media Card / Secure Digital Host Controller	Peripherals	<p>four MMC/SD/SDIO controller IPs are identical and are based on the uSDHC IP. They are:</p> <ul style="list-style-type: none"> Fully compliant with MMC command/response sets and Physical Layer as defined in the Multimedia Card System Specification, v4.5/4.2/4.3/4.4/4.41/ including high-capacity (size > 2 GB) cards HC MMC. Fully compliant with SD command/response sets and Physical Layer as defined in the SD Memory Card Specifications, v3.0 including high-capacity SDHC cards up to 32 GB. Fully compliant with SDIO command/response sets and interrupt/read-wait mode as defined in the SDIO Card Specification, Part E1, v3.0 All four ports support: 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR104 mode (104 MB/s max) 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards up to 52 MHz in both SDR and DDR modes (104 MB/s max) However, the SoC level integration and I/O muxing logic restrict the functionality to the following: Instances #1 and #2 are primarily intended to serve as interfaces to on-board peripherals. These ports are equipped with “Card detection” and “Write Protection” pads and do not support hardware reset. Instance #3 is intended to serve as the primary external card slot. Instance #4 is intended to be the primary boot device via eMMC or SD, or to be a secondary external card slot. Instances #3 and #4 do not have “Card detection” and “Write Protection” pads and do support hardware reset. All ports can work with 1.8 V and 3.3 V cards. There are two completely independent I/O power domains for Ports #1 and #2 in four bit configuration (SD interface). Port #3 is placed in his own independent power domain and port #4 shares power domain with some other interfaces. 	available.
USB	Universal Serial Bus 2.0	Connectivity Peripherals	<p>USB contains:</p> <ul style="list-style-type: none"> Two high-speed OTG 2.0 modules with integrated HS USB PHYs One high-speed Host module connected to HSIC USB port 	Full Feature
VADC	Video ADC	Connectivity Peripherals	<p>Video ADC digitizes an analog video signal, such as one from an inexpensive analog camera. The video signal can be selected from one of four inputs, VIN0-VIN3, through register control.</p>	Not available

Table 3. SCM-i.MX 6SoloX modules list

Block Mnemonic	Block Name	Subsystem	Brief Description	Availability
WDOG1 WDOG3	Watch Dog	Timer Peripherals	The Watch Dog Timer supports two comparison points during each counting period. Each of the comparison points is configurable to evoke an interrupt to the ARM core, and a second point evokes an external event on the WDOG line.	Reduced WDOG pins.
WDOG2 (TZ)	Watch Dog (TrustZone)	Timer Peripherals	The TrustZone Watchdog (TZ WDOG) timer module protects against TrustZone starvation by providing a method of escaping normal mode and forcing a switch to the TZ mode. TZ starvation is a situation where the normal OS prevents switching to the TZ mode. Such situation is undesirable as it can compromise the system's security. Once the TZ WDOG module is activated, it must be serviced by TZ software on a periodic basis. If servicing does not take place, the timer times out. Upon a time-out, the TZ WDOG asserts a TZ mapped interrupt that forces switching to the TZ mode. If it is still not served, the TZ WDOG asserts a security violation signal to the CSU. The TZ WDOG module cannot be programmed or deactivated by a normal mode software.	Reduced WDOG2 pins.
XTALOSC	Crystal Oscillator Interface	Clocks, Resets, and Power Control	The XTALOSC module connects to an external crystal to provide system clocks.	Full Feature

3.1. Special signal considerations

The figure below shows critical internal module connections.

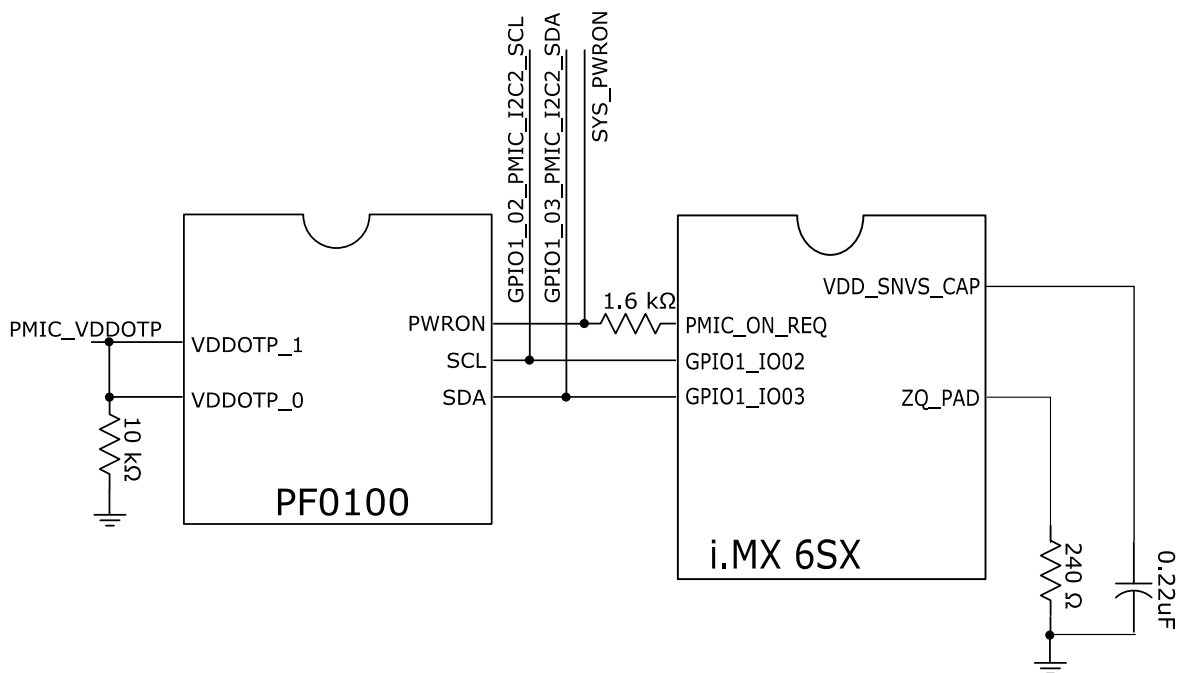


Figure 3. SCM-i.MX6SX critical internal connections

3.2. PMIC electrical deratings

The MMPF0100 PMIC has been integrated into the SCM-i.MX 6SX. However due to the reduced ball count of the 265 pin package the PMIC has been derated in both features and performance for that package. The table below details the limitations of this package.

Table 4. SCM-i.MX 6SoloX PMIC package options

Supply Name	Description	265 BGA Notes
SW1AB	0.3 – 1.875V, 2.5A	Limited to 2A
SW1C	0.3 – 1.875V, 2.0A	N/A
SW2	0.4 – 3.3V, 2.0A	Limited to 1A
SW3AB	0.4 – 3.3V, 2.5A	Limited to 1A
SW4	0.4 – 3.3V, 1.0A	N/A
SWBST	5.0 – 5.15V, 0.6A; intended for USB OTG	No restrictions
VGEN1	0.80 – 1.55V, 100mA	N/A
VGEN2	0.80 – 1.55V, 250mA	N/A
VGEN3	1.8 – 3.3V, 100mA	No restrictions
VGEN4	Dedicated 1.8V Supply – not programmable, 250mA limit.	Intended for LPDDR2, NVCC_LOW & NVCC_SD4
VGEN5	1.8 – 3.3V, 100mA	N/A
VGEN6	1.8 – 3.3V, 200mA	No restrictions

4. Electrical characteristics

4.1. Chip-level conditions

4.1.1. Absolute max ratings

Table 5. Absolute max ratings

Parameter Description	Symbol	Min	Max	Unit
PMIC System Supply Voltage Range	PMIC_VIN	-0.3	4.8	V
Temperature range (storage)	T_storage	-40	150	C
SW1AB output from PMIC	SW1LX	0	2000	mA
SW2 output from PMIC	SW2LX	0	1000	mA
SW3AB output from PMIC	SW3LX	0	1000	mA
Boost Converter output from PMIC	SWBSTLX	0	500	mA
Programmable LDO from PMIC; range: 1.8V – 3.3V	VGEN3	0	100	mA
Fixed 1.8V LDO from PMIC	SYS_VGEN4_1V8	0	250	mA
Programmable LDO from PMIC; range: 1.8V – 3.3V	VGEN6	0	200	mA

4.1.2. Thermal resistance

Table 6. FO-WLP thermal resistance data

Parameter Description	Test Condition	Symbol	Value	Unit
Junction to Ambient ^{1,6}	Single-layer board (1s); natural convection ²	$R_{\theta JA}$	36.9	°C/W
	Four-layer board (2s2p); natural convection ²	$R_{\theta JA}$	20.5	°C/W
Junction to Ambient ^{1,6}	Single-layer board (1s); air flow 200ft/min ³	$R_{\theta JMA}$	29.6	°C/W
	Four-layer board (2s2p); air flow 200ft/min ³	$R_{\theta JMA}$	17.2	°C/W
Junction to Board ^{1,4,6}	—	$R_{\theta JB}$	12.6	°C/W
Junction to top characterization parameter ^{1,5,6}	—	Ψ_{JT}	11.2	°C/W

- Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
- Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
- Per JEDEC JESD51-6 with the board horizontal.
- Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
- Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.
- Values reported are modeled and based upon a summation of power dissipation of multiple die within the package. Junction temperatures will vary between die according to power ratios and use case.

4.1.3. Operating ranges

Table 7. Operating ranges

Parameter Description	Symbol	Min	Max	Unit
PMIC System Supply Voltage Range	PMIC_VIN	3.6	4.5	V
Main CPU supply when internal LDO enabled	VDD_ARM_SOC_IN ¹	1.275	1.5	V
Main CPU supply during Standby/DSM Mode	VDD_ARM_SOC_IN ¹	1.05	1.3	V
Backup battery supply range	VDD_SNVS_IN	2.4	3.6	V
Supply for the following: VDD_HIGH_IN, NVCC_CSI, NVCC_GPIO, NVCC_HIGH, NVCC_JTAG, NVCC_KEY, NVCC_LCD1, NVCC_NAND	SYS_SW2_3V15	2.8	3.6	V
Supply for the LPDDR2 IO system	DDR_1V2_SW3FB	1.14	1.3	V
Supply for NVCC_ENET, NVCC_RGMII1, NVCC_RGMII2	NVCC_RGMII	1.63	3.6	V
Supply for NVCC_QSPI	NVCC_QSPI	1.63	3.6	V
Supply for NVCC_SD2	NVCC_SD2	1.63	3.6	V
Supply for NVCC_SD4	NVCC_SD4	1.63	3.6	V
A/D converter supply	VDDA_ADC_3P3	3.0	3.6	V
USB Supply Voltages	USB_OTG1/2_VBUS	4.4	5.25	V
Junction Temperature (industrial)	T _j	-40	105	C

- VDD_SOC_IN and VDD_ARM_IN are shorted together inside the module.

Table 8. Internal supply connections

Voltage Source	Load	Comment
VDD_HIGH_CAP	NVCC_LVDS	2.5V LDO output. 4.7uF bulk capacitor required.
	NVCC_DRAM_2P5	
SYS_SW2_3V15	VDD_HIGH_IN	Recommended design is SW2 output supplies SYS_SW2_3V15.
	NVCC_CSI	
	NVCC_GPIO	
	NVCC_HIGH	
	NVCC_JTAG	
	NVCC_KEY	
	NVCC_LCD1	
	NVCC_NAND	

5. Power supplies requirements and restrictions

5.1. Power-up sequences

Must follow the *i.MX 6SoloX industrial datasheet* (document [IMX6SXIEC](#)) recommendations for power up. The internal PMIC simplifies power sequence design.

5.2. Power-down sequences

Must follow the *i.MX 6SoloX industrial datasheet* (document [IMX6SXIEC](#)) recommendations for power down.

5.3. Power supplies usage

Must follow the *i.MX 6SoloX industrial datasheet* (document [IMX6SXIEC](#)) recommendations for power supply usage.

5.4. Boot configuration

5.4.1. OTP fuse map of PMIC

Table 9. OTP fuse map

Registers	Default Configuration	Preprogrammed OTP Configuration	Preprogrammed code (hex)	Intended Use
SW1AB_VOLT	1.375V	1.375V	2B	VDDSOC & VDDARM
SW1AB_SEQ	1	2	02	
SW1AB CONFIG	Single Phase, 2.0 MHz	Single Phase, 2.0 MHz	05	
SW2_VOLT	3.0V	3.15V	6F	VDDHIGH_IN / NVCC_xxx
SW2_SEQ	2	1	01	
SW2 CONFIG	Single Phase, 2.0 MHz	Single Phase, 2.0 MHz	01	

Table 9. OTP fuse map

Registers	Default Configuration	Preprogrammed OTP Configuration	Preprogrammed code (hex)	Intended Use
SW3A_VOLT	1.5V	1.2V	20	DDR 1.2V
SW3A_SEQ	3	4	04	
SW3A CONFIG	Single Phase, 2.0 MHz	Single Phase, 2.0 MHz	05	
SW3B_VOLT	1.5V	1.2V	20	DDR 1.2V
SW3B_SEQ	3	4	04	
SW3B CONFIG	Single Phase, 2.0 MHz	Single Phase, 2.0 MHz	01	
SWBST_VOLT	-	-	00	USB or 5V application.
SWBST_SEQ	-	4	04	
VSNVS_VOLT	3.0V	3.0V	06	VDD_SNVS_IN
VREFDDR_SEQ	3	4	04	
VGEN3_VOLT	-	-	00	Customer
VGEN3_SEQ	-	-	00	
VGEN4_VOLT	1.8V	1.8V	00	LPDDR2 / NVCC_LOW / NVCC_SD4 + Customer
VGEN4_SEQ	3	3	00	
VGEN6_VOLT	2.8V	-	00	Customer
VGEN6_SEQ	3	-	00	
PU CONFIG1, SEQ_CLK_SPEED	1.0ms	1.0ms	01	
PU CONFIG2, SWDVS_CLK	6.25 mV/us	12.5mV/us	00	
PU CONFIG3, PWRON	Level sensitive	Level sensitive	00	
PG EN	RESETBMCU in Default Mode	00		

NOTE

See *Features of Voltage Regulators in the MMPF0100* (document [AN4714](#)) and *MMPF0100 OTP Programming Instructions* (document [AN4536](#)) for further usage instructions.

The OTP registers for regulators which default to OFF are free to be programmed according to customer needs.

The OTP Lock bit is not programmed from factory.

NXP not responsible for device issues caused by customer fuse programming.

6. Boot mode configuration

6.1. Boot mode configuration pins

See *i.MX 6SoloX Applications Processors for Industrial Products - Data Sheet* (document [IMX6SXIEC](#)).

6.2. Boot devices interfaces allocation

See *i.MX 6SoloX Applications Processors for Industrial Products - Data Sheet* (document [IMX6SXIEC](#)).

7. Package information

7.1. Signal list

Table 10. Signal list

Ball Name	Ball	Comments
ADC1_IN0	AB22	
ADC1_IN1	AC21	
ADC1_IN3	Y20	
BOOT_MODE0	L17	
BOOT_MODE1	K16	
CCM_CLK1_N	AA1	
CCM_CLK1_P	AB2	
CCM_CLK2	AB6	
CSI_DATA00	U1	
CSI_DATA01	T4	
CSI_DATA02	W5	
CSI_DATA03	R5	
CSI_DATA04	L5	
CSI_DATA05	P2	
CSI_DATA06	R3	
CSI_DATA07	R1	
CSI_HSYNC	T2	
CSI_MCLK	H4	
CSI_PIXCLK	U5	
CSI_VSYNC	U3	
ENET1_TX_CLK	M16	
ENET2_RX_CLK	K18	
GND	A1, A15, A23, AC1, AC23, D4, E15, E21, E5, F18, G17, H8, J9, K10, K20, C15, M6, N7, P10, P16, P4, R11, R13, R15, R17, R19, G15, F8, G13, G9, H14, J13, K12, K14, L13, T16, T20, W11, W19, W3, W7, Y6,	Ground
GPIO1_02_PMIC_I2C2_SCL	N17	
GPIO1_03_PMIC_I2C2_SDA	N19	

Table 10. Signal list

Ball Name	Ball	Comments
GPIO1_04	N9	
GPIO1_05	L11	
GPIO1_06	B18	
GPIO1_07	Y14	
GPIO1_09	G19	
GPIO1_10	C17	
GPIO1_11	AB14	
GPIO1_12_PMIC_INT_B	B16	
GPIO1_13	M10	
I2C3_SCL	P6	
I2C3_SDA	P8	
JTAG_MOD	U11	
JTAG_TCK	V10	
JTAG_TDI	U9	
JTAG_TDO	T10	
JTAG_TMS	R7	
JTAG_TRST_B	T12	
KEY_COL0	V20	
KEY_COL1	P18	
KEY_ROW0	B14	
KEY_ROW1	L9	
LCD1_CLK	J3	
LCD1_DATA00	C1	
LCD1_DATA01	D2	
LCD1_DATA02	E3	
LCD1_DATA03	F4	
LCD1_DATA04	N1	
LCD1_DATA05	E1	
LCD1_DATA06	F2	
LCD1_DATA07	G3	
LCD1_DATA08	A3	
LCD1_DATA09	G5	
LCD1_DATA10	C7	
LCD1_DATA11	C5	
LCD1_DATA12	G1	
LCD1_DATA13	H2	
LCD1_DATA14	N5	
LCD1_DATA15	K4	
LCD1_DATA16	N3	
LCD1_DATA17	J1	
LCD1_DATA18	K2	
LCD1_DATA19	L3	
LCD1_DATA20	M4	
LCD1_DATA21	L1	
LCD1_DATA22	M2	
LCD1_DATA23	A5	
LCD1_ENABLE	B4	
LCD1_HSYNC	C3	
LCD1_RESET	B6	
LCD1_VSYNC	B2	
LVDS0_CLK_N	AA3	
LVDS0_CLK_P	AC3	
LVDS0_TX0_N	AC7	

Table 10. Signal list

Ball Name	Ball	Comments
LVDS0_TX0_P	AA7	
LVDS0_TX1_N	AC5	
LVDS0_TX1_P	AA5	
LVDS0_TX2_N	AB4	
LVDS0_TX2_P	Y4	
LVDS0_TX3_N	Y8	
LVDS0_TX3_P	AB8	
NAND_ALE	AC11	
NAND_CE0_B	AB12	
NAND_CE1_B	Y12	
NAND_CLE	V12	
NAND_DATA00	V14	
NAND_DATA01	W13	
NAND_DATA02	V16	
NAND_DATA03	W15	
NAND_DATA04	AC15	
NAND_DATA05	U15	
NAND_DATA06	W17	
NAND_DATA07	AA13	
NAND_RE_B	U13	
NAND_READY_B	AA11	
NAND_WE_B	T14	
NAND_WP_B	AC13	
ONOFF	AA21	
PMIC_ICTEST	F16	Reserved pin. Connect to GND in application.
PMIC_LICELL	E19	Coin cell supply input/output
PMIC_SDWN_B	J17	Open drain signal to indicate an imminent PMIC shutdown.
PMIC_STBY_REQ	D16	Standby input signal from processor
PMIC_VCOREREF	E17	Main band gap reference
PMIC_VDDOTP	B22	Supply to program OTP fuses
PMIC_VIN	D6, D8, D10, F10, E7, E9, E11	Main system supply
DDR_1V2_SW3FB	A17, R21	LPDDR2 IO supply
NVCC_PLL	V8	Bulk Capacitor supply pin for PLL
NVCC_QSPI	K6	Supply input for the QSPI interface.
NVCC_RGMII	U7	Supply input for the RGMII & ENET interfaces.
NVCC_SD2	L7	Supply input for the SD2 interface
NVCC_SD4	M8	Supply input for the SD4 interface
PCIE_VP_CAP	V18	Supply input for the PCIe PHY
SYS_SW2_3V15	J5, H6	Supply input for the VDD_HIGH_IN, NVCC_CSI, NVCC_GPIO, NVCC_HIGH, NVCC_JTAG, NVCC_KEY, NVCC_LCD1 & NVCC_NAND interfaces.
SYS_VGEN4_1V8	K8	Supply input for the NVCC_LOW (SD3) interface and the LPDDR2 core.
USB_OTG1_VBUS	T6	VBUS input for USB_OTG1
USB_OTG2_VBUS	V6	VBUS input for USB_OTG1
VDD_ARM_CAP	N11, P12	Supply voltage output from internal LDO_ARM. Requires external capacitor(s).
VDD_ARM_SOC_IN	M14, N13, N15, P14	Supply voltage input for internal LDO_ARM, LDO_SOC and LDO_PCIE.
VDD_HIGH_CAP	R9	Supply voltage output from internal LDO_2P5. Requires external capacitor(s).

Table 10. Signal list

Ball Name	Ball	Comments
VDD_SNVS_IN	J15	Supply voltage input to the SNVS voltage domain
VDD_SOC_CAP	T18, U17, U19	Supply voltage output from internal LDO_SOC. Requires external capacitor(s).
VDD_USB_CAP	W9	Supply voltage output from internal LDO_USB. Requires external capacitor(s).
VDDA_ADC_3P3	AA23	Supply voltage input to the ADC. This supply must be provided even if the ADC is not used.
VGEN3	Y22	VGEN3 regulator output. Bypass with a 2.2 μ F ceramic capacitor.
VGEN6	J7	VGEN6 regulator output. Bypass with a 2.2 μ F ceramic capacitor.
VSNVS_3V0	H16	LDO or coin cell output to processor. Connect to VDD_SNVS_IN.
QSPI1A_DATA0	W23	
QSPI1A_DATA1	W21	
QSPI1A_DATA2	P22	
QSPI1A_DATA3	R23	
QSPI1A_DQS	U21	
QSPI1A_SCLK	V22	
QSPI1A_SS0_B	T22	
QSPI1A_SS1_B	U23	
QSPI1B_DATA0	N23	
QSPI1B_DATA1	M20	
QSPI1B_DATA2	M22	
QSPI1B_DATA3	P20	
QSPI1B_DQS	L19	
QSPI1B_SCLK	L23	
QSPI1B_SS0_B	L21	
QSPI1B_SS1_B	N21	
RGMI1_RD0	E23	
RGMI1_RD1	F22	
RGMI1_RD2	F20	
RGMI1_RD3	G23	
RGMI1_RX_CTL	H22	
RGMI1_RXC	C23	
RGMI1_TD0	K22	
RGMI1_TD1	J21	
RGMI1_TD2	J23	
RGMI1_TD3	H20	
RGMI1_TX_CTL	G21	
RGMI1_TXC	D22	
RTC_XTALI	AB10	
RTC_XTALO	Y10	
SD2_CLK	A21	
SD2_CMD	B20	
SD2_DATA0	C21	
SD2_DATA1	A19	
SD2_DATA2	C19	
SD2_DATA3	D20	
SD3_CLK	AB20	
SD3_CMD	AC17	
SD3_DATA0	Y18	

Table 10. Signal list

Ball Name	Ball	Comments
SD3_DATA1	AA15	
SD3_DATA2	AC19	
SD3_DATA3	AA19	
SD3_DATA4	AB18	
SD3_DATA5	AA17	
SD3_DATA6	Y16	
SD3_DATA7	AB16	
SD4_CLK	A7	
SD4_CMD	B8	Internal 10kohm pullup to NVCC_SD4
SD4_DATA0	C9	
SD4_DATA1	B10	
SD4_DATA2	A9	
SD4_DATA3	C11	
SD4_DATA4	B12	
SD4_DATA5	A11	
SD4_DATA6	C13	
SD4_DATA7	D14	
SD4_RESET_B	A13	
SNVS_TAMPER	J19	
SW1FB	L15	Output voltage feedback for SW1A/B. Route this trace separately from the high current path and terminate at the output capacitance.
SW1LX	G11, H10, H12, J11	Regulator 1 switch node connection
SW2LX	F6, G7	Regulator 2 switch node connection
SW3LX	E13, F14	Regulator 3 switch node connection
SWBSTFB ¹	D18	Boost regulator feedback. Connect this pin to the output rail close to the load. Keep this trace away from other noisy traces and planes.
SWBSTIN ¹	F12	Input to SWBST regulator. Bypass with at least a 2.2 μ F ceramic capacitor and a 0.1 μ F decoupling capacitor as close to the pin as possible.
SWBSTLX ¹	D12	SWBST switch node connection
SYS_POR_B	M18	
SYS_PWRON	H18	
TEST_MODE	M12	
USB_OTG1_CHD_B	T8	
USB_OTG1_DN	V2	
USB_OTG1_DP	V4	
USB_OTG2_DN	W1	
USB_OTG2_DP	Y2	
XTALI	AC9	
XTALO	AA9	

1. If switcher is not needed then SWBSTLX and SWBSTFB should be unconnected and SWBSTIN should be connected to main system power (same as PMIC_VIN) and bypassed with a 0.1 μ F capacitor.

7.2. Ball map

Table 11. SCM-i.MX 6SoloX ball map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	
A	GND		LCD1_DATA08		LCD1_DATA23		SD4_CLK		SD4_DATA2		SD4_DATA5		SD4_RESET_B		GND		DDR_1V2_SW3FB		SD2_DATA1		SD2_CLK		GND	
B		LCD1_VSYNC		LCD1_ENABLE		LCD1_RESET		SD4_CMD		SD4_DATA1		SD4_DATA4		KEY_ROW0		GPIO1_12_P MIC_INT_B		GPIO1_06		SD2_CMD		PMIC_VDDOT P		
C	LCD1_DATA00		LCD1_HSYNC		LCD1_DATA11		LCD1_DATA10		SD4_DATA0		SD4_DATA3		SD4_DATA6		GND		GPIO1_10		SD2_DATA2		SD2_DATA0		RGMI11_RXC	
D		LCD1_DATA01		GND		PMIC_VIN		PMIC_VIN		PMIC_VIN		SWBSTLX		SD4_DATA7		PMIC_STBY_R EQ		SWBSTFB		SD2_DATA3		RGMI11_TXC		
E	LCD1_DATA05		LCD1_DATA02		GND		PMIC_VIN		PMIC_VIN		PMIC_VIN		SW3LX		GND		PMIC_VCORE REF		PMIC_LICELL		GND		RGMI11_RD0	
F		LCD1_DATA06		LCD1_DATA03		SW2LX		GND		PMIC_VIN		SWBSTIN		SW3LX		PMIC_ICTEST		GND		RGMI11_RD2		RGMI11_RD1		
G	LCD1_DATA12		LCD1_DATA07		LCD1_DATA09		SW2LX		GND		SW1LX		GND		GND		GND		GPIO1_09		RGMI11_TX_C TL		RGMI11_RD3	
H		LCD1_DATA13		CSI_MCLK		SYS_SW2_3V1 5		GND		SW1LX		SW1LX		GND		VSNVS_3V0		SYS_PWRON		RGMI11_TD3		RGMI11_RX_C TL		
J	LCD1_DATA17		LCD1_CLK		SYS_SW2_3V1 5		VGEN6		GND		SW1LX		GND		VDD_SNV5_IN		PMIC_SDWV B		SNV5_TAMPE R		RGMI11_TD1		RGMI11_TD2	
K		LCD1_DATA18		LCD1_DATA15		NVCC_QSPI		SYS_VGEN4_1 V8		GND		GND		GND		BOOT_MODE 1		ENET2_RX_C K		GND		RGMI11_TD0		
L	LCD1_DATA21		LCD1_DATA19		CSI_DATA04		NVCC_SD2		KEY_ROW1		GPIO1_05		GND		SW1FB		BOOT_MODE 0		QSPI1B_DOS		QSPI1B_S50 B		QSPI1B_SCLK	
M		LCD1_DATA22		LCD1_DATA20		GND		NVCC_SD4		GPIO1_13		TEST_MODE		VDD_ARM_S OC_IN		ENET1_TX_C K		SYS_POR_B		QSPI1B_DATA 1		QSPI1B_DATA 2		
N	LCD1_DATA04		LCD1_DATA16		LCD1_DATA14		GND		GPIO1_04		VDD_ARM_C AP		VDD_ARM_S OC_IN		VDD_ARM_S OC_IN		GPIO1_02_P MIC_I2C2_SCL		GPIO1_03_P MIC_I2C2_SD		QSPI1B_S51 B		QSPI1B_DATA 0	
P		CSI_DATA05		GND		I2C3_SCL		I2C3_SDA		GND		VDD_ARM_C AP		VDD_ARM_S OC_IN		GND		KEY_COL1		QSPI1B_DATA 3		QSPI1A_DATA 2		
R	CSI_DATA07		CSI_DATA06		CSI_DATA03		JTAG_TMS		VDD_HIGH_C AP		GND		GND		GND		GND		GND		DDR_1V2_SW3FB		QSPI1A_DATA 3	

Package information

AC	AB	AA	Y	W	V	U	T
GND		CCM_CLK1_N	USB_OTG2_D_P	USB_OTG2_D_N	USB_OTG1_D_N	CSI_DATA00	CSI_HSYNC
LVDS0_CLK_P	CCM_CLK1_P			GND		CSI_VSYNC	
	LVDS0_TX2_N	LVDS0_CLK_N	LVDS0_TX2_P		USB_OTG1_D_P		CSI_DATA01
LVDS0_TX1_N		LVDS0_TX1_P		CSI_DATA02		CSI_PIXCLK	
	CCM_CLK2		GND		USB_OTG2_VBUS		USB_OTG1_VBUS
LVDS0_TX0_N		LVDS0_TX0_P		GND		NVCC_RGMII	
	LVDS0_TX3_P		LVDS0_TX3_N		NVCC_PIL		USB_OTG1_CHD_B
XTALI		XTALO		VDD_USB_CAP		JTAG_TDI	
	RTC_XTALI		RTC_XTALO		JTAG_TCK		JTAG_TDO
NAND_ALE		NAND_READY_B		GND		JTAG_MOD	
	NAND_CEO_B		NAND_CE1_B		NAND_CLE		JTAG_TRST_B
NAND_WP_B		NAND_DATA0_7		NAND_DATA0_1		NAND_RE_B	
	GPIO1_11		GPIO1_07		NAND_DATA0_0		NAND_WE_B
NAND_DATA0_4		SD3_DATA1		NAND_DATA0_3		NAND_DATA0_5	
	SD3_DATA7		SD3_DATA6		NAND_DATA0_2		GND
SD3_CMD		SD3_DATA5		NAND_DATA0_6		VDD_SOC_CAP	
	SD3_DATA4		SD3_DATA0		PCIE_VP_CAP		VDD_SOC_CAP
SD3_DATA2		SD3_DATA3		GND		VDD_SOC_CAP	
	SD3_CLK		ADC1_IN3		KEY_COL0		GND
ADC1_IN1		ONOFF		QSPI1A_DATA_1		QSPI1A_DQS	
	ADC1_IN0		VGEN3		QSPI1A_SCLK		QSPI1A_SSO_B
GND		VDDA_ADC_3_P3		QSPI1A_DATA_0		QSPI1A_SS1_B	

7.3. Package drawings

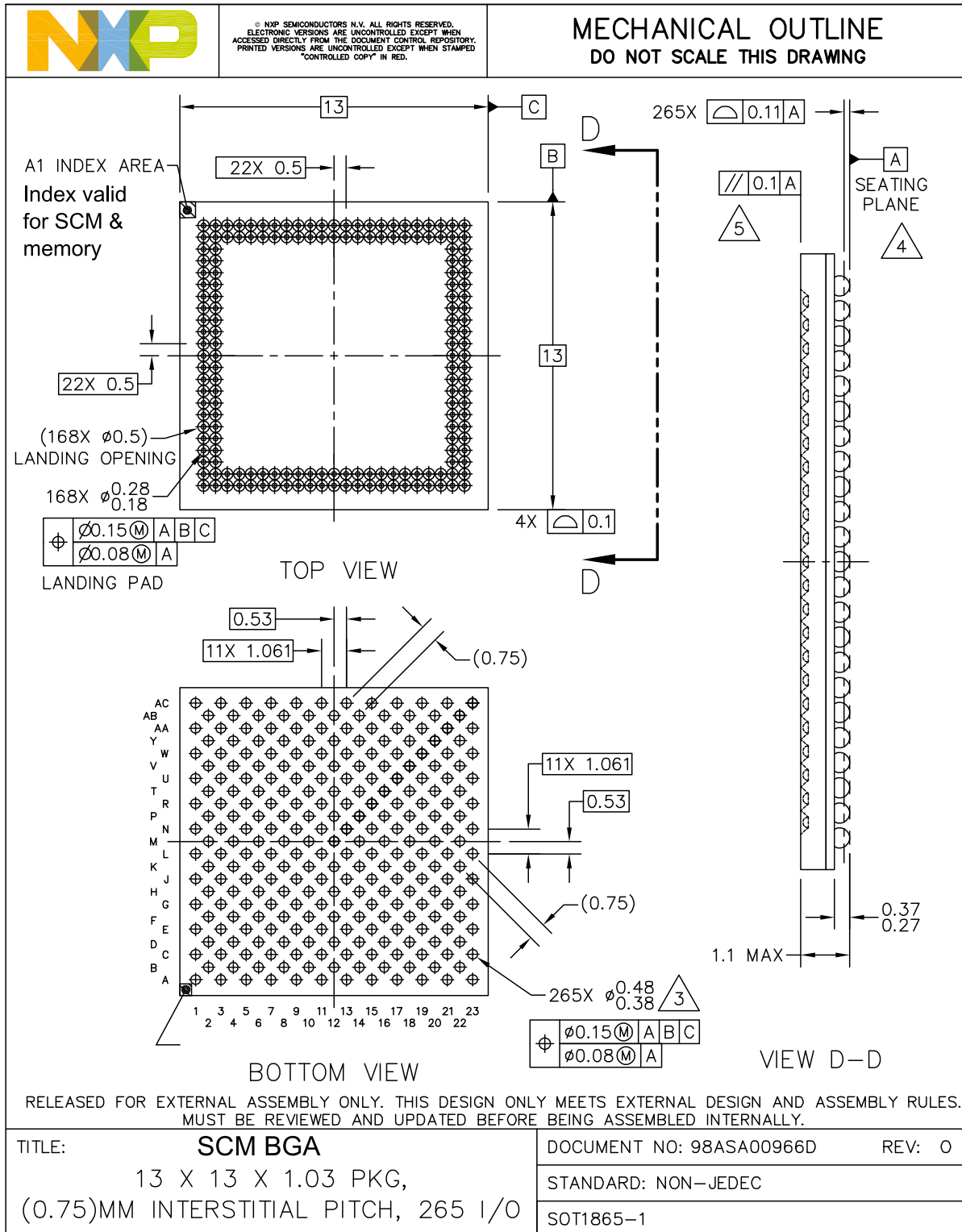


Figure 4. SCM-i.MX 6SoloX 265pin BGA without memory

8. Revision history

Table 12. SCM-i.MX 6SoloX revision history

Revision number	Date	Substantive changes
0	02/2017	Initial release

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