GMAC97A6

SENSITIVE GATE TRIACS SILICON BIDIRECTIONAL THYRISTORS 0.8A, 400V

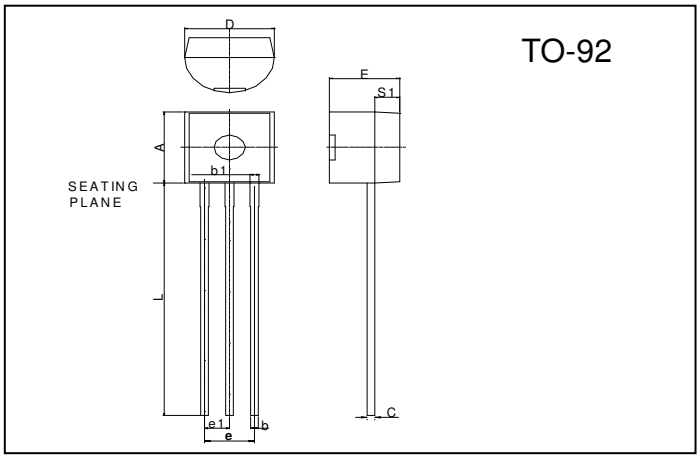
Description

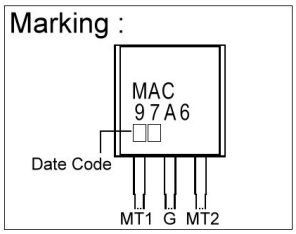
The GMAC97A6 device is designed for use in solid relays, MPU interface, TTL logic and any other light industrial or consumer application.
Supplied in an inexpensive TO-92 package which is readily adaptable for use in automatic insertion equipment.

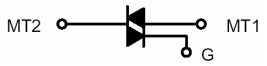
Features

- Sensitive Gate Triggering in Four Trigger Modes (Quadrants) for all possible Combinations of Trigger Sources, and especially for Circuits that Source Gate Drives
- All Diffused and Glassivated Junction for Maximum Uniformity of parameters and Reliability

Package Dimensions







REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	4.45	4.7	D	4.44	4.7
S_1	1.02	-	E	3.30	3.81
b	0.36	0.51	L	12.70	-
b_1	0.36	0.76	e1	1.150	1.390
C	0.36	0.51	e	2.42	2.66

Absolute Maximum Ratings (T_J=25℃ unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Repetitive Off-State Voltage(Note1) Sine Wave, 50 to 60Hz, Gate Open (T_J=-40 to 110℃)	V_{DRM} V_{RRM}	400	V
On-state RMS Current, Full Cycle Sine Wave 50 to 60Hz (T_C=50℃)	$I_{T(RMS)}$	0.6	A
Peak Non-Repetitive Surge Current One Full Cycle, Sine Wave, 60Hz (T_C=110℃)	I_{TSM}	8	A
Circuit Fusing Consideration (t=8.3ms)	I^2t	0.26	A^2S
Peak Gate Power (t ≤ 2.0μs, T_C=80℃)	P_{GM}	5.0	W
Average Gate Power (t ≤ 8.3ms, T_C=80℃)	$P_{G(AV)}$	0.1	W
Peak Gate Current (t ≤ 2.0μs, T_C=80℃)	I_{GM}	1.0	A
Peak Gate Voltage (t ≤ 2.0μs, T_C=80℃)	V_{GM}	5.0	V
Operating Junction Temperature Rang	T_J	-40 ~ +110	℃
Storage Temperature Rage	T_{stg}	-40 ~ +150	℃

Note 1.V_{DRM} and V_{RRM} for all types can be applied on a continuous basis. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.

Thermal Characteristics

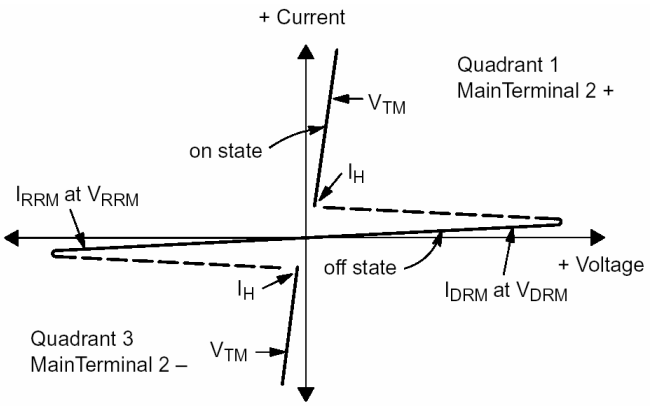
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to-case	$R_{\theta JC}$	75	℃/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	200	℃/W
Maximum Lead Temperature for soldering Purposes for 10 Seconds	T_L	260	℃

Electrical Characteristics (T_C = 25℃ unless otherwise noted; Electricals apply in both directions)

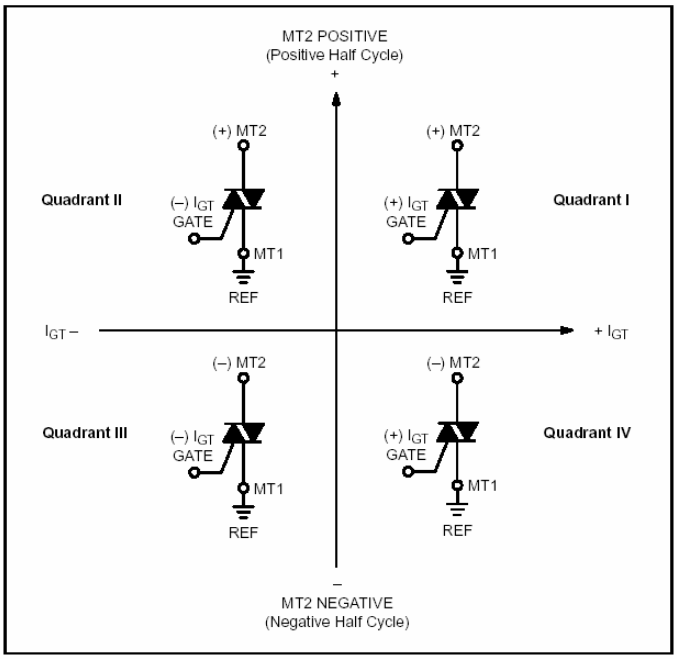
Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Peak Repetitive Blocking Current (Note2) (V_{DRM}=400V and V_{RRM}=400V; Gate Open) T_J=25℃ T_J=110℃	I_{DRM},I_{RRM}	-	-	10 100	μA
On Characteristics					
Peak On-State Voltage ≤ 2.0μs) (I_{TM}=±0.85A Peak; Pulse Width ≤ 2.0ms, Duty Cycle ≤ 2.0%)	V_{TM}	-	-	1.9	V
Gate Trigger Current (Continuous dc) (V_D=12.0 Vdc, R_L=100Ω) MT2(+), G(+) MT2(+), G(-) MT2(-), G(-) MT2(-), G(+)	I_{GT}	 - - - -	 - - - -	 5.0 5.0 5.0 7.0	mA
Gate Trigger Voltage (Continuous dc) (V_D=12.0 Vdc, R_L=100Ω) MT2(+), G(+) All Types MT2(+), G(-) All Types MT2(-), G(-) All Types MT2(-), G(+) All Types	V_{GT}	 - - - -	 0.66 0.77 0.84 0.88	 2.0 2.0 2.0 2.5	V
Gate Non-Trigger Voltage (V_D=12.0 V, R_L=100Ω T_J=110℃) All Four Quadrants	V_{GD}	0.1	-	-	V
Holding Current (V_D=12.0 Vdc, Initiating Current=200mA, Gate Open)	I_H	-	1.5	10	mA
Turn-On Time (V_D= V_{DRM}=400V, I_{TM}=1.0A pk, I_G=25mA)	tgt	-	2.0	-	μs
Dynamic Characteristics					
Critical Rate of Rise of Commutation Voltage (V_D=V_{DRM}=400V, I_{TM}=0.84A, Commutation di/dt=0.3A/ms, Gate Unenergized, T_C=50℃)	dV/dt (c)	-	5.0	-	V/μs
Critical Rate of Rise of Off-State Voltage (V_D=V_{DRM}=400V, T_C=110℃, Gate Open, Exponential Waveform)	dv/dt	-	25	-	V/μs

Voltage Current Characteristic of Triacs (Bidirectional Device)

Symbol	Parameter
V_{DRM}	Peak Repetitive Forward Off State Voltage
I_{DRM}	Peak Forward Blocking Current
V_{RRM}	Peak Repetitive Reverse Off State Voltage
I_{RRM}	Peak Reverse Blocking Current
V_{TM}	Maximum On State Voltage
I_H	Holding Current



Quadrant Definitions for a Triac



All polarities are referenced to MT1.
With in-phase signals (using standard AC lines) quadrants Ⅰ and Ⅲ are used

Characteristics Curve

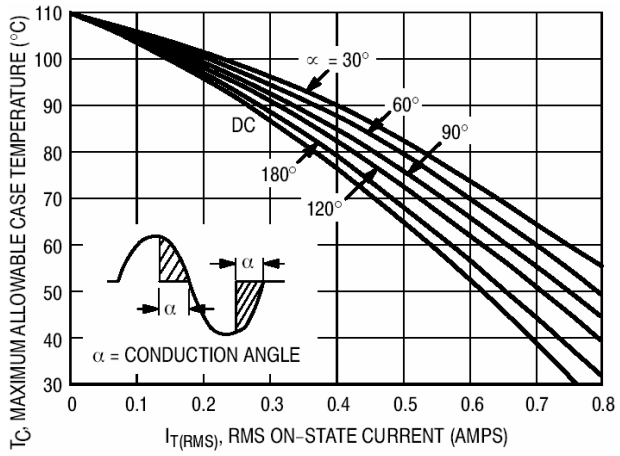


Fig 1. RMS Current Derating

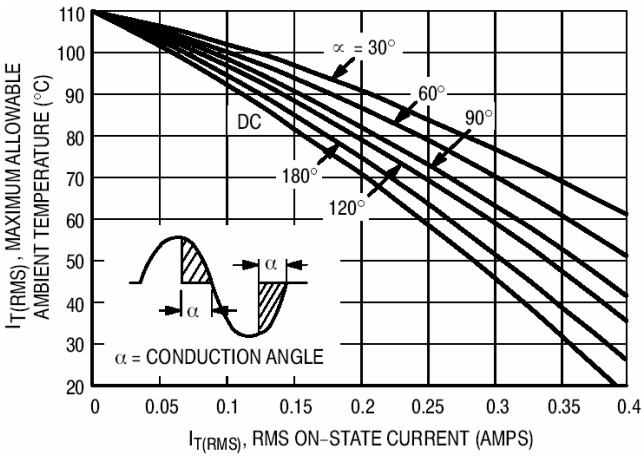


Fig 2. RMS Current Derating

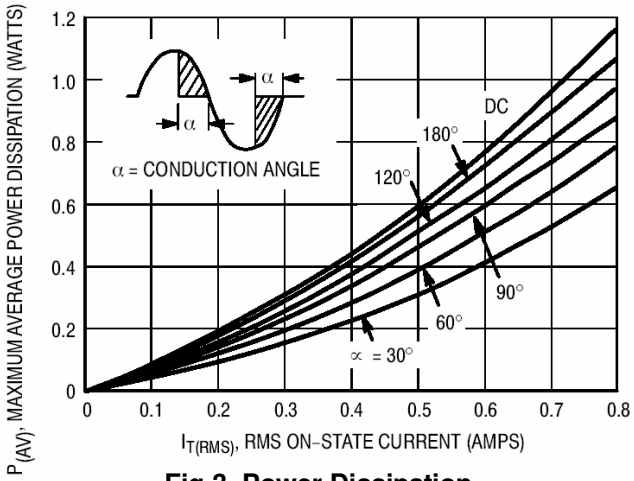


Fig 3. Power Dissipation

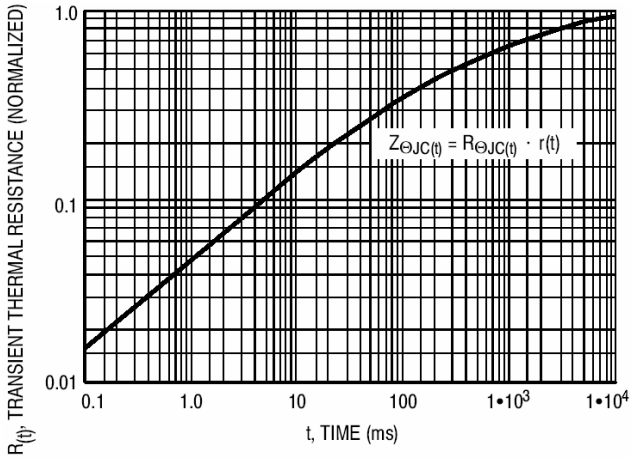


Fig 4. Transient Thermal Response

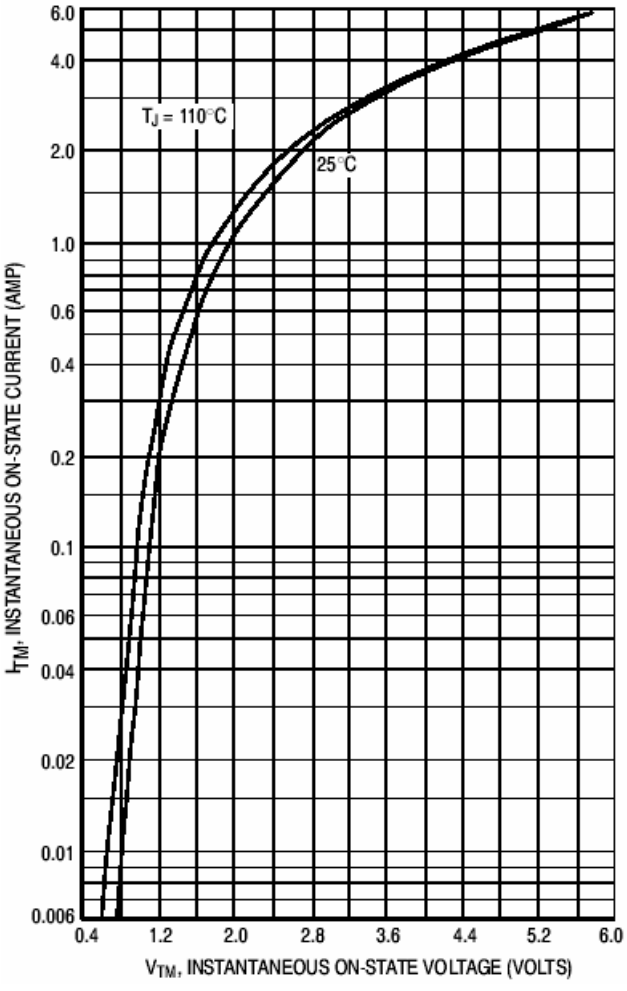


Fig 5. On-State Characteristics

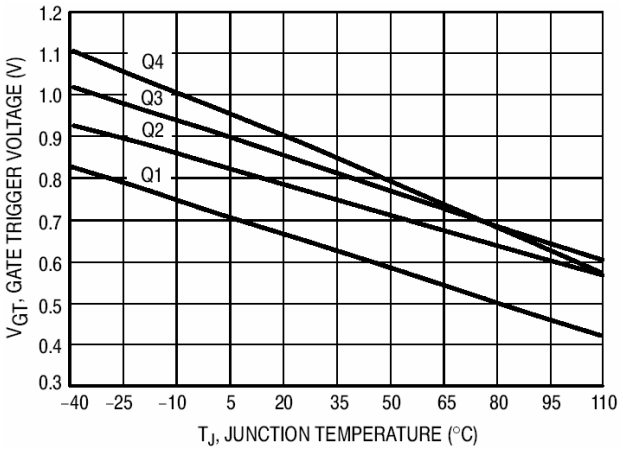


Fig 6. Typical Gate Trigger Voltage v.s. Junction Temperature

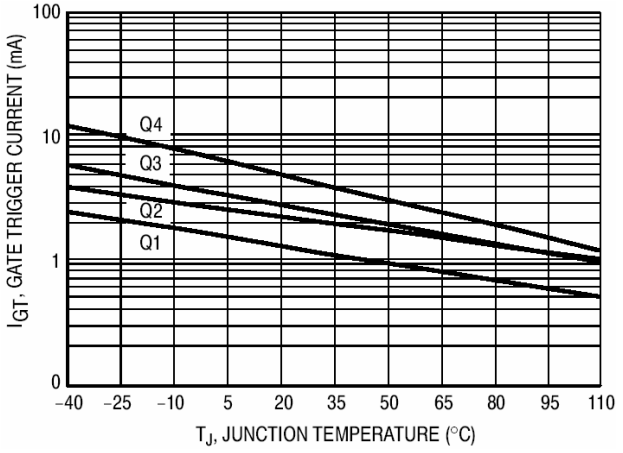


Fig 7. Typical Gate Trigger Current v.s. Junction Temperature

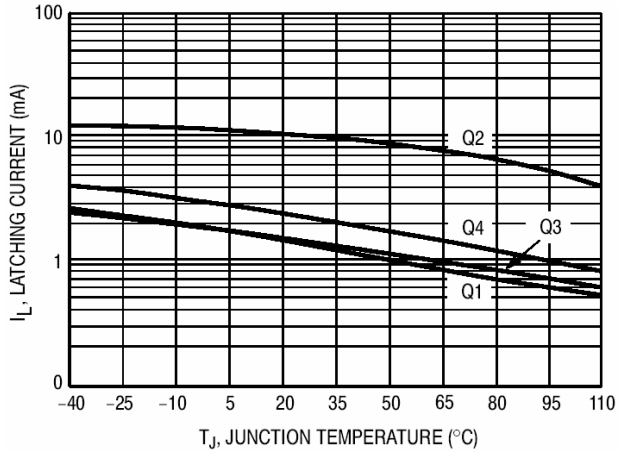


Fig 8. Typical Latching Current v.s. Junction Temperature

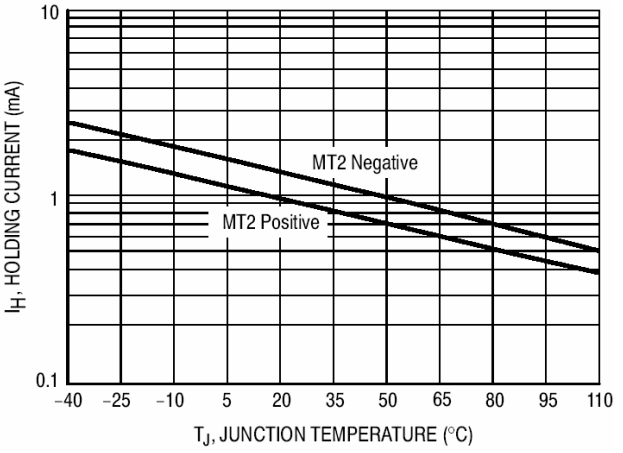


Fig 9. Typical Holding Current v.s. Junction Temperature

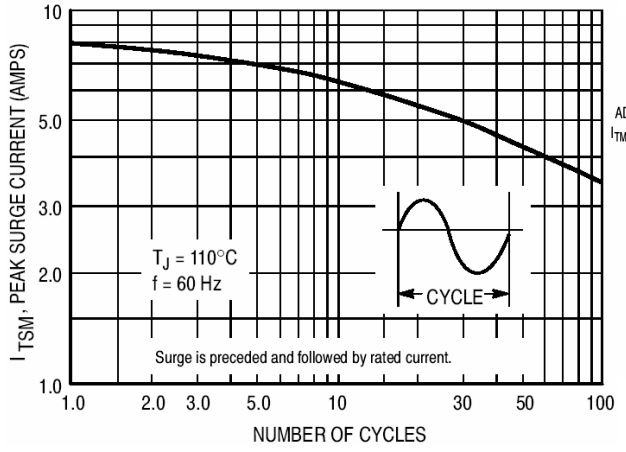


Fig 10. Maximum Allowable Surge Current

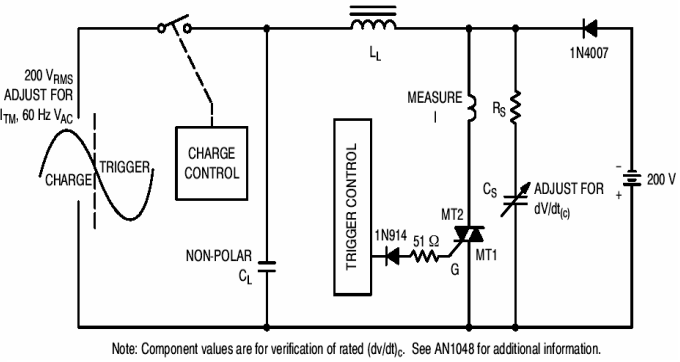


Fig 11. Simplified Test Circuit to Measure the Critical Rate of Rise of Commutating Voltage $(dV/dt)_c$

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