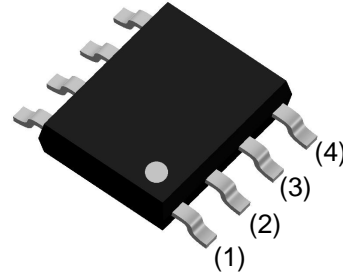
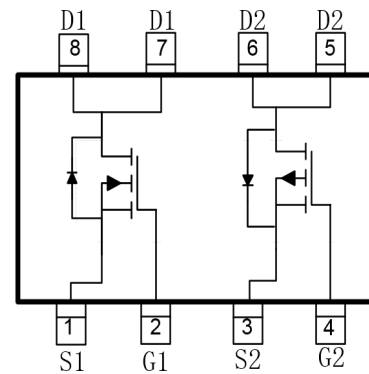
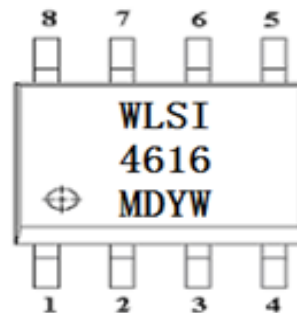


WCM4616
N- and P-Channel Complementary, 20V, MOSFET
<http://www.sh-willsemi.com>

V_{DS} (V)	Typical $R_{DS(on)}$ (Ω)
N-Channel 20	0.020@ $V_{GS}=10V$
	0.023@ $V_{GS}=4.5V$
P-Channel -20	0.028@ $V_{GS}=-10V$
	0.035@ $V_{GS}=-4.5V$


SOP-8L
Descriptions

The WCM4616 is the N-Channel and P-Channel enhancement MOS Field Effect Transistor as a single package for DC-DC converter or level shift applications, uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. Standard Product WCM4616 is Pb-free and Halogen-free.


Pin configuration (Top View)


4616 = Device Code

MD = Special Code

Y = Year

W = Week(A~z)

Marking
Order Information
Features

- Trench Technology
- Supper high density cell design
- Excellent ON resistance
- Extremely Low Threshold Voltage
- Package SOP-8L

Applications

- Driver: Relays, Solenoids, Lamps, Hammers
- Power supply converters circuit
- Load/Power Switching for portable device

Device	Package	Shipping
WCM4616-8/TR	SOP-8L	4000/Tape&Reel

Absolute Maximum Ratings ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	N-Channel		P-Channel		Unit	
		10 s	Steady State	10 s	Steady State		
V_{DSS}	Drain-to-Source Voltage	20		-20		V	
V_{GSS}	Gate-to-Source Voltage	± 20		± 20		V	
I_D	Continuous Drain Current ^{a d}	$T_A=25^{\circ}\text{C}$	6.5	5.1	-6.4	-5.0	A
		$T_A=70^{\circ}\text{C}$	5.2	4.1	-5.1	-4.0	
P_D	Power Dissipation ^{a d}	$T_A=25^{\circ}\text{C}$	1.9	1.2	1.8	1.1	W
		$T_A=70^{\circ}\text{C}$	1.2	0.8	1.1	0.7	
I_D	Continuous Drain Current ^{b d}	$T_A=25^{\circ}\text{C}$	6.0	4.9	-5.9	-4.8	A
		$T_A=70^{\circ}\text{C}$	4.8	3.9	-4.7	-3.8	
P_D	Power Dissipation ^{b d}	$T_A=25^{\circ}\text{C}$	1.6	1.1	1.5	1.0	W
		$T_A=70^{\circ}\text{C}$	1.1	0.7	1.0	0.6	
I_{DM}	Pulsed Drain Current ^c	26		-25		A	
T_J	Operation junction temperature	-55 to 150				$^{\circ}\text{C}$	
T_L	Lead Temperature	260				$^{\circ}\text{C}$	
T_{stg}	Storage temperature range	-55 to 150				$^{\circ}\text{C}$	

Thermal Resistance Ratings ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

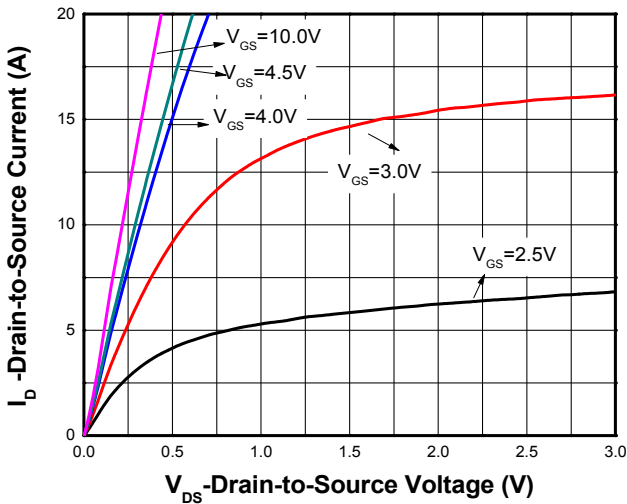
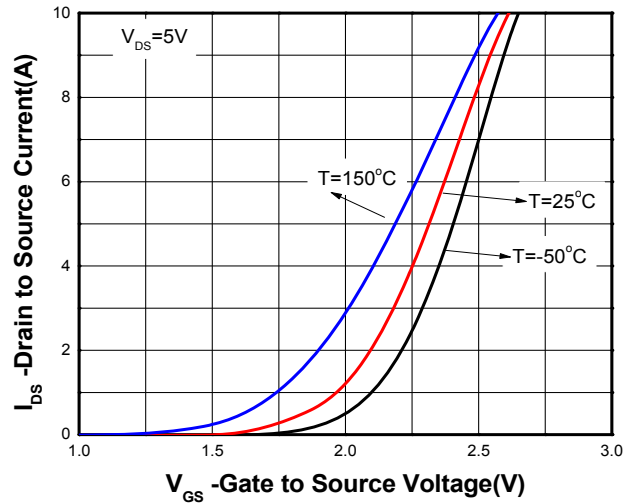
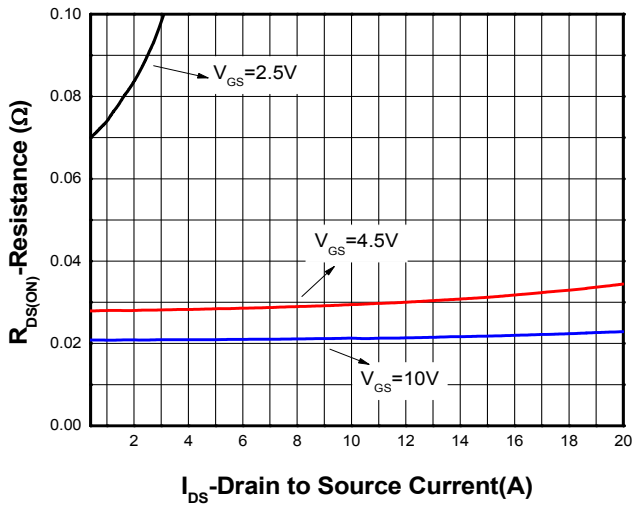
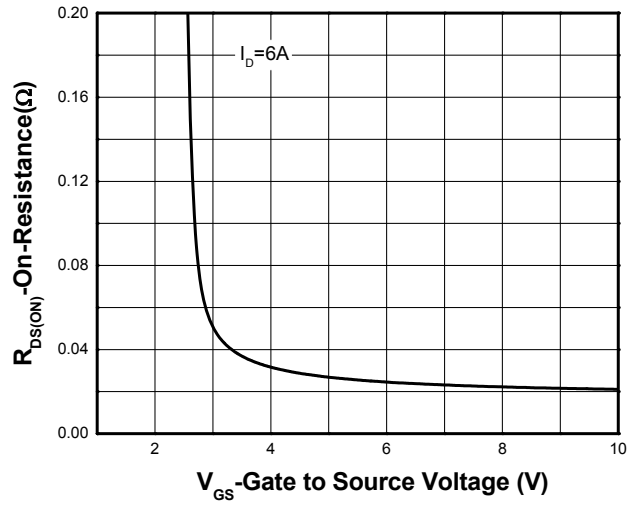
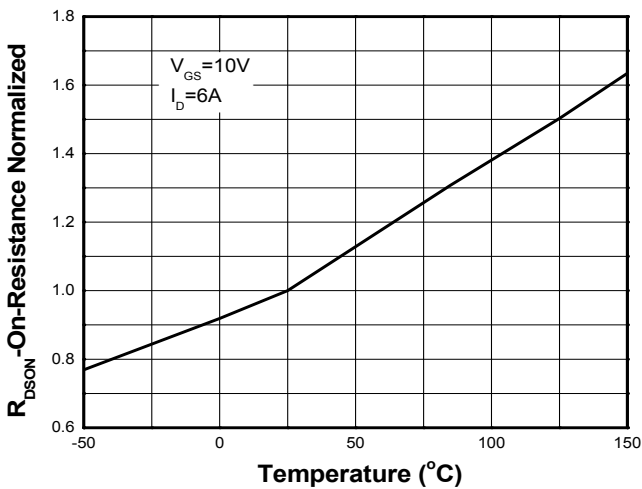
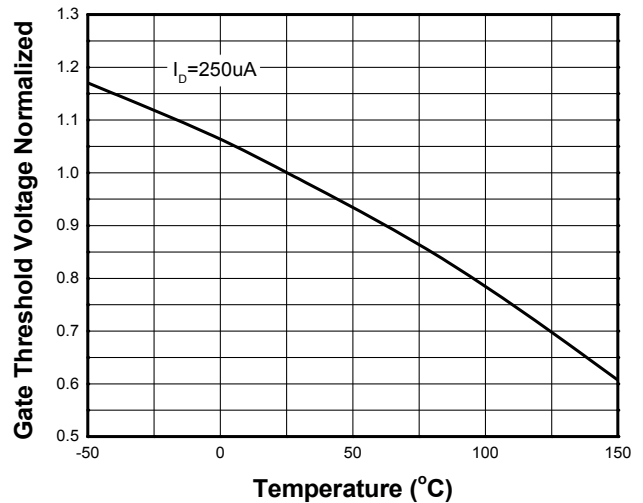
Parameter		Symbol	Typical	Maximum	Unit
Junction-to-Ambient Thermal Resistance ^a	$t \leq 10$ s	$R_{\theta JA}$	56	65	$^{\circ}\text{C/W}$
	Steady State		87	105	
Junction-to-Ambient Thermal Resistance ^b	$t \leq 10$ s	$R_{\theta JA}$	64	76	
	Steady State		96	115	
Junction-to-Case Thermal Resistance	Steady State	$R_{\theta JC}$	32	40	

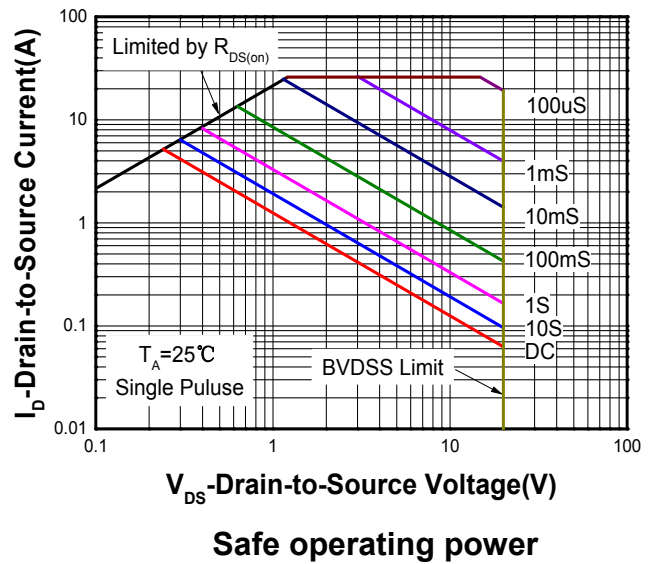
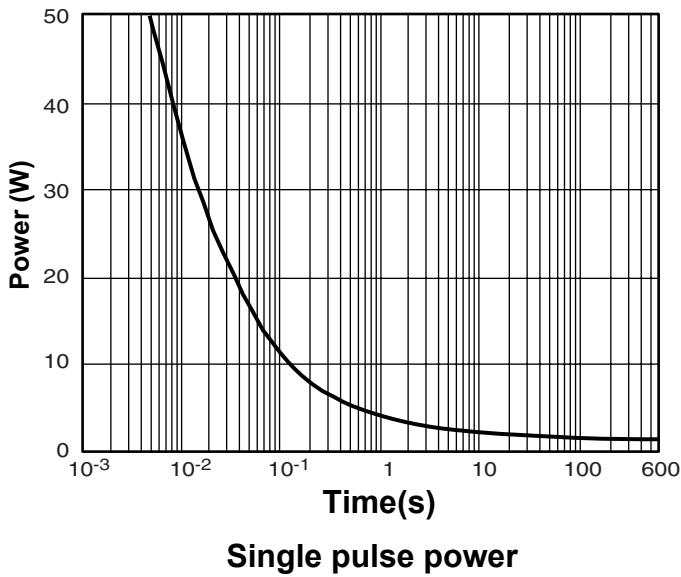
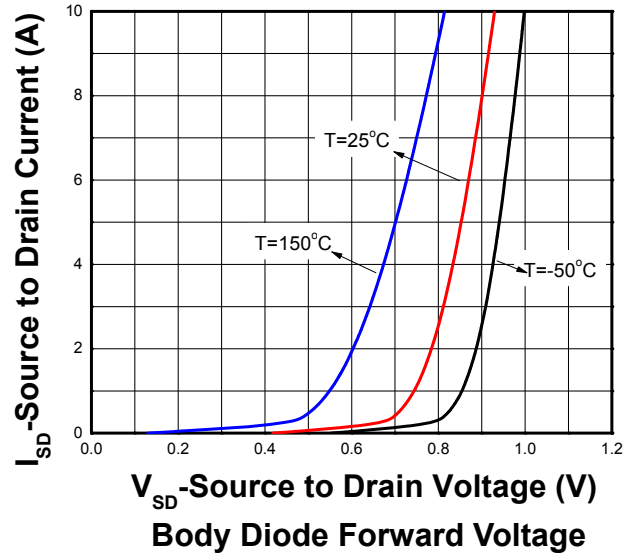
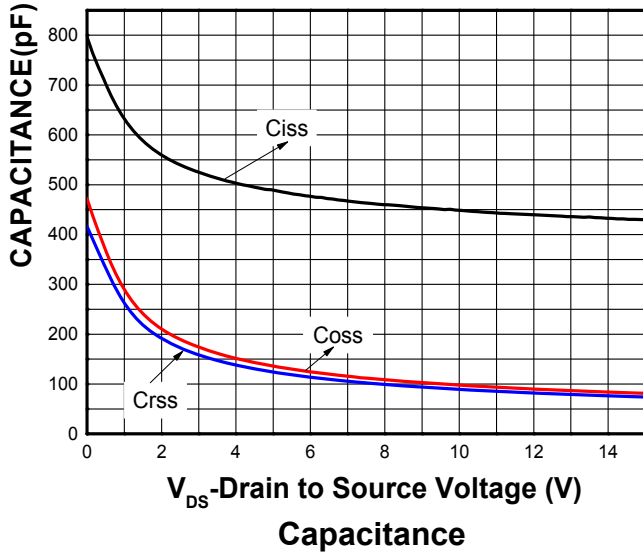
- a Surface mounted on FR4 Board using 1 square inch pad size, 1oz copper
- b Surface mounted on FR4 board using minimum pad size, 1oz copper
- c Repetitive rating, pulse width limited by junction temperature, $t_p=10\mu\text{s}$, Duty Cycle=1%
- d Repetitive rating, pulse width limited by junction temperature $T_J=150^{\circ}\text{C}$.

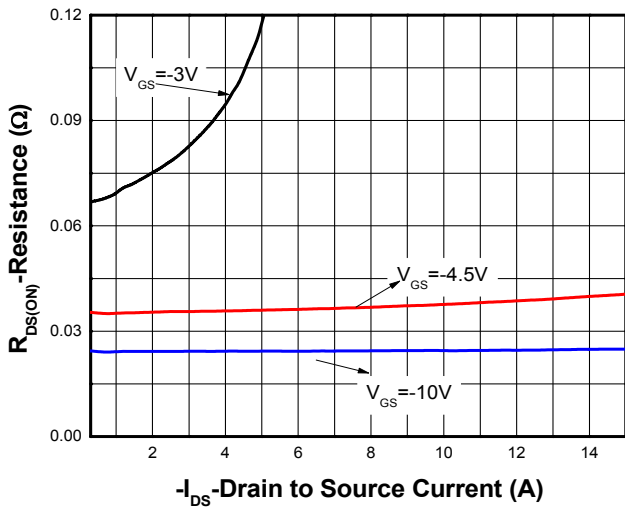
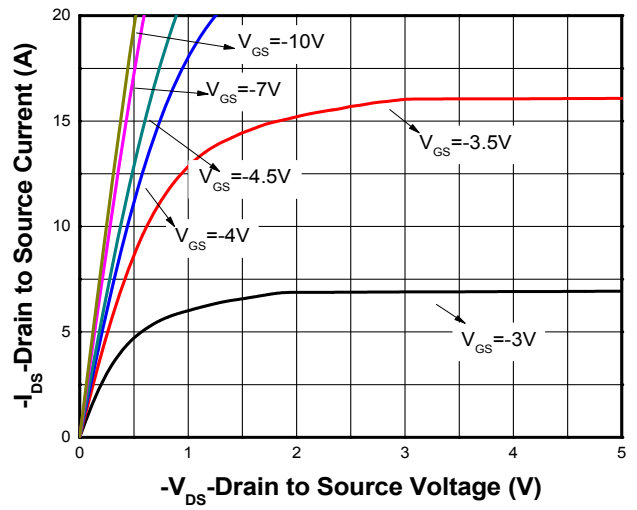
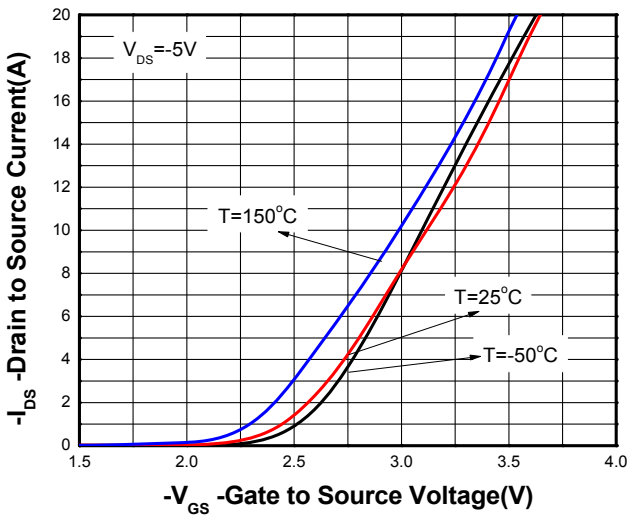
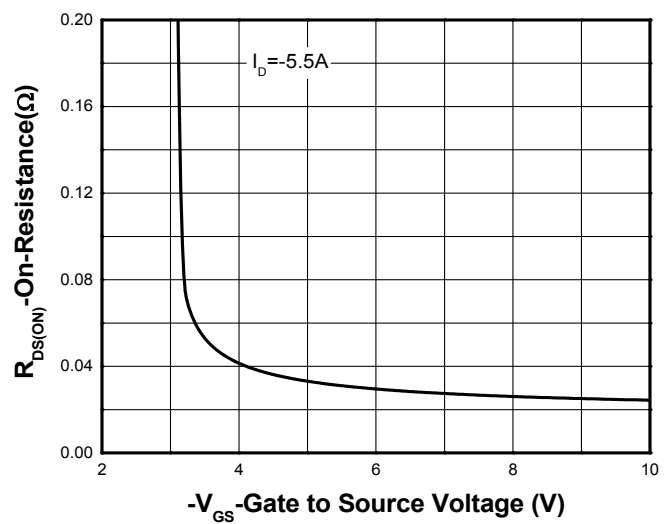
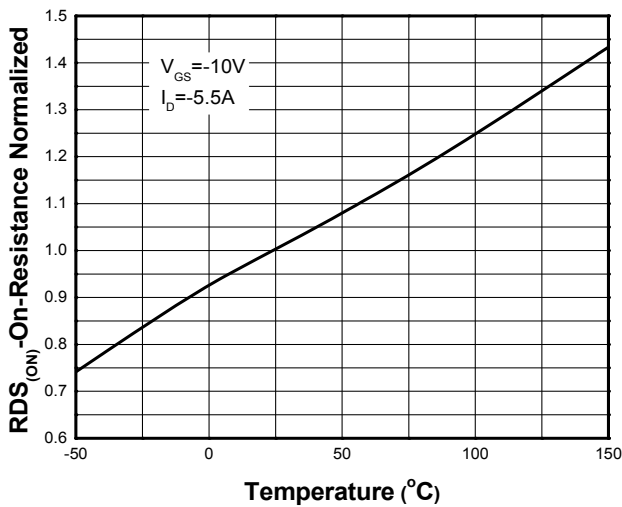
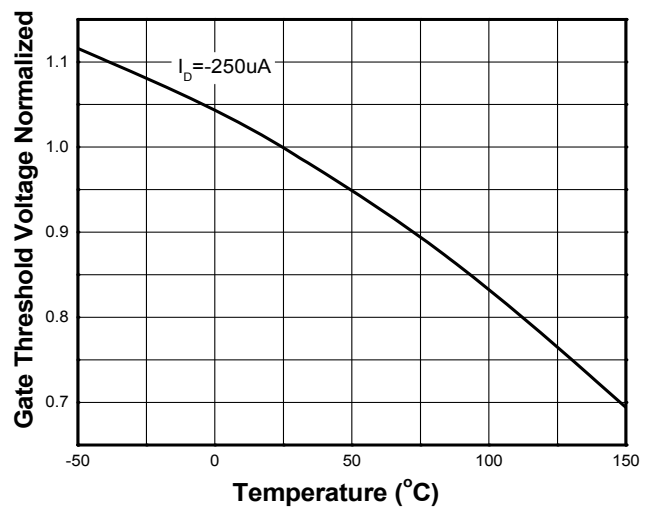
Electronics Characteristics (T_A=25°C unless otherwise noted)

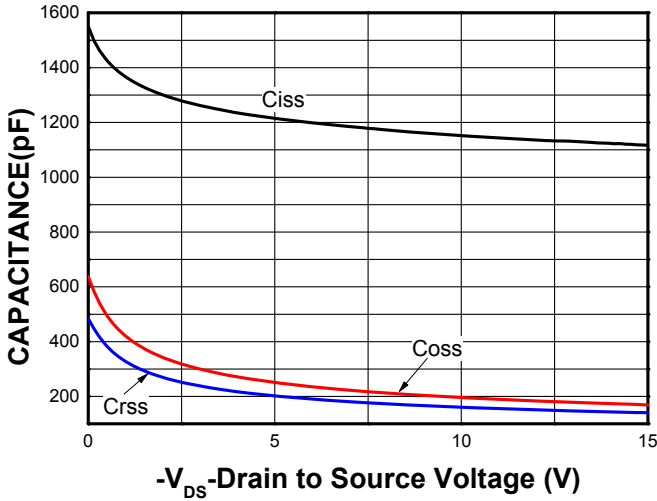
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit	
Off Characteristics							
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	N-Ch	20		V	
		V _{GS} =0V, I _D =-250uA	P-Ch	-20			
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =16V, V _{GS} =0V	N-Ch		1	uA	
		V _{DS} =-16V, V _{GS} =0V	P-Ch		-1		
I _{GSS}	Gate –Source leakage current	V _{DS} =0V, V _{GS} =±20V	N-Ch		±100	nA	
			P-Ch		±100		
ON Characteristics							
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D =250uA	N-Ch	1.0	1.5	2.5	V
		V _{DS} = V _{GS} , I _D =-250uA	P-Ch	-1.0	-1.5	-2.5	
R _{DS(on)}	Drain-Source On-Resistance	V _{GS} =10V, I _D =6A	N-Ch		20	31	mΩ
		V _{GS} =-10V, I _D =-5.5A	P-Ch		23	35	
		V _{GS} =4.5V, I _D =5.0A	N-Ch		28	41	
		V _{GS} =-4.5V, I _D =-5.0A	P-Ch		35	45	
Dynamic Characteristics							
C _{iss}	Input Capacitance	Nmos: V _{DS} =15V, V _{GS} =0V, F=1MHz	N-Ch		429	pF	
C _{oss}	Output Capacitance		P-Ch		1109		
C _{rss}	Reverse Transfer Capacitance	Pmos: V _{DS} =-15V, V _{GS} =0V, f=1MHz	N-Ch		81		
			P-Ch		167		
td(on) ^e	Turn-On Delay Time	Nmos: V _{DD} =5V, V _{GS} =4.5V, I _D =3.0A, R _G =3Ω	N-Ch	4	12		24
			P-Ch	9	27		54
tr ^e	Turn-On Rise Time	Pmos: V _{DD} =-5V, V _{GS} =-4.5V, I _D =-3A, R _G =3Ω	N-Ch	3	11	22	
			P-Ch	7	22	44	
td(off) ^e	Turn-Off Delay Time		N-Ch	7	21	42	
			P-Ch	14	41	82	
tf ^e	Turn-Off Fall Time		N-Ch	3	10	20	
			P-Ch	8	24	48	
BODY DIODE CHARACTERISTICS							
V _{SD}	Forward Voltage	V _{GS} =0 V, I _S = 1.0A	N-Ch		0.75	1.5	V
		V _{GS} =0 V, I _S =-1.0A	P-Ch		-0.75	-1.5	

^e Guaranteed by design

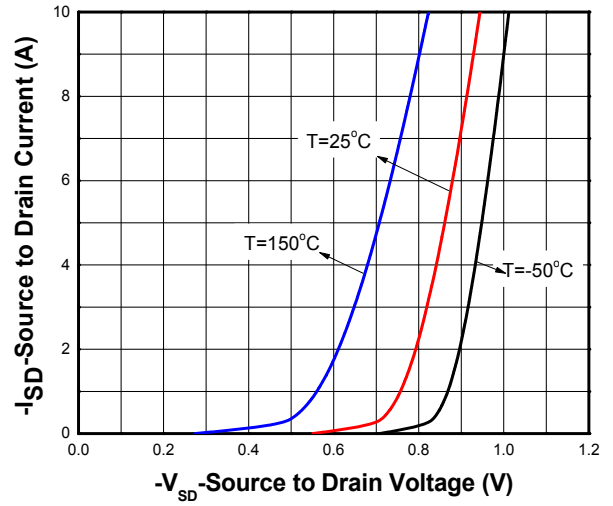
Typical Characteristics (N-Channel Ta=25°C, unless otherwise noted)

Output characteristics

Transfer characteristics

On-Resistance vs. Drain current

On-Resistance vs. Gate-to-source

On-Resistance vs. Junction temperature

Threshold voltage vs. Temperature



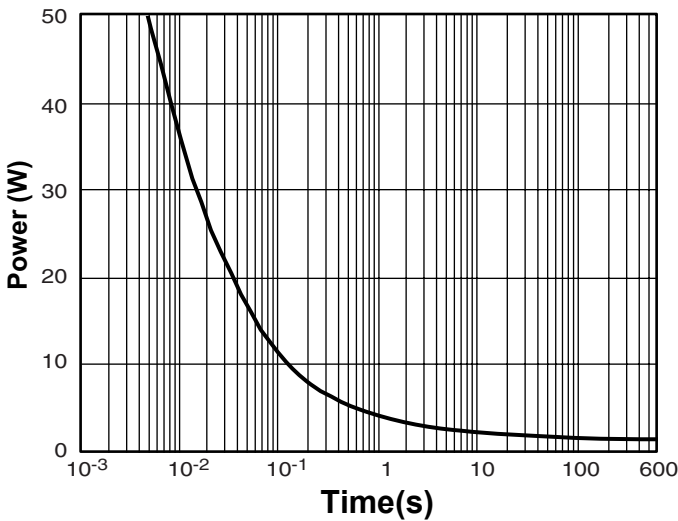
Typical Characteristics (P-Channel Ta=25°C, unless otherwise noted)

Output characteristics

Transfer characteristics

On-Resistance vs. Drain current

On-Resistance vs. Gate-to-source voltage

On-Resistance vs. Junction temperature

Threshold voltage vs. Temperature



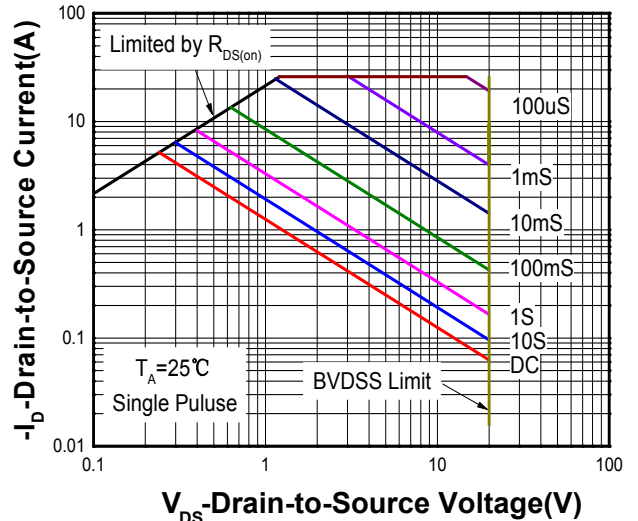
Capacitance



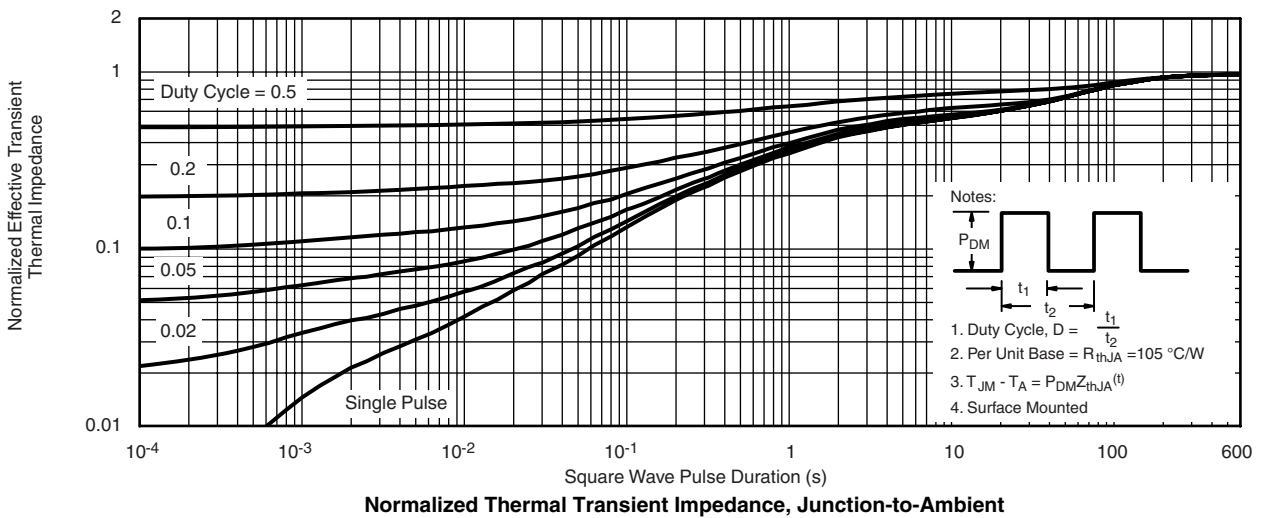
Body Diode Forward Voltage



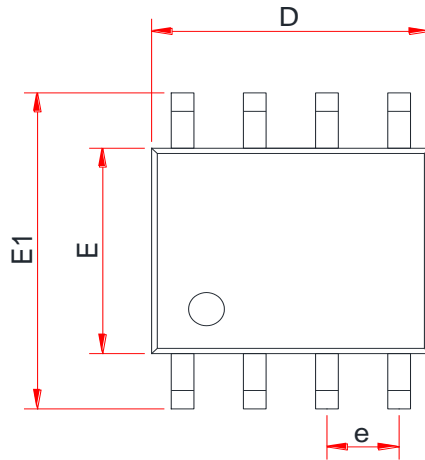
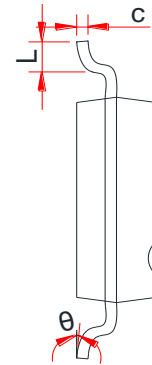
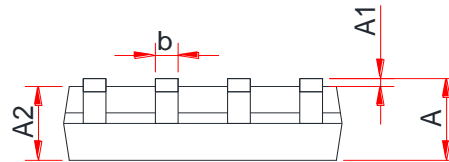
Single pulse power



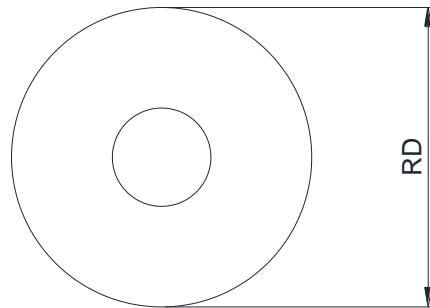
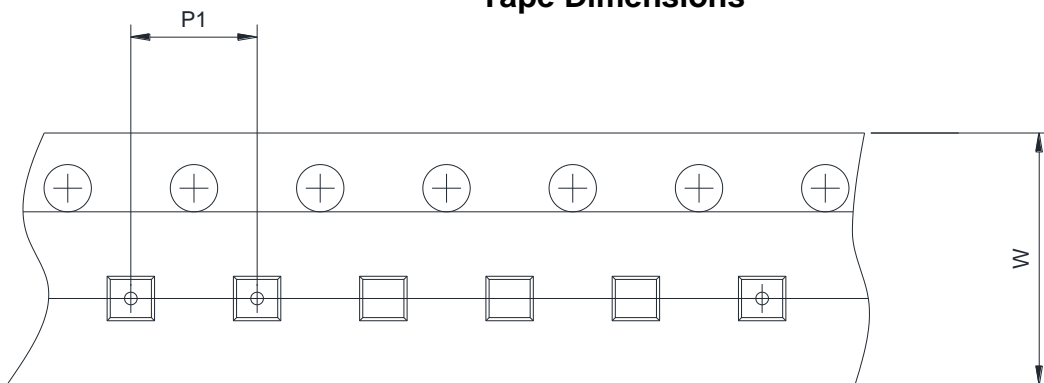
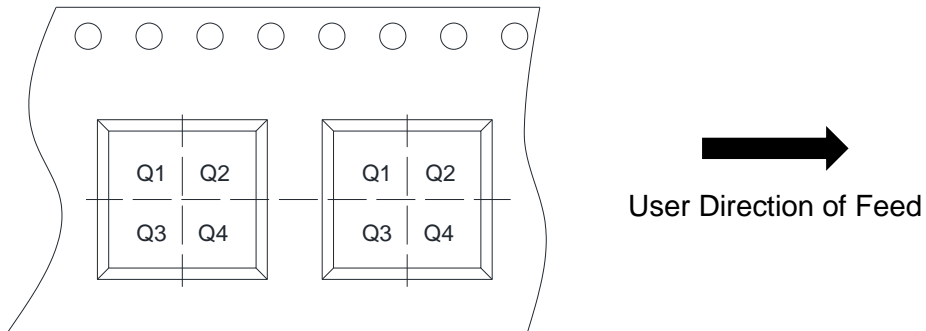
Safe operating power



Normalized Thermal Transient Impedance, Junction-to-Ambient

PACKAGE OUTLINE DIMENSIONS
SOP-8L

TOP VIEW

SIDE VIEW

SIDE VIEW

Symbol	Dimensions In Millimeters (mm)		
	Min.	Typ.	Max.
A	1.35	1.55	1.75
A1	0.05	0.15	0.25
A2	1.25	1.40	1.65
b	0.33	-	0.51
c	0.15	-	0.26
D	4.70	4.90	5.10
E	3.70	3.90	4.10
E1	5.80	6.00	6.20
e	1.27BSC		
L	0.40	-	1.27
θ	0°	-	8°

Reel Dimensions

Tape Dimensions

Quadrant Assignments For PIN1 Orientation In Tape


RD	Reel Dimension	<input type="checkbox"/> 7inch	<input checked="" type="checkbox"/> 13inch		
W	Overall width of the carrier tape	<input type="checkbox"/> 8mm	<input checked="" type="checkbox"/> 12mm		
P1	Pitch between successive cavity centers	<input type="checkbox"/> 2mm	<input type="checkbox"/> 4mm	<input checked="" type="checkbox"/> 8mm	
Pin1	Pin1 Quadrant	<input checked="" type="checkbox"/> Q1	<input type="checkbox"/> Q2	<input type="checkbox"/> Q3	<input type="checkbox"/> Q4