

MCF8316A Sensorless Field Oriented Control (FOC) Integrated FET BLDC Driver

ADVANCE INFORMATION

1 Features

- Three-phase BLDC motor driver with integrated motor control algorithm
 - Code-free Field Oriented Control (FOC)
 - Offline motor parameters measurement with Motor Parameter Extraction Tool (MPET)
 - 5-point configurable speed profile support
 - Windmilling support through forward resynchronization and reverse drive
 - Configurable motor startup and stop options
 - Anti-voltage surge protections prevents overvoltage
 - Improved acoustic performance with automatic dead time compensation
 - Variable monitoring through DACOUT
- 4.5- to 35-V operating voltage (40-V abs max)
- High output current capability: 8-A peak
- Low MOSFET on-state resistance
 - 95-mΩ $R_{DS(ON)}$ (HS + LS) at $T_A = 25^\circ\text{C}$
- Low power sleep mode
 - 3-μA (maximum) at $V_{VM} = 24\text{-V}$, $T_A = 25^\circ\text{C}$
- Speed loop accuracy: 3% with internal clock and 1% with external clock reference
- Customer-configurable non-volatile memory (EEPROM) to store device configuration
- Supports up to 75-kHz PWM frequency for low inductance motor support
- Does not require external current sense resistors, built-in current sensing
- Built-in 3.3-V $\pm 5\%$, 20-mA LDO regulator
- Built-in 3.3-V/5-V, 170-mA buck regulator
- DRVOFF independent pin to disable output
- Spread spectrum and slew rate for EMI mitigation
- Suite of Integrated protection features
 - Supply undervoltage lockout (UVLO)
 - Motor lock detection (5 different types)
 - Charge pump undervoltage (CPUV)
 - Overcurrent protection (OCP)
 - Thermal warning and shutdown (OTW/OTSD)
 - Fault condition indication pin (nFAULT)
 - Optional fault diagnostics over I2C interface

2 Applications

- [Brushless-DC \(BLDC\) Motor Modules](#)
- [Residential and living Fans](#)
- [Air Purifiers and Humidifier fans](#)
- [Washer and Dishwashers pumps](#)
- [Automotive Fan and Blowers](#)
- [Medical CPAP blowers](#)

3 Description

The MCF8316A provides a single-chip code-free sensorless FOC solution for customers driving speed-controlled 12- to 24-V brushless-DC motors (BLDC) or Permanent Magnet Synchronous motor (PMSM) with 8-A peak current capability. The MCF8316A integrates three 1/2-H bridges with 40-V absolute maximum capability and a very low $R_{DS(ON)}$ of 95 mΩ (high-side plus low-side). Power management features of an adjustable buck regulator and LDO generate the 3.3-V or 5.0-V voltage rails for the device and can be used to power external circuits.

The algorithm configuration can be set in non-volatile EEPROM, which allows the device to operate stand-alone once it has been configured. The device receives a speed command through a PWM input, analog voltage, or I2C command. There are a large number of protection features integrated into the MCF8316A, intended to protect the device, motor, and system against fault events.

Note

Some of the register in EEPROM can change in final production release.

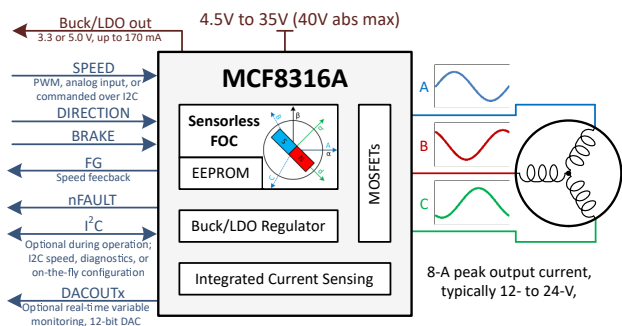
Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
MCF8316A1V	VQFN (40)	7.00 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Documentation for reference:

- Refer [E2E FAQ](#) for clarification.
- Refer [MCF8316A tuning guide](#)
- Refer to the [MCT8316A EVM GUI](#)



Simplified Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. ADVANCE INFORMATION for preproduction products; subject to change without notice.

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4 Revision History

DATE	REVISION	NOTES
August 2021	*	Initial release.

5 Pin Configuration and Functions

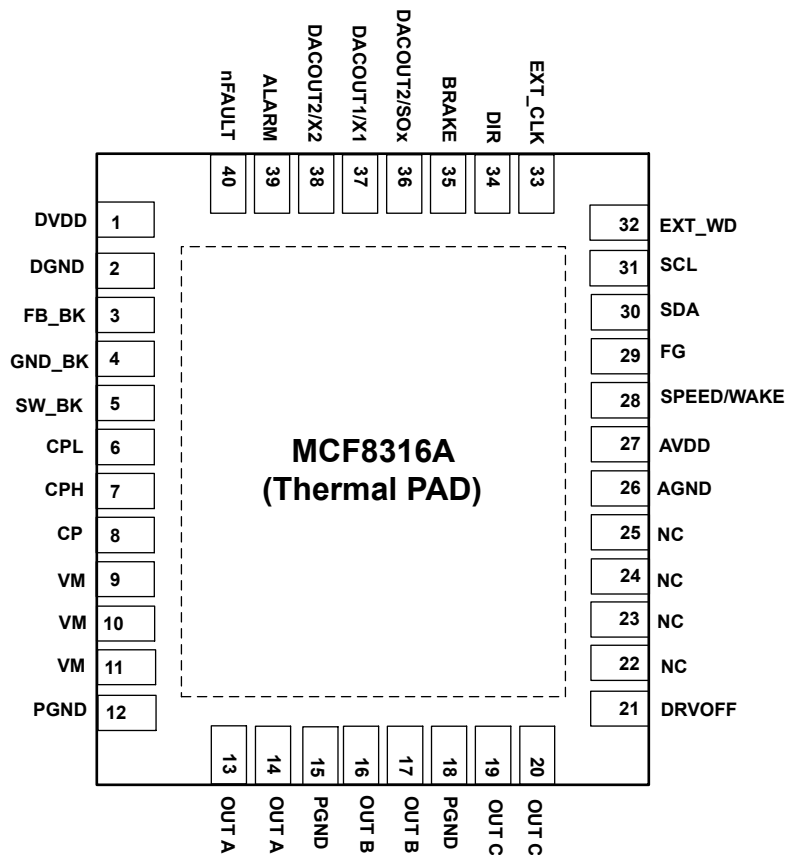


Figure 5-1. MCF8316A 40-Pin VQFN With Exposed Thermal Pad Top View

Table 5-1. Pin Functions

PIN	40-pin Package	TYPE ⁽¹⁾	DESCRIPTION
NAME	MCF8316A		
AGND	26	GND	Device analog ground. Refer Layout Guidelines for connections recommendation.
ALARM	39	O	Fault warning indicator. Pulled logic-low with fault condition; Open-drain output requires an external pull-up resistor to 1.8V to 5.0V.
AVDD	27	PWR O	3.3-V internal regulator output. Connect a X5R or X7R, 1- μ F, 6.3-V ceramic capacitor between the AVDD1 and AGND pins. This regulator can source up to 20 mA externally.
BRAKE	35	I	High \rightarrow Brake the motor when High Low \rightarrow normal operation
CP	8	PWR O	Charge pump output. Connect a X5R or X7R, 1- μ F, 16-V ceramic capacitor between the CP and VM pins.
CPH	7	PWR	Charge pump switching node. Connect a X5R or X7R, 47-nF, ceramic capacitor between the CPH and CPL pins. TI recommends a capacitor voltage rating at least twice the normal operating voltage of the device.
CPL	6	PWR	
DACOUT2/SOx	36	I	Multipurpose pin: DAC output when configured as DACOUT2 CSA output configured as SOx
DACOUT1/X1	37	I/O	Multipurpose pin: DAC output when configured as DACOUT1 Crystal oscillator input, connected to one end of crystal in external crystal oscillator mode when configured as X1

Table 5-1. Pin Functions (continued)

PIN NAME	40-pin Package MCF8316A	TYPE ⁽¹⁾	DESCRIPTION
DACOUT2/X 2	38	I	Multipurpose pin: DAC output when configured as DACOUT2 Crystal oscillator output, connect to one end of crystal in external crystal oscillator mode when configured as X2
DGND	2	GND	Device digital ground. Refer Layout Guidelines for connections recommendation.
DIR	34	I	Direction of motor spinning; When low, phase driving sequence is OUT A → OUT B → OUT C When high, phase driving sequence is OUT A → OUT C → OUT B
DRVOFF	21	I	Coast (Hi-Z) all six MOSFETs.
DVDD	1	PWR O	1.5-V internal regulator output. Connect a X5R or X7R, 1-μF, 6.3-V ceramic capacitor between the DVDD and DGND pins.
EXT_CLK	33	I	Clock reference input in external clock reference mode when configured as EXT_CLK
EXT_WD	32	I	External Watch Dog input
FB_BK	3	PWR I	Feedback for buck regulator. Connect to buck regulator output after the inductor/resistor.
GND_BK	4	GND	Buck regulator ground. Refer Layout Guidelines for connections recommendation.
FG	29	O	Motor Speed indicator output. Open-drain output requires an external pull-up resistor to 1.8V to 5.0V.
NC	22,23,24,25	-	No connection, open
nFAULT	40	O	Fault indicator. Pulled logic-low with fault condition; Open-drain output requires an external pull-up resistor to 1.8V to 5.0V.
OUTA	13, 14	PWR O	Half bridge output A
OUTB	16, 17	PWR O	Half bridge output B
OUTC	19, 20	PWR O	Half bridge output C
PGND	12, 15, 18	GND	Device power ground. Refer Layout Guidelines for connections recommendation.
SCL	31	I	I ² C clock input
SDA	30	I/O	I ² Data line
SPEED/ WAKE	28	I	Device speed input, supports analog or PWM speed input, The speed pin input can be configured through ANA_PWM_SPD_SET
SW_BK	5	PWR O	Buck switch node. Connect this pin to an inductor or resistor.
VM	9, 10, 11	PWR I	Device and motor power supply. Connect to motor supply voltage; bypass to GND with two 0.1-μF capacitors (for each pin) plus one bulk capacitor. TI recommends a capacitor voltage rating at least twice the normal operating voltage of the device.
Thermal pad		GND	Must be connected to ground

(1) I = input, O = output, GND = ground pin, PWR = power, NC = no connect

6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)⁽¹⁾

	MIN	MAX	UNIT
Power supply pin voltage (VM)	-0.3	40	V
Power supply voltage ramp at power up (VM)		4	V/μs
Voltage difference between ground pins (GND_BK, PGND, AGND)	-0.3	0.3	V
Charge pump voltage (CPH, CP)	-0.3	V _M + 6	V
Charge pump negative switching pin voltage (CPL)	-0.3	V _M + 0.3	V
Switching regulator pin voltage (FB_BK)	-0.3	5.75	V
Switching node pin voltage (SW_BK)	-0.3	V _M + 0.3	V
Analog regulators pin voltage (AVDD)	-0.3	5.75	V
Analog regulators pin voltage (DVDD)	-0.3	1.7	V
Logic pin input voltage (DRVOFF, DIR, SPEED, nBRAKE etc)	-0.3	6	V
Logic pin output voltage (nFAULT, FG)	-0.3	6	V
Output pin voltage (OUTA, OUTB, OUTC)	-1	V _M + 1	V
Ambient temperature, T _A	-40	125	°C
Junction temperature, T _J	-40	150	°C
Storage temperature, T _{stg}	-65	150	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±1000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾	±250	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V _{VM}	Power supply voltage	V _{VM}	4.5	24	35	V
I _{OUT} ⁽¹⁾	Peak output winding current	OUTA, OUTB, OUTC			8	A
V _{IN}	Logic input voltage	DRVOFF, SPEED, SDA	-0.1		5.5	V
V _{OD}	Open drain pullup voltage	nFAULT, FG	-0.1		5.5	V
I _{OD}	Open drain output current capability	nFAULT, FG			5	mA
T _A	Operating ambient temperature		-40		125	°C
T _J	Operating Junction temperature		-40		150	°C

- (1) Power dissipation and thermal limits must be observed

6.4 Thermal Information

THERMAL METRIC		MCF8316A	
		VQFN (RGF)	
		40 Pins	
			UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	25.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	15.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	7.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.0	°C/W

6.5 Electrical Characteristics

$T_J = -40^{\circ}\text{C}$ to $+150^{\circ}\text{C}$, $V_{VM} = 4.5$ to 35 V (unless otherwise noted). Typical limits apply for $T_A = 25^{\circ}\text{C}$, $V_{VM} = 24\text{ V}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES						
I_{VMQ}	VM sleep mode current	$V_{VM} > 6\text{ V}$, $V_{SPEED} = 0$, $T_A = 25^{\circ}\text{C}$		2.5	3	μA
		$V_{SPEED} = 0$, $T_A = 125^{\circ}\text{C}$		4	10	μA
I_{VMS}	VM standby mode current	$V_{VM} > 6\text{ V}$, $V_{SPEED} > V_{EN_SB}$, DRVOFF = High, $T_A = 25^{\circ}\text{C}$, $L_{BK} = 47\text{ uH}$, $C_{BK} = 22\text{ }\mu\text{F}$		10		mA
		$V_{VM} > 6\text{ V}$, $V_{SPEED} > V_{EN_SB}$, DRVOFF = High, $T_A = 25^{\circ}\text{C}$, $R_{BK} = 22\text{ }\Omega$, $C_{BK} = 22\text{ }\mu\text{F}$		27		mA
		$V_{VM} > 6\text{ V}$, $V_{SPEED} > V_{EN_SB}$, DRVOFF = High, $L_{BK} = 47\text{ uH}$, $C_{BK} = 22\text{ }\mu\text{F}$		11		mA
		$V_{VM} > 6\text{ V}$, $V_{SPEED} > V_{EN_SB}$, DRVOFF = High, $R_{BK} = 22\text{ }\Omega$, $C_{BK} = 22\text{ }\mu\text{F}$		27		mA
I_{VM}	VM operating mode current	$V_{VM} > 6\text{ V}$, $V_{SPEED} > V_{EX_SL}$, PWM_FREQ_OUT = 0011b (25 kHz), $T_J = 25^{\circ}\text{C}$, $L_{BK} = 47\text{ uH}$, $C_{BK} = 22\text{ }\mu\text{F}$, No Motor Connected		14		mA
		$V_{VM} > 6\text{ V}$, $V_{SPEED} > V_{EX_SL}$, PWM_FREQ_OUT = 0011b (25 kHz), $T_J = 25^{\circ}\text{C}$, $R_{BK} = 22\text{ }\Omega$, $C_{BK} = 22\text{ }\mu\text{F}$, No Motor Connected		30		mA
		$V_{VM} > 6\text{ V}$, $V_{SPEED} > V_{EX_SL}$, PWM_FREQ_OUT = 0011b (25 kHz), $L_{BK} = 47\text{ uH}$, $C_{BK} = 22\text{ }\mu\text{F}$, No Motor Connected		15		mA
		$V_{VM} > 6\text{ V}$, $V_{SPEED} > V_{EX_SL}$, PWM_FREQ_OUT = 0011b (25 kHz), $R_{BK} = 22\text{ }\Omega$, $C_{BK} = 22\text{ }\mu\text{F}$, No Motor Connected		32		mA
V_{AVDD}	Analog regulator voltage	$0\text{ mA} \leq I_{AVDD} \leq 30\text{ mA}$	3.135	3.3	3.465	V
I_{AVDD}	External analog regulator load				20	mA
V_{DVDD}	Digital regulator voltage		1.4	1.55	1.65	V
V_{VCP}	Charge pump regulator voltage	VCP with respect to VM		4.7		V
f_{CP}	Charge pump switching frequency			400		kHz

$T_J = -40^{\circ}\text{C}$ to $+150^{\circ}\text{C}$, $V_{VM} = 4.5$ to 35 V (unless otherwise noted). Typical limits apply for $T_A = 25^{\circ}\text{C}$, $V_{VM} = 24\text{ V}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BUCK REGULATOR						
V_{BK}	Buck regulator average voltage ($L_{BK} = 47\ \mu\text{H}$, $C_{BK} = 22\ \mu\text{F}$)	$V_{VM} > 6\text{ V}$, $0\text{ mA} \leq I_{BK} \leq 200\text{ mA}$, BUCK_SEL = 00b	3.1	3.3	3.5	V
		$V_{VM} > 6\text{ V}$, $0\text{ mA} \leq I_{BK} \leq 200\text{ mA}$, BUCK_SEL = 01b	4.6	5.0	5.4	V
		$V_{VM} > 6\text{ V}$, $0\text{ mA} \leq I_{BK} \leq 200\text{ mA}$, BUCK_SEL = 10b	3.7	4.0	4.3	V
		$V_{VM} > 6.7\text{ V}$, $0\text{ mA} \leq I_{BK} \leq 200\text{ mA}$, BUCK_SEL = 11b	5.2	5.7	6.2	V
		$V_{VM} < 6.0\text{ V}$ (BUCK_SEL = 00b, 01b, 10b) or $V_{VM} < 6.0\text{ V}$ (BUCK_SEL = 11b), $0\text{ mA} \leq I_{BK} \leq 200\text{ mA}$		$V_{VM} - I_{BK} \cdot (R_{LBK} + 2)$ (1)		V
V_{BK}	Buck regulator average voltage ($L_{BK} = 22\ \mu\text{H}$, $C_{BK} = 22\ \mu\text{F}$)	$V_{VM} > 6\text{ V}$, $0\text{ mA} \leq I_{BK} \leq 50\text{ mA}$, BUCK_SEL = 00b	3.1	3.3	3.5	V
		$V_{VM} > 6\text{ V}$, $0\text{ mA} \leq I_{BK} \leq 50\text{ mA}$, BUCK_SEL = 01b	4.6	5.0	5.4	V
		$V_{VM} > 6\text{ V}$, $0\text{ mA} \leq I_{BK} \leq 50\text{ mA}$, BUCK_SEL = 10b	3.7	4.0	4.3	V
		$V_{VM} > 6.7\text{ V}$, $0\text{ mA} \leq I_{BK} \leq 50\text{ mA}$, BUCK_SEL = 11b	5.2	5.7	6.2	V
		$V_{VM} < 6.0\text{ V}$ (BUCK_SEL = 00b, 01b, 10b) or $V_{VM} < 6.7\text{ V}$ (BUCK_SEL = 11b), $0\text{ mA} \leq I_{BK} \leq 50\text{ mA}$		$V_{VM} - I_{BK} \cdot (R_{LBK} + 2)$ (1)		V
V_{BK}	Buck regulator average voltage ($R_{BK} = 22\ \Omega$, $C_{BK} = 22\ \mu\text{F}$)	$V_{VM} > 6\text{ V}$, $0\text{ mA} \leq I_{BK} \leq 40\text{ mA}$, BUCK_SEL = 00b	3.1	3.3	3.5	V
		$V_{VM} > 6\text{ V}$, $0\text{ mA} \leq I_{BK} \leq 40\text{ mA}$, BUCK_SEL = 01b	4.6	5.0	5.4	V
		$V_{VM} > 6\text{ V}$, $0\text{ mA} \leq I_{BK} \leq 40\text{ mA}$, BUCK_SEL = 10b	3.7	4.0	4.3	V
		$V_{VM} > 6.7\text{ V}$, $0\text{ mA} \leq I_{BK} \leq 40\text{ mA}$, BUCK_SEL = 11b	5.2	5.7	6.2	V
		$V_{VM} < 6.0\text{ V}$ (BUCK_SEL = 00b, 01b, 10b) or $V_{VM} < 6.7\text{ V}$ (BUCK_SEL = 11b), $0\text{ mA} \leq I_{BK} \leq 40\text{ mA}$		$V_{VM} - I_{BK} \cdot (R_{BK} + 2)$		V
V_{BK_RIP}	Buck regulator ripple voltage	$V_{VM} > 6\text{ V}$, $0\text{ mA} \leq I_{BK} \leq 200\text{ mA}$, $L_{BK} =$ $47\ \mu\text{H}$, $C_{BK} = 22\ \mu\text{F}$	-100		100	mV
		$V_{VM} > 6\text{ V}$, $0\text{ mA} \leq I_{BK} \leq 50\text{ mA}$, Buck regulator with inductor, $L_{BK} = 22\ \mu\text{H}$, $C_{BK} =$ $22\ \mu\text{F}$	-100		100	mV
		$V_{VM} > 6\text{ V}$, $0\text{ mA} \leq I_{BK} \leq 50\text{ mA}$, Buck regulator with resistor; $R_{BK} = 22\ \Omega$, $C_{BK} =$ $22\ \mu\text{F}$	-100		100	mV
I_{BK}	External buck regulator load	$L_{BK} = 47\ \mu\text{H}$, $C_{BK} = 22\ \mu\text{F}$, BUCK_PS_DIS = 1b			170	mA
		$L_{BK} = 47\ \mu\text{H}$, $C_{BK} = 22\ \mu\text{F}$, BUCK_PS_DIS = 0b			170 – I_{AVDD}	mA
		$L_{BK} = 22\ \mu\text{H}$, $C_{BK} = 22\ \mu\text{F}$, BUCK_PS_DIS = 1b			20	mA
		$L_{BK} = 22\ \mu\text{H}$, $C_{BK} = 22\ \mu\text{F}$, BUCK_PS_DIS = 0b			20 – I_{AVDD}	mA
		$R_{BK} = 22\ \Omega$, $C_{BK} = 22\ \mu\text{F}$, BUCK_PS_DIS = 1b			10	mA
		$R_{BK} = 22\ \Omega$, $C_{BK} = 22\ \mu\text{F}$, BUCK_PS_DIS = 0b			10 – I_{AVDD}	mA

$T_J = -40^{\circ}\text{C}$ to $+150^{\circ}\text{C}$, $V_{VM} = 4.5$ to 35 V (unless otherwise noted). Typical limits apply for $T_A = 25^{\circ}\text{C}$, $V_{VM} = 24$ V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{\text{SW_BK}}$	Buck regulator switching frequency	Regulation Mode			535	kHz
		Linear Mode			535	kHz
$V_{\text{BK_UV}}$	Buck regulator undervoltage lockout	V_{BK} rising, BUCK_SEL = 00b	2.7	2.8	2.9	V
		V_{BK} falling, BUCK_SEL = 00b	2.5	2.6	2.7	V
		V_{BK} rising, BUCK_SEL = 01b	4.3	4.4	4.5	V
		V_{BK} falling, BUCK_SEL = 01b	4.1	4.2	4.3	V
		V_{BK} rising, BUCK_SEL = 10b	2.7	2.8	2.9	V
		V_{BK} falling, BUCK_SEL = 10b	2.5	2.6	2.7	V
		V_{BK} rising, BUCK_SEL = 11b	4.3	4.4	4.5	V
		V_{BK} falling, BUCK_SEL = 11b	4.1	4.2	4.3	V
$V_{\text{BK_UV_HYS}}$	Buck regulator undervoltage lockout hysteresis	Rising to falling threshold		200		mV
$I_{\text{BK_CL}}$	Buck regulator Current limit threshold	BUCK_CL = 0b		600	900	mA
		BUCK_CL = 1b		150		mA
$I_{\text{BK_OCP}}$	Buck regulator Overcurrent protection trip point		2	3	4	A
$t_{\text{BK_RETRY}}$	Overcurrent protection retry time			1		ms
DRIVER OUTPUTS						
$R_{\text{DS(ON)}}$	Total MOSFET on resistance (High-side + Low-side)	$V_{\text{VM}} > 6$ V, $I_{\text{OUT}} = 1$ A, $T_A = 25^{\circ}\text{C}$		95	125	m Ω
		$V_{\text{VM}} < 6$ V, $I_{\text{OUT}} = 1$ A, $T_A = 25^{\circ}\text{C}$		105	130	m Ω
		$V_{\text{VM}} > 6$ V, $I_{\text{OUT}} = 1$ A, $T_J = 150^{\circ}\text{C}$		140	185	m Ω
		$V_{\text{VM}} < 6$ V, $I_{\text{OUT}} = 1$ A, $T_J = 150^{\circ}\text{C}$		145	190	m Ω
SR	Phase pin slew rate switching low to high (Rising from 20 % to 80 %)	$V_{\text{VM}} = 24$ V, SLEW = 00b		25		V/us
		$V_{\text{VM}} = 24$ V, SLEW = 01b		50		V/us
		$V_{\text{VM}} = 24$ V, SLEW = 10b		125		V/us
		$V_{\text{VM}} = 24$ V, SLEW = 11b		200		V/us
SR	Phase pin slew rate switching high to low (Falling from 80 % to 20 %)	$V_{\text{VM}} = 24$ V, SLEW = 00b		25		V/us
		$V_{\text{VM}} = 24$ V, SLEW = 01b		50		V/us
		$V_{\text{VM}} = 24$ V, SLEW = 10b		125		V/us
		$V_{\text{VM}} = 24$ V, SLEW = 11b		200		V/us
t_{DEAD}	Output dead time (high to low / low to high)	$V_{\text{VM}} = 24$ V, SR = 00b, HS driver ON to LS driver OFF		2500	3400	ns
		$V_{\text{VM}} = 24$ V, SR = 01b, HS driver ON to LS driver OFF		1200	1550	ns
		$V_{\text{VM}} = 24$ V, SR = 10b, HS driver ON to LS driver OFF		750	1000	ns
		$V_{\text{VM}} = 24$ V, SR = 11b, HS driver ON to LS driver OFF		500	750	ns
SPEED INPUT - PWM MODE						
$V_{\text{DIG_IH}}$	PWM input high voltage		0.65*AV DD			V
$V_{\text{DIG_IL}}$	PWM input low voltage		0.25*AV DD			V
f_{PWM}	PWM input frequency		0.01		100	kHz

$T_J = -40^{\circ}\text{C}$ to $+150^{\circ}\text{C}$, $V_{VM} = 4.5$ to 35 V (unless otherwise noted). Typical limits apply for $T_A = 25^{\circ}\text{C}$, $V_{VM} = 24\text{ V}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Res _{PWM}	PWM input resolution	f _{PWM} = 0.01 to 8 kHz		12		bits
		f _{PWM} = 8 to 16 kHz		11		bits
		f _{PWM} = 16 to 32 kHz		10		bits
		f _{PWM} = 32 to 64 kHz		9		bits
		f _{PWM} = 64 to 100 kHz		8		bits
SPEED INPUT - ANALOG MODE						
V _{ANA_FS}	Analog full-speed voltage		2.9	3	3.1	V
R _{in(SPEED)}	Speed pin input impedance	Sleep Mode	30			MΩ
R _{in(SPEED)}	Speed pin input impedance	Active Mode	20			MΩ
V _{ANA_RES}	Analog voltage resolution			732		μV
SLEEP MODE						
V _{EN_SL}	Analog voltage to enter sleep mode	ANA_PWM_SPD_SET = 0b (analog mode)			100	mV
V _{EX_SL}	Analog voltage to exit sleep mode	ANA_PWM_SPD_SET = 0b (analog mode)	2.2			V
t _{EX_SL_ANA}	Time needed to detect wake up signal on SPEED pin	ANA_PWM_SPD_SET = 0b (analog mode) V _{SPEED} > V _{EX_SL}	0.5	1	1.5	μs
t _{EX_SL_PWM}		ANA_PWM_SPD_SET = 1b (PWM mode) V _{SPEED} > V _{DIG_IH}	0.5	1	1.5	μs
t _{EX_SL_DR_ANA}	Time taken to drive motor after exiting from sleep mode	ANA_PWM_SPD_SET = 0b (analog mode) V _{SPEED} > V _{EN_SL} , ISD_EN = 0 (ISD disabled)		30		ms
t _{EX_SL_DR_PWM}		ANA_PWM_SPD_SET = 1b (PWM mode) V _{SPEED} > V _{DIG_IH} , ISD_EN = 0 (ISD disabled)		30		ms
t _{EN_SL_ANA}	Time needed to enter sleep mode	ANA_PWM_SPD_SET = 0b (analog mode) V _{SPEED} < V _{EN_SL}		20		ms
t _{EN_SL_PWM}		ANA_PWM_SPD_SET = 1b (PWM mode) V _{SPEED} < V _{DIG_IL}		20		ms
STANDBY MODE						
V _{EN_SB}	Analog voltage to enter standby mode	ANA_PWM_SPD_SET = 0b (analog mode)			100	mV
V _{EX_SB}	Analog voltage to exit standby mode	ANA_PWM_SPD_SET = 0b (analog mode)	170			mV
t _{EX_SB_ANA}	Time needed to detect speed command on SPEED pin	ANA_PWM_SPD_SET = 0b (analog mode) V _{SPEED} > V _{EX_SB}	0.5	1	1.5	ms
t _{EX_SB_PWM}		ANA_PWM_SPD_SET = 1b (PWM mode) V _{SPEED} > V _{DIG_IH}	0.5	1	1.5	μs
t _{EX_SB_DR_ANA}	Time taken to drive motor after exiting standby mode	ANA_PWM_SPD_SET = 0b (analog mode) V _{SPEED} > V _{EN_SL} , ISD_EN = 0b (ISD disabled)		30		ms
t _{EX_SB_DR_PWM}		ANA_PWM_SPD_SET = 1b (PWM mode) V _{SPEED} > V _{DIG_IH} , ISD_EN = 0b (ISD disabled)		30		ms

$T_J = -40^{\circ}\text{C}$ to $+150^{\circ}\text{C}$, $V_{VM} = 4.5$ to 35 V (unless otherwise noted). Typical limits apply for $T_A = 25^{\circ}\text{C}$, $V_{VM} = 24$ V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{EN_SB_ANA}$	Time needed to enter standby mode	ANA_PWM_SPD_SET = 0b (analog mode) $V_{SPEED} < V_{EN_SB}$		20		ms
$t_{EN_SB_PWM}$		ANA_PWM_SPD_SET = 1b (PWM mode) $V_{SPEED} < V_{DIG_IL}$		20		ms
LOW SPEED LOGIC-LEVEL INPUTS (SCL, SDA, SPEED, DIR, etc)						
V_{IL}	Input logic low voltage	AVDD = 3 to 5.5 V			$0.25 \cdot AV_{DD}$	V
V_{IH}	Input logic high voltage	AVDD = 3 to 5.5 V	$0.65 \cdot AV_{DD}$			V
V_{HYS}	Input hysteresis		110	500	800	mV
I_{IL}	Input logic low current	AVDD = 3 to 5.5 V	0		0.1	μA
I_{IH}	Input logic high current	AVDD 3 to 5.5 V	-0.2		0	μA
OPEN-DRAIN OUTPUTS (nFAULT, FG, etc)						
V_{OL}	Output logic low voltage	$I_{OD} = -5$ mA			0.4	V
I_{OZ}	Output logic high current	$V_{OD} = 5$ V	0		0.5	μA
I²C Serial Interface						
V_{I2C_L}	LOW-level input voltage		-0.5		$0.3 \cdot AV_{DD}$	V
V_{I2C_H}	HIGH-level input voltage		$0.7 \cdot AV_{DD}$		5.5	V
V_{I2C_HYS}	Hysterisis		$0.05 \cdot AV_{DD}$			V
V_{I2C_OL}	LOW-level output voltage	open-drain at 2mA sink current	0		0.4	V
I_{I2C_OL}	LOW-level output current	$V_{I2C_OL} = 0.6$ V			6	mA
I_{I2C_IL}	Input current on SDA and SCL		-10		10	μA
C_i	Capacitance for SDA and SCL				10	pF
t_{of}	Output fall time from $V_{I2C_H}(\text{min})$ to $V_{I2C_L}(\text{max})$	Standard Mode			250	ns
		Fast Mode			250	ns
t_{SP}	Pulse width of spikes that must be suppressed by the input filter	Fast Mode	0		50	ns
EEPROM						
EE_{Prog}	Programing voltage		1.35	1.5	1.65	V
EE_{RET}	Retention	$T_A = 25^{\circ}\text{C}$		100		Years
		$T_J = -40$ to 150°C	10			Years
EE_{END}	Endurance	$T_J = -40$ to 150°C	1000			Cycles
		$T_J = -40$ to 85°C	20000			Cycles
OSCILLATOR						
f_{oscXT}	External crystal oscillator			32.768		kHz
f_{oscXT_TOL}	Crystal oscillator frequency tolerance	$T_A = 25$ C	-20		+20	ppm
f_{oscXT_CL}	Crystal oscillator load capacitance				12	pF
f_{oscXT_CS}	Crystal oscillator shunt capacitance				2.5	pF

$T_J = -40^{\circ}\text{C}$ to $+150^{\circ}\text{C}$, $V_{VM} = 4.5$ to 35 V (unless otherwise noted). Typical limits apply for $T_A = 25^{\circ}\text{C}$, $V_{VM} = 24$ V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{OSCREF}	External clock reference	EXT_CLK_CONFIG = 000b		8		kHz
		EXT_CLK_CONFIG = 001b		16		kHz
		EXT_CLK_CONFIG = 010b		32		kHz
		EXT_CLK_CONFIG = 011b		64		kHz
		EXT_CLK_CONFIG = 100b		128		kHz
		EXT_CLK_CONFIG = 101b		256		kHz
		EXT_CLK_CONFIG = 110b		512		kHz
		EXT_CLK_CONFIG = 111b		1024		kHz

$T_J = -40^\circ\text{C}$ to $+150^\circ\text{C}$, $V_{VM} = 4.5$ to 35 V (unless otherwise noted). Typical limits apply for $T_A = 25^\circ\text{C}$, $V_{VM} = 24$ V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PROTECTION CIRCUITS						
V_{UVLO}	Supply undervoltage lockout (UVLO)	VM rising	4.3	4.4	4.5	V
		VM falling	4.1	4.2	4.3	V
V_{UVLO_HYS}	Supply undervoltage lockout hysteresis	Rising to falling threshold	140	200	350	mV
t_{UVLO}	Supply undervoltage deglitch time		3	5	7	μs
V_{OVP}	Supply overvoltage protection (OVP)	Supply rising, OVP_EN = 1, OVP_SEL = 0	32.5	34	35	V
		Supply falling, OVP_EN = 1, OVP_SEL = 0	31.8	33	34.3	V
		Supply rising, OVP_EN = 1, OVP_SEL = 1	20	22	23	V
		Supply falling, OVP_EN = 1, OVP_SEL = 1	19	21	22	V
V_{OVP_HYS}	Supply overvoltage protection (OVP)	Rising to falling threshold, OVP_SEL = 1	0.9	1	1.1	V
		Rising to falling threshold, OVP_SEL = 0	0.7	0.8	0.9	V
t_{OVP}	Supply overvoltage deglitch time			5		μs
V_{CPUV}	Charge pump undervoltage lockout (above VM)	Supply rising		2.5		V
		Supply falling		2.4		V
V_{CPUV_HYS}	Charge pump UVLO hysteresis	Rising to falling threshold		100		mV
V_{AVDD_UV}	Analog regulator undervoltage lockout	Supply rising	2.7	2.85	3	V
		Supply falling	2.5	2.65	2.8	V
$V_{AVDD_UV_HYS}$	Analog regulator undervoltage lockout hysteresis	Rising to falling threshold		200		mV
V_{DVDD_UVLO}	Digital regulator undervoltage lockout (DVDD-UVLO)	Supply rising	1.2	1.25	1.32	V
		Supply falling	1.05	1.15	1.25	V
$V_{DVDD_UVLO_HYS}$	Digital regulator UVLO hysteresis	Rising to falling threshold	90	100	130	mV
I_{OCP}	Overcurrent protection trip point	OCP_LVL = 0b	10	16	20	A
		OCP_LVL = 1b	15	24	28	A
I_{OCP}	Overcurrent protection trip point (HW Device)	OCP pin tied to AGND	10	16	21.5	A
I_{OCP}		OCP pin tied to AVDD	15	24	31	A
t_{OCP}	Overcurrent protection deglitch time	OCP_DEG = 00b		0.2		μs
		OCP_DEG = 01b		0.6		μs
		OCP_DEG = 10b		1.1		μs
		OCP_DEG = 11b		1.6		μs
t_{RETRY}	Overcurrent protection retry time	OCP_RETRY = 0		5		ms
		OCP_RETRY = 1		500		ms
T_{OTW}	Thermal warning temperature	Die temperature (T_J)	135	145	160	$^\circ\text{C}$
T_{OTW_HYS}	Thermal warning hysteresis	Die temperature (T_J)		25		$^\circ\text{C}$
T_{TSD}	Thermal shutdown temperature	Die temperature (T_J)	150	160	175	$^\circ\text{C}$
T_{TSD_HYS}	Thermal shutdown hysteresis	Die temperature (T_J)		25		$^\circ\text{C}$
TOTW	Thermal Warning Temperature Controller		115	145	160	$^\circ\text{C}$
TOTW_HYS	Thermal Warning Hysteresis Controller			25		$^\circ\text{C}$

(1) R_{LBK} is resistance of inductor L_{BK}

6.6 Characteristics of the SDA and SCL bus for Standard and Fast mode

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
Fast-mode						
f_{SCL}	SCL clock frequency		0		400	KHz
t_{HD_STA}	Hold time (repeated) START condition	After this period, the first clock pulse is generated	0.6			μ s
t_{LOW}	LOW period of the SCL clock		1.3			μ s
t_{HIGH}	HIGH period of the SCL clock		0.6			μ s
t_{SU_STA}	Set-up time for a repeated START condition		0.6			μ s
t_{HD_DAT}	Data hold time ⁽¹⁾		0 ⁽²⁾		⁽³⁾	μ s
t_{SU_DAT}	Data set-up time		100 ⁽⁴⁾			ns
t_r	Rise time for both SDA and SCL signals		20		300	ns
t_f	Fall time of both SDA and SCL signals ⁽²⁾ ^{(5) (6) (7)}		20 x ($V_{AVDD}/$ 5.5V)		300	ns
t_{SU_STO}	Set-up time for STOP condition		0.6			μ s
t_{BUF}	Bus free time between STOP and START condition		1.3			μ s
C_b	Capacitive load for each bus line ⁽⁸⁾				400	pF
t_{VD_DAT}	Data valid time ⁽⁹⁾				0.9 ⁽³⁾	μ s
t_{VD_ACK}	Data valid acknowledge time ⁽¹⁰⁾				0.9 ⁽³⁾	μ s
V_{nL}	Noise margin at the LOW level	For each connected device (including hysteresis)	0.1*AVD D			V
V_{nh}	Noise margin at the HIGH level	For each connected device (including hysteresis)	0.2*AVD D			V

- (1) t_{HD_DAT} is the data hold time that is measured from the falling edge of SCL, applies to data in transmission and the acknowledge.
- (2) A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the $V_{IH(min)}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- (3) The maximum t_{HD_DAT} could be 3.45 μ s and .9 μ s for Standard-mode and Fast-mode, but must be less than the maximum of t_{VD_DAT} or t_{VD_ACK} by a transition time. This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretched the SCL, the data must be valid by the set-up time before it releases the clock.
- (4) A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement t_{SU_DAT} 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU_DAT} = 1000 + 250 = 1250$ ns (according to the Standard-mode I2C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.
- (5) If mixed with Hs-mode devices, faster fall times according to Table 10 are allowed.
- (6) The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f .
- (7) In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.
- (8) The maximum bus capacitance allowable may vary from the value depending on the actual operating voltage and frequency of the application.
- (9) t_{VD_DAT} = time for data signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).
- (10) t_{VD_ACK} = time for Acknowledgement signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).

7 Detailed Description

7.1 Overview

The MCF8316A provides a single-chip code-free sensorless FOC solution for customers driving speed-controlled 12- to 24-V brushless-DC motors with 8-A peak current capability.

The MCF8316A integrates three 1/2-H bridges with 40-V absolute maximum capability and a very low RDS(ON) of 95mOhms (high-side plus low-side) to enable high power drive capability. Current is sensed using an integrated current sensing feature which eliminates the need for external sense resistors. Power management features of an adjustable buck regulator and LDO generate the necessary voltage rails for the device and can be used to power external circuits.

MCF8316A implements Sensorless FOC, and so an external microcontroller is not required to spin the brushless-DC motor. The algorithm is implemented in a fixed-function state machine, so no coding is needed. The algorithm is highly configurable through register settings ranging from motor start-up behavior to closed loop operation. Register settings can be set in non-volatile EEPROM, which allows the device to operate stand-alone once it has been configured. MCF8316A allows for a high level monitoring; any variable in the algorithm can be displayed and observed as an analog output via two DACs. This feature provides an effective method to tune speed loops as well as motor acceleration. The device receives a speed command through a PWM input, analog voltage, or I2C command.

These features include power-supply undervoltage lockout (UVLO), charge-pump undervoltage lockout (CPUV), overcurrent protection (OCP), AVDD undervoltage lockout (AVDD_UV), buck regulator ULVO, motor lock detection and overtemperature shutdown (OTW and OTSD). Fault events are indicated by the nFAULT pin with detailed information available in the registers.

The MCF8316A device is available in 0.5-mm pin pitch, VQFN surface-mount packages. The VQFN package size is 7 mm × 5 mm and 1 mm height.

7.2 Functional Block Diagram

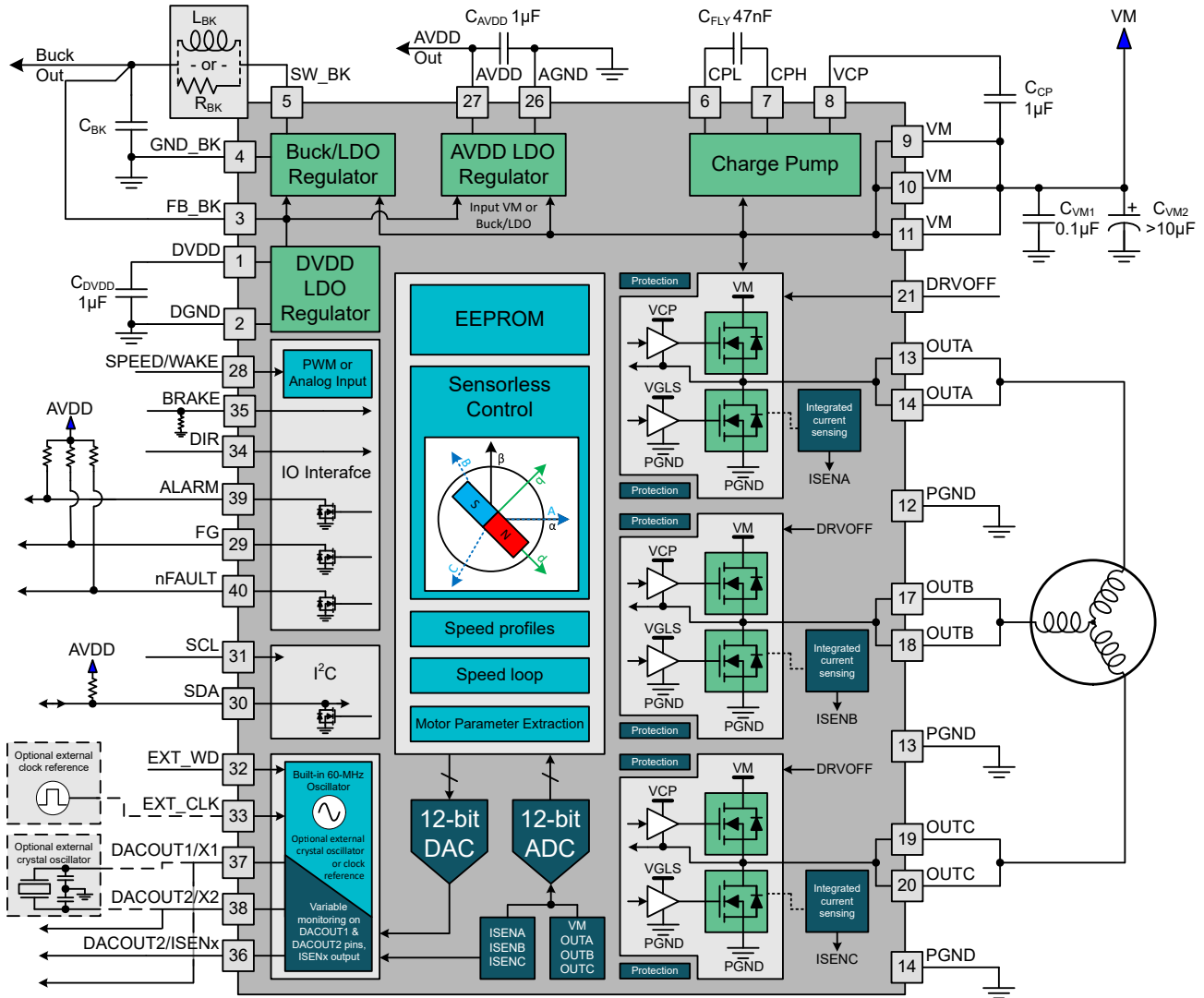


Figure 7-1. MCF8316A Block Diagram

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7.3 Feature Description

7.3.1 Output Stage

The MCF8316A device consists of an integrated 95-mΩ (combined high-side and low-side FET's on-state resistance) NMOS FET's connected in a three-phase bridge configuration. A doubler charge pump provides the proper gate-bias voltage to the high-side NMOS FET's across a wide operating-voltage range in addition to providing 100% duty-cycle support. An internal linear regulator provides the gate-bias voltage for the low-side MOSFETs.

7.3.2 Device Interface Modes

The MCF8316A supports I²C interface to let the end application design for either flexibility or simplicity. MCF8316A allows controlling the motor operation and system through inputs which are BRAKE, DRVOFF, DIR, EXT_CLK, SPEED/WAKE, X1 and X2. MCF8316A also provides different signals used for monitoring speed and fault monitoring through output which are DACOUT1, DACOUT2, FG, nFAULT and SOx .

7.3.2.1 Interface - Control and Monitoring

Motor Control Signals

- When BRAKE pin is driven active 'High' MCF8316A enters brake state. Brake state can be configured to either low side braking (see [Low Side Braking](#)) or align brake (see [Align Braking](#)) configured through BRAKE_PIN_MODE. MCF8316A decreases output speed to value defined by BRAKE_SPEED_THRESHOLD before entering brake state. As long as BRAKE is driving active 'High', MCF8316A stays in brake state. Brake pin input can be overwritten by configuring BRAKE_INPUT over the I²C interface.
- The DIR pin decides the direction of motor spin, when driven active HIGH the sequence is OUT A → OUT B → OUT C, and when driven 'LOW' the sequence is OUT A → OUT C → OUT B. DIR pin input can be overwritten by configuring DIR_INPUT over the I²C interface.
- When DRVOFF pin is driven active 'High', MCF8316A stops driving the motor by turning OFF all MOSFETs (coast state). When DRVOFF is released, MCF8316A returns to normal state of operation, as if it was restarting motor (see [DRVOFF functionality](#)). DRVOFF does not cause the device to go to sleep or standby mode; the digital core is still active. Entry and exit from sleep or standby condition is still controlled by SPEED pin.
- SPEED/WAKE pin is used to control motor speed and wake up MCF8316A from sleep mode. SPEED pin can be configured to accept PWM or analog input signals. It is used to enter and exit from sleep and standby mode (see [Table 7-6](#)).

Oscillator Control Signals (Optional)

- EXT_CLK pin may be used to provide an external clock reference (see [External Clock Source](#)).

Output Signals

- DACOUT1 outputs internal variable defined by address in register DACOUT1_VAR_ADDR, the output of DACOUT1 is refreshed every PWM cycle (see [DAC output](#))
- DACOUT2 outputs internal variable defined by address in register DACOUT2_VAR_ADDR, the output of DACOUT2 is refreshed every PWM cycle (see [DAC output](#))
- FG pins outputs pulses which are proportional to speed of motor (see [FG Customized Configuration](#))
- nFAULT pins outputs status of fault in device or motor operation.
- SOx pins provide the output of one of the current sense amplifier.

7.3.2.2 I²C Interface

The serial interface device MCF8316A support I²C serial communication bus that lets an external controller send and receive data with MCF8316A. This support lets the external controller configure EEPROM and read detailed fault and motor state information. The interface is a 2 wire interface using the SCL and SDA pins which are described as follows:

- The SCL pin is clock signal input.
- The SDA pin is the data input and output.

7.3.3 Step-Down Mixed-Mode Buck Regulator

The MCF8316A has an integrated mixed-mode buck regulator in conjunction with AVDD to supply regulated 3.3 V or 5.0 V power for an external controller or system voltage rail. Additionally, the buck output can also be configured to 4.0 V or 5.7 V for supporting the extra headroom for external LDO for generating a 3.3 V or 5.0 V supplies. The output voltage of the buck is set by BUCK_SEL.

The buck regulator has a low quiescent current of ~1-2 mA during light loads to prolong battery life. The device improves performance during line and load transients by implementing a pulse-frequency current-mode control scheme which requires less output capacitance and simplifies frequency compensation design.

Table 7-1. Recommended settings for Buck Regulator

Buck Mode	Buck output voltage	Max output current from AVDD (I_{AVDD})	Max output current from Buck (I_{BK})	Buck current limit	AVDD power sequencing
Inductor - 47 μ H	3.3 V or 4.0 V	20 mA	170 mA - I_{AVDD}	600 mA (BUCK_CL = 0b)	Not supported (BUCK_PS_DIS = 1)
Inductor - 47 μ H	5.0 V or 5.7 V	20 mA	170 mA - I_{AVDD}	600 mA (BUCK_CL = 0b)	Supported (BUCK_PS_DIS = 0)
Inductor - 22 μ H	5.0 V or 5.7 V	20 mA	20 mA - I_{AVDD}	150 mA (BUCK_CL = 1b)	Not supported (BUCK_PS_DIS = 1)
Inductor - 22 μ H	3.3 V or 4.0 V	20 mA	20 mA - I_{AVDD}	150 mA (BUCK_CL = 1b)	Supported (BUCK_PS_DIS = 0)
Resistor - 22 μ H	5.0 V or 5.7 V	20 mA	10 mA - I_{AVDD}	150 mA (BUCK_CL = 1b)	Not supported (BUCK_PS_DIS = 1)
Resistor - 22 μ H	3.3 V or 4.0 V	20 mA	10 mA - I_{AVDD}	150 mA (BUCK_CL = 1b)	Supported (BUCK_PS_DIS = 0)

7.3.3.1 Buck in Inductor Mode

The buck regulator in MCF8316A device is primarily designed to support low inductance of 47 μ H and 22 μ H inductors. A 47 μ H inductor allows the buck regulator to operate up to 170 mA load current support, whereas applications requiring current up to 20 mA can use a 22- μ H inductor which saves component size.

Figure 7-2 shows the connection of buck regulator in inductor mode.

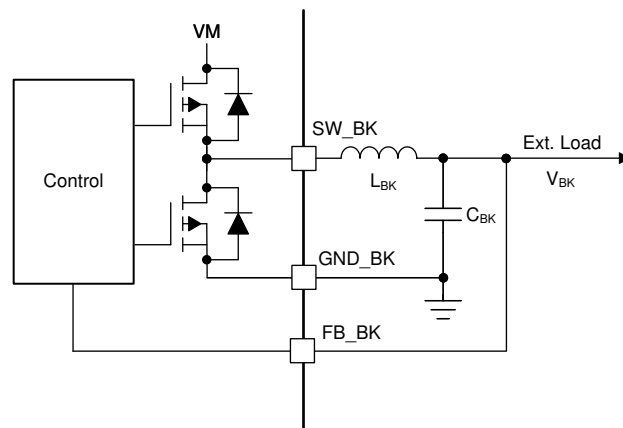


Figure 7-2. Buck (Inductor Mode)

7.3.3.2 Buck in Resistor mode

If the external load requirements is less than 10mA, the inductor can be replaced with a resistor. In resistor mode the power is dissipated across the external resistor and the efficiency is lower than buck in inductor mode.

Figure 7-3 shows the connection of buck in resistor mode.

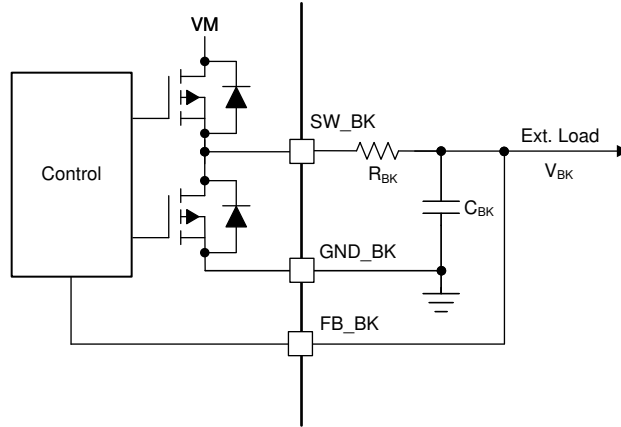


Figure 7-3. Buck (Resistor Mode)

7.3.3.3 Buck Regulator with External LDO

The buck regulator also supports the voltage requirement to fed to external LDO to generate standard 3.3 V or 5.0 V output rail with higher accuracies. The buck output voltage should be configured to 4 V or 5.5 V to provide for a extra headroom to support the external LDO for generating 3.3 V or 5 V rail as shown in [Figure 7-4](#). This allows for a lower-voltage LDO design to save cost and better thermal management due to low drop-out voltage.

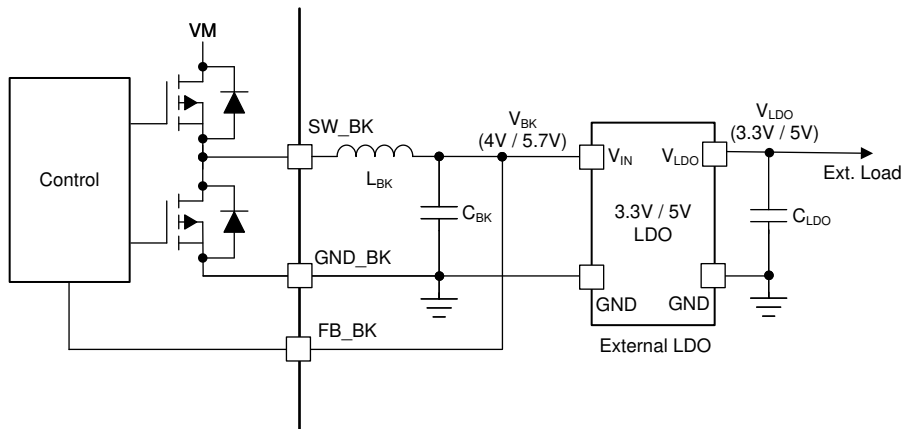


Figure 7-4. Buck Regulator with External LDO

7.3.3.4 AVDD Power Sequencing on Buck Regulator

The AVDD LDO has an option of using the power supply from mixed mode buck regulator to reduce power dissipation internally. The power sequencing mode allows on-the-fly changeover of LDO power supply from DC mains (VM) to buck output (VBK) as shown in [Figure 7-5](#). This sequencing can be configured through the BUCK_PS_DIS bit . Power sequencing is supported only when buck output voltage is set to 5.0 V or 5.7 V.

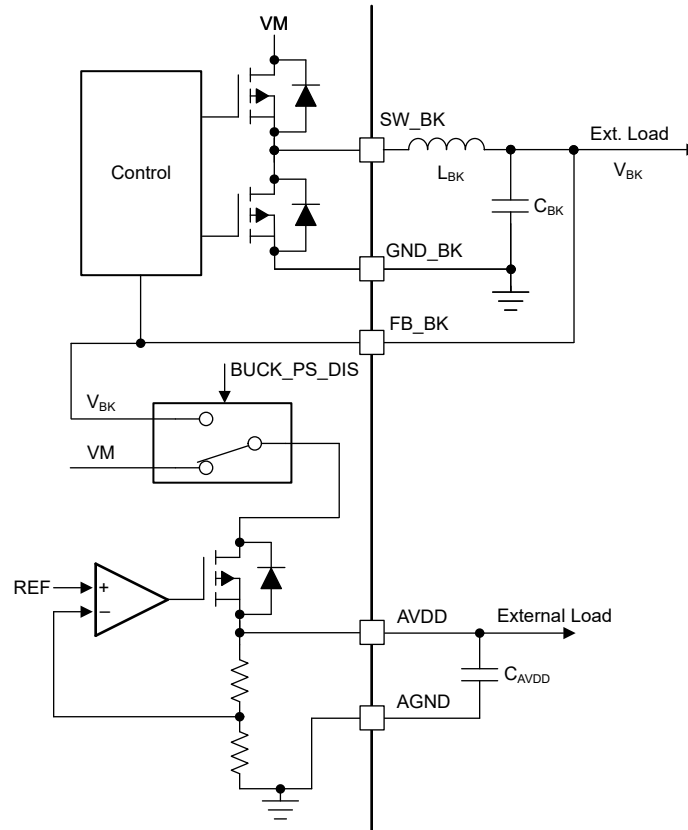


Figure 7-5. AVDD Power Sequencing on mixed mode Buck Regulator

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7.3.3.5 Mixed mode Buck Operation and Control

The buck regulator implements a pulse frequency modulation (PFM) architecture with peak current mode control. The output voltage of the buck regulator is compared with the internal reference voltage (V_{BK_REF}) which is internally generated depending on the buck-output voltage setting (BUCK_SEL) which constitutes an outer voltage control loop. Depending on the comparator output going high ($V_{BK} < V_{BK_REF}$) or low ($V_{BK} > V_{BK_REF}$), the high-side power FET of the buck turns on and turns off respectively. An independent current control loop monitors the current in high-side power FET (I_{BK}) and turns off the high-side FET when the current becomes higher than the buck current limit (I_{BK_CL}). This implements a current limit control for the buck regulator. Figure 7-6 shows the architecture of the buck and various control/protection loops.

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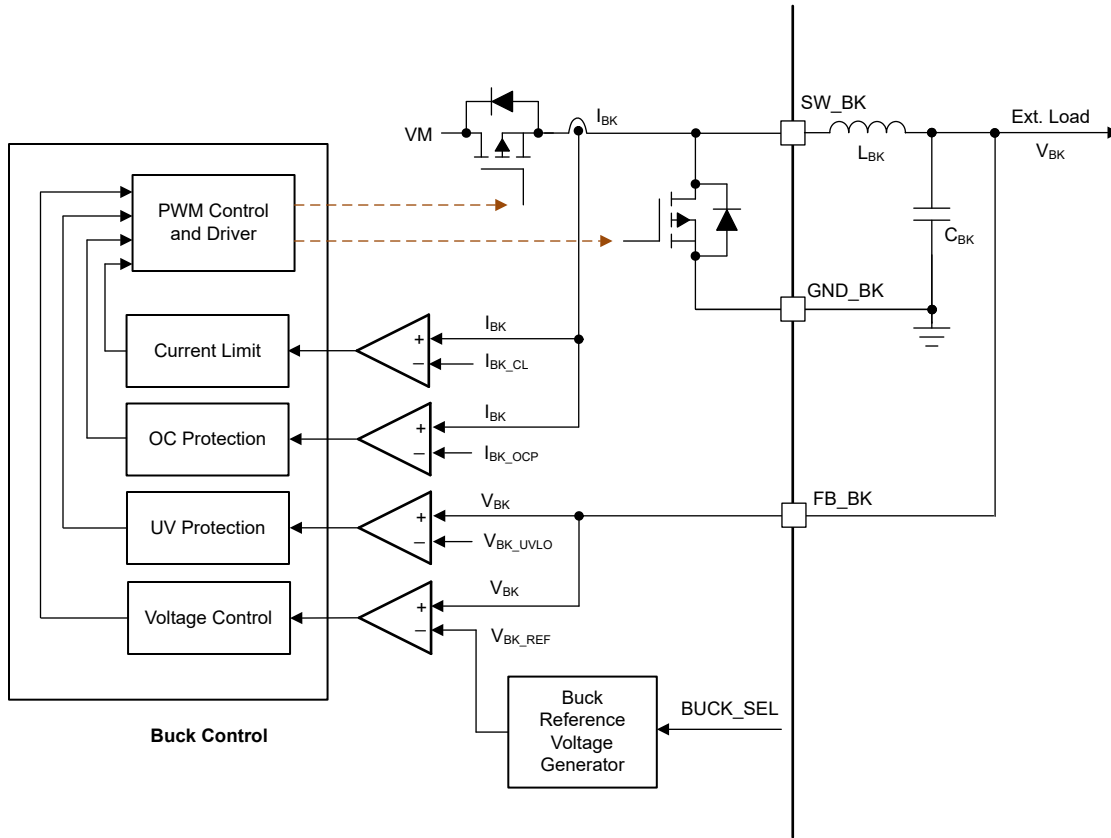


Figure 7-6. Buck Operation and Control Loops

7.3.3.6 Buck Undervoltage Protection

If at any time the input supply voltage on the FB_BK pin falls lower than the V_{BK_UVLO} threshold, both the high-side and low-side MOSFETs of the buck regulator are disabled. Internal circuitry in MCF8316A is powered through buck regulator, MCF8316A goes into reset state whenever buck UV event occurs.

7.3.3.7 Buck Overcurrent Protection

The buck overcurrent event is sensed by monitoring the current flowing through high-side MOSFET of the buck regulator. If the current across high-side MOSFET exceeds the I_{BK_OCP} threshold for longer than the t_{OCP_DEG} deglitch time, a buck OCP event is recognized. Internal circuitry in MCF8316A is powered through buck regulator, MCF8316A goes into reset state whenever buck OCP event occurs.

7.3.4 AVDD Linear Voltage Regulator

A 3.3-V, linear regulator is integrated into the MCF8316A family of devices and is available for use by external circuitry. The AVDD regulator is used for powering up the internal digital circuitry of the device and additionally, this regulator can also provide the supply voltage for a low-power MCU or other circuitry supporting low current (up to 20 mA). The output of the AVDD regulator should be bypassed near the AVDD pin with a X5R or X7R, 10- μ F, 6.3-V ceramic capacitor routed directly back to the adjacent AGND ground pin.

The AVDD nominal, no-load output voltage is 3.3 V.

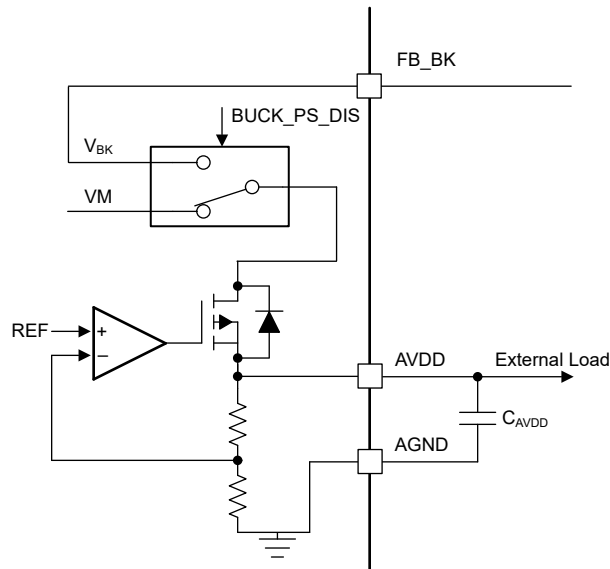


Figure 7-7. AVDD Linear Regulator Block Diagram

Use Equation 1 to calculate the power dissipated in the device by the AVDD linear regulator with VM as supply (BUCK_PD_DIS = 1)

$$P = (V_{VM} - V_{AVDD}) \times I_{AVDD} \quad (1)$$

For example, at a V_{VM} of 24 V, drawing 20 mA out of AVDD results in a power dissipation as shown in Equation 2.

$$P = (24 \text{ V} - 3.3 \text{ V}) \times 20 \text{ mA} = 414 \text{ mW} \quad (2)$$

Use Equation 3 to calculate the power dissipated in the device by the AVDD linear regulator with buck output as supply (BUCK_PD_DIS = 0)

$$P = (V_{FB_BK} - V_{AVDD}) \times I_{AVDD} \quad (3)$$

7.3.5 Charge Pump

Because the output stages use N-channel FETs, the device requires a gate-drive voltage higher than the VM power supply to enhance the high-side FETs fully. The MCF8316A integrates a charge-pump circuit that generates a voltage above the VM supply for this purpose.

The charge pump requires two external capacitors for operation. See the block diagram and pin descriptions for details on these capacitors (value, connection, and so forth).

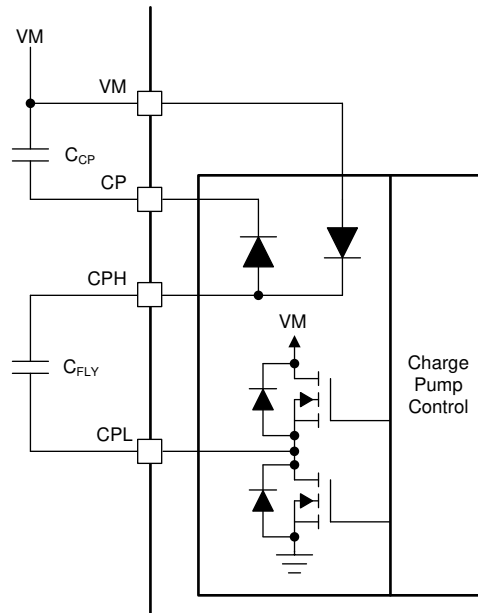


Figure 7-8. Charge Pump

7.3.6 Slew Rate Control

An adjustable gate-drive current control for the MOSFETs in the output stage is implemented to achieve the slew rate control. The MOSFET VDS slew rates are a critical factor for optimizing radiated emissions, total energy and duration of diode recovery spikes and switching voltage transients related to parasitic elements of the PCB. These slew rates are predominantly determined by the control of the internal MOSFET gate current as shown in Figure 7-9.

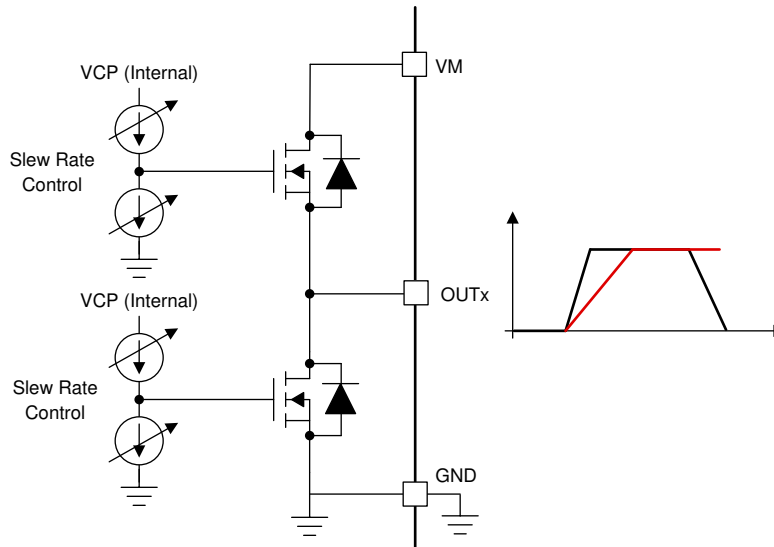


Figure 7-9. Slew Rate Circuit Implementation

The slew rate of each half-bridge can be adjusted through SLEW settings. Slew rate can be configured as 25-V/ μ s, 50-V/ μ s, 125-V/ μ s or 200-V/ μ s. The slew rate is calculated by the rise-time and fall-time of the voltage on OUTx pin as shown in Figure 7-10.

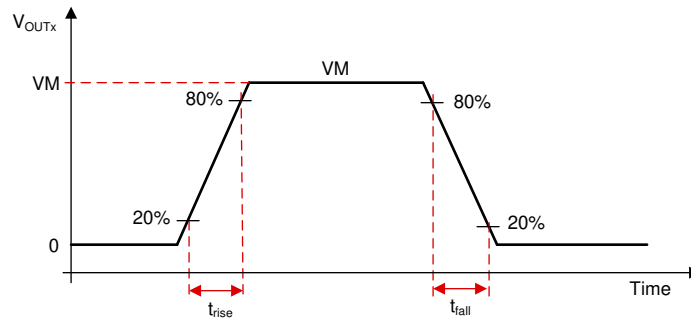


Figure 7-10. Slew Rate Timings

7.3.7 Cross Conduction (Dead Time)

The device is fully protected against any cross conduction of the MOSFETs. The high-side and low-side MOSFETs are carefully controlled to avoid any shoot-through events by inserting a dead time (t_{dead}). This is implemented by sensing the gate-source voltage (VGS) of the high-side and low-side MOSFETs and ensuring that the VGS of high-side MOSFET has reached below turn-off levels before switching on the low-side MOSFET of same half-bridge as shown in Figure 7-11 and Figure 7-12 and vice versa.

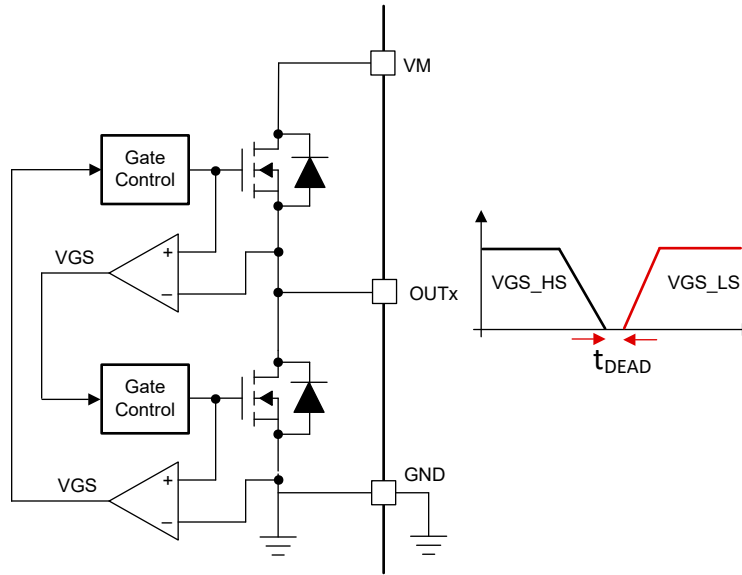


Figure 7-11. Cross Conduction Protection

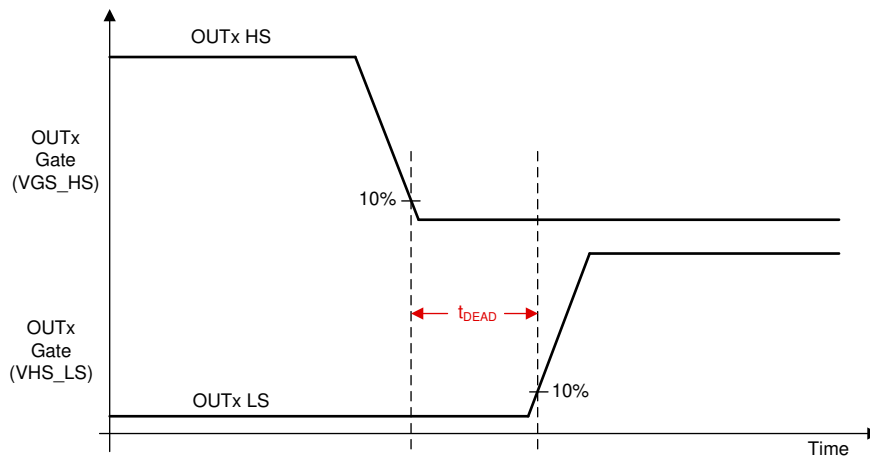


Figure 7-12. Dead Time

7.3.8 SPEED Control

The MCF8316A device offers three methods of directly controlling the speed of the motor. . The speed command can be controlled in one of three ways.

- PWM input on SPEED pin by varying duty cycle of input signal
- Analog input on SPEED pin by varying amplitude of input signal
- Over I²C by configuring DIGITAL_SPEED_CTRL register

The speed can be indirectly controlled by varying the supply voltage (V_M).

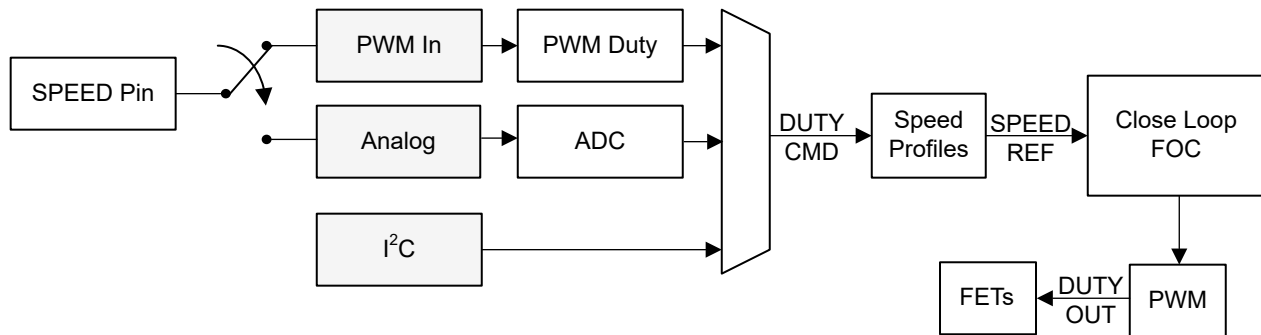


Figure 7-13. Multiplexing the Speed Command

7.3.8.1 Analog-Mode Speed Control

Analog mode can be configured by setting ANA_PWM_SPD_SET to 0b. When configured for analog mode, the voltage range on the SPEED pin can be varied from 0 to V_{ANA_FS} . If $SPEED > V_{ANA_FS}$, the speed command is calmped to maximum. If $0 \leq SPEED < V_{ANA_FS}$, the speed command changes linearly according to the magnitude of the voltage applied at the SPEED pin. If $SPEED < V_{EN_SL}$ device the speed command is set to stop the motor. Figure 7-14 shows the speed command when operating in analog mode.

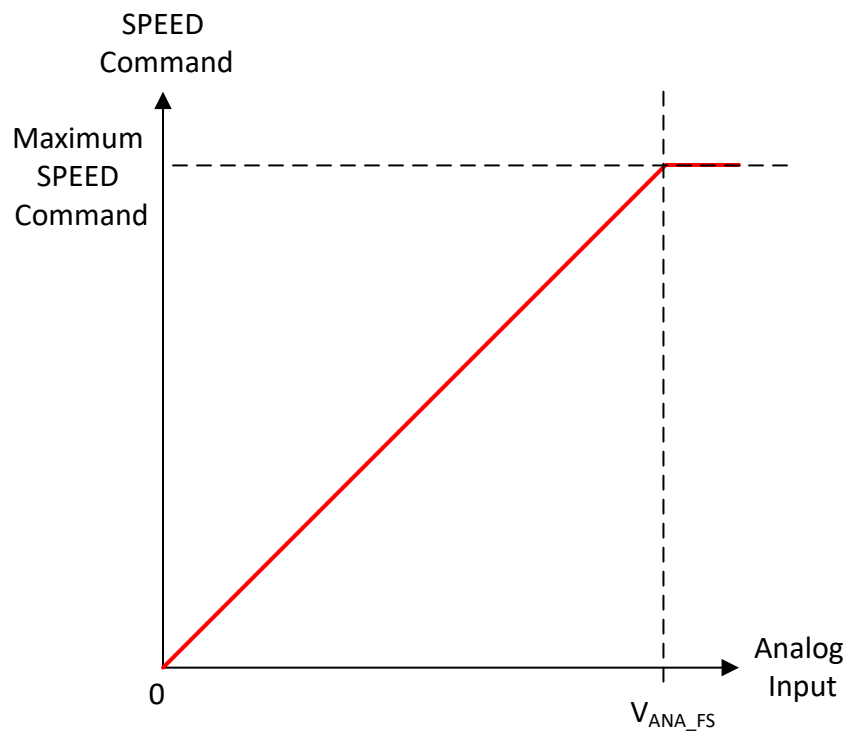


Figure 7-14. Analog-Mode Speed Command

7.3.8.2 PWM-Input Speed Control

PWM mode can be configured by setting ANA_PWM_SPD_SET to 1b. In this mode, the PWM duty cycle applied to the SPEED pin can be varied from 0 to 100%. The speed command is proportional to the PWM input duty cycle. The speed command stops the motor when the PWM input keeps at 0 for $t_{EN_SL_PWM}$ (see [Figure 7-15](#)). The frequency of the PWM input signal applied to the SPEED pin is defined as f_{PWM} and range for this frequency can be configured through SPD_RANGE_SELECT.

Note

f_{PWM} is the frequency the device can accept to control motor speed. It does not correspond to the PWM output frequency that is applied to the motor phase. The PWM output frequency can be configured through PWM_SEL (see [Section 7.3.17](#)).

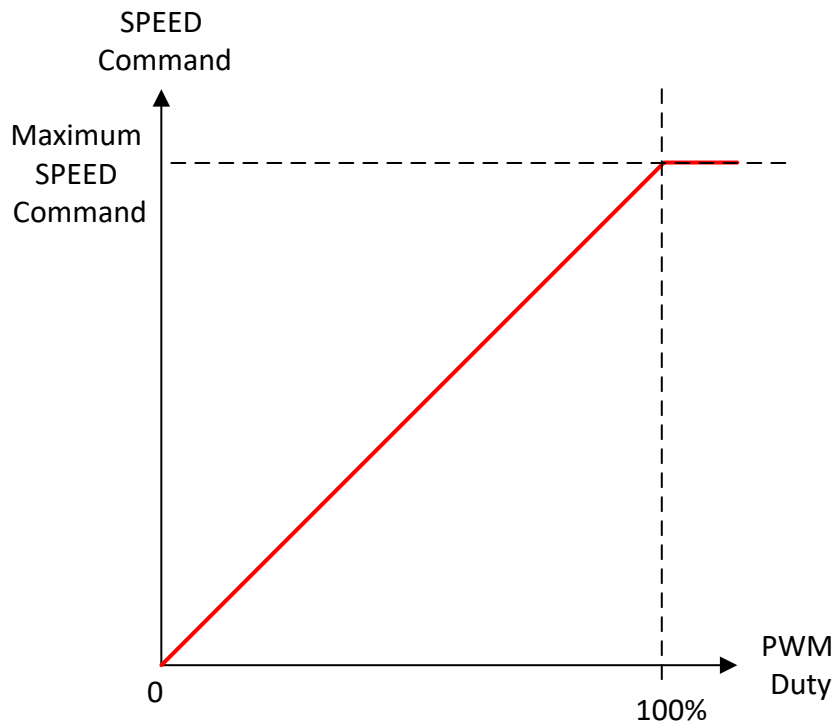


Figure 7-15. PWM-Mode Speed Command

7.3.8.3 Serial-Mode Speed Control

The user can also command the speed through the Serial I2C interface, this mode is configured by setting OVERRIDE to 1. The speed command can be set through DIGITAL_SPEED_CTRL. In this mode, SPEED/WAKE pin can be used to wake up device from sleep state by configuring SPEED_PIN_CONFIG. When wake up signal is applied on SPEED/WAKE pin, MCF8316A puts device in standby state and speed is controlled only through DIGITAL_SPEED_CTRL.

7.3.8.4 Speed Profiles

MCF8316A supports different kind of speed profiles to support different kinds of user commands. There are three kinds of speed profiles supported which can be configured through SPEED_PROFILE_CONFIG.

7.3.8.4.1 Linear Speed Profiles

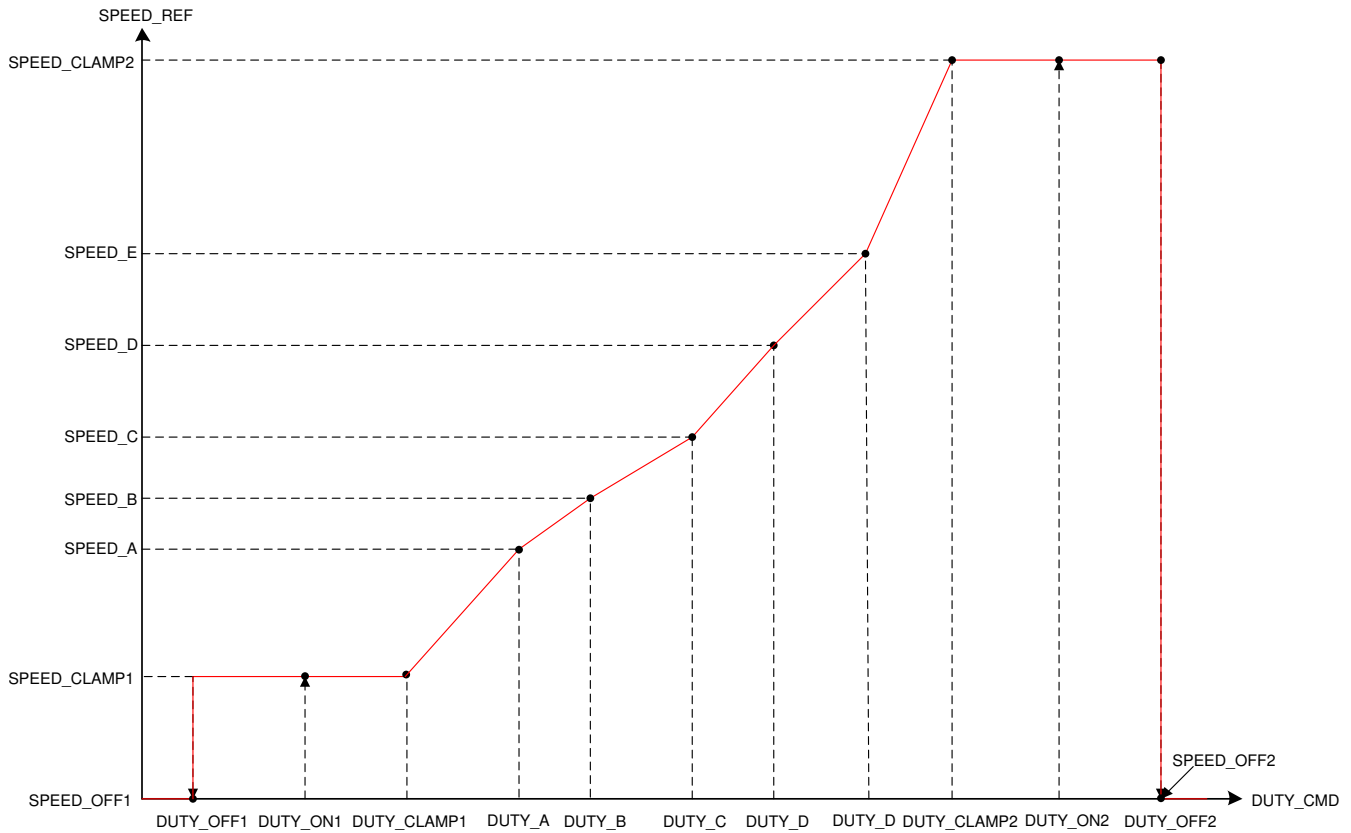


Figure 7-16. Linear Speed Profiles

Linear speed profiles can be configured by setting SPEED_PROFILE_CONFIG to 0b00. Linear speed profiles feature speed references which changes linearly between DUTY_CLAMP1 and DUTY_CLAMP2 with different slopes which can be set by configuring DUTY_x and SPEED_x combination.

- DUTY_OFF1 configures the duty command at which the MCF8316A will be in the off state. SPEED_OFF1 configures the speed reference for a duty command below DUTY_OFF1.
- DUTY_ON1 configures the duty command above which the MCF8316A will be in a normal running state.
- DUTY_CLAMP1 configures the duty command at which speed reference will be constant. SPEED_CLAMP1 configures a constant speed reference between DUTY_CLAMP1 and DUTY_OFF1.
- DUTY_A configures the duty command for speed reference SPEED_A. The speed reference changes linearly between DUTY_CLAMP1 and DUTY_A.
- DUTY_B configures the duty command for speed reference SPEED_B. The speed reference changes linearly between DUTY_A and DUTY_B.
- DUTY_C configures the duty command for speed reference SPEED_C. The speed reference changes linearly between DUTY_B and DUTY_C.
- DUTY_D configures the duty command for speed reference SPEED_D. The speed reference changes linearly between DUTY_C and DUTY_D.
- DUTY_E configures the duty command for speed reference SPEED_E. The speed reference changes linearly between DUTY_D and DUTY_E.
- DUTY_CLAMP2 configures the duty command above which the speed reference will be constant. The speed reference changes linearly between DUTY_E and DUTY_CLAMP2.
- DUTY_OFF2 configures the duty command above which the MCF8316A will be in off state. SPEED_OFF2 configures the speed reference for a duty command above DUTY_OFF2.
- DUTY_ON2 configures the duty command below which the MCF8316A will be in a normal running state.

7.3.8.4.2 Staircase Speed Profiles

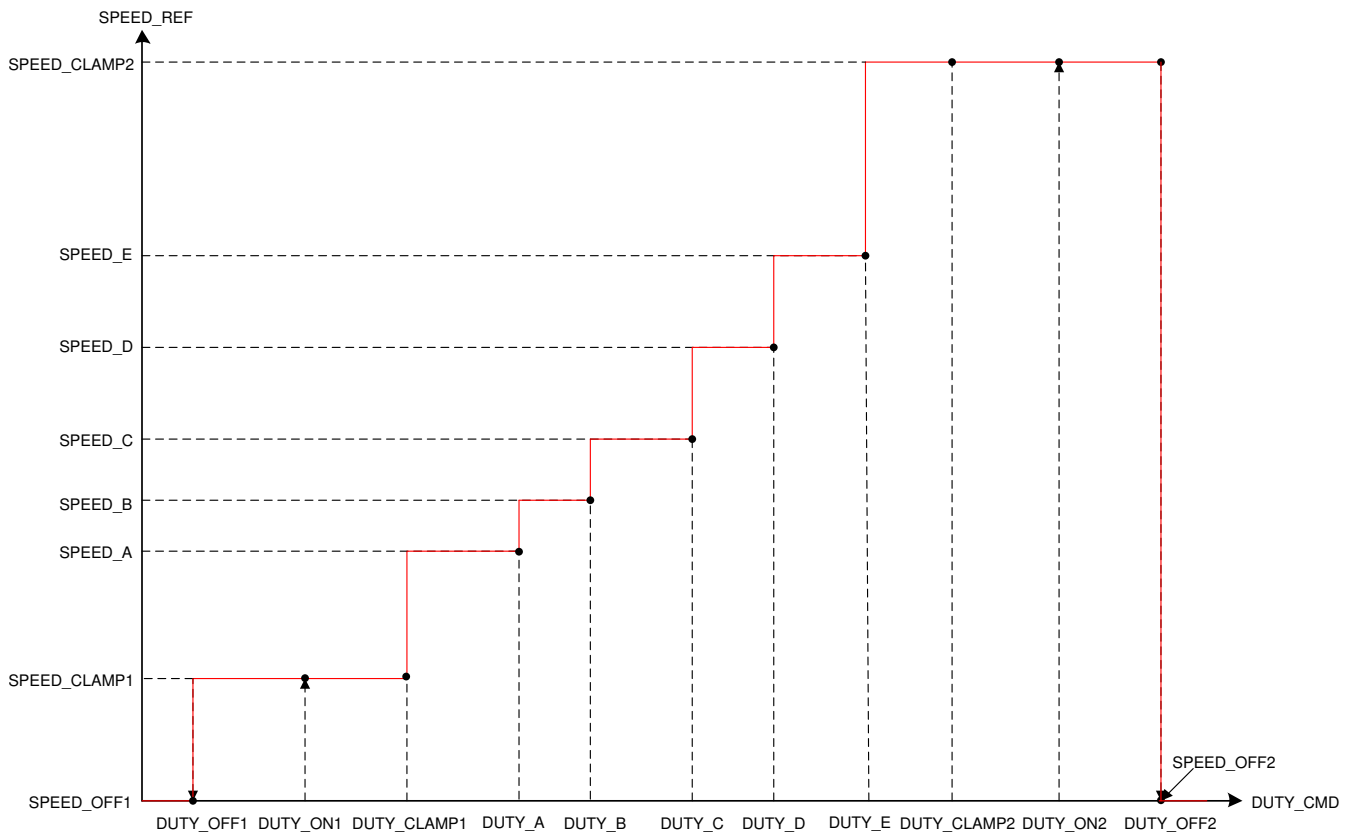


Figure 7-17. Staircase Speed Profiles

Staircase speed profiles can be configured by setting SPEED_PROFILE_CONFIG to 0b01. Staircase speed profiles feature speed changes in steps between DUTY_CLAMP1 and DUTY_CLAMP2. DUTY_x and SPEED_x configures the speed and duty command at which the step is increased

- DUTY_OFF1 configures the duty command at which the MCF8316A will be in the off state. SPEED_OFF1 configures the speed reference for a duty command below DUTY_OFF1.
- DUTY_ON1 configures the duty command above which the MCF8316A will be in a normal running state.
- DUTY_CLAMP1 configures the duty command at which speed reference will be constant. SPEED_CLAMP1 configures a constant speed reference between DUTY_CLAMP1 and DUTY_OFF1.
- DUTY_A configures the duty command for speed reference SPEED_A. The speed reference changes in step between DUTY_CLAMP1 and DUTY_A.
- DUTY_B configures the duty command for speed reference SPEED_B. The speed reference changes in step between DUTY_A and DUTY_B.
- DUTY_C configures the duty command for speed reference SPEED_C. The speed reference changes in step between DUTY_B and DUTY_C.
- DUTY_D configures the duty command for speed reference SPEED_D. The speed reference changes in step between DUTY_C and DUTY_D.
- DUTY_E configures the duty command for speed reference SPEED_E. The speed reference changes in step between DUTY_D and DUTY_E.
- DUTY_CLAMP2 configures the duty command above which the speed reference will be constant. The speed reference changes in step between DUTY_E and DUTY_CLAMP2.
- DUTY_OFF2 configures the duty command above which the MCF8316A will be in the off state. SPEED_OFF2 configures the speed reference for a duty command above DUTY_OFF2.
- DUTY_ON2 configures the duty command below which the MCF8316A will be in a normal running state.

7.3.8.4.3 Forward-Reverse Speed Profiles

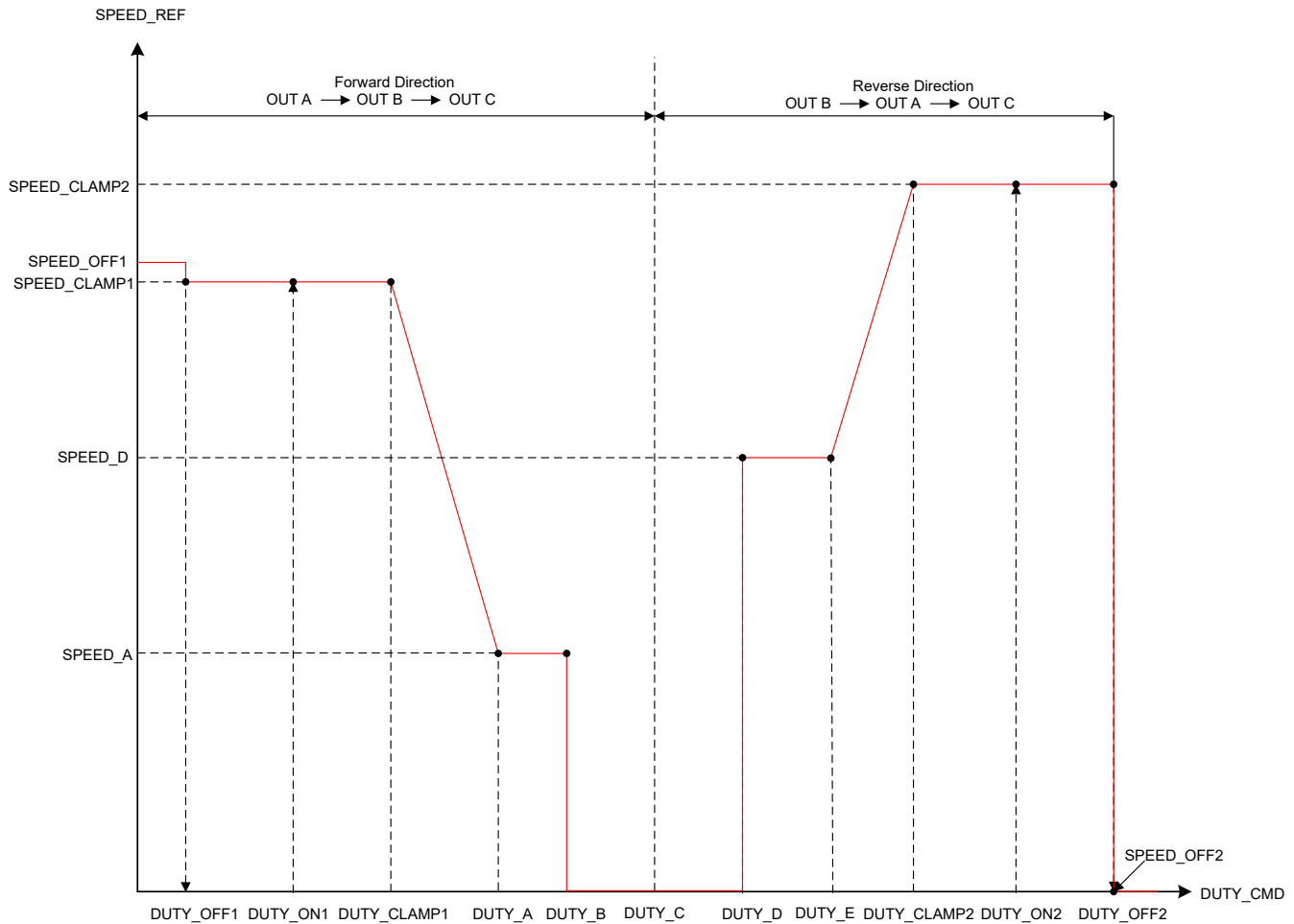


Figure 7-18. Forward Reverse Speed Profiles

Forward-Reverse speed profiles can be configured by setting SPEED_PROFILE_CONFIG to 0b10. Forward-Reverse speed profiles feature direction change through adjusting the input speed command. DUTY_C configures duty command at which the direction will be changed. The Forward-Reverse speed profile can remove the need to use a separate signal to control the motor direction.

- DUTY_OFF1 configures the duty command at which the MCF8316A will be in off state in forward direction. SPEED_OFF1 configures the speed reference for a duty command below DUTY_OFF1.
- DUTY_ON1 configures the duty command above which the MCF8316A will be in a normal running state in forward direction.
- DUTY_CLAMP1 configures the duty command at which speed reference will be the constant in forward direction. SPEED_CLAMP1 configures constant speed reference between DUTY_CLAMP1 and DUTY_OFF1.
- DUTY_A configures the duty command for speed reference SPEED_A. The speed reference changes linearly between DUTY_CLAMP1 and DUTY_A.
- DUTY_B configures the duty command above which the MCF8316A will be in off state in forward direction. The speed reference remains constant between DUTY_A and DUTY_B.
- DUTY_C configures the duty command at which the direction is changed
- DUTY_D configures the duty command above which the MCF8316A will be in a normal running state in reverse direction. SPEED_D configures constant speed reference between DUTY_D and DUTY_E
- DUTY_CLAMP2 configures the duty command above which speed reference will be constant in reverse direction. The speed reference changes linearly between DUTY_D and DUTY_CLAMP2.

- DUTY_OFF2 configures the duty command above which the MCF8316A will be constant in off state in reverse direction. SPEED_OFF2 configures the speed reference for duty command above DUTY_OFF2.
- DUTY_ON2 configures the duty command below which the MCF8316A will be in a normal running state in reverse direction.

7.3.9 Starting the Motor Under Different Initial Conditions

The motor can be in one of three states when the MCF8316A device begins the start-up process. The motor may be stationary, spinning in the forward direction, or spinning in the reverse direction. The MCF8316A device includes a number of features to allow for reliable motor start under all of these conditions. Figure 7-19 shows the motor start-up flow for each of the three initial motor states.

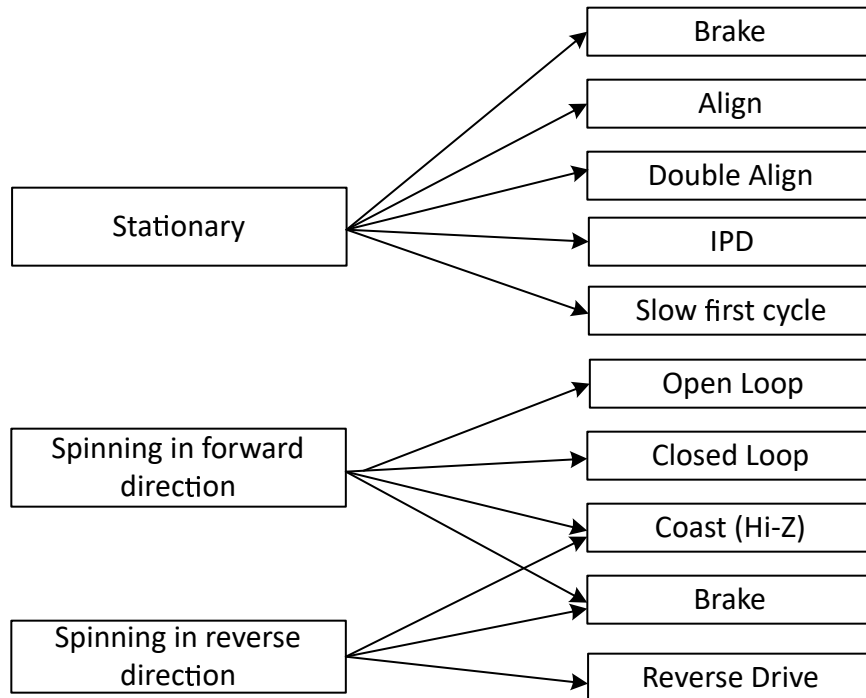


Figure 7-19. Starting the motor under different initial conditions

Note

"Forward" means "spinning in the same direction as the intended commanded speed", and "Reverse" means "spinning in the reverse direction as the intended commanded speed".

7.3.9.1 Case 1 – Motor is Stationary

If the motor is stationary, the commutation must be initialized to be in phase with the position of the motor. The MCF8316A device provides various options to initialize the commutation logic to the motor position.

- The align-and-go and double align technique forces the motor into alignment by applying a voltage across a particular motor phase to force the motor to rotate in alignment with this phase.
- Initial position detect (IPD) determines the position of the motor based on the deterministic inductance variation, which is often present in BLDC motors.
- The Slow first cycle method starts motor by applying low frequency cycle to align the rotor position to the applied commutation by the end of one electrical rotation.

Device enters open loop acceleration after going through initial motor start up state.

7.3.9.2 Case 2 – Motor is Spinning in the Forward Direction

If the motor is spinning forward (same direction as the intended command) with enough velocity, the MCF8316A device resynchronizes with the spinning motor and continues commutation by going directly to closed loop

operation. By resynchronizing to the spinning motor, the user achieves the fastest possible start-up time for this initial condition. In MCF8316A this feature can be enabled or disabled through RESYNC_EN. When resynchronization feature is disabled, the MCF8316A will wait for the motor coast to stop or apply a brake it before re-starting motor start-up sequence. In this case the device proceeds as in Case 1 above considering the motor is stationary.

7.3.9.3 Case 3 – Motor is Spinning in the Reverse Direction

If the motor is spinning in the reverse direction (the opposite direction as the intended command), the MCF8316A device provides several methods to control the motor and change the direction.

The reverse drive method allows the motor to be driven so that it decelerates through zero velocity. The motor achieves the shortest possible spin-up time in systems where the motor is spinning in the reverse direction.

If reverse drive is not enabled, then the MCF8316A can be configured either to wait for the motor coast to a stop or apply a brake to the motor. After the motor has stopped spinning, the motor start-up sequence proceeds as in Case 1, considering the motor is stationary.

Note

Take care when using the reverse drive or brake feature to ensure that the current is limited to an acceptable level and that the supply voltage does not surge as a result of energy being returned to the power supply.

7.3.10 Motor Start Sequence

Figure 7-20 shows the motor-start sequence implemented in the MCF8316A device.

ADVANCE INFORMATION

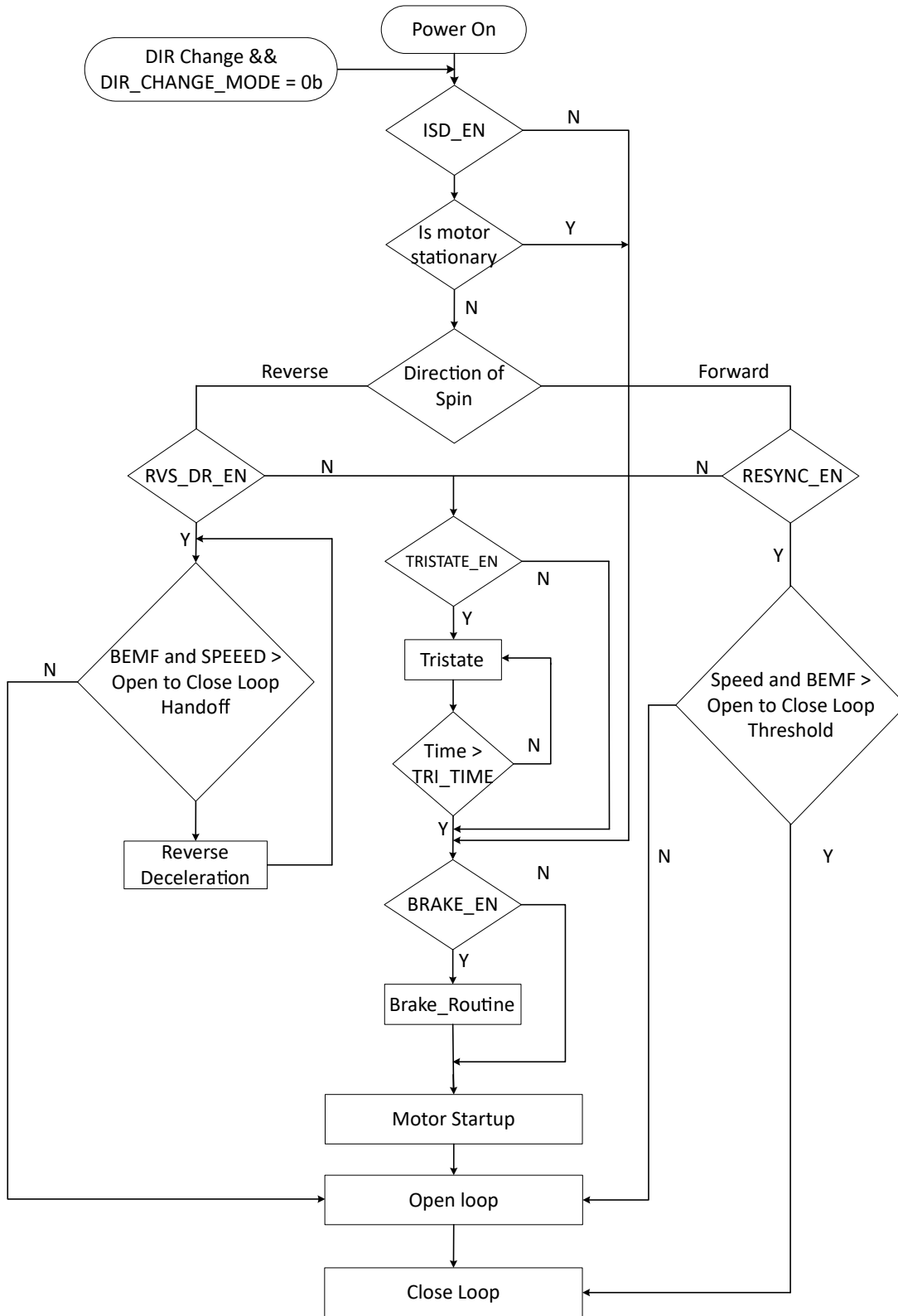


Figure 7-20. Motor Starting-Up Flow

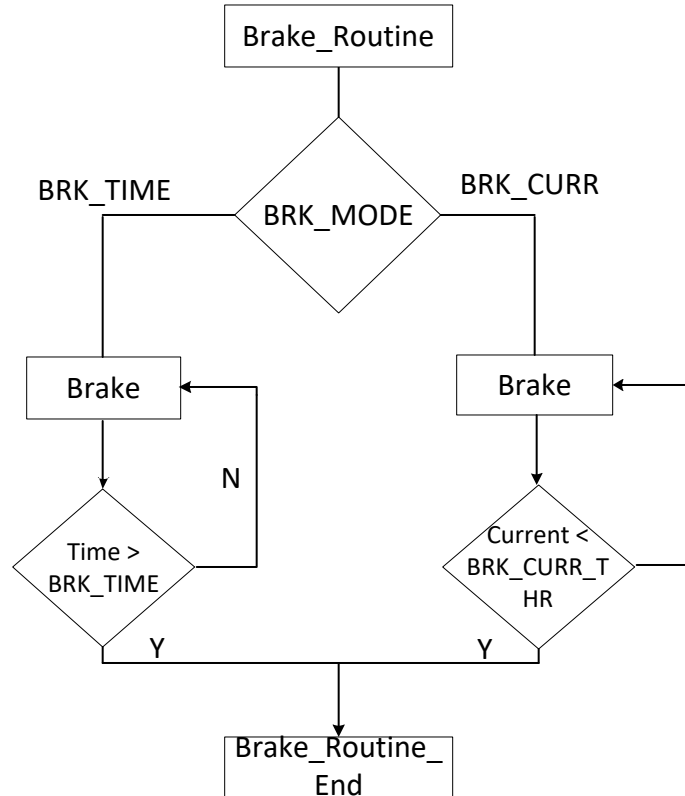


Figure 7-21. Motor Starting-Up Flow: Brake Routine

Power-On State	This is the initial power-on state of the Motor Start Sequence (MSS). The MSS starts in this state on initial power-up or whenever the MCF8316A device comes out of standby or sleep mode.
Brake Routine	The device performs the brake routine (see Motor Brake (Motor is stationary)).
BRAKE_EN Judgment	The MSS checks to determine whether the brake function is enabled (BRAKE_EN = 1). If the brake function is enabled, the MSS advances to the brake routine.
Closed Loop State	In this state, the MCF8316A device drives the motor with FOC.
DIR Pin Change Judgment	If the DIR pin is changed during any of above states, MCF8316A device stops driving the motor and restarts from the beginning.
Direction of Spin Judgment	The MSS determines whether the motor is spinning in the forward or the reverse direction. If the motor is spinning in the forward direction, the MCF8316A device executes the resynchronization (see Motor Resynchronization) process by transitioning directly into the closed loop state. If the motor is spinning in the reverse direction, the MSS proceeds to check whether Reverse drive is enabled.
ISD State	The MSS determines the initial condition of the motor (see Initial Speed Detect (ISD)).
ISD_EN Judgment	After power-on, the MCF8316A MSS enters the ISD_EN judgment where it checks to see if the initial speed detect (ISD) function is enabled (ISD_EN = 1). If ISD is disabled, the MSS proceeds directly to the BRK_EN Judgment. If ISD is enabled, the motor start sequence advances to the ISD state.
RVS_DR_EN Judgment	The MSS checks to see if the reverse drive function is enabled (RVS_DR_EN = 1). If it is, the MSS transitions to check speed of the motor in reverse direction. If the reverse drive function is not enabled, the MSS advances to the TRI_EN judgment.

Reverse Drive State	The MCF8316A resynchronizes in the reverse direction, decelerates the motor in closed loop and then changes direction when speed and BEMF falls below the hand-off threshold. (see Reverse Drive). Next, the MCF8316A accelerates into forward direction
BEMF and SPEED > HANDOFF Judgement	The MSS checks to see if the reverse speed is low enough and the Back-EMF is small enough for MCF8316A to decelerate in close loop. If it is, then the MSS decelerates motor into open loop and then and changes direction
Coast Routine	The device coasts the motor by turning OFF all MOSFETs (Hi-Z) and then waits for HIZ_TIME time .
HIZ_EN Judgment	The MSS checks to determine whether the coast function is enabled (HIZ_EN =1). If the coast function is enabled, the MSS advances to the coast routine.

7.3.10.1 Initial Speed Detect (ISD)

The ISD function is used to identify the initial condition of the motor. The initial speed and direction is determined by sampling the phase voltage through the internal ADC. ISD can be disabled through ISD_EN. If the function is disabled, the MCF8316A device does not perform the initial speed detect function and treats the motor as if it is stationary.

7.3.10.2 Motor Resynchronization

The motor resynchronization function works when the ISD function is enabled and the device determines that the initial state of the motor is spinning in the forward direction (same direction as the input command). The speed and position information measured during ISD are used to initialize the drive state of the MCF8316A device, which can transition directly into closed loop running state without needing to stop the motor. In the MCF8316A, Motor resynchronization can be enabled/disabled through RESYNC_EN bit.

7.3.10.3 Reverse Drive

After the ISD function measures the initial speed and the initial position; the MCF8316A reverse drive function acts to reverse decelerate the motor through zero speed, change direction, and accelerate in open loop until the device can transition into closed loop. (see [Figure 7-22](#)).

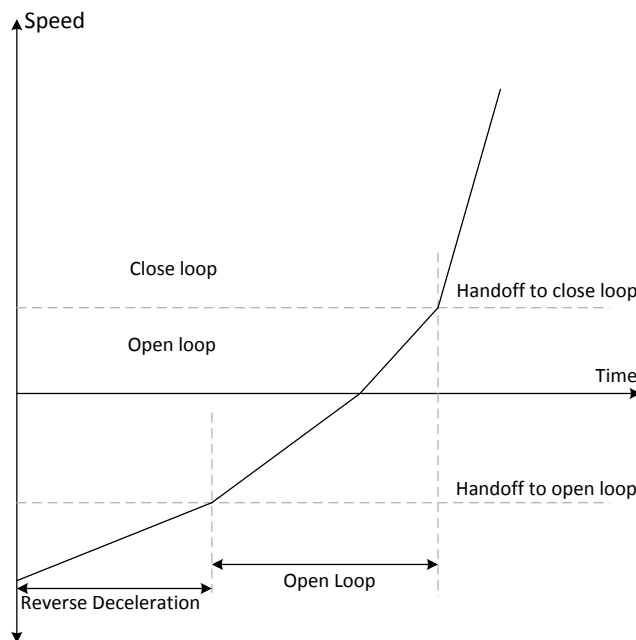


Figure 7-22. Reverse Drive Function

7.3.10.3.1 Reverse Drive Tuning

With ISD enabled the reverse drive functionality can be enabled using RVS_DR_EN. [Figure 7-22](#) shows the sequence of reverse drive. The speed at which motor would enter the open loop in reverse direction can be

configured using REV_DRV_HANDOFF_THR. This value would typically be same as the value configured for handoff speed threshold and may require tuning if the motor is expected to change direction on load.

Configure REV_DRV_CONFIG to choose between forward and reverse drive setting. For REV_DRV_CONFIG = 1b, open loop current and acceleration coefficients (A1, A2) are based on reverse drive settings. For REV_DRV_CONFIG = 0b, open loop current and acceleration coefficients (A1, A2) are based on forward drive settings. In reverse drive for a smooth transition without jerks or loss of synchronism, user can configure the current reference when the motor is spinning open loop during speed reversal using REV_DRV_OPEN_LOOP_CURRENT (when REV_DRV_CONFIG = 1b). In open loop the motor decelerates to zero speed and then accelerates in the intended direction of rotation. After zero speed, the reverse drive open loop acceleration speed slew rate coefficients A1 and A2 are defined using REV_DRV_OPEN_LOOP_ACCEL_A1 and REV_DRV_OPEN_LOOP_ACCEL_A2. The reverse drive open loop deceleration speed slew rate, when the motor is decelerating the opposite direction to zero speed, can be configured a percentage of reverse drive open loop acceleration using REV_DRV_OPEN_LOOP_DEC.

7.3.10.3.2 Active Braking During Reverse Drive

When Motor ISD Reverse Drive is enabled, the motor will be caught on the fly when spinning in opposite to intended direction, and the motor would then decelerate to low speed. Decelerating the motor against load requires motor mechanical energy to be extracted and disposed. DC voltage goes high if this energy is returned to DC power supply. When active braking is enabled, energy is still taken from DC power supply and is used to brake the motor. The mechanical energy of the motor and energy taken from source, both are dissipated within motor itself. Configure ACTIVE_BRAKE_EN to enable active braking during reverse drive to reduce dc bus voltage overshoot.

The maximum limit on the current sourced from the DC bus during active braking can be configured using ACTIVE_BRAKE_CURRENT_LIMIT. The power flow towards the motor during is active braking is achieved by using both Q-axis (i_q) and D-axis (i_d) components of current. The D-axis current reference (i_{d_ref}) is generated from the error between DC bus current limit (i_{dc_ref}) and the estimated DC bus current (i_{dc}) using a PI controller. The i_{dc} value is estimated from the measured phase currents, phase voltage and DC bus voltage, using power balance equation (equating the instantaneous DC bus power to sum of all three instantaneous phase power assuming 100% efficiency). During active braking the DC bus current limit (i_{dc_ref}) starts from zero and linearly increases to ACTIVE_BRAKE_CURRENT_LIMIT with current slew rate as defined by ACTIVE_BRAKE_BUS_CURRENT_SLEW_RATE. The gain constants of PI controller can be configured using ACTIVE_BRAKE_KP and ACTIVE_BRAKE_KI. Figure 7-23 shows the active braking i_d current control loop.

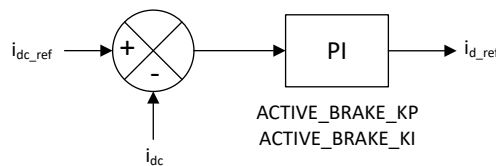


Figure 7-23. Active Braking Current Control Loop for i_{d_ref}

7.3.10.4 Motor Brake (Motor is stationary)

This brake functionality can be used when ISD is disabled or motor is stationary by configuring bit STAT_BRK_EN to 1. The motor brake function can be used to stop the spinning motor before attempting to start the motor. The brake is applied by turning on all three of the low-side driver MOSFETs for time configured by STARTUP_BRK_TIME

7.3.10.5 Motor Coast (Hi-Z)

A motor Hi-Z state can be enabled by configuring HIZ_EN to 1. During coast (Hi-Z) state, all high-side and low-side MOSFETs are turned OFF. The MCF8316A enters the coast (Hi-Z) state for a certain time configured by HIZ_TIME.

7.3.10.6 Motor Startup

There are different options available for motor startup from a stationary position and these options can be configured by MTR_STARTUP. In align and double align mode, the motor is aligned to a known position by

injecting a DC current. In IPD mode, the rotor position is estimated by applying 6 different high-frequency pulses. In slow first cycle mode, the motor is started by applying a low frequency cycle

7.3.10.6.1 Align

Align is enabled by configuring MTR_STARTUP to 00b. The MCF8316A device aligns the motor by injecting a DC current through a particular phase pattern for a certain time (configured by ALIGN_TIME[2:0]). The phase pattern during align is generated based on align angle and it is configured through ALIGN_ANGLE. In the MCF8316A, the current limit threshold during align is configured through ALIGN_OR_SLOW_CURRENT LIMIT. At the end of the align routine the motor should be aligned at the known position.

A fast change in the applied drive current may result in a sudden change in the driving torque. In some applications, this could result in acoustic noise. To avoid this, the MCF8316A device ramps up the current from 0 to the maximum current set by the user. ALIGN_RAMP_RATE[2:0] sets the maximum current ramp-up rate that is applied to the motor.

7.3.10.6.2 Double Align

Double align is enabled by configuring MTR_STARTUP to 01b. Sometimes a single align is not enough when the starting position of the rotor is out of phase with the applied phase pattern. In this case, it is possible to have start-up failures using single align. In these cases if single align is not enough, the MCF8316A provides the option of double align. The phase pattern for the second align is 90 degrees out of phase from the first align. In the MCF8316A, the current limit threshold during the first and second align is configured through ALIGN_OR_SLOW_CURRENT LIMIT. At the end of the align routine, the motor should be aligned to a known position.

7.3.10.6.3 IPD

IPD can be enabled by configuring MTR_STARTUP. The inductive sense method is used to determine the initial position of the motor when IPD is enabled.

Align or double align may result in the motor spinning in the reverse direction before starting entering open loop acceleration. IPD can be used in such applications where reverse rotation of the motor is unacceptable. Because IPD does not wait for the motor to align with the commutation, it can allow for a faster motor start sequence. IPD works well when the inductance of the motor varies as a function of position. Because it works by pulsing current to the motor, it can generate acoustics which must be taken into account when determining the best start method for a particular application.

7.3.10.6.3.1 IPD Operation

IPD operates by sequentially applying voltage across two of the three motor phases according to the following sequence: BC CB AB BA CA AC (see [Figure 7-24](#)). When the current reaches the threshold configured in IPD_CURR_THR, the MCF8316A stops driving. The MCF8316A device measures the time it takes from when the voltage is first applied until the current threshold is reached. The time varies as a function of the inductance in the motor windings. The state with the shortest time represents the state with the minimum inductance. The minimum inductance is because of the alignment of the north pole of the motor with this particular driving state.

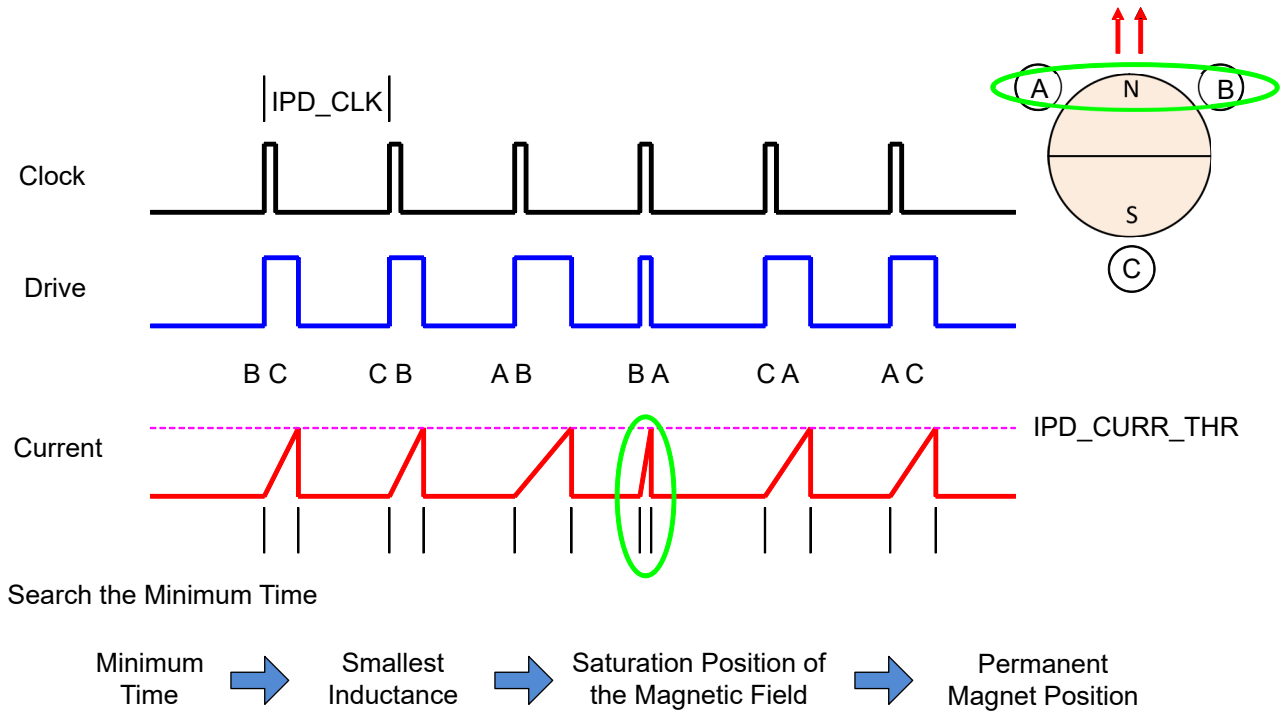


Figure 7-24. IPD Function

7.3.10.6.3.2 IPD Release Mode

Two options are available for configuring how the MCF8316A stops driving the motor when the current threshold is reached. The recirculate mode is selected if IPD_RLS_MODE = 0. In this configuration, the low-side (LSC) MOSFET remains on to allow the current to recirculate between the MOSFET (LSC) and body diode (LSA) (see Figure 7-25). Hi-Z mode is selected if IPD_RLS_MODE = 1. Both the high-side (HSA) and low-side (LSC) MOSFETs are turned off and the current recirculates through the body diodes back to the power supply (see Figure 7-26).

In the high-impedance state, the phase current has a faster settle-down time, but that can result in a voltage increase on V_M . The user must manage this with an appropriate selection of either a clamp circuit or by providing sufficient capacitance between V_M and GND to absorb the energy. If the voltage surge cannot be contained or if it is unacceptable for the application, then select the recirculate mode. When selecting the recirculate mode, select the IPD_CLK_FREQ to give the current in the motor windings enough time to decay to 0A before the next IPD cycle begins..

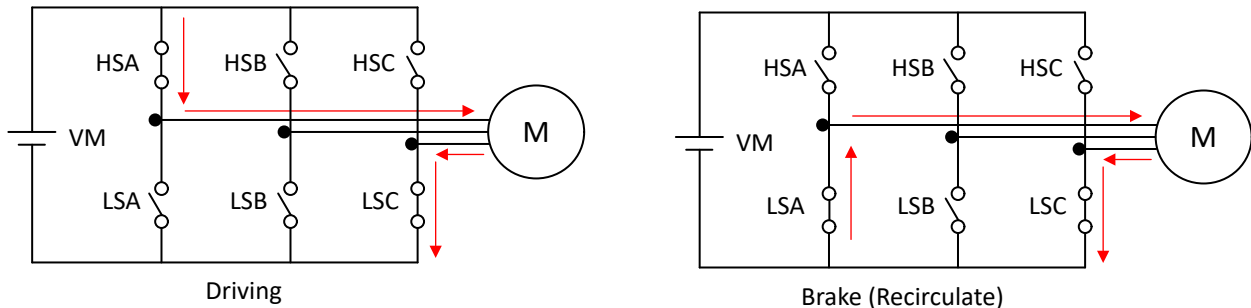


Figure 7-25. IPD Release Mode 0

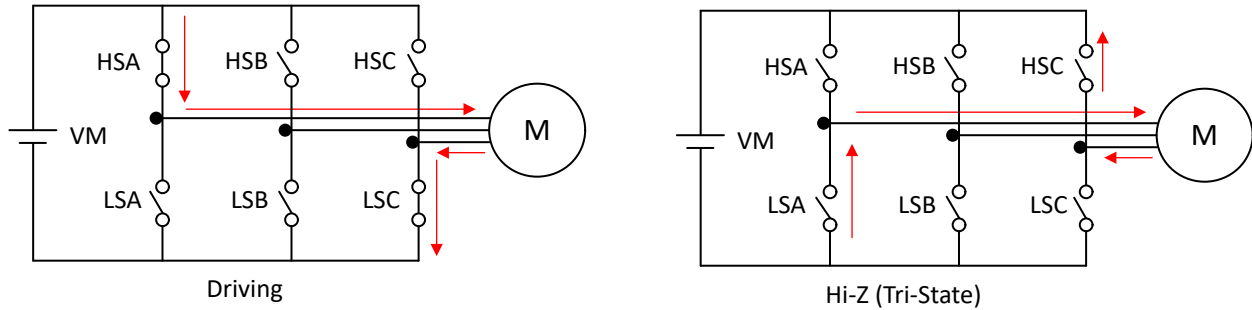


Figure 7-26. IPD Release Mode 1

7.3.10.6.3.3 IPD Advance Angle

After the initial position is detected, the MCF8316A device begins driving the motor in open loop at an angle specified by IPD_ADV_ANGLE.

Advancing the drive angle anywhere from 0° to 180° results in positive torque. Advancing the drive angle by 90° results in maximum initial torque. Applying maximum initial torque could result in uneven acceleration to the rotor. Select the IPD_ADV_ANGLE to allow for smooth acceleration in the application (see [Figure 7-27](#)).

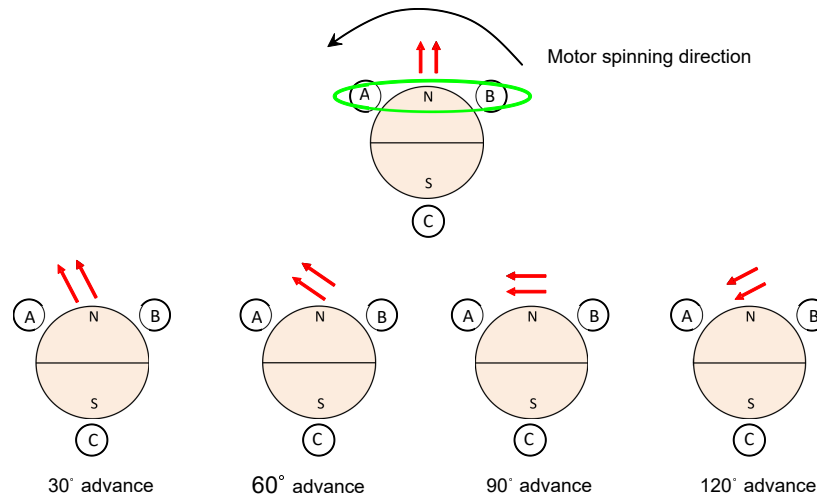


Figure 7-27. IPD Advance Angle

7.3.10.6.4 Slow First Cycle Startup

Slow First Cycle is enabled by configuring MTR_STARTUP to 11b. In slow first cycle configuration, the MCF8316A starts motor commutation at a frequency defined by SLOW_FIRST_CYCLE_FREQ. The frequency configured is used only for first cycle, and it has to be configured to be slow enough to allow motor to synchronize with the commutation sequence. This mode is useful when fast startup is desired as it significantly reduces the align time.

7.3.10.6.5 Open loop

After the motor initialization with either with align, double align, IPD, or slow first cycle, the MCF8316A device begins to accelerate the motor in open loop. During open loop, the speed is increased with a fixed current limit. In open loop, the current control PI loop for Iq and Id are active to actively controlling the current. The angle during open loop is provided from the ramp generator as shown in [Figure 7-28](#)

ADVANCE INFORMATION

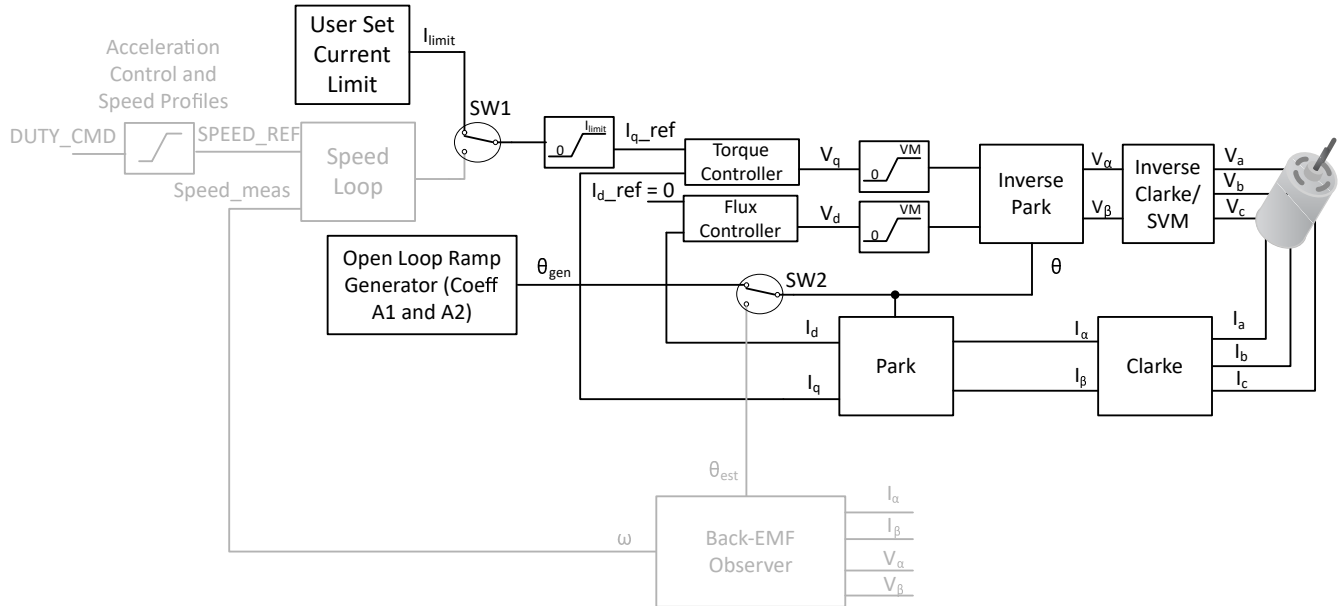


Figure 7-28. Open Loop

In MCF8316A, the current limit threshold is configured through `OL_ILIMIT_CONFIG` and is determined by `ILIMIT` or `OL_ILIMIT` based on configuration of `OL_ILIMIT_CONFIG`. The function of the open-loop operation is to drive the motor to a minimum speed so that the motor generates sufficient back-EMF to allow the back-EMF observer to accurately detect the position of the rotor. The motor is accelerated in open loop and speed at any given time is determined by Equation 4. In MCF8316A, `A1` and `A2` are configured through `OL_ACC_A1` and `OL_ACC_A2`.

$$\text{Speed}(t) = \text{OL_ACC_A1} * t + 0.5 * \text{OL_ACC_A2} * t^2 \quad (4)$$

7.3.10.6.6 Transition from Open to Closed Loop

Once the motor has reached a sufficient speed for the back-EMF observer to estimate angle and speed of the motor, the MCF8316A transition into closed loop state. The frequency of this handoff is automatically determined based on the measured back-EMF and motor speed. User also have option to manually set the handoff speed by configuring `OPN_CL_HANDOFF_THR`. In order to have smooth transition and avoid speed transients, the θ_{error} ($\theta_{\text{gen}} - \theta_{\text{est}}$) is decreased linearly after transition. The ramp rate of θ_{error} reduction can be configured using `THETA_ERROR_RAMP_RATE`. If the current limit set during the open loop is high and if it is not reduced before transition the motor speed may increase momentarily higher than `SPEED_REF` after transition into closed loop. In order to avoid speed excursions, configure the `IQ_RAMP_EN` bit to high, so that i_{q_ref} decreases prior to transition into closed loop. However if the final speed reference (`SPEED_REF`) is more than two times the open loop to closed loop hand off speed (`OPN_CL_HANDOFF_THR`), then i_{q_ref} is not decreased independent of the `IQ_RAMP_EN` setting, to enable faster motor acceleration.

After hand off to closed loop at a sufficient speed, there could be still some θ_{error} , as the estimators may not be fully aligned. A slow acceleration can be used after the open loop to closed loop transition, ensuring that the θ_{error} reduces to zero. The slow acceleration can be configured using `CL_SLOW_ACC`.

Figure 7-29 shows the control sequence in open to closed to loop transition. The current i_{q_ref} reduces to a lower value in current decay region, if `IQ_RAMP_EN` is set to high. If `IQ_RAMP_EN` is configured to logic low, then current decay region will not be there in the transition sequence.

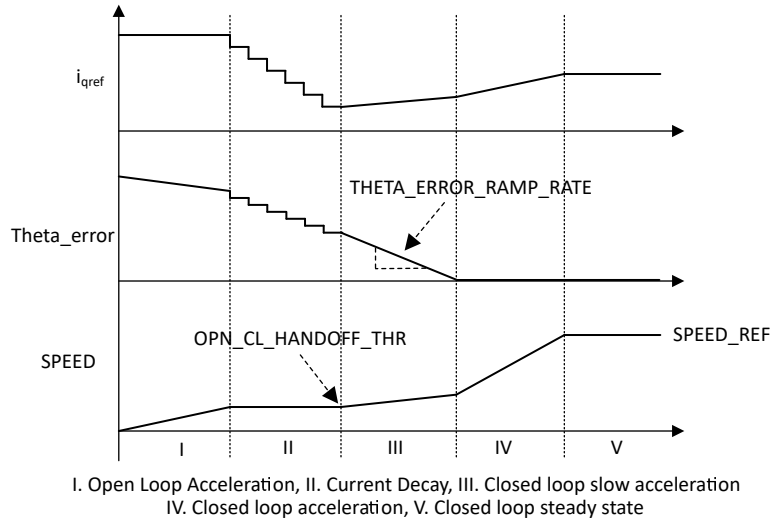


Figure 7-29. Control Sequence in Open to Closed Loop Transition

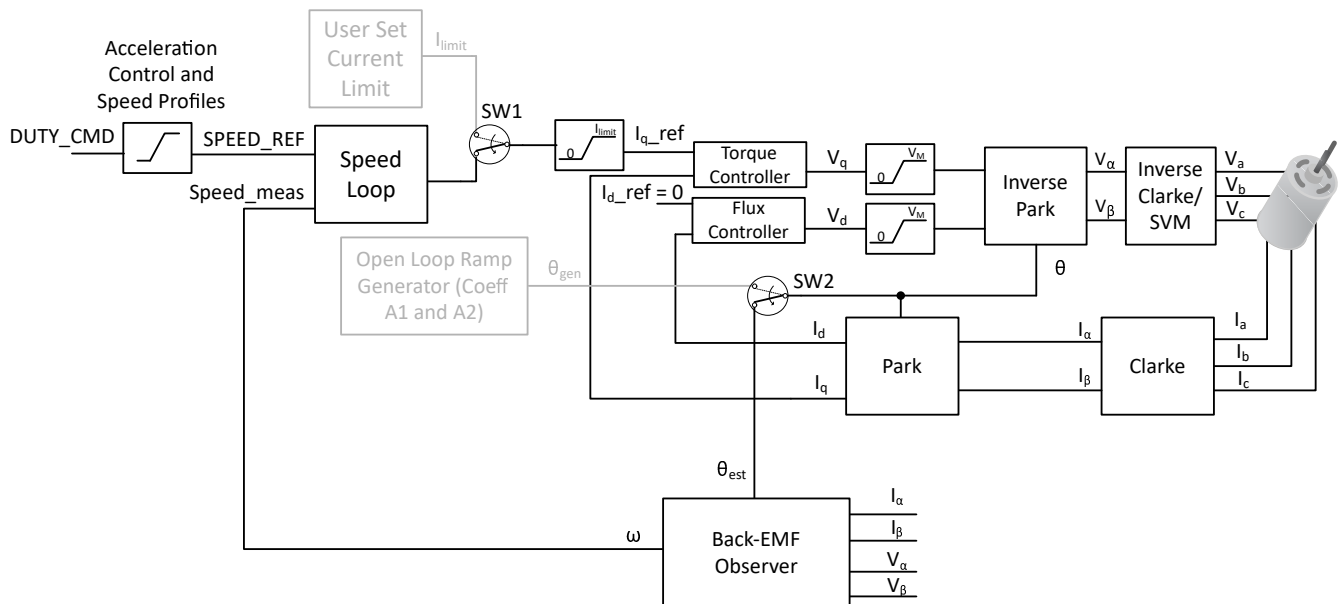


Figure 7-30. Open to Closed Loop Transition Control Block Diagram

7.3.11 Closed Loop Operation (FOC)

The MCF8316A drives the motor using Field Oriented Control(FOC) as shown in [Figure 7-31](#). In closed loop operation, the motor angle (θ_{est}) and speed (Speed_meas) are estimated using the back-EMF observer. The speed and current regulation are achieved using PI control loop. In order to achieve maximum efficiency, the direct axis current is set to zero ($I_{d_ref} = 0$), which will ensure that stator and rotor field are orthogonal (90 degrees out of phase) to each other.

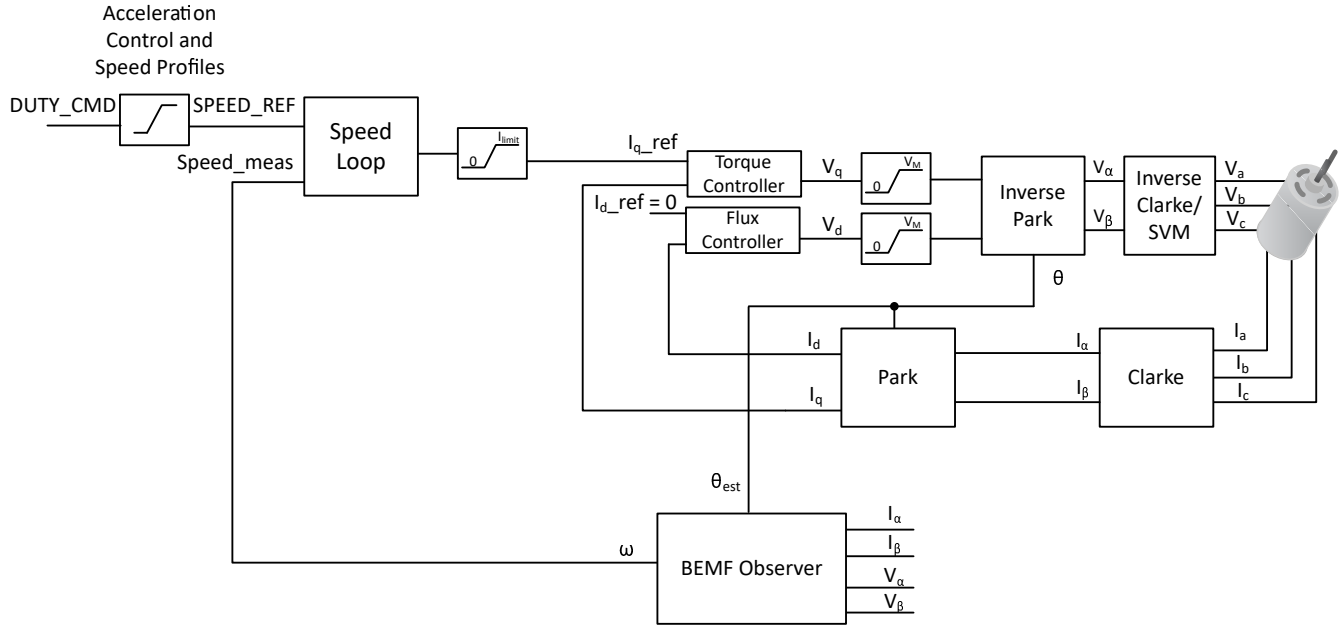


Figure 7-31. Closed Loop FOC Control

7.3.11.1 Closed loop accelerate

To prevent sudden changes in the torque applied to the motor which could result in acoustic noise, the MCF8316A device provides the option of limiting the maximum rate at which the speed command can change. The closed loop accelerate parameter sets the maximum rate at which the speed command changes (shown in Figure 7-32). In the MCF8316A, closed loop acceleration is configured through CL_ACC.

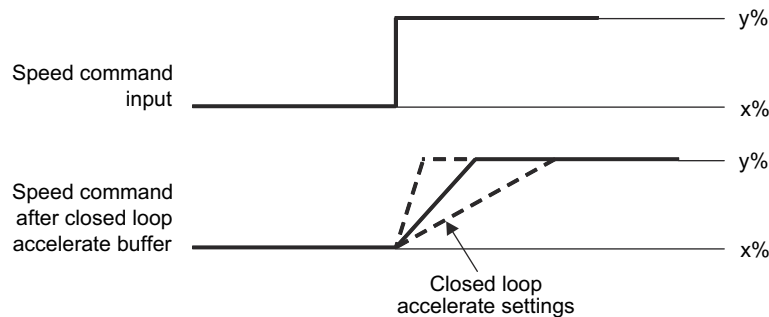


Figure 7-32. Closed loop accelerate

7.3.11.2 Speed PI Control

The integrated speed loop helps maintain a constant speed over varying operating conditions. The K_p and K_i coefficients are configured through SPD_LOOP_KP and SPD_LOOP_KI. The output of the speed loop (SPEED_PI_OUT) is used to generate the reference for torque control (I_{q_ref}). The output of the speed loop is limited to implement a current limit. The current limit is set by configuring I_LIMIT. When output of the speed loop saturates, the integrator is disabled to prevent the integral term from getting windup (increasing).

SPEED_REF is derived from the commanded speed, maximum motor speed profiles configured by the user and SPEED_MEAS is the estimated speed from the back-EMF observer

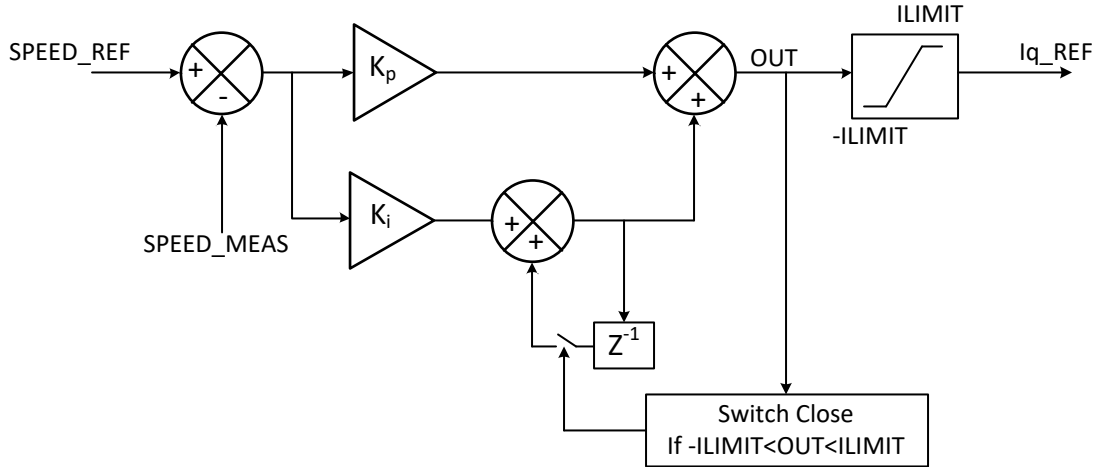


Figure 7-33. Speed PI Control

7.3.11.3 Current PI Control

The MCF8316A has two PI controllers for I_d and I_q to control torque and flux separately. K_p and K_i coefficients are the same for both parameters and are configured through CURR_LOOP_KP and CURR_LOOP_KI. The outputs of the current control loops is used to generate voltage signals V_d and V_q to be applied to the motor. The outputs of the current loops are clamped to supply voltage V_m . I_d PI current loop is executed first and output of I_d current loop V_d is checked for saturation. When the output of the current loop saturates, the integration is disabled to prevent integral term from getting windup (increasing).

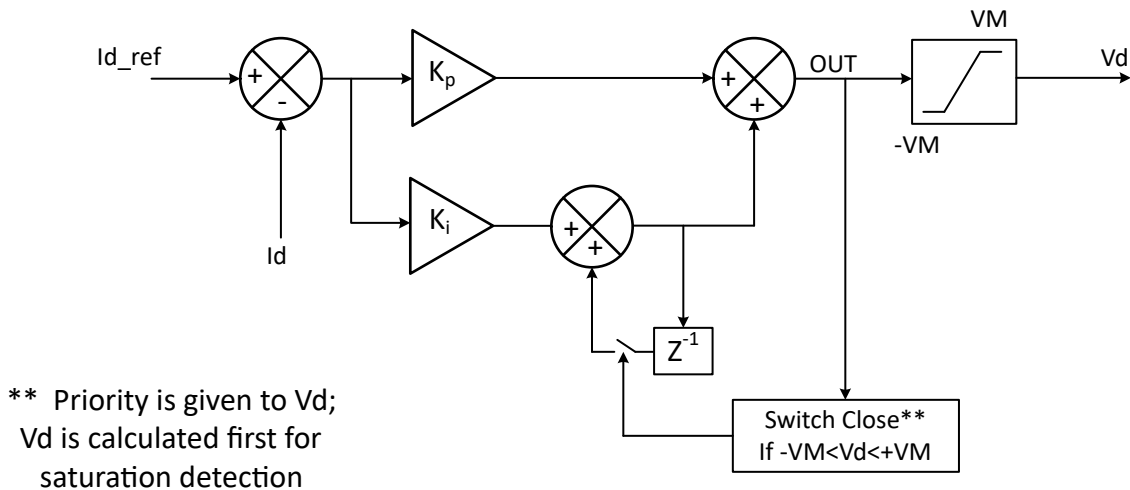


Figure 7-34. I_d Current PI Control

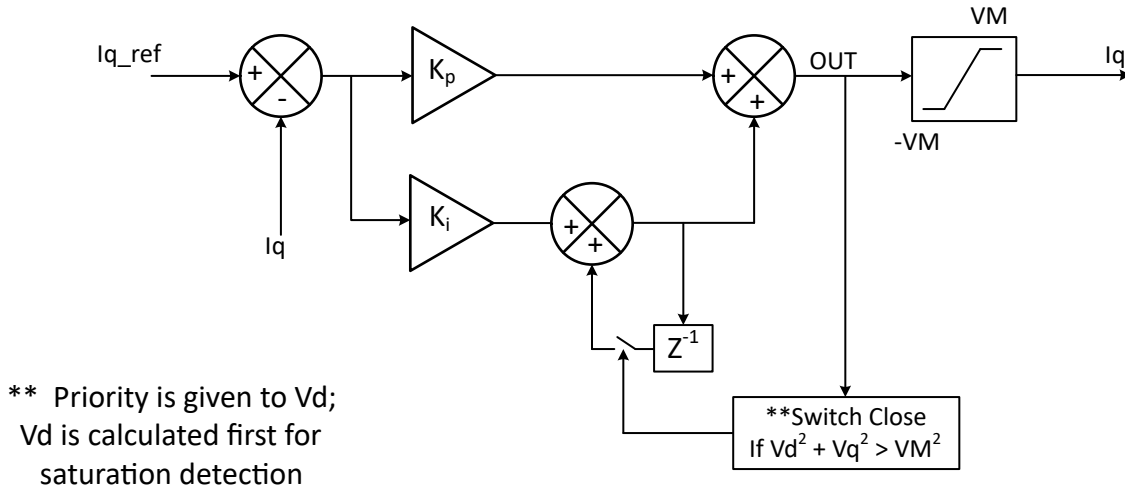


Figure 7-35. Iq Current PI Control

7.3.11.4 Motor Parameters

The MCF8316A uses the motor resistance, motor inductance and motor back-EMF constant to estimate motor position in when operating in closed. The MCF8316A has the capability of measuring these motor parameters in the offline state (see [Motor Parameter Extraction Tool \(MPET\)](#)). Offline measurement of parameters when enabled place before normal motor operation. The user can also disable the offline measurement and configure motor parameters through EEPROM. This feature of motor parameter measurement is useful to account for motor to motor variation during manufacturing.

7.3.11.4.1 Motor Resistance

For a wye-connected motor, the motor phase resistance refers to the resistance from the phase output to the center tap, R_{PH} (denoted as R_{PH} in [Figure 7-36](#)). For a delta-connected motor, the motor phase resistance refers to the equivalent phase to center tap in the wye configuration in [Figure 7-36](#).

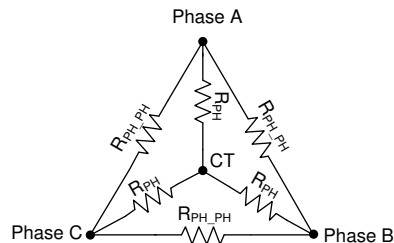


Figure 7-36. Motor Resistance

For both the delta-connected motor and the wye-connected motor, the easy way to get the equivalent R_{PH} is to measure the resistance between two phase terminals (R_{PH_PH}), and then divide this value by two, $R_{PH} = \frac{1}{2} R_{PH_PH}$. In wye-connected motor, if user have access to center tap (CT), L_{PH} can also be measured between center tap (CT) and phase terminal.

Configure the motor resistance (R_{PH}) to a nearest value from [Table 7-2](#).

Table 7-2. Motor Resistance Look-Up Table

MOTOR_RES (HEX)	R _{PH} (Ω)	MOTOR_RES (HEX)	R _{PH} (Ω)	MOTOR_RES (HEX)	R _{PH} (Ω)	MOTOR_RES (HEX)	R _{PH} (Ω)
0x00	Self Measurement (see Motor Parameter Extraction Tool (MPET))	0x40	0.145	0x80	0.465	0xC0	2.1
0x01	0.006	0x41	0.150	0x81	0.470	0xC1	2.2
0x02	0.007	0x42	0.155	0x82	0.475	0xC2	2.3
0x03	0.008	0x43	0.160	0x83	0.480	0xC3	2.4
0x04	0.009	0x44	0.165	0x84	0.485	0xC4	2.5
0x05	0.010	0x45	0.170	0x85	0.490	0xC5	2.6
0x06	0.011	0x46	0.175	0x86	0.495	0xC6	2.7
0x07	0.012	0x47	0.180	0x87	0.50	0xC7	2.8
0x08	0.013	0x48	0.185	0x88	0.51	0xC8	2.9
0x09	0.014	0x49	0.190	0x89	0.52	0xC9	3.0
0x0A	0.015	0x4A	0.195	0x8A	0.53	0xCA	3.2
0x0B	0.016	0x4B	0.200	0x8B	0.54	0xCB	3.4
0x0C	0.017	0x4C	0.205	0x8C	0.55	0xCC	3.6
0x0D	0.018	0x4D	0.210	0x8D	0.56	0xCD	3.8
0x0E	0.019	0x4E	0.215	0x8E	0.57	0xCE	4.0
0x0F	0.020	0x4F	0.220	0x8F	0.58	0xCF	4.2
0x10	0.022	0x50	0.225	0x90	0.59	0xD0	4.4
0x11	0.024	0x51	0.230	0x91	0.60	0xD1	4.6
0x12	0.026	0x52	0.235	0x92	0.61	0xD2	4.8
0x13	0.028	0x53	0.240	0x93	0.62	0xD3	5.0
0x14	0.030	0x54	0.245	0x94	0.63	0xD4	5.2
0x15	0.032	0x55	0.250	0x95	0.64	0xD5	5.4
0x16	0.034	0x56	0.255	0x96	0.65	0xD6	5.6
0x17	0.036	0x57	0.260	0x97	0.66	0xD7	5.8
0x18	0.038	0x58	0.265	0x98	0.67	0xD8	6.0
0x19	0.040	0x59	0.270	0x99	0.68	0xD9	6.2
0x1A	0.042	0x5A	0.275	0x9A	0.69	0xDA	6.4
0x1B	0.044	0x5B	0.280	0x9B	0.70	0xDB	6.6
0x1C	0.046	0x5C	0.285	0x9C	0.72	0xDC	6.8
0x1D	0.048	0x5D	0.290	0x9D	0.74	0xDD	7.0
0x1E	0.050	0x5E	0.295	0x9E	0.76	0xDE	7.2
0x1F	0.052	0x5F	0.300	0x9F	0.78	0xDF	7.4
0x20	0.054	0x60	0.305	0xA0	0.80	0xE0	7.6
0x21	0.056	0x61	0.310	0xA1	0.82	0xE1	7.8
0x22	0.058	0x62	0.315	0xA2	0.84	0xE2	8.0
0x23	0.060	0x63	0.320	0xA3	0.86	0xE3	8.2
0x24	0.062	0x64	0.325	0xA4	0.88	0xE4	8.4
0x25	0.064	0x65	0.330	0xA5	0.90	0xE5	8.6
0x26	0.066	0x66	0.335	0xA6	0.92	0xE6	8.8
0x27	0.068	0x67	0.340	0xA7	0.94	0xE7	9
0x28	0.070	0x68	0.345	0xA8	0.96	0xE8	9.2

Table 7-2. Motor Resistance Look-Up Table (continued)

MOTOR_RES (HEX)	R _{PH} (Ω)	MOTOR_RES (HEX)	R _{PH} (Ω)	MOTOR_RES (HEX)	R _{PH} (Ω)	MOTOR_RES (HEX)	R _{PH} (Ω)
0x29	0.072	0x69	0.350	0xA9	0.98	0xE9	9.4
0x2A	0.074	0x6A	0.355	0xAA	1.00	0xEA	9.6
0x2B	0.076	0x6B	0.360	0xAB	1.05	0xEB	9.8
0x2C	0.078	0x6C	0.365	0xAC	1.10	0xEC	10.0
0x2D	0.080	0x6D	0.370	0xAD	1.15	0xED	10.5
0x2E	0.082	0x6E	0.375	0xAE	1.20	0xEE	11.0
0x2F	0.084	0x6F	0.380	0xAF	1.25	0xEF	11.5
0x30	0.086	0x70	0.385	0xB0	1.30	0xF0	12.0
0x31	0.088	0x71	0.390	0xB1	1.35	0xF1	12.5
0x32	0.090	0x72	0.395	0xB2	1.40	0xF2	13.0
0x33	0.092	0x73	0.400	0xB3	1.45	0xF3	13.5
0x34	0.094	0x74	0.405	0xB4	1.50	0xF4	14.0
0x35	0.096	0x75	0.410	0xB5	1.55	0xF5	14.5
0x36	0.098	0x76	0.415	0xB6	1.60	0xF6	15.0
0x37	0.100	0x77	0.420	0xB7	1.65	0xF7	15.5
0x38	0.105	0x78	0.425	0xB8	1.70	0xF8	16.0
0x39	0.110	0x79	0.430	0xB9	1.75	0xF9	16.5
0x3A	0.115	0x7A	0.435	0xBA	1.80	0xFA	17.0
0x3B	0.120	0x7B	0.440	0xBB	1.85	0xFB	17.5
0x3C	0.125	0x7C	0.445	0xBC	1.90	0xFC	18.0
0x3D	0.130	0x7D	0.450	0xBD	1.95	0xFD	18.5
0x3E	0.135	0x7E	0.455	0xBE	2.00	0xFE	19.0
0x3F	0.140	0x7F	0.460	0xBF	2.05	0xFF	20.0

7.3.11.4.2 Motor Inductance

For a wye-connected motor, the motor phase inductance refers to the inductance from the phase output to the center tap, L_{PH} (denoted as L_{PH} in Figure 7-37). For a delta-connected motor, the motor phase inductance refers to the equivalent phase to center tap in the wye configuration in Figure 7-37.

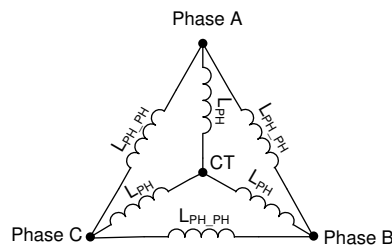


Figure 7-37. Motor Inductance

For both the delta-connected motor and the wye-connected motor, the easy way to get the equivalent L_{PH} is to measure the inductance between two phase terminals (L_{PH_PH}), and then divide this value by two, L_{PH} = ½ L_{PH_PH}. In wye-connected motor, if user have access to center tap (CT), L_{PH} can also be measured between center tap (CT) and phase terminal.

Configure the motor inductance (L_{PH}) to a nearest value from Table 7-3.

Table 7-3. Motor Inductance Look-Up Table

MOTOR_IND (HEX)	L _{PH} (mH)	MOTOR_IND (HEX)	L _{PH} (mH)	MOTOR_IND (HEX)	L _{PH} (mH)	MOTOR_IND (HEX)	L _{PH} (mH)
0x00	Self Measurement (see Motor Parameter Extraction Tool (MPET))	0x40	0.145	0x80	0.465	0xC0	2.1
0x01	0.006	0x41	0.150	0x81	0.470	0xC1	2.2
0x02	0.007	0x42	0.155	0x82	0.475	0xC2	2.3
0x03	0.008	0x43	0.160	0x83	0.480	0xC3	2.4
0x04	0.009	0x44	0.165	0x84	0.485	0xC4	2.5
0x05	0.010	0x45	0.170	0x85	0.490	0xC5	2.6
0x06	0.011	0x46	0.175	0x86	0.495	0xC6	2.7
0x07	0.012	0x47	0.180	0x87	0.50	0xC7	2.8
0x08	0.013	0x48	0.185	0x88	0.51	0xC8	2.9
0x09	0.014	0x49	0.190	0x89	0.52	0xC9	3.0
0x0A	0.015	0x4A	0.195	0x8A	0.53	0xCA	3.2
0x0B	0.016	0x4B	0.200	0x8B	0.54	0xCB	3.4
0x0C	0.017	0x4C	0.205	0x8C	0.55	0xCC	3.6
0x0D	0.018	0x4D	0.210	0x8D	0.56	0xCD	3.8
0x0E	0.019	0x4E	0.215	0x8E	0.57	0xCE	4.0
0x0F	0.020	0x4F	0.220	0x8F	0.58	0xCF	4.2
0x10	0.022	0x50	0.225	0x90	0.59	0xD0	4.4
0x11	0.024	0x51	0.230	0x91	0.60	0xD1	4.6
0x12	0.026	0x52	0.235	0x92	0.61	0xD2	4.8
0x13	0.028	0x53	0.240	0x93	0.62	0xD3	5.0
0x14	0.030	0x54	0.245	0x94	0.63	0xD4	5.2
0x15	0.032	0x55	0.250	0x95	0.64	0xD5	5.4
0x16	0.034	0x56	0.255	0x96	0.65	0xD6	5.6
0x17	0.036	0x57	0.260	0x97	0.66	0xD7	5.8
0x18	0.038	0x58	0.265	0x98	0.67	0xD8	6.0
0x19	0.040	0x59	0.270	0x99	0.68	0xD9	6.2
0x1A	0.042	0x5A	0.275	0x9A	0.69	0xDA	6.4
0x1B	0.044	0x5B	0.280	0x9B	0.70	0xDB	6.6
0x1C	0.046	0x5C	0.285	0x9C	0.72	0xDC	6.8
0x1D	0.048	0x5D	0.290	0x9D	0.74	0xDD	7.0
0x1E	0.050	0x5E	0.295	0x9E	0.76	0xDE	7.2
0x1F	0.052	0x5F	0.300	0x9F	0.78	0xDF	7.4
0x20	0.054	0x60	0.305	0xA0	0.80	0xE0	7.6
0x21	0.056	0x61	0.310	0xA1	0.82	0xE1	7.8
0x22	0.058	0x62	0.315	0xA2	0.84	0xE2	8.0
0x23	0.060	0x63	0.320	0xA3	0.86	0xE3	8.2
0x24	0.062	0x64	0.325	0xA4	0.88	0xE4	8.4
0x25	0.064	0x65	0.330	0xA5	0.90	0xE5	8.6
0x26	0.066	0x66	0.335	0xA6	0.92	0xE6	8.8
0x27	0.068	0x67	0.340	0xA7	0.94	0xE7	9
0x28	0.070	0x68	0.345	0xA8	0.96	0xE8	9.2

Table 7-3. Motor Inductance Look-Up Table (continued)

MOTOR_IND (HEX)	L _{PH} (mH)	MOTOR_IND (HEX)	L _{PH} (mH)	MOTOR_IND (HEX)	L _{PH} (mH)	MOTOR_IND (HEX)	L _{PH} (mH)
0x29	0.072	0x69	0.350	0xA9	0.98	0xE9	9.4
0x2A	0.074	0x6A	0.355	0xAA	1.00	0xEA	9.6
0x2B	0.076	0x6B	0.360	0xAB	1.05	0xEB	9.8
0x2C	0.078	0x6C	0.365	0xAC	1.10	0xEC	10.0
0x2D	0.080	0x6D	0.370	0xAD	1.15	0xED	10.5
0x2E	0.082	0x6E	0.375	0xAE	1.20	0xEE	11.0
0x2F	0.084	0x6F	0.380	0xAF	1.25	0xEF	11.5
0x30	0.086	0x70	0.385	0xB0	1.30	0xF0	12.0
0x31	0.088	0x71	0.390	0xB1	1.35	0xF1	12.5
0x32	0.090	0x72	0.395	0xB2	1.40	0xF2	13.0
0x33	0.092	0x73	0.400	0xB3	1.45	0xF3	13.5
0x34	0.094	0x74	0.405	0xB4	1.50	0xF4	14.0
0x35	0.096	0x75	0.410	0xB5	1.55	0xF5	14.5
0x36	0.098	0x76	0.415	0xB6	1.60	0xF6	15.0
0x37	0.100	0x77	0.420	0xB7	1.65	0xF7	15.5
0x38	0.105	0x78	0.425	0xB8	1.70	0xF8	16.0
0x39	0.110	0x79	0.430	0xB9	1.75	0xF9	16.5
0x3A	0.115	0x7A	0.435	0xBA	1.80	0xFA	17.0
0x3B	0.120	0x7B	0.440	0xBB	1.85	0xFB	17.5
0x3C	0.125	0x7C	0.445	0xBC	1.90	0xFC	18.0
0x3D	0.130	0x7D	0.450	0xBD	1.95	0xFD	18.5
0x3E	0.135	0x7E	0.455	0xBE	2.00	0xFE	19.0
0x3F	0.140	0x7F	0.460	0xBF	2.05	0xFF	20.0

7.3.11.4.3 Motor Back-EMF constant

The back-EMF constant describes the motor phase-to-neutral back-EMF voltage as a function of the motor velocity. For a wye-connected motor, the motor BEMF constant refers to the BEMF as a function of time from the phase output to the center tap, $K_{t_{PH_N}}$ (denoted as $K_{t_{PH_N}}$ in Figure 7-38). For a delta-connected motor, the motor BEMF constant refers to the equivalent phase to center tap in the wye configuration in Figure 7-38.

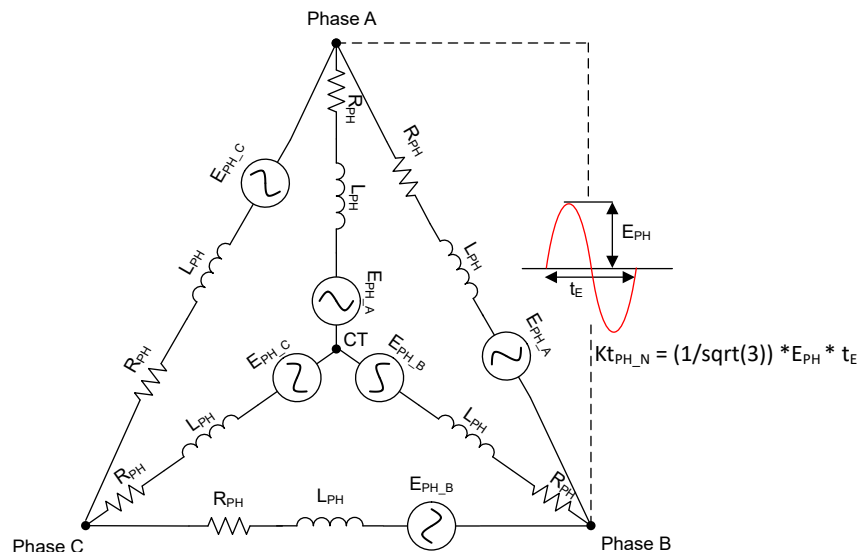


Figure 7-38. Motor back-EMF constant

For both the delta-connected motor and the wye-connected motor, the easy way to get the equivalent $K_{t_{PH_N}}$ is to measure the peak value of BEMF on scope for one electrical cycle between two phase terminals (E_{PH}), and then multiply by time duration of one electrical cycle and in order to convert from phase-to-phase to phase-to-neutral divide by $\sqrt{3}$ as shown in [Equation 5](#).

$$K_{t_{PH_N}} = \frac{1}{\sqrt{3}} \times E_{PH} \times t_E \quad (5)$$

Configure the motor BEMF constant ($K_{t_{PH_N}}$) to a nearest value from [Table 7-4](#).

Table 7-4. Motor BEMF constant Look-Up Table

MOTOR_BEMF_CONST (HEX)	$K_{t_{PH_N}}$ (mV/Hz)	MOTOR_BEMF_CONST (HEX)	$K_{t_{PH_N}}$ (mV/Hz)	MOTOR_BEMF_CONST (HEX)	$K_{t_{PH_N}}$ (mV/Hz)	MOTOR_BEMF_CONST (HEX)	$K_{t_{PH_N}}$ (mV/Hz)
0x00	Self Measurement (see Motor Parameter Extraction Tool (MPET))	0x40	14.5	0x80	46.5	0xC0	210
0x01	0.6	0x41	15.0	0x81	47.0	0xC1	220
0x02	0.7	0x42	15.5	0x82	47.5	0xC2	230
0x03	0.8	0x43	16.0	0x83	48.0	0xC3	240
0x04	0.9	0x44	16.5	0x84	48.5	0xC4	250
0x05	1.0	0x45	17.0	0x85	49.0	0xC5	260
0x06	1.1	0x46	17.5	0x86	49.5	0xC6	270
0x07	1.2	0x47	18.0	0x87	50.0	0xC7	280
0x08	1.3	0x48	18.5	0x88	51	0xC8	290
0x09	1.4	0x49	19.0	0x89	52	0xC9	300
0x0A	1.5	0x4A	19.5	0x8A	53	0xCA	320
0x0B	1.6	0x4B	20.0	0x8B	54	0xCB	340
0x0C	1.7	0x4C	20.5	0x8C	55	0xCC	360
0x0D	1.8	0x4D	21.0	0x8D	56	0xCD	380
0x0E	1.9	0x4E	21.5	0x8E	57	0xCE	400
0x0F	2.0	0x4F	22.0	0x8F	58	0xCF	420
0x10	2.2	0x50	22.5	0x90	59	0xD0	440
0x11	2.4	0x51	23.0	0x91	60	0xD1	460
0x12	2.6	0x52	23.5	0x92	61	0xD2	480
0x13	2.8	0x53	24.0	0x93	62	0xD3	500
0x14	3.0	0x54	24.5	0x94	63	0xD4	520
0x15	3.2	0x55	25.0	0x95	64	0xD5	540
0x16	3.4	0x56	25.5	0x96	65	0xD6	560
0x17	3.6	0x57	26.0	0x97	66	0xD7	580
0x18	3.8	0x58	26.5	0x98	67	0xD8	600
0x19	4.0	0x59	27.0	0x99	68	0xD9	620
0x1A	4.2	0x5A	27.5	0x9A	69	0xDA	640
0x1B	4.4	0x5B	28.0	0x9B	70	0xDB	660
0x1C	4.6	0x5C	28.5	0x9C	72	0xDC	680
0x1D	4.8	0x5D	29.0	0x9D	74	0xDD	700
0x1E	5.0	0x5E	29.5	0x9E	76	0xDE	720
0x1F	5.2	0x5F	30.0	0x9F	78	0xDF	740
0x20	5.4	0x60	30.5	0xA0	80	0xE0	760

Table 7-4. Motor BEMF constant Look-Up Table (continued)

MOTOR_BEMF_ CONST (HEX)	Kt _{PH_N} (mV/Hz)	MOTOR_BEMF_ CONST (HEX)	Kt _{PH_N} (mV/Hz)	MOTOR_BEMF_ CONST (HEX)	Kt _{PH_N} (mV/Hz)	MOTOR_BEMF_ F_CONST (HEX)	Kt _{PH_N} (mV/Hz)
0x21	5.6	0x61	31.0	0xA1	82	0xE1	780
0x22	5.8	0x62	31.5	0xA2	84	0xE2	800
0x23	6.0	0x63	32.0	0xA3	86	0xE3	820
0x24	6.2	0x64	32.5	0xA4	88	0xE4	840
0x25	6.4	0x65	33.0	0xA5	90	0xE5	860
0x26	6.6	0x66	33.5	0xA6	92	0xE6	880
0x27	6.8	0x67	34.0	0xA7	94	0xE7	900
0x28	7.0	0x68	34.5	0xA8	96	0xE8	920
0x29	7.2	0x69	35.0	0xA9	98	0xE9	940
0x2A	7.4	0x6A	35.5	0xAA	100	0xEA	960
0x2B	7.6	0x6B	36.0	0xAB	105	0xEB	980
0x2C	7.8	0x6C	36.5	0xAC	110	0xEC	1000
0x2D	8.0	0x6D	37.0	0xAD	115	0xED	1050
0x2E	8.2	0x6E	37.5	0xAE	120	0xEE	1100
0x2F	8.4	0x6F	38.0	0xAF	125	0xEF	1150
0x30	8.6	0x70	38.5	0xB0	130	0xF0	1200
0x31	8.8	0x71	39.0	0xB1	135	0xF1	1250
0x32	9.0	0x72	39.5	0xB2	140	0xF2	1300
0x33	9.2	0x73	40.0	0xB3	145	0xF3	1350
0x34	9.4	0x74	40.5	0xB4	150	0xF4	1400
0x35	9.6	0x75	41.0	0xB5	155	0xF5	1450
0x36	9.8	0x76	41.5	0xB6	160	0xF6	1500
0x37	10.0	0x77	42.0	0xB7	165	0xF7	1550
0x38	10.5	0x78	42.5	0xB8	170	0xF8	1600
0x39	11.0	0x79	43.0	0xB9	175	0xF9	1650
0x3A	11.5	0x7A	43.5	0xBA	180	0xFA	1700
0x3B	12.0	0x7B	44.0	0xBB	185	0xFB	1750
0x3C	12.5	0x7C	44.5	0xBC	190	0xFC	1800
0x3D	13.0	0x7D	45.0	0xBD	195	0xFD	1850
0x3E	13.5	0x7E	45.5	0xBE	200	0xFE	1900
0x3F	14.0	0x7F	46.0	0xBF	205	0xFF	2000

7.3.12 Motor Parameter Extraction Tool (MPET)

The MCF8316A uses motor winding resistance, motor winding inductance and Back-EMF constant to estimate motor position in closed loop operation. The MCF8316A has capability of automatically measuring motor parameters in offline state, rather than having the user enter the values themselves. The MPET routine measures motor winding resistance, inductance, back EMF constant and mechanical load inertia and frictional coefficients. Offline measurement of parameters takes place before normal motor operation. TI recommends to estimate the motor parameters before motor startup to minimize the impact caused due to possible parameter variations.

Initiate the motor parameter measurement routine by configuring the MPET start command bit MPET_CMD to 1. Make sure the motor is stationary before enabling MPET start command.

TI proprietary MPET routine includes following sequence of operation.

- **IPD:** The MPET routine starts with IPD, if the user enables motor winding resistance or inductance measurement by setting MPET_R = 1b and MPET_L = 1b or if the user defines MOTOR_RES = 0 or

MOTOR_IND = 0. The IPD during MPET can be configured using MPET specific configuration parameters or using the normal motor operation IPD configuration parameters. The IPD configuration selection is done using MPET_IPD_SELECT. With MPET_IPD_SELECT = 1b, the IPD current limit is configured using MPET_IPD_CURRENT_LIMIT and the IPD repeat number is configured using MPET_IPD_FREQ. With MPET_IPD_SELECT = 0b, the IPD current limit and the repeat number is configured using IPD_CURR_THR and IPD_REPEAT. The IPD timer over flow or the IPD current decay time more than three times the current ramp up time can result in MPET_IPD_FAULT. TI recommends to run the MPET multiple times to observe for consistent resistance and inductance reading.

- **Open loop Acceleration:**

After IPD, the MPET routine run align and then open loop acceleration if the back-EMF constant or mechanical parameter measurement are enabled by setting MPET_KE = 1b and MPET_MECH = 1b. The MPET routine incorporates the sequences for mechanical parameter measurement, if the speed loop PI constants are defined as zero, even if MPET_MECH = 0b. User can configure MPET specific open loop configuration parameters or use normal motor operation open loop configuration parameters. The open loop configuration selection is done using MPET_KE_MEAS_PARAMETER_SELECT. With MPET_KE_MEAS_PARAMETER_SELECT = 1b, the speed slew rate is defined using MPET_OPEN_LOOP_SLEW_RATE, the open loop current reference is defined using MPET_OPEN_LOOP_CURR_REF and the open loop speed reference is defined using MPET_OPEN_LOOP_SPEED_REF. With MPET_KE_MEAS_PARAMETER_SELECT = 0b, the speed slew rate is defined using OL_ACC_A1 and OL_ACC_A2, 80% of I_LIMIT for current reference and 50% of MAX_SPEED for speed reference.

- **Current Ramp Down:** After open loop acceleration, if the mechanical parameter measurement is enabled, then the MPET routine optimizes the motor current to lower value sufficient to support the load. If mechanical parameter measurement is disabled (MPET_MECH = 0b, or non-zero speed loop PI parameters) then the MPET will not have the current ramp down sequence.
- **Coasting:** MPET routine completes the sequence by allowing the motor to coast by enabling Hi-Z. The motor back EMF and indicative values of mechanical parameters are measured during the motor coasting period. If the motor back EMF is lower than the threshold defined in STAT_DETECT_THR, the MPET_BEMF_FAULT is generated.

Figure 7-39 shows the sequence of operation in MPET routine, listing the the configuration bits for a specific sequence to be a part of the MPET routine.

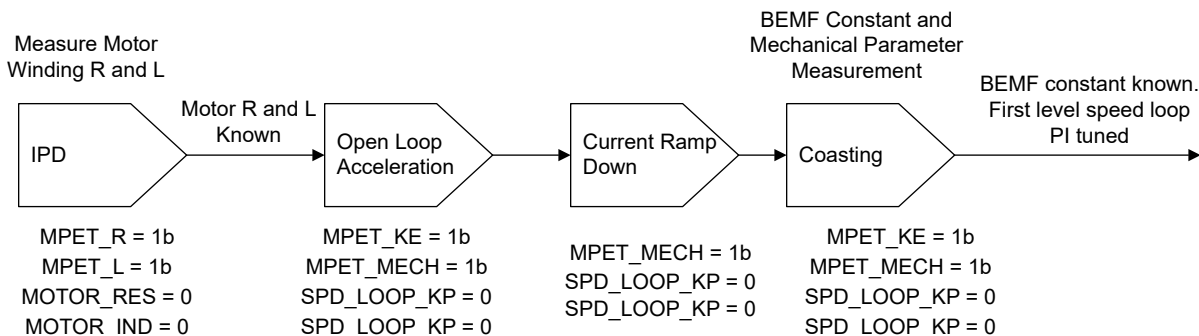


Figure 7-39. MPET Control Sequence

During the MPET routine, the algorithm does an estimation of the mechanical parameters including the inertia and frictional coefficient at the shaft (includes both motor and shaft coupled load). These values are used to set an initial coefficient for the speed loop KP and KI. The estimated speed loop KP and KI setting can be used as an initial setting only and TI recommends to tune these parameters on application by the user based on the performance requirement. The measured values are available in the MTR_PARAMS Register. The ALGO_STATUS_MPET register shows the status of the MPET measurement. Setting the MPET_WRITE_SHADOW bit to 1, writes the measured parameters to the shadow registers and the user written values on MOTOR_RES, MOTOR_IND, MOTOR_BEMF_CONST, CURR_LOOP_KP, CURR_LOOP_KI, SPD_LOOP_KP and SPD_LOOP_KI will be overwritten by the measured parameters from MPET. Writing any of the motor parameters to zero, enable the use of the MPET measured values independent of the

MPET_WRITE_SHADOW setting. The MPET calculates the current loop KP and KI by using the measured resistance and inductance.

7.3.13 Anti-Voltage Surge Function (AVS)

When a motor is driven, energy is transferred from the power supply into the motor. Some of this energy is stored in the form of inductive energy or as mechanical energy. If the speed command suddenly drops such that the BEMF voltage generated by the motor is greater than the voltage that is applied to the motor, then the mechanical energy of the motor is returned to the power supply and the V_M voltage surges. The AVS function works to prevent this from happening. AVS can be disabled through the register configuration AVS_EN. When AVS is disabled then deceleration rate is configured through CL_DEC_CONFIG

7.3.14 PWM Modulation Schemes

The MCF8316 support continuous and discontinuous space vector PWM modulation schemes. In continuous PWM modulation all the three phases switches all the time as per the defined switching frequency. In discontinuous PWM modulation, one of the phases is clamped to ground for 120-degree electrical period, and the other two phases are pulse width modulated. The modulation scheme is configured using the bits PWM_MOD. Figure 7-40 shows the modulated average phase voltages for different modulation schemes.

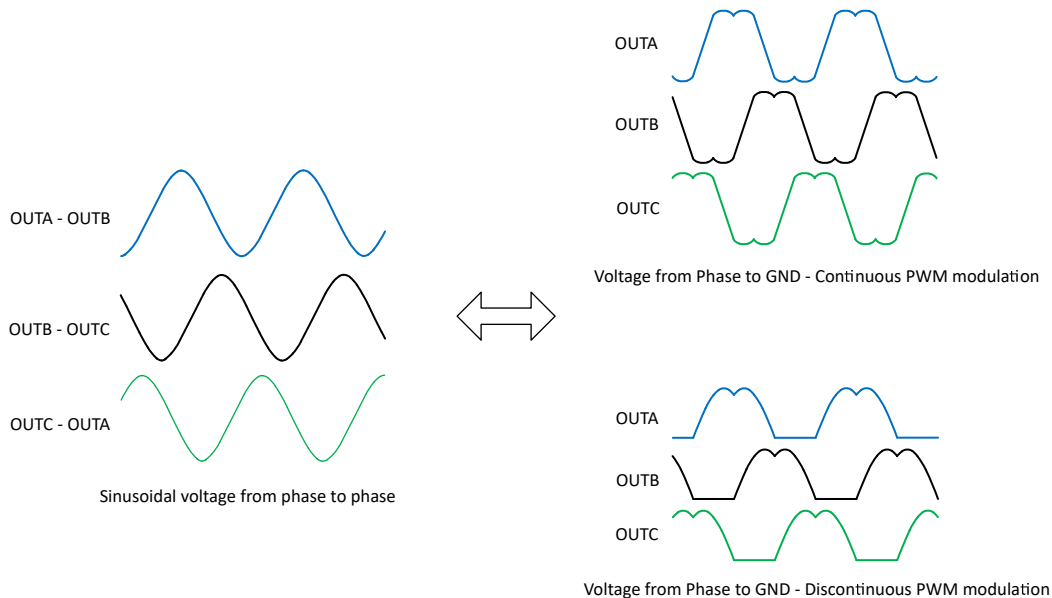


Figure 7-40. Continuous and Discontinuous PWM Modulation Phase Voltages

7.3.15 Dead Time Compensation

Dead time is inserted between the switching instants of high side and low side MOSFET in a half bridge leg to avoid shoot through condition. Due to dead time insertion, the expected voltage and applied voltage at the phase node differ based on the phase current direction. The phase node voltage distortion introduces undesired distortion in the phase current causing audible noise. The distortion in current waveform due to dead time appear as sixth harmonic of fundamental frequency in the dq reference frame. The MCF8316 integrates a proprietary dead time compensation using a resonant controller to control the sixth harmonic component in phase current to zero, ensuring that the current distortion due to dead time is alleviated. The resonant controller is employed in both i_q and i_d control paths. The dead time compensation can be enabled or disabled by configuring DEADTIME_COMP_EN.

7.3.16 Motor Stop Options

The MCF8316A provides different options for stopping the motor which can be configured by MTR_STOP.

7.3.16.1 Coast(Hi-Z) Mode

Coast(Hi-Z) mode is configured by setting MTR_STOP to 000b. When motor stop command is received, the MCF8316A will transition into a high impedance (Hi-Z) state by turning off all MOSFETs. When the MCF8316A device transitions from driving the motor into a Hi-z state, the inductive current in the motor windings continues to flow and the energy returns to the power supply through the intrinsic body diodes in the MOSFET output stage (see example [Figure 7-41](#)).

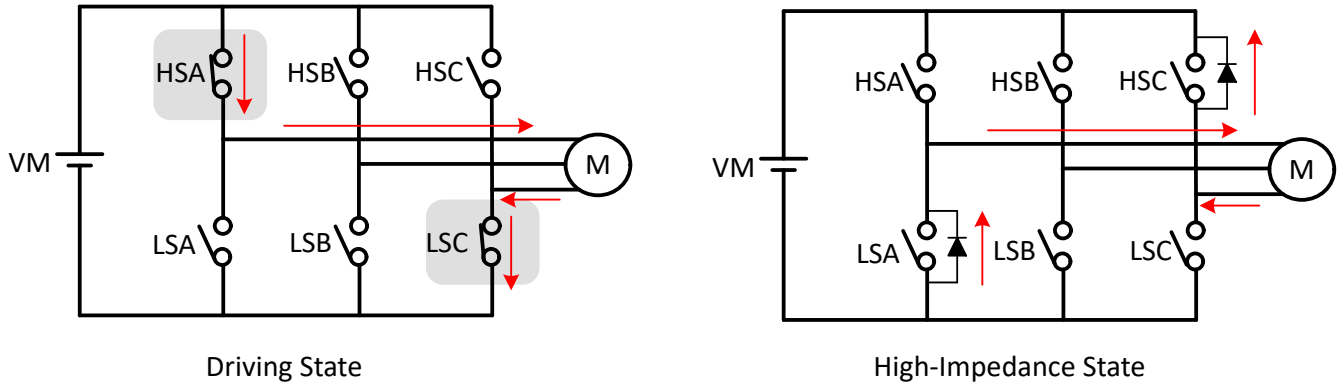


Figure 7-41. Coast(Hi-Z) Mode

In this example, current is applied to the motor through the high-side MOSFET (HSA) and returned through the low-side MOSFET (S6). When motor stop command is received all 6 MOSFETs transition to Hi-Z state and the inductive energy returns to supply through body diodes of MOSFETs S2 and S5.

7.3.16.2 Recirculation Mode

Recirculation mode is configured by setting MTR_STOP to 001b. In order to prevent the energy returning into supply, the MCF8316A allows current to circulate within the MOSFETs by turning OFF the MOSFET which is switching for fixed amount and then it transition into Hi-z by turning OFF remaining MOSFETs. The recirculation time is calculated by MCF8316A based on state of MOSFET and motor frequency.

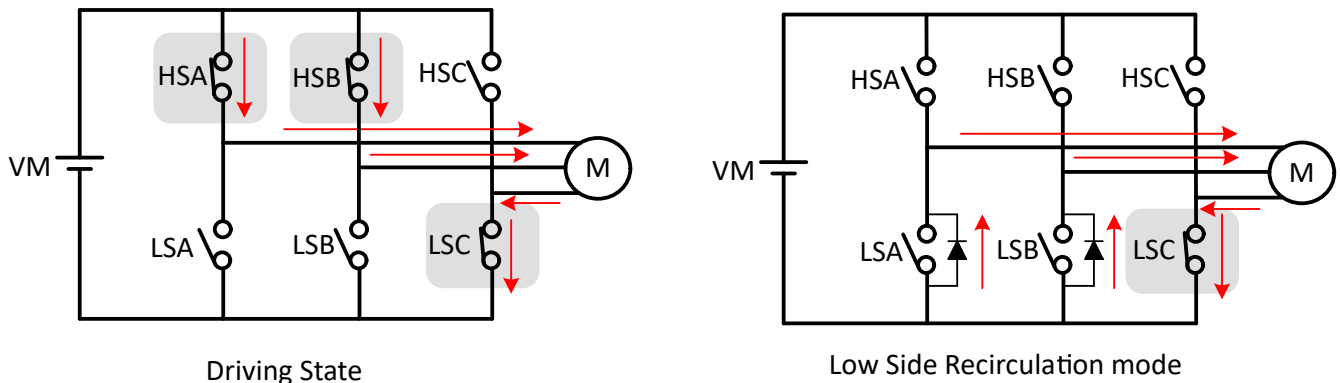


Figure 7-42. Low Side Recirculation

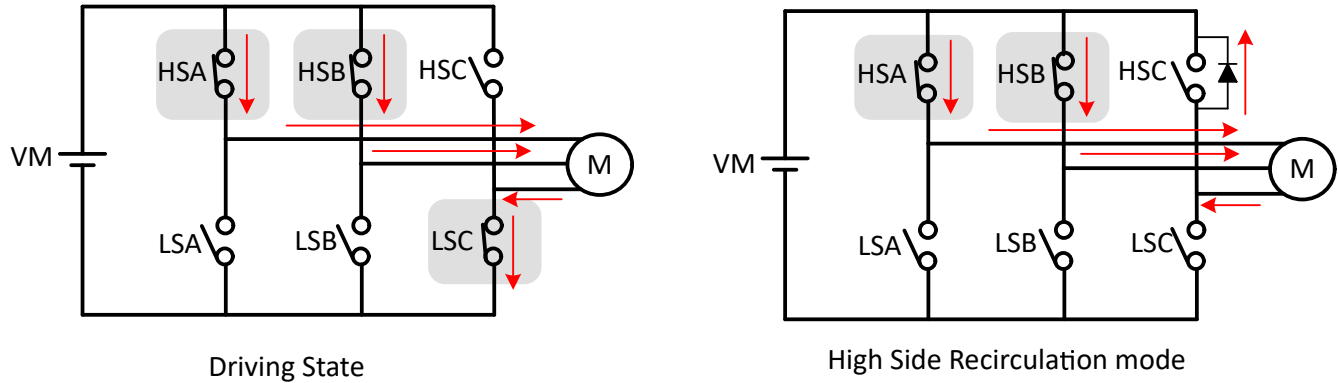


Figure 7-43. High Side Recirculation

7.3.16.3 Low Side Braking

Low side braking mode is configured by setting MTR_STOP to 010b. The MCF8316A can also enter low side braking through BRAKE pin. When stop command is received output speed is reduced to value defined by BRAKE_SPEED_THRESHOLD prior to turning all low side MOSFETs ON (see example Figure 7-44) for BRAKE_TIME time. If the motor speed is below BRAKE_SPEED_THRESHOLD prior to receiving stop command, then the MCF8316A transition directly into the brake state. After applying the brake state for BRAKE_TIME, the MCF8316A transitions into the Hi-Z state by turning OFF all MOSFETs.

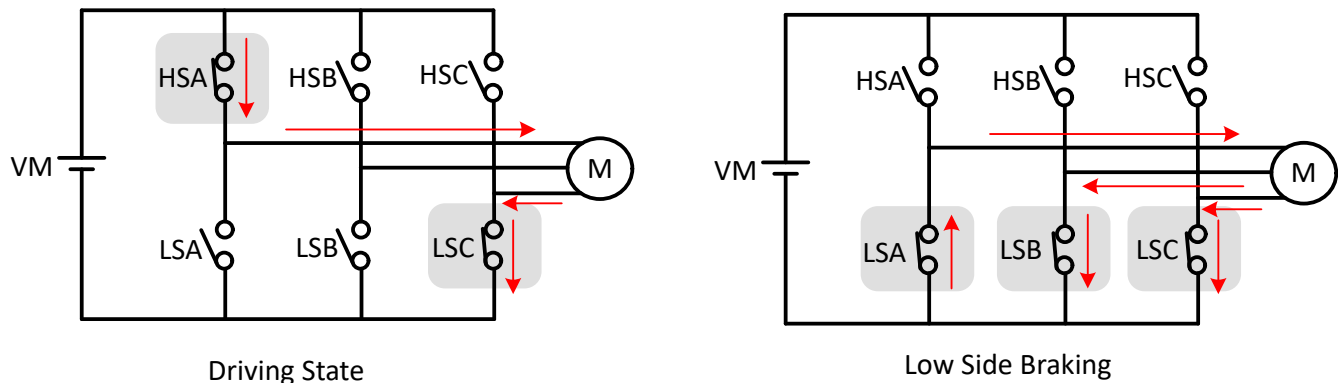


Figure 7-44. Low Side Braking

7.3.16.4 High Side Braking

High side braking mode is configured by setting MTR_STOP to 011b. When a motor stop command is received, the output speed is reduced to a value defined by BRAKE_SPEED_THRESHOLD prior to turning all high side MOSFETs ON (see example Figure 7-45) for BRAKE_TIME time. If the motor speed is below BRAKE_SPEED_THRESHOLD prior to receiving stop command, then the MCF8316A transition directly into the brake state. After applying the brake state for BRAKE_TIME, the MCF8316A transitions into Hi-Z state by turning OFF all MOSFETs.

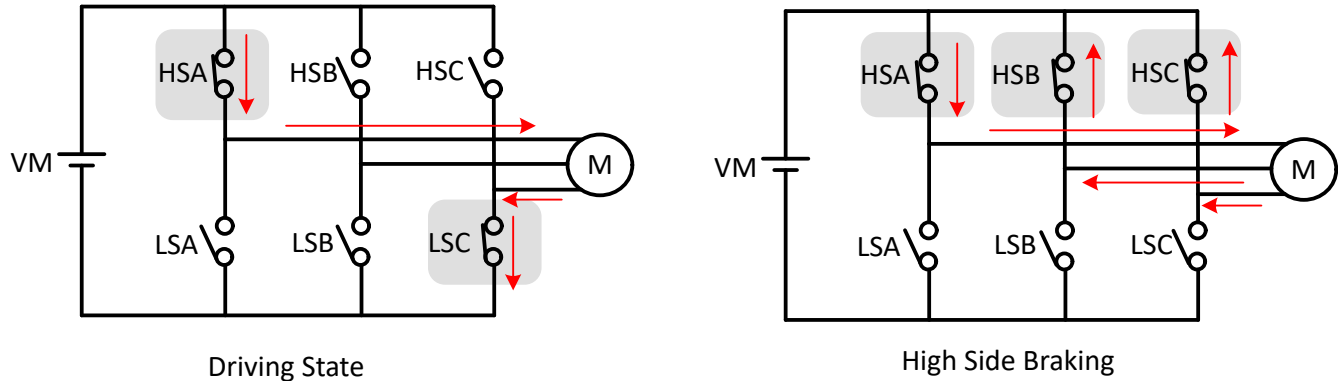


Figure 7-45. High Side Braking

7.3.16.5 Active Spin-Down

Active spin down mode is configured by setting MTR_STOP to 100b. When a motor stop command is received, the MCF8316A reduces SPEED_REF to a lower value configured using ACT_SPIN_THR and then it transition to a Hi-Z state. The advantage of this mode is that by reducing SPEED_REF, the motor is decelerated to lower speed and hence lowering the current in the motor. Now, when the motor transitions into Hi-Z state at lower speed, the energy transfer to the power supply is reduced. The threshold ACT_SPIN_BRK_THR needs to be configured such that it is not low enough for MCF8316A to synchronize with the motor and hit motor lock.

7.3.16.6 Align Braking

Align braking mode is configured by setting MTR_STOP to 101b. The MCF8316A can also enter align brake state through the BRAKE pin. In this mode, the MCF8316A aligns the motor by injecting a DC current through a particular phase pattern for a certain time (configured by ALIGN_TIME). The phase pattern during align is generated based on the angle at which align needs to be performed and it can be configured through ALIGN_ANGLE or the last commutation state. ALIGN_BRAKE_ANGLE_SEL can be configured to decide which align angle is used by the MCF8316A. The current limit threshold during align is configured through ALIGN_OR_SLOW_CURRENT_LIMIT.

7.3.17 PWM Output

The MCF8316A has the option to configure the output PWM switching frequency of the MOSFETs by configuring PWM_FREQ_OUT. PWM_FREQ_OUT has a range of 5-75 kHz. In order to select optimal output PWM frequency, user has to make a tradeoff between the current ripple and the switching losses. Generally, motors having a lower L/R ratio require higher PWM switching frequency to reduce current ripple.

The MCF8316A supports two different modulation techniques, i.e., continuous and discontinuous (see [PWM Modulation Schemes](#)). Continuous modulation helps with reducing current ripple for motors having low motor inductance but it has higher switching losses because all three phases are switching, while discontinuous mode has less losses due to only two phases switching at a time, but higher ripple in current. PWM modulation can be configured using PWM_MOD.

7.3.18 FG Customized Configuration

The MCF8316A device provides information about the motor speed through the *frequency generate* (FG) pin. In the MCF8316A, the FG pin is configured through FG_CONFIG. When FG_CONFIG is configured to 0 (Active FG mode), the FG output is active as long as the MCF8316A is driving the motor. When FG_CONFIG is configured to 1b (Extended FG mode), the MCF8316A provides an FG output until the motor back-EMF falls below FG_BEMF_THR.

7.3.18.1 FG Output Frequency

The FG output frequency can be configured by FG_DIV. Many applications require configuration of the FG output so that it provides a pulse corresponding with one mechanical rotation of the motor. The configuration bits provided in the MCF8316A can accomplish this for 2-pole up to 32-pole motors.

Figure 7-46 shows the MCF8316A device has been configured to provide FG pulses once every electrical cycle (2 poles), once every two electrical cycle (4 poles), once every three electrical cycles (6 poles), once every four electrical cycles (8 poles), and so on.

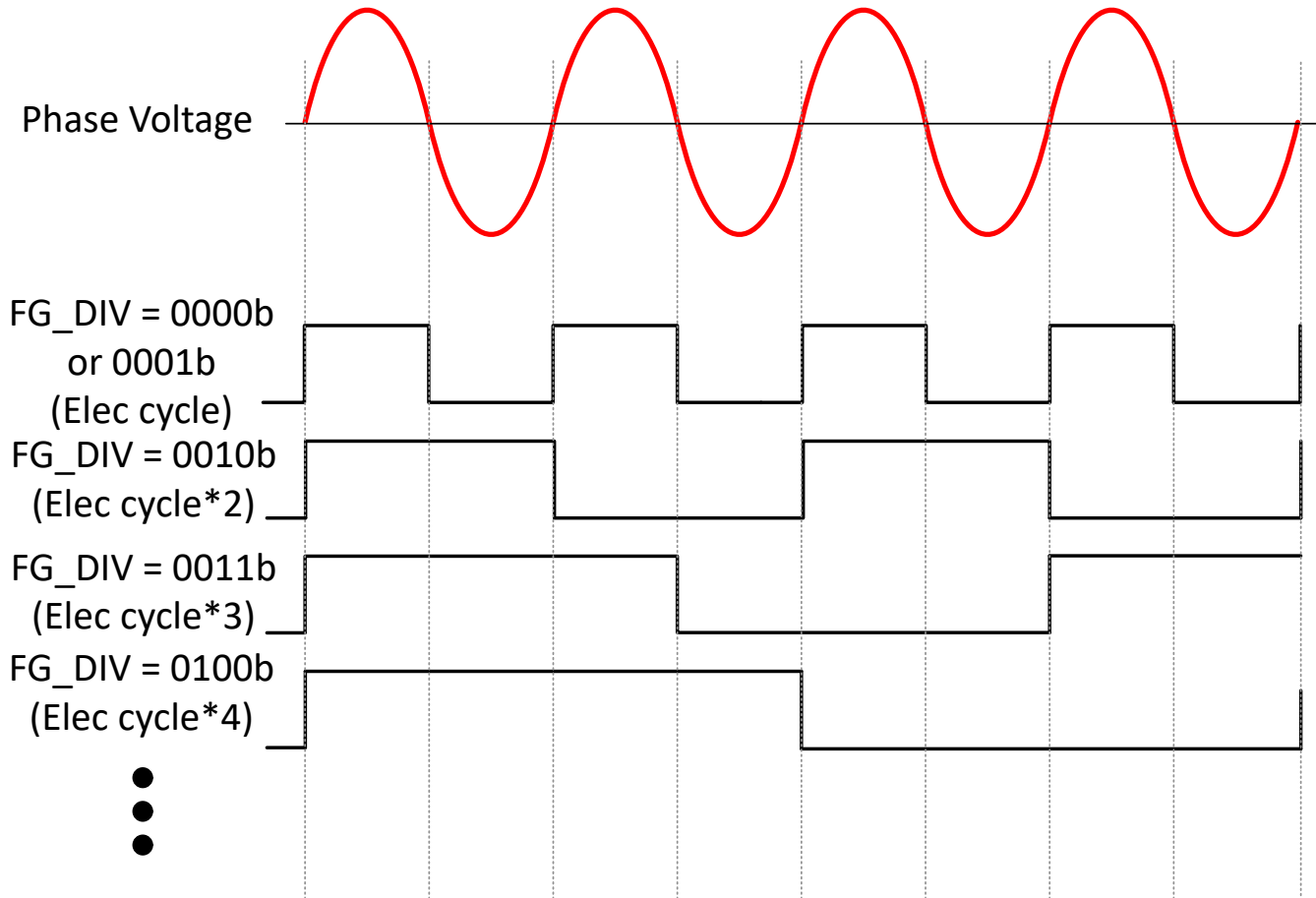


Figure 7-46. FG Frequency Divider

7.3.18.2 FG Open-Loop and Lock Behavior

Note that the FG output reflects the driving state of the motor. During normal closed loop behavior, the driving state and the actual state of the motor are synchronized. During open-loop acceleration, however, this may not reflect the actual motor speed. During a locked-motor condition, the FG output is driven high.

The MCF8316A provides three options for controlling the FG output during open loop, as shown in Figure 7-47. The selection of these options is determined by configuring the FG_Sel.

- 00b: When in open loop, the FG output is based on the driving frequency
- 01b: When in open loop, the FG output is not toggled and will be left high
- 10b: The FG output will reflect the first driving frequency with the first motor start at power on, but will be held high if the MCF8316A enters open loop after that (for example any subsequent motor starting events)

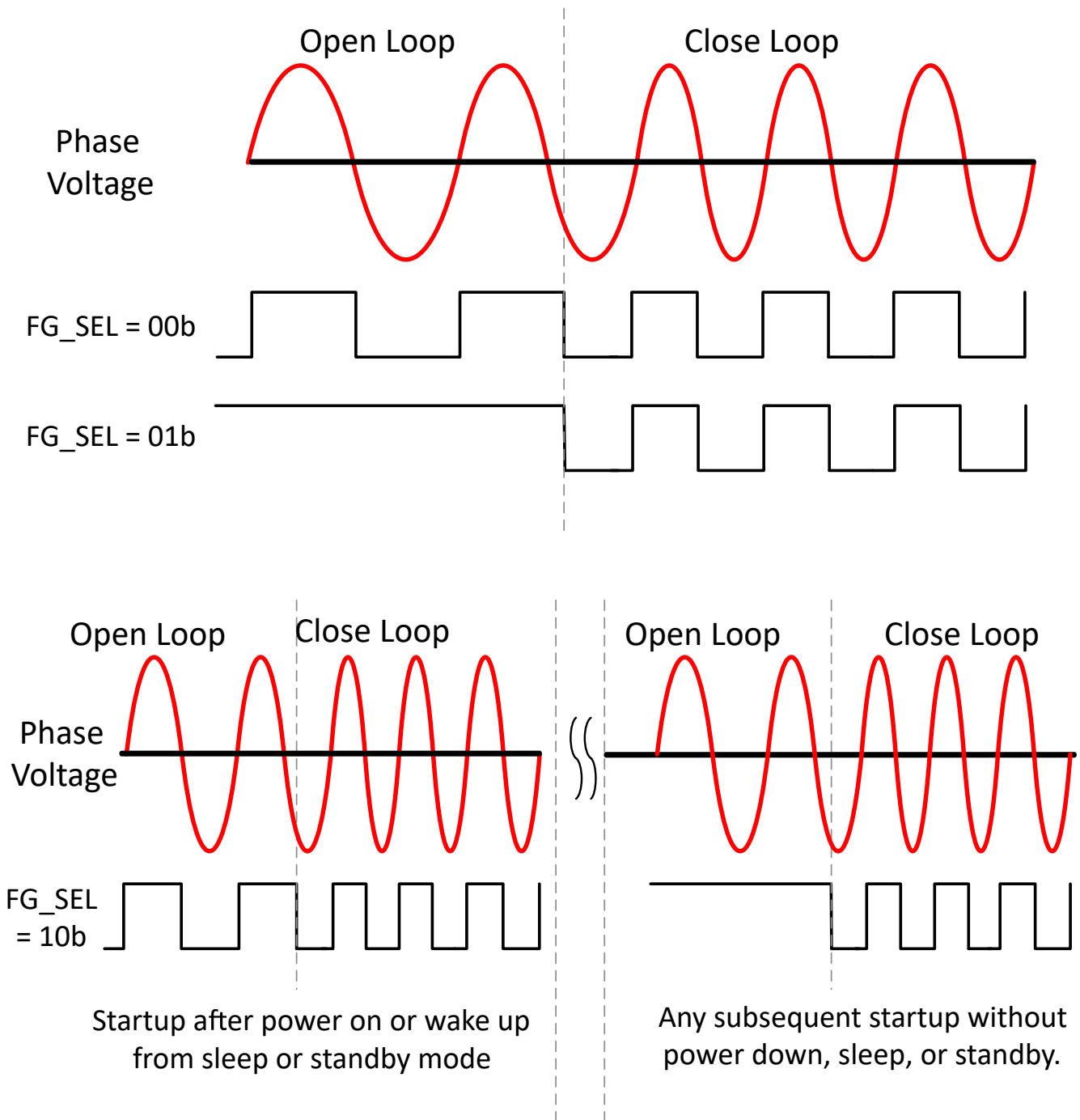


Figure 7-47. FG Behavior During Open Loop

7.3.19 Anti-Voltage Surge Function (AVS)

When a motor is driven, energy is transferred from the power supply into the motor. Some of this energy is stored in the form of inductive energy or as mechanical energy. If the speed command suddenly drops such that the BEMF voltage generated by the motor is greater than the voltage that is applied to the motor, then the mechanical energy of the motor is returned to the power supply and the V_M voltage surges. The AVS function works to prevent this from happening. AVS can be disabled through the register configuration AVS_EN. When AVS is disabled then deceleration rate is configured through CL_DEC_CONFIG

7.3.20 DC Bus Current Limit

The DC bus current limit feature can be used in applications to limit the current supplied by source without entering the constant current mode. The DC bus current limit feature can be enabled by setting `BUS_CURRENT_LIMIT_ENABLE`. The DC bus current limit threshold can be configured using `BUS_CURRENT_LIMIT`. The DC bus current limit limits the speed reference and a functional diagram is shown in [Figure 7-48](#). Enabling this feature may restricts the speed of the motor so that current drawn from source is limited. The algorithm estimates the bus current using the measured phase currents, phase voltage and DC bus voltage. The current limit status is reported on `BUS_CURRENT_LIMIT_STATUS`.

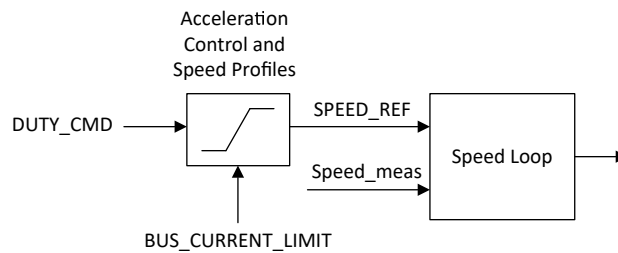


Figure 7-48. DC Bus Current Limit Functional Block Diagram

7.3.21 Protections

The family of devices is protected against Motor lock, VM undervoltage, charge pump undervoltage and Overcurrent events. [Table 7-5](#) summarizes various faults details.

Table 7-5. Fault Action and Response

FAULT	CONDITION	CONFIGURATION	REPORT	H-BRIDGE	LOGIC	RECOVERY
VM undervoltage (NPOR)	$V_{VM} < V_{UVLO}$	—	—	Hi-Z	Disabled	Automatic: $V_{VM} > V_{UVLO_R}$
AVDD undervoltage (NPOR)	$V_{AVDD} < V_{AVDD_UV}$	—	—	Hi-Z	Disabled	Automatic: $V_{AVDD} > V_{AVDD_UV_R}$
Buck undervoltage (BUCK_UV)	$V_{FB_BK} < V_{BK_UV}$	—	—	Hi-Z	Disabled	Automatic: $V_{FB_BK} > V_{BUCK_UV_R}$
Charge pump undervoltage (VCP_UV)	$V_{CP} < V_{CPLUV}$	—	nFAULT	Hi-Z	Active	Automatic: $V_{VCP} > V_{CPLUV}$
OverVoltage Protection (OVP)	$V_{VM} > V_{OVP}$	OVP_EN = 0b	None	Active	Active	No action (OVP Disabled)
		OVP_EN = 1b	FAULT	Hi-Z	Active	Automatic: $V_{VM} < V_{OVP}$
Overcurrent Protection (OCP)	$I_{PHASE} > I_{OCP}$	OCP_MODE = 00b	nFAULT	Hi-Z	Active	Latched: CLR_FLT
		OCP_MODE = 01b	nFAULT	Hi-Z	Active	Retry: t_{RETRY}
		OCP_MODE = 10b	nFAULT	Active	Active	No action
		OCP_MODE = 11b	None	Active	Active	No action
Buck Overcurrent Protection (BUCK_OCP)	$I_{BK} > I_{BK_OC}$	—	—	Hi-Z	Disabled	Retry: t_{RETRY}
Motor Lock (MTR_LCK)	Motor lock: Abnormal Speed; No Motor Lock; Abnormal BEMF	MTR_LCK_MODE = 0000b	nFAULT	Hi-Z	Active	Latched: CLR_FLT
		MTR_LCK_MODE = 0001b	nFAULT	Recirculation	Active	Latched: CLR_FLT
		MTR_LCK_MODE = 0010b	nFAULT	High side brake	Active	Latched: CLR_FLT
		MTR_LCK_MODE = 0011b	nFAULT	Low side brake	Active	Latched: CLR_FLT
		MTR_LCK_MODE = 0100b	nFAULT	Hi-Z	Active	Retry: t_{LCK_RETRY}
		MTR_LCK_MODE = 0101b	nFAULT	Recirculation	Active	Retry: t_{LCK_RETRY}
		MTR_LCK_MODE = 0110b	nFAULT	High side brake	Active	Retry: t_{LCK_RETRY}
		MTR_LCK_MODE = 0111b	nFAULT	Low side brake	Active	Retry: t_{LCK_RETRY}
		MTR_LCK_MODE = 1000b	nFAULT	Active	Active	No action
		MTR_LCK_MODE = 1xx1b	None	Active	Active	No action
Hardware Lock-Detection Current Limit (HW_LOCK_ILIMIT)	$V_{SOX} > HW_LOCK_ILIMIT$	HW_LOCK_ILIMIT_MOD E = 0000b	nFAULT	Hi-Z	Active	Latched: CLR_FLT
		HW_LOCK_ILIMIT_MOD E = 0001b	nFAULT	Recirculation	Active	Latched: CLR_FLT
		HW_LOCK_ILIMIT_MOD E = 0010b	nFAULT	High side brake	Active	Latched: CLR_FLT
		HW_LOCK_ILIMIT_MOD E = 0011b	nFAULT	Low side brake	Active	Latched: CLR_FLT
		HW_LOCK_ILIMIT_MOD E = 0100b	nFAULT	Hi-Z	Active	Retry: t_{LCK_RETRY}
		HW_LOCK_ILIMIT_MOD E = 0101b	nFAULT	Recirculation	Active	Retry: t_{LCK_RETRY}
		HW_LOCK_ILIMIT_MOD E = 0110b	nFAULT	High side brake	Active	Retry: t_{LCK_RETRY}
		HW_LOCK_ILIMIT_MOD E = 0111b	nFAULT	Low side brake	Active	Retry: t_{LCK_RETRY}
		HW_LOCK_ILIMIT_MOD E = 1000b	nFAULT	Active	Active	No action
		HW_LOCK_ILIMIT_MOD E = 1xx1b	None	Active	Active	No action

Table 7-5. Fault Action and Response (continued)

FAULT	CONDITION	CONFIGURATION	REPORT	H-BRIDGE	LOGIC	RECOVERY
Software Lock-Detection Current Limit (LOCK_ILIMIT)	$V_{sox} > LOCK_ILIMIT$	LOCK_ILIMIT_MODE = 0000b	nFAULT	Hi-Z	Active	Latched: CLR_FLT
		LOCK_ILIMIT_MODE = 0001b	nFAULT	Recirculation	Active	Latched: CLR_FLT
		LOCK_ILIMIT_MODE = 0010b	nFAULT	High side brake	Active	Latched: CLR_FLT
		LOCK_ILIMIT_MODE = 0011b	nFAULT	Low side brake	Active	Latched: CLR_FLT
		LOCK_ILIMIT_MODE = 0100b	nFAULT	Hi-Z	Active	Retry: t_{CLK_RETRY}
		LOCK_ILIMIT_MODE = 0101b	nFAULT	Recirculation	Active	Retry: t_{CLK_RETRY}
		LOCK_ILIMIT_MODE = 0110b	nFAULT	High side brake	Active	Retry: t_{CLK_RETRY}
		LOCK_ILIMIT_MODE = 0111b	nFAULT	Low side brake	Active	Retry: t_{CLK_RETRY}
		LOCK_ILIMIT_MODE = 1000b	nFAULT	Active	Active	No action
		LOCK_ILIMIT_MODE = 1xx1b	None	Active	Active	No action
IPD Timeout Fault (IPD_T1_FAULT and IPD_T2_FAULT)	IPD TIME > 500ms (approx), during IPD current ramp up or ramp down	IPD_TIMEOUT_FAULT_EN = 1	nFAULT	Hi-Z	Active	Latched: CLR_FLT
IP Frequency Fault (IPD_FREQ_FAULT)	IPD pulse before the current decay in previous IPD	IPD_FREQ_FAULT_EN = 1	nFAULT	Hi-Z	Active	Latched: CLR_FLT
MPET IPD Fault (MPET_IPD_FAULT)	Same as IPD Timeout Fault.	MPET_CMD = 1 MPET_R or MPET_L = 1	nFAULT	Hi-Z	Active	Latched: CLR_FLT
MPET Back-EMF Fault (MPET_BEMF_FAULT)	Motor Back EMF < STAT_DETECT_THR	MPET_CMD = 1 MPET_KE = 1	nFAULT	Hi-Z	Active	Latched: CLR_FLT
Thermal warning (OTW)	$T_J > T_{OTW}$	OTW_REP = 0b	None	Active	Active	No action
		OTW_REP = 1b	nFAULT	Active	Active	Automatic: $T_J < T_{OTW} - T_{HYS}$ CLR_FLT
Thermal shutdown (OTSD)	$T_J > T_{OTSD}$	—	nFAULT	Hi-Z	Active	Automatic: $T_J < T_{OTSD} - T_{HYS}$ CLR_FLT

ADVANCE INFORMATION

7.3.21.1 VM Supply Undervoltage Lockout

If at any time the input supply voltage on the VM pin falls lower than the V_{UVLO} threshold (VM UVLO falling threshold), all of the integrated FETs, driver charge-pump and digital logic are disabled as shown in Figure 7-49. MCF8316A goes into reset state whenever VM UVLO event occurs.

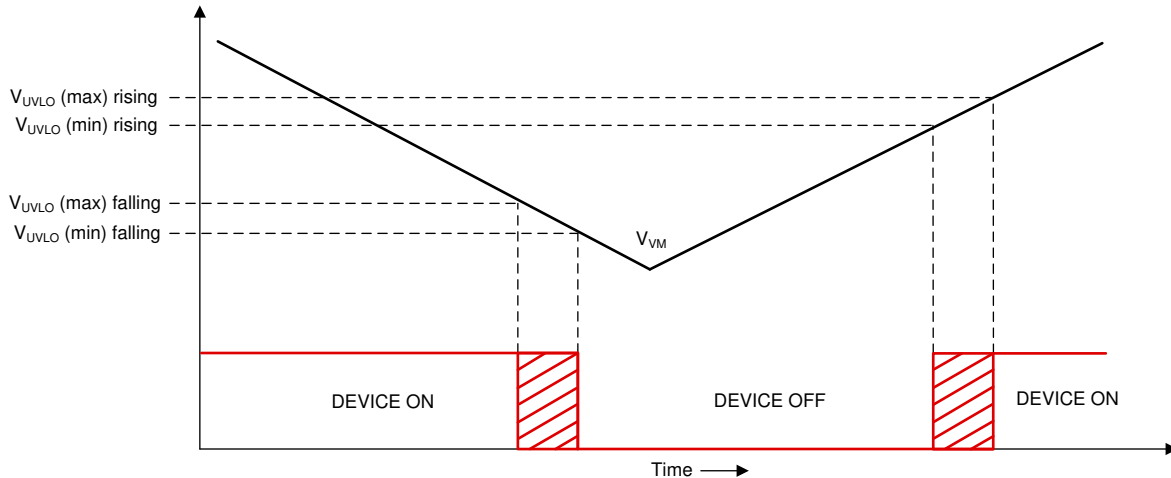


Figure 7-49. VM Supply Undervoltage Lockout

7.3.21.2 AVDD Undervoltage Lockout (AVDD_UV)

If at any time the voltage on AVDD pin falls lower than the V_{AVDD_UV} threshold, all of the integrated FETs, driver charge-pump and digital logic controller are disabled. Internal circuitry in MCF8316A is powered through AVDD regulator, MCF8316A goes into reset state whenever AVDD UV event occurs.

7.3.21.3 BUCK Undervoltage Lockout (BUCK_UV)

If at any time the input supply voltage on the FB_BK pin falls lower than the V_{BK_UVLO} threshold, both the high-side and low-side MOSFETs of the buck regulator are disabled. Internal circuitry in MCF8316A is powered through buck regulator, MCF8316A goes into reset state whenever buck UV event occurs.

7.3.21.4 VCP Charge Pump Undervoltage Lockout (CPUV)

If at any time the voltage on the VCP pin (charge pump) falls lower than the V_{CPUV} threshold voltage of the charge pump, all of the integrated FETs are disabled and the nFAULT pin is driven low. The FAULT and VCP_UV bits are also latched high in the registers. Normal operation starts again (driver operation and the nFAULT pin is released) when the VCP undervoltage condition clears. The CPUV bit stays set until cleared through the CLR_FLT bit.

7.3.21.5 Overvoltage Protections (OV)

If at any time input supply voltage on the VM pins rises higher lower than the V_{OVP} threshold voltage, all of the integrated FETs are disabled and the nFAULT pin is driven low. The FAULT and OVP bits are also latched high in the registers. Normal operation starts again (driver operation and the nFAULT pin is released) when the OVP condition clears. The OVP bit stays set until cleared through the CLR_FLT bit. Setting the OVP_EN bit high enables this protection feature.

The OVP threshold can be set to 20-V or 32-V based on the OVP_SEL bit.

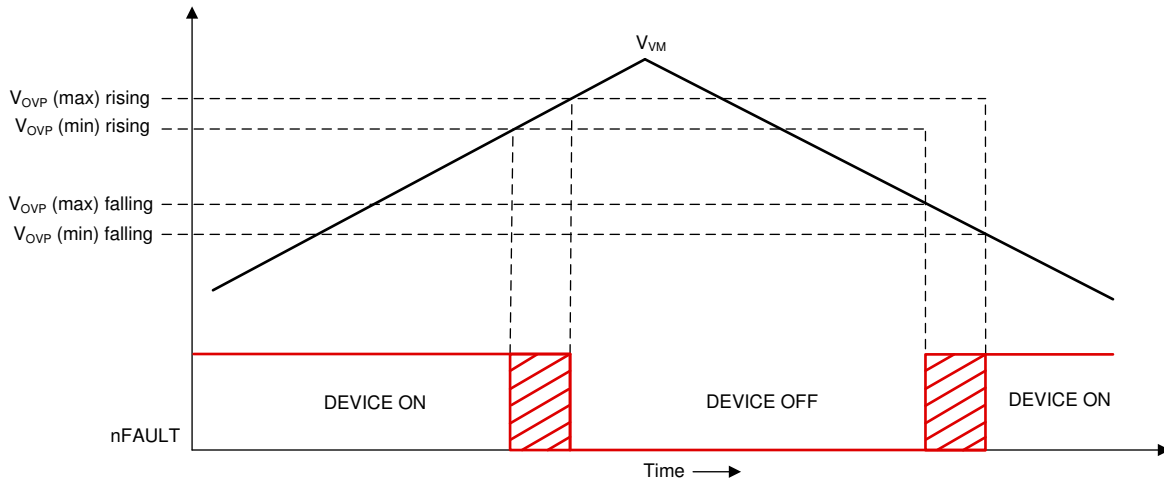


Figure 7-50. Over Voltage Protection

7.3.21.6 Overcurrent Protection (OCP)

A MOSFET overcurrent event is sensed by monitoring the current flowing through FETs. If the current across a FET exceeds the I_{OCP} threshold for longer than the t_{OCP} deglitch time, a OCP event is recognized and action is done according to the OCP_MODE bit. The I_{OCP} threshold is set through the OCP_LVL, the t_{OCP_DEG} is set through the OCP_DEG and the OCP_MODE bit can operate in four different modes: OCP latched shutdown, OCP automatic retry, OCP report only, and OCP disabled.

7.3.21.6.1 OCP Latched Shutdown (OCP_MODE = 00b)

After a OCP event in this mode, all MOSFETs are disabled and the nFAULT pin is driven low. The FAULT, OCP, and corresponding FET's OCP bits are latched high in the registers. Normal operation starts again (driver operation and the nFAULT pin is released) when the OCP condition clears and a clear faults command is issued through the CLR_FLT bit.

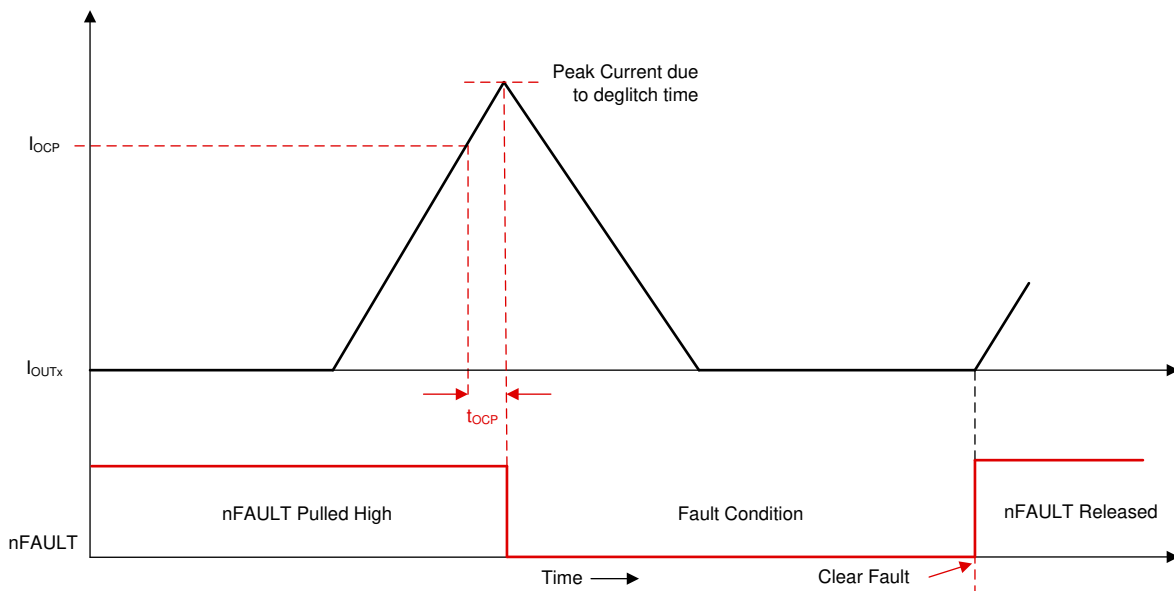


Figure 7-51. Overcurrent Protection - Latched Shutdown Mode

7.3.21.6.2 OCP Automatic Retry (OCP_MODE = 01b)

After a OCP event in this mode, all the FETs are disabled and the nFAULT pin is driven low. The FAULT, OCP, and corresponding FET's OCP bits are latched high. Normal operation starts again automatically (driver operation and the nFAULT pin is released) after the t_{RETRY} time elapses. The FAULT bits stay latched until the t_{RETRY} period expires. The OCP, and corresponding FET's OCP bits are latched high until cleared through the CLR_FLT bit.

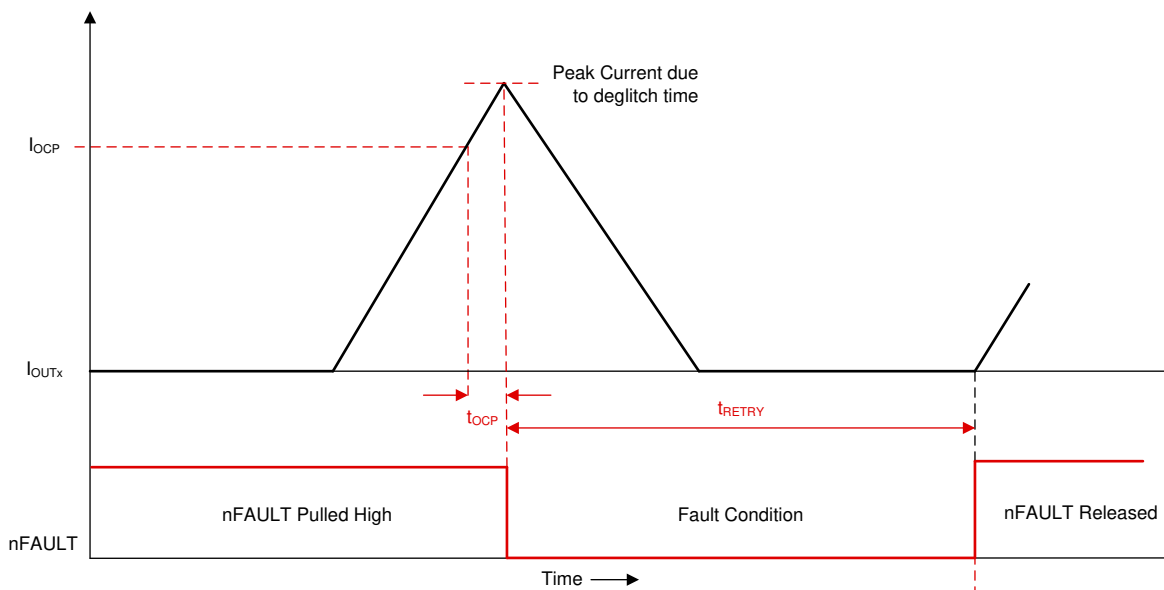


Figure 7-52. Overcurrent Protection - Automatic Retry Mode

7.3.21.6.3 OCP Report Only (OCP_MODE = 10b)

No protective action occurs after a OCP event in this mode. The overcurrent event is reported by driving the nFAULT pin low and latching the FAULT, OCP, and corresponding FET's OCP bits high. The device continue to operate as usual. The external controller manages the overcurrent condition by acting appropriately. The reporting clears (nFAULT pin is released) when the OCP condition clears and a clear faults command is issued through the CLR_FLT bit.

7.3.21.6.4 OCP Disabled (OCP_MODE = 11b)

No action occurs after a OCP event in this mode.

7.3.21.7 Buck Overcurrent Protection

The buck overcurrent event is sensed by monitoring the current flowing through high-side MOSFET of the buck regulator. If the current across high-side MOSFET exceeds the I_{BK_OCP} threshold for longer than the t_{OCP_DEG} deglitch time, a buck OCP event is recognized. Internal circuitry in MCF8316A is powered through buck regulator, MCF8316A goes into reset state whenever buck OCP event occurs.

7.3.21.8 Hardware Lock Detection Current Limit (HW_LOCK_ILIMIT)

The lock-detection current-limit function provides a configurable threshold for limiting the current to prevent damage to the system. The output of current sense amplifier is connected to hardware comparator. If at any time the voltage on the output of CSA exceeds threshold HW_LOCK_ILIMIT longer than $t_{HW_LOCK_ILIMIT}$ a HW_LOCK_ILIMIT event is recognized and action is done according to the HW_LOCK_ILIMIT_MODE bit. The threshold is set through the HW_LOCK_ILIMIT register, the $t_{HW_LCK_ILIMIT}$ is set through the HW_LOCK_ILIMIT_DEG. HW_LOCK_ILIMIT_MODE bit can operate in four different modes: HW_LOCK_ILIMIT latched shutdown, HW_LOCK_ILIMIT automatic retry, HW_LOCK_ILIMIT report only, and HW_LOCK_ILIMIT disabled.

7.3.21.8.1 HW_LOCK_ILIMIT Latched Shutdown (HW_LOCK_ILIMIT_MODE = 00xxb)

After a HW_LOCK_ILIMIT event in this mode, the status of MOSFET will be configured by LOCK_ILIMIT_MODE and nFAULT is driven low. Status of MOSFET during HW_LOCK_ILIMIT:

- HW_LOCK_ILIMIT_MODE = 0000b: All MOSFETs are disabled
- HW_LOCK_ILIMIT_MODE = 0001b: MOSFET which was switching is disabled while the one which was conducting stays ON to recirculate inductive energy
- HW_LOCK_ILIMIT_MODE = 0010b: All high side MOSFETs are turned ON
- HW_LOCK_ILIMIT_MODE = 0011b: All low side MOSFETs are turned ON

The FAULT and HW_LOCK_ILIMIT bits are latched high in the registers. Normal operation starts again (driver operation and the nFAULT pin is released) when the HW_LOCK_ILIMIT condition clears and a clear faults command is issued through the CLR_FLT bit.

7.3.21.8.2 HW_LOCK_ILIMIT Automatic recovery (HW_LOCK_ILIMIT_MODE = 01xxb)

After a HW_LOCK_ILIMIT event in this mode, the status of MOSFET will be configured by HW_LOCK_ILIMIT_MODE and nFAULT is driven low. Status of MOSFET during HW_LOCK_ILIMIT:

- HW_LOCK_ILIMIT_MODE = 0100b: All MOSFETs are disabled
- HW_LOCK_ILIMIT_MODE = 0101b: MOSFET which was switching is disabled while the one which was conducting stays ON to recirculate inductive energy
- HW_LOCK_ILIMIT_MODE = 0110b: All high side MOSFETs are turned ON
- HW_LOCK_ILIMIT_MODE = 0111b: All low side MOSFETs are turned ON

The FAULT and HW_LOCK_ILIMIT bits are latched high in the registers. Normal operation starts again automatically (gate driver operation and the nFAULT pin is released) after the t_{LCK_RETRY} time elapses. The FAULT bit stay latched until the t_{LCK_RETRY} period expires. The HW_LOCK_ILIMIT bit stay latched until cleared through the CLR_FLT bit.

7.3.21.8.3 HW_LOCK_ILIMIT Report Only (HW_LOCK_ILIMIT_MODE = 1000b)

No protective action occurs after a HW_LOCK_ILIMIT event in this mode. The lock detection current limit event is reported by driving the nFAULT pin low and latching the FAULT and HW_LOCK_ILIMIT bits high in the registers. The gate drivers continue to operate. The external controller manages this condition by acting appropriately. The reporting clears (nFAULT released) when the HW_LOCK_ILIMIT condition clears and a clear faults command is issued through the CLR_FLT bit.

7.3.21.8.4 HW_LOCK_ILIMIT Disabled (HW_LOCK_ILIMIT_MODE= 1xx1b)

No action occurs after a HW_LOCK_ILIMIT event in this mode.

7.3.21.9 Thermal Warning (OTW)

If the die temperature exceeds the trip point of the thermal warning (T_{OTW}), the OT bit and OTW bit in the status register is set. The reporting of OTW on the nFAULT pin can be enabled by setting the over-temperature warning reporting (OTW_REP) bit in the configuration control register. The device performs no additional action and continues to function. In this case, the nFAULT pin releases when the die temperature decreases below the hysteresis point of the thermal warning (T_{OTW_HYS}). The OTW bit remains set until cleared through the CLR_FLT bit and the die temperature is lower than thermal warning trip (T_{OTW}).

Note

Over Temperature warning is not reported on nFAULT pin by default.

7.3.21.10 Thermal Shutdown (OTS)

If the die temperature exceeds the trip point of the thermal shutdown limit (T_{OTS}), all the FETs are disabled, the charge pump is shut down, and the nFAULT pin is driven low. In addition, the FAULT, OT and OTS bit in the status register is set. Normal operation starts again (driver operation and the nFAULT pin is released) when the overtemperature condition clears. The OTS bit stays latched high indicating that a thermal event occurred until a clear fault command is issued through the CLR_FLT bit. This protection feature cannot be disabled.

7.3.21.11 Motor Lock (MTR_LCK)

When a event of motor lock condition is detected, the MCF8316A takes action according to MTR_LOCK_MODE bits. The MCF8316A device continuously check for motor lock conditions (see [Motor Lock Detection](#), when one of the enabled lock is triggered, a MTR_LCK event is recognized and action is done according to the MTR_LCK_MODE.

All locks can be enabled or disabled individually and retry times can be configured through LCK_RETRY . MTR_LCK_MODE bit can operate in four different modes: MTR_LCK latched shutdown, MTR_LCK automatic retry, MTR_LCK report only, and MTR_LCK disabled.

7.3.21.11.1 MTR_LCK Latched Shutdown (MTR_LCK_MODE = 00xxb)

After a MTR_LCK event in this mode, the status of MOSFET will be configured by MTR_LCK_MODE and nFAULT is driven low. Status of MOSFET during MTR_LCK:

- MTR_LCK_MODE = 0000b: All MOSFETs are disabled
- MTR_LCK_MODE = 0001b: MOSFET which was switching is disabled while the one which was conducting stays ON to recirculate inductive energy
- MTR_LCK_MODE = 0010b: All high side MOSFETs are turned ON
- MTR_LCK_MODE = 0011b: All low side MOSFETs are turned ON

The FAULT, MTR_LCK and respective motor lock bits are latched high in the registers. Normal operation starts again (gate driver operation and the nFAULT pin is released) when the MTR_LCK condition clears and a clear faults command is issued through the CLR_FLT bit.

7.3.21.11.2 MTR_LCK Automatic recovery (MTR_LCK_MODE= 01xxb)

After a MTR_LCK event in this mode, the status of MOSFET will be configured by MTR_LCK_MODE and nFAULT is driven low. Status of MOSFET during MTR_LCK:

- MTR_LCK_MODE = 0100b: All MOSFETs are disabled
- MTR_LCK_MODE = 0101b: MOSFET which was switching is disabled while the one which was conducting stays ON to recirculate inductive energy
- MTR_LCK_MODE = 0110b: All high side MOSFETs are turned ON
- MTR_LCK_MODE = 0111b: All low side MOSFETs are turned ON

The FAULT, MTR_LCK and respective motor lock bits are latched high in the registers. Normal operation starts again automatically (gate driver operation and the nFAULT pin is released) after the t_{LCK_RETRY} time elapses. The FAULT bit stay latched until the t_{LCK_RETRY} period expires. The MTR_LCK and respective motor lock bits stay latched until cleared through the CLR_FLT bit..

7.3.21.11.3 MTR_LCK Report Only (MTR_LCK_MODE = 1000b)

No protective action occurs after a MTR_LCK event in this mode. The motor lock event is reported by driving the nFAULT pin low and latching the FAULT, MTR_LCK and respective motor lock bits high in the registers. The gate drivers continue to operate. The external controller manages this condition by acting appropriately. The reporting clears (nFAULT released) when the MTR_LCK condition clears and a clear faults command is issued through the CLR_FLT bit.

7.3.21.11.4 MTR_LCK Disabled (MTR_LCK_MODE = 1xx1b)

No action occurs after a MTR_LCK event in this mode.

7.3.21.12 Motor Lock Detection

The MCF8316A device provides several options for determining if the motor becomes locked as a result of some excessive external torque. Several schemes work together to ensure the lock condition is detected quickly and reliably. In addition to detecting if there is a locked motor condition, the MCF8316A device also identifies and takes action if there is no motor connected to the system. Each of the lock-detect schemes and the no-motor detection can be disabled by their respective register bits.

7.3.21.12.1 Lock1: Abnormal Speed (ABN_SPEED)

MCF8316A monitors the speed continuously and at any time the speed exceeds threshold LOCK_ABN_SPEED, a ABN_SPEED lock event is recognized and action is done according to the MTR_LCK_MODE.

The The threshold is set through the ABN_SPD_THR register. ABN_SPEED lock functionality can be enabled/disabled by LOCK1_EN

7.3.21.12.2 Lock2: Abnormal BEMF (ABN_BEMF)

MCF8316A estimated back-EMF in order to run motor optimally in closed loop. This estimated back-EMF is compared against the expected back-EMF calculated using the estimated speed and the BEMF constant. Whenever motor is stalled the estimated back-EMF is inaccurate due to lower back-EMF at low speed. When the difference between estimated and expected back-EMF exceeds ABNORMAL_BEMF_THR, an abnormal BEMF fault is triggered and action is taken according to the MTR_LCK_MODE.

ABN_BEMF lock functionality can be enabled/disabled by LOCK2_EN

7.3.21.12.3 Lock3: No-Motor Fault (NO_MTR)

The MCF8316A continuously low side phase current on all three phases and at any time if it falls below threshold NO_MTR_THR then the NO_MTR event is recognized. The response to NO_MRT event is configured through MTR_LOCK_MODE .

The threshold is set through the NO_MTR_THR register. NO_MTR lock functionality can be enabled/disabled by LOCK3_EN

7.3.21.13 MPET Faults

An error during resistance and inductance measurement is reported using MPET_IPD_FAULT. The MPET_IPD_FAULT gets triggered when the IPD timer overflows due to unsuccessful attempt to ramp up the current to the threshold value, same as explained in [Section 7.3.21.14](#). The fault typically gets triggered when there is no motor connected to MCF8316 or when the MPET IPD current threshold is set high for motors with high resistance.

An error during BEMF constant measurement is reported using MPET_BEMF_FAULT. This fault gets triggered when the measured back EMF is less than the threshold set in STAT_DETECT_THR. One example of such fault scenario can be the motor stall while running in open loop due to incorrect open loop configuration used.

7.3.21.14 IPD Faults

The MCF8316 uses 12-bit timers to estimate the time during the current ramp up and ramp down during IPD, when the motor startup is configured as IPD (MTR_STRATUP = IPD). During IPD, the algorithm check for a successful current ramp-up upto IPD_CURR_THR, starting with an IPD clock of 10MHz and if unsuccessful repeat with other clocks of 1MHz, 100kHz, and 10kHz sequentially. If the IPD timer overflows (current does not reach IPD_CURR_THR) in all the four trials , then the IPD_T1_FAULT gets triggered. Similarly the algorithm check for a successful current decay to zero during IPD current ramp down using all the mentioned IPD clock frequencies. If the IPD timer overflows (current doesnot ramp down to zero) in all the four trials, then the IPD_T2_FAULT gets triggered. The IPD time out during current ramp up and ramp down is approximately 500ms. The user can enable IPD timeout (IPD timer overflow) by configuring IPD_TIMEOUT_FAULT_EN.

IPD gives incorrect results if the next IPD pulse is commanded before the complete decay of current due to present IPD pulse. The MCF8316A can generate a fault during such a scenario by enabling IPD_FREQ_FAULT_EN. The user can use enable the IPD frequency fault especially if IPD frequency is too high for the set IPD current limit and the IPD release mode.

7.4 Device Functional Modes

7.4.1 Functional Modes

7.4.1.1 Sleep Mode

In sleep mode, all FETs are disabled, sense amplifiers are disabled, buck regulator is disabled, the charge pump is disabled, the AVDD regulator is disabled, and the I²C bus is disabled. The device can be configured to be in sleep mode by configuring register bits DEV_MODE. SPEED pin determines entry and exit from sleep state.

In sleep mode and when $V_{VM} < V_{UVLO}$, all MOSFETs are disabled.

Note

During power up and power down of the device, the nFAULT pin is held low as the internal regulators are enable or disable. After the regulators have enabled or disabled, the nFAULT pin is automatically released.

7.4.1.2 Operating Mode

In standby mode the charge pump, AVDD and Buck regulator, and I²C bus are active. The device can be configured to be in standby mode by configuring register bits DEV_MODE. SPEED pin determines entry and exit from standby state as described in [Table 7-6](#)

7.4.1.3 Fault Reset (CLR_FLT)

In the case of device latched faults, the device goes to a partial shutdown state to help protect the power MOSFETs and system. When the fault condition clears, the device can go to the operating state again by setting the CLR_FLT.

Table 7-6. Conditions to Enter or Exit Sleep or Standby Modes

SPEED COMMAND MODE	ENTER STANDBY CONDITION	ENTER SLEEP CONDITION	EXIT FROM STANDBY CONDITION	EXIT FROM SLEEP CONDITION
Analog	SPEED pin voltage $< V_{EN_SB}$ for $t_{EN_SB_ANA}$	SPEED pin voltage $< V_{EN_SL}$ for $t_{EN_SL_ANA}$	SPEED pin voltage $> V_{EX_SB}$ for $t_{EX_SB_ANA}$	SPEED pin voltage $> V_{EX_SL}$ for $t_{EX_SL_ANA}$ or
PWM	SPEED pin low ($V < V_{DIG_IL}$) for $t_{EN_SB_PWM}$	SPEED pin low ($V < V_{DIG_IL}$) for $t_{EN_SL_PWM}$	SPEED pin high ($V > V_{DIG_IH}$) for $t_{EX_SB_PWM}$	SPEED pin high ($V > V_{DIG_IH}$) for $t_{EX_SL_PWM}$
I ² C	DIGITAL_SPEED_CTRL is programmed as 0.	DIGITAL_SPEED_CTRL and OVERRIDE are configured as 0 and SPEED pin voltage $< V_{EN_SL}$ for $t_{EN_SL_ANA}$ (Analog Mode) SPEED pin low ($V < V_{DIG_IL}$) for $t_{EN_SL_PWM}$ (PWM mode)	DIGITAL_SPEED_CTRL is programmed as non-zero.	SPEED pin voltage $> V_{EX_SL}$ for $t_{EX_SL_ANA}$ (Analog mode) or SPEED pin high ($V > V_{DIG_IH}$) for $t_{EX_SL_PWM}$ (PWM mode)

7.5 External Interface

7.5.1 DRVOFF functionality

When DRVOFF pin is high, all six MOSFETs are disabled. In this mode if SPEED pin is high, the charge pump, AVDD regulator, Buck Regulator and I²C bus are active, driver related faults like OCP will be inactive.

7.5.2 DAC output

MCF8316A has two 12-bits DAC which outputs analog voltage equivalent of digital variables on DACOUT1 and DACOUT2 pins with resolution of 12 bits and max voltage is 3V. Signals available on DACOUT pins is useful in tracking algorithm variables in real time and can be used for tuning speed controller or other driver configuration or bus current monitoring. The address for variables for DACOUT1 and DACOUT2 are configured using register bits DACOUT1_VAR_ADDR and DACOUT2_VAR_ADDR. The device pins should be configured as DACOUT1 and DACOUT2 using PIN_36_37_CONFIG or PIN_38_CONFIG.

7.5.3 SOx output

MCF8316A can output the signals from built-in current sense amplifiers on SOx pin. Register bits PIN_38_CONFIG should be configured to select CSA output on SOx pin.

7.5.4 Oscillator Source

MCF8316A devices has built-in oscillator and is used as clock source for all digital peripherals and timing measurements. Default configuration for MCF8316A is to use internal oscillator and it is sufficient to drive motor without need of any external crystal or clock sources.

In case MCF8316A does not meet accuracy requirements of timing measurement or speed loop accuracy then MCF8316A has options to support crystal oscillator or external clock reference.

In order to improve EMI performance, MCF8316A provides option of modulating the clock frequency by enabling Spread Spectrum Modulation (SSM) through SSM_EN bit.

7.5.4.1 External Crystal Oscillator mode

MCF8316A has optional crystal oscillator which can support external crystal with frequency of 32.768kHz (f_{OSCXT}). External crystal oscillator can be used in case more accuracy is needed compared to internal oscillator. Connect external crystal between pins X1 and X2 as shown in Figure 7-53. In external crystal oscillator mode internal clock will be calibrated only after crystal is completely active in 2 sec. External Crystal Mode can be selected by changing register setting of CLK_SEL.

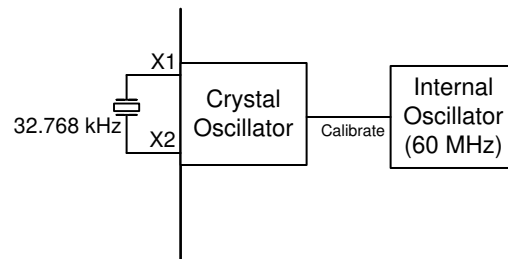


Figure 7-53. External Crystal Oscillator

7.5.4.2 External Clock Source

Accuracy of MCF8316A can also be improved also by providing more accurate optional clock reference on EXT_CLK pin as shown in Figure 7-54. EXT_CLK will be used to calibrate internal clock oscillator and match accuracy of external clock. External clock source can be selected by configuring CLK_SEL and setting EXT_CLK_EN. The external clock source frequency can be configured through EXT_CLK_CONFIG.

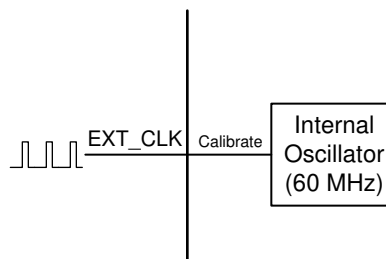


Figure 7-54. External Clock Reference

Note

External crystal oscillator or external clock are only optional and can be used only when higher accuracy of clock is needed. MCF8316A will always power up using internal oscillator in all mode.

7.6 EEPROM access and I²C interface

7.6.1 EEPROM Access

MCF8316 has 1024 bits (16 rows of 64 bits each) of EEPROM data, which are used to store the tuned motor parameters. Erase operations are row-wise (all 64 bits are erased in a single erase operation), but 32-bit read and program operations are supported. EEPROM data can be read and programmed using the I²C Serial Interface but erase operation cannot be performed using I²C serial interface. The procedure for programming and reading the EEPROM data is as follows.

Note

MCF8316 allows EEPROM program and read operations only when the motor is not spinning.

EEPROM Program

1. Write register 0x000080(ISD_CONFIG) with ISD and reverse drive configuration like resync enable, reverse drive enable, stationary detect threshold, reverse drive handoff threshold etc.
2. Write register 0x000082(REV_DRIVE_CONFIG) with reverse drive and active brake configuration like reverse drive open loop acceleration, active brake current limit, Kp, Ki values etc.
3. Write register 0x000084(MOTOR_STARTUP1) with motor start-up configuration like start-up method, IPD parameters, align parameters etc.
4. Write register 0x000086(MOTOR_STARTUP2) with motor start-up configuration like open loop acceleration, open loop current limit, first cycle frequency etc.
5. Write register 0x000088(CLOSED_LOOP1) with motor control configuration like closed loop acceleration, overmodulation enable, PWM frequency, FG signal parameters etc.
6. Write register 0x00008A(CLOSED_LOOP2) with motor control configuration like motor winding resistance and inductance, motor stop options, brake speed threshold etc.
7. Write register 0x00008C(CLOSED_LOOP3) with motor control configuration like motor BEMF constant, current loop Kp, Ki etc.
8. Write register 0x00008E(CLOSED_LOOP4) with motor control configuration like speed loop Kp, Ki and maximum speed.
9. Write register 0x000090(FAULT_CONFIG1) with fault control configuration software and hardware current limits, lock current limit and actions, retry times etc.
10. Write register 0x000092(FAULT_CONFIG2) with fault control configuration like hardware current limit actions, OV, UV limits and actions, abnormal speed level, no motor threshold etc.
11. Write registers 0x000094 – 0x00009E(SPEED_PROFILES1-6) with speed profile configuration like profile type, duty cycle, speed clamp level, duty cycle clamp level etc.
12. Write register 0x0000A0(INT_ALGO1) with miscellaneous configuration like ISD run time and timeout, MPET parameters etc.
13. Write register 0x0000A2(INT_ALGO2) with miscellaneous configuration like additional MPET parameters, IPD high resolution enable, active brake current slew rate, closed loop slow acceleration etc.
14. Write registers 0x0000A4 (PIN_CONFIG1) with pin configuration for speed input mode(analog or PWM), BRAKE pin mode, DACOUT1/2 output addresses etc.
15. Write registers 0x0000A6 and 0x0000A8(DEVICE_CONFIG1 and DEVICE_CONFIG2) with device configuration like pins 36, 37 configuration, pin 38 configuration, dynamic CSA gain enable, dynamic voltage gain enable, clock source select, speed range select etc.
16. Write register 0x0000AA(PERI_CONFIG1) with peripheral configuration like dead time, bus current limit, DIR input, SSM enable etc.
17. Write registers 0x0000AC and 0x0000AE(GD_CONFIG1 and GD_CONFIG2) with gate driver configuration like slew rate, CSA gain, OCP level, mode, OVP enable, level, buck voltage level, buck current limit etc.
18. Write 0x8A500000 into register 0x0000EA to program the shadow register(0x000080-0x0000AE) values into the EEPROM.
19. Wait for 100ms for the EEPROM program operation to complete

Steps 1-17 can be selectively executed based on registers/parameters that need to be modified. After all shadow registers have been updated with the required values, step 18 should be executed to copy the contents of the shadow registers into the EEPROM.

EEPROM Read

1. Write 0x40000000 into register 0x0000EA to read the EEPROM data into the shadow registers(0x000080-0x0000AE).
2. Wait for 100ms for the EEPROM read operation to complete.
3. Read the shadow register values using I2C, 1 or 2 registers at a time, using the I2C read command as explained in [Section 7.6.2](#). Shadow register addresses are in the range of 0x000080-0x0000AE. Register address increases in steps of 2 for 32-bit read operation(since each address is a 16-bit location).

7.6.2 I²C Serial Interface

MCF8316A interfaces with an external MCU over an I2C serial interface. MCF8316A is an I2C target to be interfaced with a controller. The I²C data word format is shown in [Table 7-7](#). External MCU can use this protocol to read/write to any non-reserved register in MCF8316A.

Table 7-7. I2C Data Word Format

TARGET_ID	R/W	CONTROL WORD	DATA	CRC-8
A6 - A0	W0	CW23 - CW0	D15 / D31/ D63 - D0	C7 - C0

Target ID and R/W Bit: The first byte includes the 7-bit I²C target ID (0x60), followed by the read/write command bit. Every packet in MCF8316A communication protocol starts with writing a 24-bit control word and hence the R/W bit is always 0.

24-bit Control Word: The Target Address is followed by a 24-bit control bit. The control word format is shown in [Table 7-8](#).

Table 7-8. 24-bit Control Word Format

OP_R/W	CRC_EN	DLEN	MEM_SEC	MEM_PAGE	MEM_ADDR
CW23	CW22	CW21- CW20	CW19 - CW16	CW15 - CW12	CW11 - CW0

Each field in the control word is explained in detail below.

OP_R/W – Read/Write: R/W bit gives information on whether this is a read operation or write operation. Bit value 0 indicates it is a write operation. Bit value 1 indicates it is a read operation. For write operation, MCF8316A will expect data bytes to be sent after the 24-bit control word. For read operation, MCF8316A will expect an I²C read request with repeated start or normal start after the 24-bit control word.

CRC_EN – Cyclic Redundancy Check(CRC) Enable: MCF8316A supports CRC to verify the data integrity. This bit controls whether the CRC feature is enabled or not.

DLEN – Data Length: DLEN field determines the length of the data that will be sent by external MCU to MCF8316A. MCF8316A protocol supports three data lengths: 16-bit, 32-bit and 64-bit.

Table 7-9. Data Length Configuration

DLEN Value	Data Length
0b'00	16-bit
0b'01	32-bit
0b'10	64-bit
0b'11	Reserved

MEM_SEC – Memory Section: Each memory location in MCF8316A is addressed using three separate entities in the control word – Memory Section, Memory Page, Memory Address. Memory Section is a 4-bit field which denotes the memory section to which the memory location belongs like RAM, ROM etc.

MEM_PAGE – Memory Page: Memory page is a 4-bit field which denotes the memory page to which the memory location belongs.

MEM_ADDR – Memory Address: Memory address is the last 12-bits of the address. The complete 22-bit address is constructed internally by MCF8316A using all three fields – Memory Section, Memory Page, Memory Address. For memory locations 0x000000-0x000400, memory section is 0x0, memory page is 0x0 and memory address is the lowest 12 bits(0x000 for 0x000000, 0x080 for 0x000080 and 0x400 for 0x000400)

Data Bytes: For a write operation to MCF8316A, the 24-bit control word is followed by data bytes. The DLEN field in the control word should correspond with the number of bytes sent in this section.

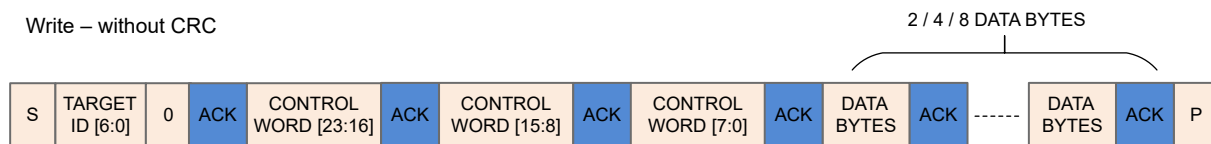
CRC Byte: If the CRC feature is enabled in the control word, CRC byte has to be sent at the end of a write transaction. Procedure to calculate CRC is explained in CRC Byte Calculation below.

Write Operation

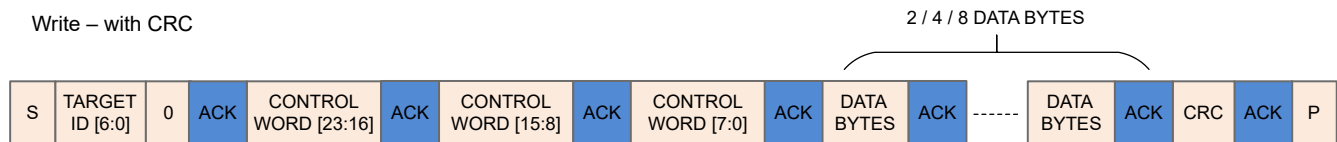
MCF8316A write operation over I²C involves the following sequence.

1. I2C start condition.
2. The sequence starts with I2C target start byte, made up of 7-bit target ID (0x60) to identify the MCF8316A along with the R/W bit set to 0.
3. The start byte is followed by 24-bit control word. Bit 23 in the control word has to be 0 as it is a write operation.
4. The 24-bit control word is then followed by the data bytes. The length of the data byte depends on the DLEN field.
 - a. While sending data bytes, the LSB byte is sent first. Refer below examples for more details.
 - b. 16-bit/32-bit write – The data sent is written to the address mentioned in Control Word.
 - c. 64-bit Write – 64-bit is treated as two 32-bit writes. The address mentioned in Control word is taken as Addr 0. Addr 1 is calculating internally by MCF8316A by incrementing Addr 0 by 2. A total of 8 data bytes are sent. The first 4 bytes (sent in LSB first way) are written to Addr 0 and the next 4 bytes are written to Addr 1.
5. If CRC is enabled, the packet ends with a CRC byte. CRC is calculated for the entire packet (Target ID + W bit, Control Word, Data Bytes).
6. I2C stop condition.

Write – without CRC



Write – with CRC



CRC includes {TARGET ID,0}, CONTROL WORD[23:0], DATA BYTES

Figure 7-55. I2C Write Operation Sequence

Read Operation

MCF8316A Read Operation over I²C involves the following sequence.

1. I2C start condition.
2. The sequence starts with I2C target Start Byte.
3. The Start Byte is followed by 24-bit Control Word. Bit 23 in the control word has to be 1 as it is a read operation.
4. The control word is followed by a repeated start or normal start.

5. MCF8316A sends the data bytes on SDA. The number of bytes sent by MCF8316A depends on the DLEN field value in the control word.
 - a. While sending data bytes, the LSB byte is sent first. Refer the examples below for more details.
 - b. 16-bit/32-bit Read – The data from the address mentioned in Control Word is sent back.
 - c. 64-bit Read – 64-bit is treated as two 32-bit read. The address mentioned in Control Word is taken as Addr 0. Addr 1 is calculating internally by MCF8316A by incrementing Addr 0 by 2. A total of 8 data bytes are sent by MCF8316A. The first 4 bytes (sent in LSB first way) are read from Addr 0 and the next 4 bytes are read from Addr 1.
 - d. MCF8316A takes some time to process the control word and read data from the given address. This involves some delay. It is quite possible that the repeated start with Target ID will be NACK'd. If the I2C read request has been NACK'd by MCF8316A, retry after few cycles. During this retry, it is not necessary to send the entire packet along with the control word. It is sufficient to send only the start condition with target ID and read bit.
6. If CRC is enabled, then MCF8316A sends an additional CRC byte at the end. If CRC is enabled, external MCU I2C controller has to read this additional byte before sending the stop bit. CRC is calculated for the entire packet (Target ID + W bit, Control Word, Target ID + R bit, Data Bytes).
7. I2C stop condition.

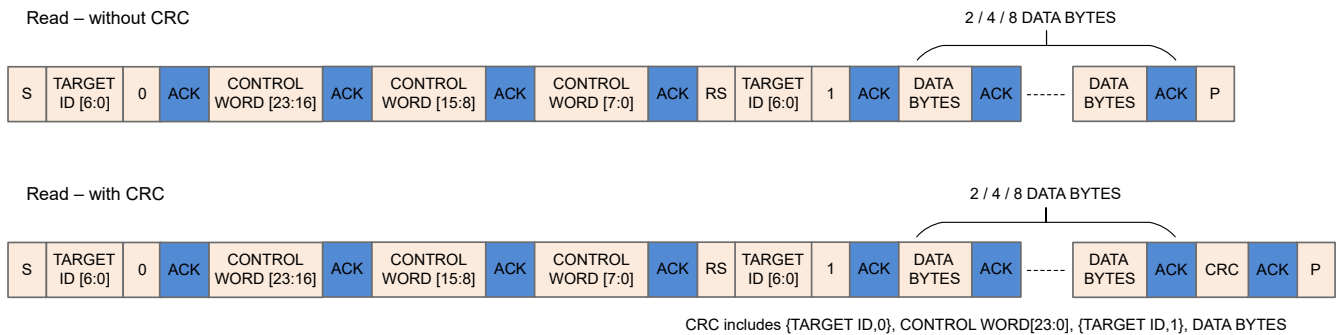


Figure 7-56. I2C Write Operation Sequence

Examples of MCF8316A I2C Communication Protocol Packet

All values used in this example section are in hex format. I2C target ID used in the examples is 0x60.

Example for 32-bit Write Operation: Address – 0x00000080, Data – 0x1234ABCD, CRC Byte – 0x45 (Sample value; does not match with the actual CRC calculation)

Table 7-10. Example for 32-bit Write Operation Packet

Start Byte		Control Word 0				Control Word 1		Control Word 2	Data Bytes				CRC
Target ID	I2C Write	OP_R/W	CRC_EN	DLEN	MEM_SEC	MEM_PAGE	MEM_ADDR	MEM_ADDR	DB0	DB1	DB2	DB3	CRC Byte
A6-A0	W0	CW23	CW22	CW21-CW20	CW19-CW16	CW15-CW12	CW11-CW8	CW7-CW0	D7-D0	D7-D0	D7-D0	D7-D0	C7-C0
0x60	0x0	0x0	0x1	0x1	0x0	0x0	0x0	0x80	0xCD	0xAB	0x34	0x12	0x45
0xC0		0x50				0x00		0x80	0xCD	0xAB	0x34	0x12	0x45

Example for 64-bit Write Operation: Address - 0x00000080, Data Address 0x00000080 - Data 0x01234567, Data Address 0x00000082 – Data 0x89ABCDEF, CRC Byte – 0x45 (Sample value; does not match with the actual CRC calculation)

Table 7-11. Example for 64-bit Write Operation Packet

Start Byte		Control Word 0				Control Word 1		Control Word 2	Data Bytes	CRC
Target ID	I2C Write	OP_R/W	CRC_EN	DLEN	MEM_SEC	MEM_PAGE	MEM_ADDR	MEM_ADDR	DB0 - DB7	CRC Byte

Table 7-11. Example for 64-bit Write Operation Packet (continued)

A6-A0	W0	CW23	CW22	CW21- CW20	CW19- CW16	CW15- CW12	CW11-CW8	CW7-CW0	[D7-D0] x 8	C7-C0
0x60	0x0	0x0	0x1	0x2	0x0	0x0	0x0	0x80	0x67452301EFCDA89	0x45
0xC0		0x60				0x00		0x80	0x67452301EFCDA89	0x45

Example for 32-bit Read Operation: Address – 0x00000080, Data – 0x1234ABCD, CRC Byte – 0x56 (Sample value; does not match with the actual CRC calculation)

Table 7-12. Example for 32-bit Read Operation Packet

Start Byte		Control Word 0				Control Word 1			Control Word 2	Start Byte		Byte 0	Byte 1	Byte 2	Byte 3	Byte 4
Target ID	I2C Write	R/W	CRC_EN	DLEN	MEM_SEC	MEM_PAGE	MEM_ADDR	MEM_ADDR	Target ID	I2C Read	DB0	DB1	DB2	DB3	CRC Byte	
A6-A0	W0	CW23	CW22	CW21- CW20	CW19- CW16	CW15- CW12	CW11- CW8	CW7- CW0	A6-A0	W0	D7-D0	D7-D0	D7-D0	D7-D0	C7-C0	
0x60	0x0	0x1	0x1	0x1	0x0	0x0	0x0	0x80	0x60	0x1	0xCD	0xAB	0x34	0x12	0x56	
0xC0		0xD0				0x00		0x80	0xC1		0xCD	0xAB	0x34	0x12	0x56	

Details on MCF8316A Internal Buffers and Special Scenarios

MCF8316x uses buffers internally to store the data received on I2C. Highest priority is given to collecting data on the I2C Bus. There are 2 buffers (ping-pong) for I2C Rx Data and 2 buffers (ping-pong) for I²C Tx Data.

A write request from external MCU is stored in Rx Buffer 1 and then the parsing block is triggered to work on this data in Rx Buffer 1. While MCF8316A is processing a write packet from Rx Buffer 1, if there is another new read/write request, the entire data from the I²C bus is stored in Rx Buffer 2 and it will be processed after the current request.

MCF8316A can accommodate a maximum of two consecutive read/write requests. If MCF8316A is busy due to high priority interrupts, the data sent will be stored in internal buffers (Rx Buffer 1 and Rx Buffer 2). At this point, if there is a third read/write request, the Target ID will be NACK'd as the buffers are already full.

During read operations, the read request is processed and the read data from the register is stored in the Tx Buffer along with the CRC byte, if enabled. Now if the external MCU initiates an I2C Read (Target ID + R bit), the data from this Tx Buffer is sent over I2C. Since there are two Tx Buffers, register data from 2 MCF8316A reads can be buffered. Given this scenario, if there is a third read request, the control word will be stored in the Rx Buffer 1, but it will not be processed by MCF8316A as the Tx Buffers are full.

Once if a data is read from Tx Buffer, the data is no longer stored in the Tx buffer. The buffer is cleared and it becomes available for the next data to be stored. If the read transaction was interrupted in between and if the MCU had not read all the bytes, external MCU can initiate another I²C read (only I²C read, without any control word information) to read all the data bytes from first.

CRC Byte Calculation

An 8-bit CCIT polynomial ($x^8 + x^2 + x + 1$) is used for CRC computation.

CRC Calculation in Write Operation: When the external MCU writes to MCF8216, if the CRC is enabled, the external MCU has to compute an 8-bit CRC byte and add the CRC byte at the end of the data. MCF8316A will compute CRC using the same polynomial internally and if there is a mismatch, the write request is discarded. Input data for CRC calculation by external MCU for write operation are listed below:

1. Target ID + write bit.
2. Control word – 3 bytes
3. Data bytes – 2/4/8 bytes

CRC Calculation in Read Operation: When the external MCU reads from MCF8316A, if the CRC is enabled, MCF8316A sends the CRC byte at the end of the data. The CRC computation in read operation involves the

start byte, control words sent by external MCU along with data bytes sent by MCF8316A. Input data for CRC calculation by external MCU to verify the data sent by MCF8316A are listed below:

1. Target ID + write bit
2. Control word – 3 bytes
3. Target ID + read bit
4. Data bytes – 2/4/8 bytes

7.7 EERPOM (Non-Volatile) Register Map

7.7.1 Algorithm_Configuration Registers

[ALGORITHM_CONFIGURATION Registers](#) lists the memory-mapped registers for the Algorithm_Configuration registers. All register offset addresses not listed in [ALGORITHM_CONFIGURATION Registers](#) should be considered as reserved locations and the register contents should not be modified.

Table 7-13. ALGORITHM_CONFIGURATION Registers

Address	Acronym	Register Name	Section
80h	ISD_CONFIG	ISD Configuration	Section 7.7.1.1
82h	REV_DRIVE_CONFIG	Reverse Drive Configuration	Section 7.7.1.2
84h	MOTOR_STARTUP1	Motor Startup Configuration1	Section 7.7.1.3
86h	MOTOR_STARTUP2	Motor Startup Configuration2	Section 7.7.1.4
88h	CLOSED_LOOP1	Close Loop Configuration1	Section 7.7.1.5
8Ah	CLOSED_LOOP2	Close Loop Configuration2	Section 7.7.1.6
8Ch	CLOSED_LOOP3	Close Loop Configuration3	Section 7.7.1.7
8Eh	CLOSED_LOOP4	Close Loop Configuration4	Section 7.7.1.8
94h	SPEED_PROFILES1	Speed Profile Configuration1	Section 7.7.1.9
96h	SPEED_PROFILES2	Speed Profile Configuration2	Section 7.7.1.10
98h	SPEED_PROFILES3	Speed Profile Configuration3	Section 7.7.1.11
9Ah	SPEED_PROFILES4	Speed Profile Configuration4	Section 7.7.1.12
9Ch	SPEED_PROFILES5	Speed Profile Configuration5	Section 7.7.1.13
9Eh	SPEED_PROFILES6	Speed Profile Configuration6	Section 7.7.1.14

Complex bit access types are encoded to fit into small table cells. [Algorithm_Configuration Access Type Codes](#) shows the codes that are used for access types in this section.

Table 7-14. Algorithm_Configuration Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.7.1.1 ISD_CONFIG Register (Address = 80h) [Reset = 0000000h]

ISD_CONFIG is shown in [ISD_CONFIG Register](#) and described in [ISD_CONFIG Register Field Descriptions](#).

Return to the [ALGORITHM_CONFIGURATION Registers](#).

Register to configure initial speed detect settings

Figure 7-57. ISD_CONFIG Register

31	30	29	28	27	26	25	24
PARITY	ISD_EN	BRAKE_EN	HIZ_EN	RVS_DR_EN	RESYNC_EN	FW_DRV_RESYN_THR	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	
23	22	21	20	19	18	17	16
FW_DRV_RESYN_THR		BRK_MODE	BRK_CONFIG	BRK_CURR_THR			BRK_TIME
R/W-0h		R/W-0h	R/W-0h	R/W-0h			R/W-0h
15	14	13	12	11	10	9	8
BRK_TIME			HIZ_TIME				STAT_DETECT_THR
R/W-0h			R/W-0h				R/W-0h
7	6	5	4	3	2	1	0
STAT_DETECT_THR		REV_DRV_HANDOFF_THR				REV_DRV_OPEN_LOOP_CURRENT	
R/W-0h		R/W-0h				R/W-0h	

Table 7-15. ISD_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30	ISD_EN	R/W	0h	ISD Enable 0h = Disable 1h = Enable
29	BRAKE_EN	R/W	0h	Brake enable 0h = Disable 1h = Enable
28	HIZ_EN	R/W	0h	Hi-Z enable 0h = Disable 1h = Enable
27	RVS_DR_EN	R/W	0h	Reverse Drive Enable 0h = Disable 1h = Enable
26	RESYNC_EN	R/W	0h	Resynchronization Enable 0h = Disable 1h = Enable

Table 7-15. ISD_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25-22	FW_DRV_RESYN_THR	R/W	0h	Minimum Speed threshold to resynchronize to close loop (% of MAX_SPEED) 0h = 5% 1h = 10% 2h = 15% 3h = 20% 4h = 25% 5h = 30% 6h = 35% 7h = 40% 8h = 45% 9h = 50% Ah = 55% Bh = 60% Ch = 70% Dh = 80% Eh = 90% Fh = 100%
21	BRK_MODE	R/W	0h	Brake mode 0h = All three high side FETs turned ON 1h = All three low side FETs turned ON
20	BRK_CONFIG	R/W	0h	Brake configuration 0h = Brake time is used to come out of Brake state 1h = Brake current threshold is used to come out of Brake state
19-17	BRK_CURR_THR	R/W	0h	Brake current threshold (A) 0h = 0.1 A 1h = 0.2 A 2h = 0.3 A 3h = 0.5 A 4h = 1.0 A 5h = 2.0 A 6h = 4.0 A 7h = 8.0 A
16-13	BRK_TIME	R/W	0h	Brake time 0h = 10 ms 1h = 50 ms 2h = 100 ms 3h = 200 ms 4h = 300 ms 5h = 400 ms 6h = 500 ms 7h = 750 ms 8h = 1 s 9h = 2 s Ah = 3 s Bh = 4 s Ch = 5 s Dh = 7.5 s Eh = 10 s Fh = 15 s

ADVANCE INFORMATION

Table 7-15. ISD_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12-9	HIZ_TIME	R/W	0h	Hi-Z time 0h = 10 ms 1h = 50 ms 2h = 100 ms 3h = 200 ms 4h = 300 ms 5h = 400 ms 6h = 500 ms 7h = 750 ms 8h = 1 s 9h = 2 s Ah = 3 s Bh = 4 s Ch = 5 s Dh = 7.5 s Eh = 10 s Fh = 15 s
8-6	STAT_DETECT_THR	R/W	0h	BEMF threshold to detect if motor is stationary 0h = 50 mV 1h = 75 mV 2h = 100 mV 3h = 250 mV 4h = 500 mV 5h = 750 mV 6h = 1000 mV 7h = 1500 mV
5-2	REV_DRV_HANDOFF_THR	R/W	0h	Speed threshold used to transition to open loop during reverse deceleration (% of MAX_SPEED) 0h = 2.5% 1h = 5% 2h = 7.5% 3h = 10% 4h = 12.5% 5h = 15% 6h = 20% 7h = 25% 8h = 30% 9h = 40% Ah = 50% Bh = 60% Ch = 70% Dh = 80% Eh = 90% Fh = 100%
1-0	REV_DRV_OPEN_LOOP_CURRENT	R/W	0h	Open loop current limit during speed reversal (A) 0h = 1.5 A 1h = 2.5 A 2h = 3.5 A 3h = 5.0 A

7.7.1.2 REV_DRIVE_CONFIG Register (Address = 82h) [Reset = 0000000h]

REV_DRIVE_CONFIG is shown in [REV_DRIVE_CONFIG Register](#) and described in [REV_DRIVE_CONFIG Register Field Descriptions](#).

Return to the [ALGORITHM_CONFIGURATION Registers](#).

Register to configure reverse drive settings

Figure 7-58. REV_DRIVE_CONFIG Register

31	30	29	28	27	26	25	24
PARITY	REV_DRV_OPEN_LOOP_ACCEL_A1				REV_DRV_OPEN_LOOP_ACCEL_A2		
R/W-0h		R/W-0h				R/W-0h	
23	22	21	20	19	18	17	16
REV_DRV_OPEN_LOOP_ACCEL_A2	ACTIVE_BRAKE_CURRENT_LIMIT				ACTIVE_BRAKE_KP		
R/W-0h		R/W-0h				R/W-0h	
15	14	13	12	11	10	9	8
ACTIVE_BRAKE_KP						ACTIVE_BRAKE_KI	
R/W-0h				R/W-0h			
7	6	5	4	3	2	1	0
ACTIVE_BRAKE_KI							
R/W-0h							

Table 7-16. REV_DRIVE_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-27	REV_DRV_OPEN_LOOP_ACCEL_A1	R/W	0h	Open loop acceleration coefficient A1 during reverse drive 0h = 0.01 Hz/s 1h = 0.05 Hz/s 2h = 1 Hz/s 3h = 2.5 Hz/s 4h = 5 Hz/s 5h = 10 Hz/s 6h = 25 Hz/s 7h = 50 Hz/s 8h = 75 Hz/s 9h = 100 Hz/s Ah = 250 Hz/s Bh = 500 Hz/s Ch = 750 Hz/s Dh = 1000 Hz/s Eh = 5000 Hz/s Fh = 10000 Hz/s

Table 7-16. REV_DRIVE_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26-23	REV_DRV_OPEN_LOOP_ACCEL_A2	R/W	0h	Open loop acceleration coefficient A2 during reverse drive 0h = 0.0 Hz/s ² 1h = 0.05 Hz/s ² 2h = 1 Hz/s ² 3h = 2.5 Hz/s ² 4h = 5 Hz/s ² 5h = 10 Hz/s ² 6h = 25 Hz/s ² 7h = 50 Hz/s ² 8h = 75 Hz/s ² 9h = 100 Hz/s ² Ah = 250 Hz/s ² Bh = 500 Hz/s ² Ch = 750 Hz/s ² Dh = 1000 Hz/s ² Eh = 5000 Hz/s ² Fh = 10000 Hz/s ²
22-20	ACTIVE_BRAKE_CURRENT_LIMIT	R/W	0h	Bus current limit during active braking (A) 0h = 0.5 A 1h = 1 A 2h = 2 A 3h = 3 A 4h = 4 A 5h = 5 A 6h = 6 A 7h = 7 A
19-10	ACTIVE_BRAKE_KP	R/W	0h	10-bit value for active braking loop Kp. $K_p = \text{ACTIVE_BRAKE_KP} / 2^7$
9-0	ACTIVE_BRAKE_KI	R/W	0h	10-bit value for active braking loop Ki. $K_i = \text{ACTIVE_BRAKE_KI} / 2^9$

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7.7.1.3 MOTOR_STARTUP1 Register (Address = 84h) [Reset = 0000000h]

MOTOR_STARTUP1 is shown in [MOTOR_STARTUP1 Register](#) and described in [MOTOR_STARTUP1 Register Field Descriptions](#).

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Register to configure motor startup settings¹

Figure 7-59. MOTOR_STARTUP1 Register

31	30	29	28	27	26	25	24
PARITY	MTR_STARTUP		ALIGN_SLOW_RAMP_RATE			ALIGN_TIME	
R/W-0h	R/W-0h		R/W-0h			R/W-0h	
23	22	21	20	19	18	17	16
ALIGN_TIME		ALIGN_OR_SLOW_CURRENT_ILIMIT			IPD_CLK_FREQ		
R/W-0h		R/W-0h			R/W-0h		
15	14	13	12	11	10	9	8
IPD_CLK_FREQ		IPD_CURR_THR			IPD_RLS_MODE		
R/W-0h		R/W-0h			R/W-0h		
7	6	5	4	3	2	1	0
IPD_ADV_ANGLE		IPD_REPEAT		OL_ILIMIT_CONFIG	IQ_RAMP_EN	ACTIVE_BRAKE_REV_DRV_EN	REV_DRV_CONFIG
R/W-0h		R/W-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-17. MOTOR_STARTUP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-29	MTR_STARTUP	R/W	0h	Motor startup options 0h = Align 1h = Double Align 2h = IPD 3h = Slow first cycle
28-25	ALIGN_SLOW_RAMP_RATE	R/W	0h	Align, slow first cycle and open loop current ramp rate 0h = 0.1 A/s 1h = 1 A/s 2h = 5 A/s 3h = 10 A/s 4h = 15 A/s 5h = 25 A/s 6h = 50 A/s 7h = 100 A/s 8h = 150 A/s 9h = 200 A/s Ah = 250 A/s Bh = 500 A/s Ch = 1000 A/s Dh = 2000 A/s Eh = 5000 A/s Fh = No Limit A/s

Table 7-17. MOTOR_STARTUP1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24-21	ALIGN_TIME	R/W	0h	Align time 0h = 10 ms 1h = 50 ms 2h = 100 ms 3h = 200 ms 4h = 300 ms 5h = 400 ms 6h = 500 ms 7h = 750 ms 8h = 1 s 9h = 1.5 s Ah = 2 s Bh = 3 s Ch = 4 s Dh = 5 s Eh = 7.5 s Fh = 10 s
20-17	ALIGN_OR_SLOW_CURRENT_ILIMIT	R/W	0h	Align or slow first cycle current limit (A) 0h = 0.125 A 1h = 0.25 A 2h = 0.5 A 3h = 1.0 A 4h = 1.5 A 5h = 2.0 A 6h = 2.5 A 7h = 3.0 A 8h = 3.5 A 9h = 4.0 A Ah = 4.5 A Bh = 5.0 A Ch = 5.5 A Dh = 6.0 A Eh = 7.0 A Fh = 8.0 A
16-14	IPD_CLK_FREQ	R/W	0h	IPD Clock Frequency 0h = 50 Hz 1h = 100 Hz 2h = 250 Hz 3h = 500 Hz 4h = 1000 Hz 5h = 2000 Hz 6h = 5000 Hz 7h = 10000 Hz

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Table 7-17. MOTOR_STARTUP1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13-9	IPD_CURR_THR	R/W	0h	IPD Current Threshold (A) 0h = 0.25 A 1h = 0.5 A 2h = 0.75 A 3h = 1.0 A 4h = 1.25 A 5h = 1.5 A 6h = 2.0 A 7h = 2.5 A 8h = 3.0 A 9h = 3.667 A Ah = 4.0 A Bh = 4.667 A Ch = 5.0 A Dh = 5.333 A Eh = 6.0 A Fh = 6.667 A 10h = 7.333 A 11h = 8.0 A 12h = NA 13h = NA 14h = NA 15h = NA 16h = NA 17h = NA 18h = NA 19h = NA 1Ah = NA 1Bh = NA 1Ch = NA 1Dh = NA 1Eh = NA 1Fh = NA
8	IPD_RLS_MODE	R/W	0h	IPD release mode 0h = Brake 1h = Tristate
7-6	IPD_ADV_ANGLE	R/W	0h	IPD advance angle 0h = 0° 1h = 30° 2h = 60° 3h = 90°
5-4	IPD_REPEAT	R/W	0h	Number of times IPD is executed 0h = 1 time 1h = average of 2 times 2h = average of 3 times 3h = average of 4 times
3	OL_ILIMIT_CONFIG	R/W	0h	Open loop current limit configuration 0h = Open loop current limit defined by OL_ILIMIT 1h = Open loop current limit defined by ILIMIT
2	IQ_RAMP_EN	R/W	0h	Iq ramp down after transition to close loop enable 0h = Diable Iq ramp down 1h = Enable Iq ramp down

Table 7-17. MOTOR_STARTUP1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	ACTIVE_BRAKE_REV_D RV_EN	R/W	0h	Enables active braking during reverse drive 0h = Disable Active Brake Reverse Drive 1h = Enable Active Brake Reverse Drive
0	REV_DRV_CONFIG	R/W	0h	Chooses between forward and reverse drive setting for reverse drive 0h = Open loop current, A1, A2 based on forward drive 1h = Open loop current, A1, A2 based on reverse drive

7.7.1.4 MOTOR_STARTUP2 Register (Address = 86h) [Reset = 0000000h]

MOTOR_STARTUP2 is shown in [MOTOR_STARTUP2 Register](#) and described in [MOTOR_STARTUP2 Register Field Descriptions](#).

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Register to configure motor startup settings2

Figure 7-60. MOTOR_STARTUP2 Register

31	30	29	28	27	26	25	24
PARITY	OL_ILIMIT			OL_ACC_A1			
R/W-0h		R/W-0h			R/W-0h		
23	22	21	20	19	18	17	16
OL_ACC_A1	OL_ACC_A2			AUTO_HANDOFF_FF_EN	OPN_CL_HANDOFF_THR		
R/W-0h		R/W-0h			R/W-0h		R/W-0h
15	14	13	12	11	10	9	8
OPN_CL_HANDOFF_THR			ALIGN_ANGLE				
R/W-0h			R/W-0h				
7	6	5	4	3	2	1	0
SLOW_FIRST_CYC_FREQ				FIRST_CYCLE_FREQ_SEL	THETA_ERROR_RAMP_RATE		
R/W-0h				R/W-0h		R/W-0h	

Table 7-18. MOTOR_STARTUP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-27	OL_ILIMIT	R/W	0h	Open Loop current limit (A) 0h = 0.125 A 1h = 0.25 A 2h = 0.5 A 3h = 1.0 A 4h = 1.5 A 5h = 2.0 A 6h = 2.5 A 7h = 3.0 A 8h = 3.5 A 9h = 4.0 A Ah = 4.5 A Bh = 5.0 A Ch = 5.5 A Dh = 6.0 A Eh = 7.0 A Fh = 8.0 A

Table 7-18. MOTOR_STARTUP2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26-23	OL_ACC_A1	R/W	0h	Open loop acceleration coefficient A1 0h = 0.01 Hz/s 1h = 0.05 Hz/s 2h = 1 Hz/s 3h = 2.5 Hz/s 4h = 5 Hz/s 5h = 10 Hz/s 6h = 25 Hz/s 7h = 50 Hz/s 8h = 75 Hz/s 9h = 100 Hz/s Ah = 250 Hz/s Bh = 500 Hz/s Ch = 750 Hz/s Dh = 1000 Hz/s Eh = 5000 Hz/s Fh = 10000 Hz/s
22-19	OL_ACC_A2	R/W	0h	Open loop acceleration coefficient A2 0h = 0.0 Hz/s ² 1h = 0.05 Hz/s ² 2h = 1 Hz/s ² 3h = 2.5 Hz/s ² 4h = 5 Hz/s ² 5h = 10 Hz/s ² 6h = 25 Hz/s ² 7h = 50 Hz/s ² 8h = 75 Hz/s ² 9h = 100 Hz/s ² Ah = 250 Hz/s ² Bh = 500 Hz/s ² Ch = 750 Hz/s ² Dh = 1000 Hz/s ² Eh = 5000 Hz/s ² Fh = 10000 Hz/s ²
18	AUTO_HANDOFF_EN	R/W	0h	Auto Handoff Enable 0h = Disable Auto Handoff (and use OPN_CL_HANDOFF_THR) 1h = Enable Auto Handoff

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Table 7-18. MOTOR_STARTUP2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17-13	OPN_CL_HANDOFF_THR	R/W	0h	Open to Close loop Handoff Threshold (% of MAX_SPEED) 0h = 1% 1h = 2% 2h = 3% 3h = 4% 4h = 5% 5h = 6% 6h = 7% 7h = 8% 8h = 9% 9h = 10% Ah = 11% Bh = 12% Ch = 13% Dh = 14% Eh = 15% Fh = 16% 10h = 17% 11h = 18% 12h = 19% 13h = 20% 14h = 22.5% 15h = 25% 16h = 27.5% 17h = 30% 18h = 32.5% 19h = 35% 1Ah = 37.5% 1Bh = 40% 1Ch = 42.5% 1Dh = 45% 1Eh = 47.5% 1Fh = 50%

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Table 7-18. MOTOR_STARTUP2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12-8	ALIGN_ANGLE	R/W	0h	Align Angle 0h = 0 deg 1h = 10 deg 2h = 20 deg 3h = 30 deg 4h = 45 deg 5h = 60 deg 6h = 70 deg 7h = 80 deg 8h = 90 deg 9h = 110 deg Ah = 120 deg Bh = 135 deg Ch = 150 deg Dh = 160 deg Eh = 170 deg Fh = 180 deg 10h = 190 deg 11h = 210 deg 12h = 225 deg 13h = 240 deg 14h = 250 deg 15h = 260 deg 16h = 270 deg 17h = 280 deg 18h = 290 deg 19h = 315 deg 1Ah = 330 deg 1Bh = 340 deg 1Ch = 350 deg 1Dh = Reserved 1Eh = Reserved 1Fh = Reserved
7-4	SLOW_FIRST_CYC_FRE Q	R/W	0h	Frequency of first cycle in close loop startup (% of MAX_SPEED) 0h = 1% 1h = 2% 2h = 3% 3h = 5% 4h = 7.5% 5h = 10% 6h = 12.5% 7h = 15% 8h = 17.5% 9h = 20% Ah = 25% Bh = 30% Ch = 35% Dh = 40% Eh = 45% Fh = 50%

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Table 7-18. MOTOR_STARTUP2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	FIRST_CYCLE_FREQ_SEL	R/W	0h	First cycle frequency in open loop for align, double align and IPD startup options 0h = Defined by SLOW_FIRST_CYC_FREQ 1h = 0 Hz
2-0	THETA_ERROR_RAMP_RATE	R/W	0h	Ramp rate for reducing difference between estimated theta and open loop theta (deg / ms) 0h = 0.01 deg/ms 1h = 0.05 deg/ms 2h = 0.1 deg/ms 3h = 0.15 deg/ms 4h = 0.2 deg / ms 5h = 0.5 deg/ms 6h = 1 deg/ms 7h = 2 deg/ms

7.7.1.5 CLOSED_LOOP1 Register (Address = 88h) [Reset = X]

CLOSED_LOOP1 is shown in [CLOSED_LOOP1 Register](#) and described in [CLOSED_LOOP1 Register Field Descriptions](#).

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Register to configure close loop settings1

Figure 7-61. CLOSED_LOOP1 Register

31		30		29		28		27		26		25		24	
PARITY		OVERMODULATION_ENABLE		CL_ACC								CL_DEC_CONFIG			
R/W-0h		R/W-0h		R/W-0h								R/W-0h			
23		22		21		20		19		18		17		16	
CL_DEC								PWM_FREQ_OUT							
R/W-0h								R/W-0h							
15		14		13		12		11		10		9		8	
PWM_FREQ_OUT		PWM_MOD		FG_SEL				FG_DIV							
R/W-0h		R/W-0h		R/W-0h				R/W-0h							
7		6		5		4		3		2		1		0	
FG_CONFIG		FG_BEMF_THR				AVS_EN		DEADTIME_COMP_EN		SPEED_LOOP_DIS		RESERVED			
R/W-0h		R/W-0h				R/W-0h		R/W-0h		R/W-0h		R/W-X			

Table 7-19. CLOSED_LOOP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30	OVERMODULATION_ENABLE	R/W	0h	Enables Over modulation 0h = Disable Over Modulation 1h = Enable Over Modulation

Table 7-19. CLOSED_LOOP1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
29-25	CL_ACC	R/W	0h	Closed loop acceleration (Hz / sec) 0h = 0.5 Hz/s 1h = 1 Hz/s 2h = 2.5 Hz/s 3h = 5 Hz/s 4h = 7.5 Hz/s 5h = 10 Hz/s 6h = 20 Hz/s 7h = 40 Hz/s 8h = 60 Hz/s 9h = 80 Hz/s Ah = 100 Hz/s Bh = 200 Hz/s Ch = 300 Hz/s Dh = 400 Hz/s Eh = 500 Hz/s Fh = 600 Hz/s 10h = 700 Hz/s 11h = 800 Hz/s 12h = 900 Hz/s 13h = 1000 Hz/s 14h = 2000 Hz/s 15h = 4000 Hz/s 16h = 6000 Hz/s 17h = 8000 Hz/s 18h = 10000 Hz/s 19h = 20000 Hz/s 1Ah = 30000 Hz/s 1Bh = 40000 Hz/s 1Ch = 50000 Hz/s 1Dh = 60000 Hz/s 1Eh = 70000 Hz/s 1Fh = No limit
24	CL_DEC_CONFIG	R/W	0h	Closed loop deceleration configuration 0h = Closed loop deceleration defined by CL_DEC 1h = Closed loop deceleration defined by CL_ACC

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Table 7-19. CLOSED_LOOP1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23-19	CL_DEC	R/W	0h	<p>Closed loop deceleration. This register is used only if AVS is disabled and CL_DEC_CONFIG is set to '0'</p> <p>0h = 0.5 Hz/s 1h = 1 Hz/s 2h = 2.5 Hz/s 3h = 5 Hz/s 4h = 7.5 Hz/s 5h = 10 Hz/s 6h = 20 Hz/s 7h = 40 Hz/s 8h = 60 Hz/s 9h = 80 Hz/s Ah = 100 Hz/s Bh = 200 Hz/s Ch = 300 Hz/s Dh = 400 Hz/s Eh = 500 Hz/s Fh = 600 Hz/s 10h = 700 Hz/s 11h = 800 Hz/s 12h = 900 Hz/s 13h = 1000 Hz/s 14h = 2000 Hz/s 15h = 4000 Hz/s 16h = 6000 Hz/s 17h = 8000 Hz/s 18h = 10000 Hz/s 19h = 20000 Hz/s 1Ah = 30000 Hz/s 1Bh = 40000 Hz/s 1Ch = 50000 Hz/s 1Dh = 60000 Hz/s 1Eh = 70000 Hz/s 1Fh = No limit</p>
18-15	PWM_FREQ_OUT	R/W	0h	<p>PWM output frequency</p> <p>0h = 10 kHz 1h = 15 kHz 2h = 20 kHz 3h = 25 kHz 4h = 30 kHz 5h = 35 kHz 6h = 40 kHz 7h = 45 kHz 8h = 50 kHz 9h = 55 kHz Ah = 60 kHz Bh = 65 kHz Ch = 70 kHz Dh = 75 kHz Eh = Not Applicable Fh = Not Applicable</p>

Table 7-19. CLOSED_LOOP1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	PWM_MOD	R/W	0h	PWM modulation 0h = Continuous Space Vector Modulation 1h = Discontinuous Space Vector Modulation
13-12	FG_SEL	R/W	0h	FG select 0h = Output FG in open loop and closed loop (HW config) 1h = Output FG in only closed loop 2h = Output FG in open loop for the first try. 3h = Not Defined
11-8	FG_DIV	R/W	0h	FG Division factor 0h = Divide by 1 (2-pole motor mechanical speed) 1h = Divide by 1 (2-pole motor mechanical speed) 2h = Divide by 2 (4-pole motor mechanical speed) 3h = Divide by 3 (6-pole motor mechanical speed) 4h = Divide by 4 (8-pole motor mechanical speed) ... Fh = Divide by 15 (30-pole motor mechanical speed)
7	FG_CONFIG	R/W	0h	FG output configuration 0h = FG active as long as motor is driven 1h = FG active till BEMF drops below BEMF threshold defined by FG_BEMF_THR
6-4	FG_BEMF_THR	R/W	0h	FG output BEMF threshold 0h = +/- 1mV 1h = +/- 2mV 2h = +/- 5mV 3h = +/- 10mV 4h = +/- 20mV 5h = +/- 30mV 6h = Not Applicable 7h = Not Applicable
3	AVS_EN	R/W	0h	AVS enable 0h = Disable 1h = Enable
2	DEADTIME_COMP_EN	R/W	0h	Deadtime compensation enable 0h = Disable 1h = Enable
1	SPEED_LOOP_DIS	R/W	0h	Speed Loop Disable 0h = Enable 1h = Disable
0	RESERVED	R/W	X	

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7.7.1.6 CLOSED_LOOP2 Register (Address = 8Ah) [Reset = X]

CLOSED_LOOP2 is shown in [CLOSED_LOOP2 Register](#) and described in [CLOSED_LOOP2 Register Field Descriptions](#).

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Register to configure close loop settings2

Figure 7-62. CLOSED_LOOP2 Register

31	30	29	28	27	26	25	24
PARITY		MTR_STOP				RECIR_BRK_TIME	
R/W-0h		R/W-0h				R/W-0h	
23	22	21	20	19	18	17	16
ACT_SPIN_THR				BRAKE_SPEED_THRESHOLD			
R/W-0h				R/W-0h			
15	14	13	12	11	10	9	8
MOTOR_RES							
R/W-X							
7	6	5	4	3	2	1	0
MOTOR_IND							
R/W-X							

Table 7-20. CLOSED_LOOP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-28	MTR_STOP	R/W	0h	Motor stop options 0h = Hi-z 1h = Recirculation Mode 2h = Low side braking 3h = High side braking 4h = Active spin down 5h = Align braking 6h = Not Defined 7h = Not Defined
27-24	RECIR_BRK_TIME	R/W	0h	Brake time during motor stop 0h = 0.1 ms 1h = 0.1 ms 2h = 0.25 ms 3h = 0.5 ms 4h = 1 ms 5h = 5 ms 6h = 10 ms 7h = 50 ms 8h = 100 ms 9h = 250 ms Ah = 500 ms Bh = 1000 ms Ch = 2500 ms Dh = 5000 ms Eh = 10000 ms Fh = 15000 ms

Table 7-20. CLOSED_LOOP2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23-20	ACT_SPIN_THR	R/W	0h	Speed threshold for active spin down (% of MAX_SPEED) 0h = 100 % 1h = 90 % 2h = 80 % 3h = 70 % 4h = 60% 5h = 50 % 6h = 45 % 7h = 40 % 8h = 35 % 9h = 30 % Ah = 25 % Bh = 20 % Ch = 15 % Dh = 10 % Eh = 5 % Fh = 2.5 %
19-16	BRAKE_SPEED_THRES HOLD	R/W	0h	Speed threshold for BRAKE pin and Motor stop options (Low side Braking or High Side Braking or Align Braking) (% of MAX_SPEED) 0h = 100 % 1h = 90 % 2h = 80 % 3h = 70 % 4h = 60% 5h = 50 % 6h = 45 % 7h = 40 % 8h = 35 % 9h = 30 % Ah = 25 % Bh = 20 % Ch = 15 % Dh = 10 % Eh = 5 % Fh = 2.5 %
15-8	MOTOR_RES	R/W	X	8-bit values for motor phase resistance See table x for values of phase resistance
7-0	MOTOR_IND	R/W	X	8-bit values for motor phase inductance See table in motor inductance section for values of phase inductance

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7.7.1.7 CLOSED_LOOP3 Register (Address = 8Ch) [Reset = X]

CLOSED_LOOP3 is shown in [CLOSED_LOOP3 Register](#) and described in [CLOSED_LOOP3 Register Field Descriptions](#).

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Register to configure close loop settings3

Figure 7-63. CLOSED_LOOP3 Register

31	30	29	28	27	26	25	24
PARITY		MOTOR_BEMF_CONST					
R/W-0h		R/W-X					
23	22	21	20	19	18	17	16
MOTOR_BEMF_CONST		CURR_LOOP_KP					
R/W-X		R/W-0h					
15	14	13	12	11	10	9	8
CURR_LOOP_KP				CURR_LOOP_KI			
R/W-0h				R/W-0h			
7	6	5	4	3	2	1	0
CURR_LOOP_KI					SPD_LOOP_KP		
R/W-0h					R/W-0h		

Table 7-21. CLOSED_LOOP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-23	MOTOR_BEMF_CONST	R/W	X	8-bit values for motor BEMF Constant See table in back-EMF constant section for values of back-EMF constant
22-13	CURR_LOOP_KP	R/W	0h	10-bit value for current Iq and Id loop Kp. Kp = CURR_LOOP_KP / 128. Configure 0 for auto calculation of current Kp and Ki
12-3	CURR_LOOP_KI	R/W	0h	10-bit value for current Iq and Id loop Ki. Ki = CURR_LOOP_KI / 128. Configure to 0 for auto calculation of current Kp and Ki
2-0	SPD_LOOP_KP	R/W	0h	3 MSB bits for speed loop Kp. Kp = SPD_LOOP_KP / 512

7.7.1.8 CLOSED_LOOP4 Register (Address = 8Eh) [Reset = X]

CLOSED_LOOP4 is shown in [CLOSED_LOOP4 Register](#) and described in [CLOSED_LOOP4 Register Field Descriptions](#).

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Register to configure close loop settings4

Figure 7-64. CLOSED_LOOP4 Register

31	30	29	28	27	26	25	24
PARITY		SPD_LOOP_KP					
R/W-0h		R/W-0h					
23	22	21	20	19	18	17	16
SPD_LOOP_KI							
R/W-0h							
15	14	13	12	11	10	9	8
SPD_LOOP_KI				MAX_SPEED			
R/W-0h				R/W-X			
7	6	5	4	3	2	1	0
MAX_SPEED							
R/W-X							

Table 7-22. CLOSED_LOOP4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-24	SPD_LOOP_KP	R/W	0h	7 LSB bits for speed loop Kp. Kp = SPD_LOOP_KP / 512
23-14	SPD_LOOP_KI	R/W	0h	10-bit value for speed loop Ki. Ki = SPD_LOOP_KI / 512
13-0	MAX_SPEED	R/W	X	14-bit value for setting maximum value of Speed in electrical Hz Maximum motor electrical speed (Hz): {MOTOR_SPEED/6} For example: if MOTOR_SPEED is 0x2710, then maximum motor speed (Hz) = 10000(0x2710)/6 = 1666 Hz

7.7.1.9 SPEED_PROFILES1 Register (Address = 94h) [Reset = X]

SPEED_PROFILES1 is shown in [SPEED_PROFILES1 Register](#) and described in [SPEED_PROFILES1 Register Field Descriptions](#).

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Register to configure speed profile1

Figure 7-65. SPEED_PROFILES1 Register

31	30	29	28	27	26	25	24
PARITY		SPEED_PROFILE_CONFIG			DUTY_ON1		
R/W-0h		R/W-0h			R/W-X		
23	22	21	20	19	18	17	16
DUTY_ON1			DUTY_OFF1				
R/W-X			R/W-X				
15	14	13	12	11	10	9	8
DUTY_OFF1			DUTY_CLAMP1				
R/W-X			R/W-X				
7	6	5	4	3	2	1	0
DUTY_CLAMP1			DUTY_A				
R/W-X			R/W-X				

Table 7-23. SPEED_PROFILES1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-29	SPEED_PROFILE_CONFIG	R/W	0h	Configuration for speed profiles 0h = Speed Reference Mode 1h = Linear Mode 2h = Staircase Mode 3h = Forward Reverse Mode
28-21	DUTY_ON1	R/W	X	Duty_ON1 Configuration Turn On Duty Cycle (%) = $\{(DUTY_ON1/255)*100\}$
20-13	DUTY_OFF1	R/W	X	Duty_OFF1 Configuration Turn Off Duty Cycle (%) = $\{(DUTY_OFF1/255)*100\}$
12-5	DUTY_CLAMP1	R/W	X	Duty_CLAMP1 Configuration Duty Cycle for clamping speed (%) = $\{(DUTY_CLAMP1/255)*100\}$
4-0	DUTY_A	R/W	X	5 MSB bits for Duty Cycle A

7.7.1.10 SPEED_PROFILES2 Register (Address = 96h) [Reset = X]

SPEED_PROFILES2 is shown in [SPEED_PROFILES2 Register](#) and described in [SPEED_PROFILES2 Register Field Descriptions](#).

Return to the [ALGORITHM_CONFIGURATION Registers](#).

Register to configure speed profile2

Figure 7-66. SPEED_PROFILES2 Register

31	30	29	28	27	26	25	24
PARITY	DUTY_A			DUTY_B			
R/W-0h	R/W-X			R/W-X			
23	22	21	20	19	18	17	16
DUTY_B			DUTY_C				
R/W-X			R/W-X				
15	14	13	12	11	10	9	8
DUTY_C			DUTY_D				
R/W-X			R/W-X				
7	6	5	4	3	2	1	0
DUTY_D			DUTY_E				
R/W-X			R/W-0h				

Table 7-24. SPEED_PROFILES2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-28	DUTY_A	R/W	X	3 LSB bits for Duty Cycle A Duty_A Configuration Duty Cycle A (%) = $\{(DUTY_A/255)*100\}$
27-20	DUTY_B	R/W	X	Duty_B Configuration Duty Cycle B (%) = $\{(DUTY_B/255)*100\}$
19-12	DUTY_C	R/W	X	Duty_C Configuration Duty Cycle C (%) = $\{(DUTY_C/255)*100\}$
11-4	DUTY_D	R/W	X	Duty_D Configuration Duty Cycle D (%) = $\{(DUTY_D/255)*100\}$
3-0	DUTY_E	R/W	0h	4 MSB bits for Duty Cycle E

7.7.1.11 SPEED_PROFILES3 Register (Address = 98h) [Reset = X]

SPEED_PROFILES3 is shown in [SPEED_PROFILES3 Register](#) and described in [SPEED_PROFILES3 Register Field Descriptions](#).

Return to the [ALGORITHM_CONFIGURATION Registers](#).

Register to configure speed profile3

Figure 7-67. SPEED_PROFILES3 Register

31	30	29	28	27	26	25	24
PARITY	DUTY_E				DUTY_ON2		
R/W-0h	R/W-X				R/W-X		
23	22	21	20	19	18	17	16
DUTY_ON2				DUTY_OFF2			
R/W-X				R/W-X			
15	14	13	12	11	10	9	8
DUTY_OFF2				DUTY_CLAMP2			
R/W-X				R/W-X			
7	6	5	4	3	2	1	0
DUTY_CLAMP2				RESERVED			
R/W-X				R/W-0h			

Table 7-25. SPEED_PROFILES3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-27	DUTY_E	R/W	X	4 LSB bits for Duty Cycle E Duty_E Configuration Duty Cycle E (%) = $\{(DUTY_E/255)*100\}$
26-19	DUTY_ON2	R/W	X	Duty_ON2 Configuration Turn On Duty Cycle (%) = $\{(DUTY_ON2/255)*100\}$
18-11	DUTY_OFF2	R/W	X	Duty_OFF2 Configuration Turn Off Duty Cycle (%) = $\{(DUTY_OFF2/255)*100\}$
10-3	DUTY_CLAMP2	R/W	X	Duty_CLAMP2 Configuration Duty Cycle for clamping speed (%) = $\{(DUTY_CLAMP1/255)*100\}$
2-0	RESERVED	R/W	0h	Reserved

7.7.1.12 SPEED_PROFILES4 Register (Address = 9Ah) [Reset = X]

SPEED_PROFILES4 is shown in [SPEED_PROFILES4 Register](#) and described in [SPEED_PROFILES4 Register Field Descriptions](#).

Return to the [ALGORITHM_CONFIGURATION Registers](#).

Register to configure speed profile4

Figure 7-68. SPEED_PROFILES4 Register

31	30	29	28	27	26	25	24
PARITY		SPEED_OFF1					
R/W-0h		R/W-X					
23	22	21	20	19	18	17	16
SPEED_OFF1		SPEED_CLAMP1					
R/W-X		R/W-X					
15	14	13	12	11	10	9	8
SPEED_CLAMP1		SPEED_A					
R/W-X		R/W-X					
7	6	5	4	3	2	1	0
SPEED_A		SPEED_B					
R/W-X		R/W-X					

Table 7-26. SPEED_PROFILES4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-23	SPEED_OFF1	R/W	X	Turn off speed Configuration Turn off speed (% of MAX_SPEED) = $\{(SPEED_OFF1/255)*100\}$
22-15	SPEED_CLAMP1	R/W	X	Clamp Speed Configuration Clamp Speed (% of MAX_SPEED) = $\{(SPEED_CLAMP1/255)*100\}$
14-7	SPEED_A	R/W	X	Speed A configuration SPEED A (% of MAX_SPEED) = $\{(SPEED_A/255)*100\}$
6-0	SPEED_B	R/W	X	7 MSB of SPEED_B configuration

7.7.1.13 SPEED_PROFILES5 Register (Address = 9Ch) [Reset = X]

SPEED_PROFILES5 is shown in [SPEED_PROFILES5 Register](#) and described in [SPEED_PROFILES5 Register Field Descriptions](#).

Return to the [ALGORITHM_CONFIGURATION Registers](#).

Register to configure speed profile5

Figure 7-69. SPEED_PROFILES5 Register

31	30	29	28	27	26	25	24
PARITY	SPEED_B	SPEED_C					
R/W-0h	R/W-X	R/W-X					
23	22	21	20	19	18	17	16
SPEED_C		SPEED_D					
R/W-X		R/W-X					
15	14	13	12	11	10	9	8
SPEED_D		SPEED_E					
R/W-X		R/W-X					
7	6	5	4	3	2	1	0
SPEED_E		RESERVED					
R/W-X		R/W-0h					

Table 7-27. SPEED_PROFILES5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30	SPEED_B	R/W	X	1 LSB of SPEED_B configuration Speed B Configuration $SPEED\ B(\% \text{ of } MAX_SPEED) = \{(SPEED_B/255)*100\}$
29-22	SPEED_C	R/W	X	Speed C configuration $SPEED\ C(\% \text{ of } MAX_SPEED) = \{(SPEED_A/255)*100\}$
21-14	SPEED_D	R/W	X	Speed D configuration $SPEED\ D(\% \text{ of } MAX_SPEED) = \{(SPEED_D/255)*100\}$
13-6	SPEED_E	R/W	X	Speed E Configuration $SPEED\ E(\% \text{ of } MAX_SPEED) = \{(SPEED_E/255)*100\}$
5-0	RESERVED	R/W	0h	Reserved

7.7.1.14 SPEED_PROFILES6 Register (Address = 9Eh) [Reset = X]

SPEED_PROFILES6 is shown in [SPEED_PROFILES6 Register](#) and described in [SPEED_PROFILES6 Register Field Descriptions](#).

Return to the [ALGORITHM_CONFIGURATION Registers](#).

Register to configure speed profile6

Figure 7-70. SPEED_PROFILES6 Register

31	30	29	28	27	26	25	24
PARITY	SPEED_OFF2						
R/W-0h				R/W-X			
23	22	21	20	19	18	17	16
SPEED_OFF2	SPEED_CLAMP2						
R/W-X				R/W-X			
15	14	13	12	11	10	9	8
SPEED_CLAMP2	RESERVED						
R/W-X				R/W-X			
7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

Table 7-28. SPEED_PROFILES6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-23	SPEED_OFF2	R/W	X	Turn off speed Configuration Turn off speed (% of MAX_SPEED) = $\{(SPEED_OFF2/255)*100\}$
22-15	SPEED_CLAMP2	R/W	X	Clamp Speed Configuration Clamp Speed (% of MAX_SPEED) = $\{(SPEED_CLAMP2/255)*100\}$
14-0	RESERVED	R/W	X	Reserved

7.7.2 Fault_Configuration Registers

[FAULT_CONFIGURATION Registers](#) lists the memory-mapped registers for the Fault_Configuration registers. All register offset addresses not listed in [FAULT_CONFIGURATION Registers](#) should be considered as reserved locations and the register contents should not be modified.

Table 7-29. FAULT_CONFIGURATION Registers

Address	Acronym	Register Name	Section
90h	FAULT_CONFIG1	Fault Configuration1	Section 7.7.2.1
92h	FAULT_CONFIG2	Fault Configuration2	Section 7.7.2.2

Complex bit access types are encoded to fit into small table cells. [Fault_Configuration Access Type Codes](#) shows the codes that are used for access types in this section.

Table 7-30. Fault_Configuration Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write

**Table 7-30. Fault_Configuration Access Type Codes
(continued)**

Access Type	Code	Description
Reset or Default Value		
-n		Value after reset or the default value

7.7.2.1 FAULT_CONFIG1 Register (Address = 90h) [Reset = 0000000h]

FAULT_CONFIG1 is shown in [FAULT_CONFIG1 Register](#) and described in [FAULT_CONFIG1 Register Field Descriptions](#).

Return to the [FAULT_CONFIGURATION Registers](#).

Register to configure fault settings1

Figure 7-71. FAULT_CONFIG1 Register

31	30	29	28	27	26	25	24
PARITY	ILIMIT			HW_LOCK_ILIMIT			
R/W-0h		R/W-0h			R/W-0h		
23	22	21	20	19	18	17	16
HW_LOCK_ILIMIT	LOCK_ILIMIT			LOCK_ILIMIT_MODE			
R/W-0h		R/W-0h			R/W-0h		
15	14	13	12	11	10	9	8
LOCK_ILIMIT_MODE	LOCK_ILIMIT_DEG			LCK_RETRY			
R/W-0h		R/W-0h			R/W-0h		
7	6	5	4	3	2	1	0
LCK_RETRY	MTR_LCK_MODE			IPD_TIMEOUT_FAULT_EN	IPD_FREQ_FAULT_EN	SATURATION_FLAGS_EN	
R/W-0h		R/W-0h			R/W-0h	R/W-0h	R/W-0h

Table 7-31. FAULT_CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-27	ILIMIT	R/W	0h	Reference for Torque PI Loop (A) 0h = 0.125 A 1h = 0.25 A 2h = 0.5 A 3h = 1.0 A 4h = 1.5 A 5h = 2.0 A 6h = 2.5 A 7h = 3.0 A 8h = 3.5 A 9h = 4.0 A Ah = 4.5 A Bh = 5.0 A Ch = 5.5 A Dh = 6.0 A Eh = 7.0 A Fh = 8.0 A

Table 7-31. FAULT_CONFIG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26-23	HW_LOCK_ILIMIT	R/W	0h	Comparator based lock detection current limit (A) 0h = 0.125 A 1h = 0.25 A 2h = 0.5 A 3h = 1.0 A 4h = 1.5 A 5h = 2.0 A 6h = 2.5 A 7h = 3.0 A 8h = 3.5 A 9h = 4.0 A Ah = 4.5 A Bh = 5.0 A Ch = 5.5 A Dh = 6.0 A Eh = 7.0 A Fh = 8.0 A
22-19	LOCK_ILIMIT	R/W	0h	ADC based lock detection current threshold (A) 0h = 0.125 A 1h = 0.25 A 2h = 0.5 A 3h = 1.0 A 4h = 1.5 A 5h = 2.0 A 6h = 2.5 A 7h = 3.0 A 8h = 3.5 A 9h = 4.0 A Ah = 4.5 A Bh = 5.0 A Ch = 5.5 A Dh = 6.0 A Eh = 7.0 A Fh = 8.0 A

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Table 7-31. FAULT_CONFIG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18-15	LOCK_ILIMIT_MODE	R/W	0h	<p>Lock current Limit Mode</p> <p>0h = Ilimit lock detection causes latched fault; nfault active; Gate driver is tristated</p> <p>1h = Ilimit lock detection causes latched fault; nfault active; Gate driver is in recirculation mode</p> <p>2h = Ilimit lock detection causes latched fault; nfault active; Gate driver is in high side brake mode (All high side FETs are turned ON)</p> <p>3h = Ilimit lock detection causes latched fault; nfault active; Gate driver is in low side brake mode (All low side FETs are turned ON)</p> <p>4h = Fault automatically cleared after LCK_RETRY time. Number of retries limited to AUTO_RETRY_TIMES. If number of retries exceed AUTO_RETRY_TIMES, fault is latched; Gate driver is tristated; nFault active</p> <p>5h = Fault automatically cleared after LCK_RETRY time. Number of retries limited to AUTO_RETRY_TIMES. If number of retries exceed AUTO_RETRY_TIMES, fault is latched; Gate driver is in recirculation mode; nFault active</p> <p>6h = Fault automatically cleared for AUTO_RETRY_TIMES after LCK_RETRY time; Gate driver is in high side brake mode (All high side FETs are turned ON); nFault active</p> <p>7h = Fault automatically cleared after LCK_RETRY time. Number of retries limited to AUTO_RETRY_TIMES. If number of retries exceed AUTO_RETRY_TIMES, fault is latched; Gate driver is in low side brake mode (All low side FETs are turned ON); nFault active</p> <p>8h = Ilimit lock detection current limit is in report only but no action is taken; nFault active</p> <p>9h = ILIMIT LOCK is disabled</p> <p>Ah = ILIMIT LOCK is disabled</p> <p>Bh = ILIMIT LOCK is disabled</p> <p>Ch = ILIMIT LOCK is disabled</p> <p>Dh = ILIMIT LOCK is disabled</p> <p>Eh = ILIMIT LOCK is disabled</p> <p>Fh = ILIMIT LOCK is disabled</p>
14-11	LOCK_ILIMIT_DEG	R/W	0h	<p>Lock Detection current limit deglitch time</p> <p>0h = 0.05 ms</p> <p>1h = 0.1 ms</p> <p>2h = 0.2 ms</p> <p>3h = 0.5 ms</p> <p>4h = 1 ms</p> <p>5h = 2.5 ms</p> <p>6h = 5 ms</p> <p>7h = 7.5 ms</p> <p>8h = 10 ms</p> <p>9h = 25 ms</p> <p>Ah = 50 ms</p> <p>Bh = 75 ms</p> <p>Ch = 100 ms</p> <p>Dh = 200 ms</p> <p>Eh = 500 ms</p> <p>Fh = 1000 ms</p>

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Table 7-31. FAULT_CONFIG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10-7	LCK_RETRY	R/W	0h	<p>Lock detection retry time</p> <p>0h = 100 ms</p> <p>1h = 500 ms</p> <p>2h = 1 s</p> <p>3h = 2 s</p> <p>4h = 3 s</p> <p>5h = 4 s</p> <p>6h = 5 s</p> <p>7h = 6 s</p> <p>8h = 7 s</p> <p>9h = 8 s</p> <p>Ah = 9 s</p> <p>Bh = 10 s</p> <p>Ch = 11 s</p> <p>Dh = 12 s</p> <p>Eh = 13 s</p> <p>Fh = 14 s</p>
6-3	MTR_LCK_MODE	R/W	0h	<p>Motor Lock Mode</p> <p>0h = Motor lock detection causes latched fault; nFault active; Gate driver is tristated</p> <p>1h = Motor lock detection causes latched fault; nFault active; Gate driver is in recirculation mode</p> <p>2h = Motor lock detection causes latched fault; nFault active; Gate driver is in high side brake mode (All high side FETs are turned ON)</p> <p>3h = Motor lock detection causes latched fault; nFault active; Gate driver is in low side brake mode (All low side FETs are turned ON)</p> <p>4h = Fault automatically cleared after LCK_RETRY time. Number of retries limited to AUTO_RETRY_TIMES. If number of retries exceed AUTO_RETRY_TIMES, fault is latched; Gate driver is tristated; nFault active</p> <p>5h = Fault automatically cleared after LCK_RETRY time. Number of retries limited to AUTO_RETRY_TIMES. If number of retries exceed AUTO_RETRY_TIMES, fault is latched; Gate driver is in recirculation mode; nFault active</p> <p>6h = Fault automatically cleared for AUTO_RETRY_TIMES after LCK_RETRY time; Gate driver is in high side brake mode (All high side FETs are turned ON); nFault active</p> <p>7h = Fault automatically cleared after LCK_RETRY time. Number of retries limited to AUTO_RETRY_TIMES. If number of retries exceed AUTO_RETRY_TIMES, fault is latched; Gate driver is in low side brake mode (All low side FETs are turned ON); nFault active</p> <p>8h = Motor lock detection current limit is in report only but no action is taken; nFault active</p> <p>9h = Motor lock detection is disabled</p> <p>Ah = Motor lock detection is disabled</p> <p>Bh = Motor lock detection is disabled</p> <p>Ch = Motor lock detection is disabled</p> <p>Dh = Motor lock detection is disabled</p> <p>Eh = Motor lock detection is disabled</p> <p>Fh = Motor lock detection is disabled</p>

Table 7-31. FAULT_CONFIG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	IPD_TIMEOUT_FAULT_EN	R/W	0h	IPD timeout fault Enable 0h = Disable 1h = Enable
1	IPD_FREQ_FAULT_EN	R/W	0h	IPD frequency fault Enable 0h = Disable 1h = Enable
0	SATURATION_FLAGS_EN	R/W	0h	Enables indication of current loop and speed loop saturation 0h = Disable 1h = Enable

7.7.2.2 FAULT_CONFIG2 Register (Address = 92h) [Reset = 0000000h]

FAULT_CONFIG2 is shown in [FAULT_CONFIG2 Register](#) and described in [FAULT_CONFIG2 Register Field Descriptions](#).

Return to the [FAULT_CONFIGURATION Registers](#).

Register to configure fault settings2

Figure 7-72. FAULT_CONFIG2 Register

31	30	29	28	27	26	25	24
PARITY	LOCK1_EN	LOCK2_EN	LOCK3_EN	LOCK_ABN_SPEED		ABNORMAL_BEMF_THR	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h	
23	22	21	20	19	18	17	16
ABNORMAL_BEMF_THR		NO_MTR_THR			HW_LOCK_ILIMIT_MODE		
R/W-0h		R/W-0h			R/W-0h		
15	14	13	12	11	10	9	8
HW_LOCK_ILIMIT_MODE	HW_LOCK_ILIMIT_DEG				MIN_VM_MOTOR		
R/W-0h	R/W-0h				R/W-0h		
7	6	5	4	3	2	1	0
MIN_VM_MODE	MAX_VM_MOTOR			MAX_VM_MODE	AUTO_RETRY_TIMES		
R/W-0h	R/W-0h			R/W-0h	R/W-0h		

Table 7-32. FAULT_CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30	LOCK1_EN	R/W	0h	Lock 1 (Abnormal Speed) Enable 0h = Disable 1h = Enable
29	LOCK2_EN	R/W	0h	Lock 2 (Abnormal BEMF) Enable 0h = Disable 1h = Enable
28	LOCK3_EN	R/W	0h	Lock 3 (No Motor) Enable 0h = Disable 1h = Enable
27-25	LOCK_ABN_SPEED	R/W	0h	Abnormal speed lock threshold (% of MAX_SPEED) 0h = 130% 1h = 140% 2h = 150% 3h = 160% 4h = 170% 5h = 180% 6h = 190% 7h = 200%

Table 7-32. FAULT_CONFIG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24-22	ABNORMAL_BEMF_THR	R/W	0h	Abnormal BEMF lock threshold (% of expected BEMF) 0h = 10% 1h = 20% 2h = 30% 3h = 40% 4h = 50% 5h = 60% 6h = 70% 7h = 80%
21-19	NO_MTR_THR	R/W	0h	No motor lock threshold (A) 0h = 0.05 A 1h = 0.075 A 2h = 0.1 A 3h = 0.125 A 4h = 0.25 A 5h = 0.5 A 6h = 0.75 A 7h = 1.0 A

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Table 7-32. FAULT_CONFIG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18-15	HW_LOCK_ILIMIT_MODE	R/W	0h	<p>Hardware Lock Detection current mode</p> <p>0h = Hardware Ilimit lock detection causes latched fault; nfault active; Gate driver is tristated</p> <p>1h = Hardware Ilimit lock detection causes latched fault; nfault active; Gate driver is in recirculation mode</p> <p>2h = Hardware Ilimit lock detection causes latched fault; nfault active; Gate driver is in high side brake mode (All high side FETs are turned ON)</p> <p>3h = Hardware Ilimit lock detection causes latched fault; nfault active; Gate driver is in low side brake mode (All low side FETs are turned ON)</p> <p>4h = Fault automatically cleared after LCK_RETRY time. Number of retries limited to AUTO_RETRY_TIMES. If number of retries exceed AUTO_RETRY_TIMES, fault is latched; Gate driver is tristated</p> <p>5h = Fault automatically cleared after LCK_RETRY time. Number of retries limited to AUTO_RETRY_TIMES. If number of retries exceed AUTO_RETRY_TIMES, fault is latched; Gate driver is in recirculation mode</p> <p>6h = Fault automatically cleared after LCK_RETRY time. Number of retries limited to AUTO_RETRY_TIMES. If number of retries exceed AUTO_RETRY_TIMES, fault is latched; Gate driver is in high side brake mode (All high side FETs are turned ON)</p> <p>7h = Fault automatically cleared after LCK_RETRY time. Number of retries limited to AUTO_RETRY_TIMES. If number of retries exceed AUTO_RETRY_TIMES, fault is latched; Gate driver is in low side brake mode (All low side FETs are turned ON)</p> <p>8h = Hardware ILIMIT lock detection is in report only but no action is taken</p> <p>9h = Hardware ILIMIT lock detection is disabled</p> <p>Ah = Hardware ILIMIT lock detection is disabled</p> <p>Bh = Hardware ILIMIT lock detection is disabled</p> <p>Ch = Hardware ILIMIT lock detection is disabled</p> <p>Dh = Hardware ILIMIT lock detection is disabled</p> <p>Eh = Hardware ILIMIT lock detection is disabled</p> <p>Fh = Hardware ILIMIT lock detection is disabled</p>
14-11	HW_LOCK_ILIMIT_DEG	R/W	0h	<p>Hardware Lock Detection current limit deglitch time</p> <p>0h = No Deglitch</p> <p>1h = 1 us</p> <p>2h = 2 us</p> <p>3h = 3 us</p> <p>4h = 4 us</p> <p>5h = 5 us</p> <p>6h = 6 us</p> <p>7h = 7 us</p> <p>8h = 8 us</p> <p>9h = 9 us</p> <p>Ah = 10 us</p> <p>Bh = 11 us</p> <p>Ch = 12 us</p> <p>Dh = 13 us</p> <p>Eh = 14 us</p> <p>Fh = 15 us</p>

Table 7-32. FAULT_CONFIG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10-8	MIN_VM_MOTOR	R/W	0h	Minimum voltage for running motor (V) 0h = No Limit 1h = 4.5 V 2h = 5 V 3h = 5.5 V 4h = 6 V 5h = 7.5 V 6h = 10 V 7h = 12.5 V
7	MIN_VM_MODE	R/W	0h	Undervoltage Fault Recovery Mode 0h = Latch on Undervoltage 1h = Automatic clear if voltage in bounds
6-4	MAX_VM_MOTOR	R/W	0h	Maximum voltage for running motor 0h = No Limit 1h = 20 V 2h = 22.5 V 3h = 25 V 4h = 27.5 V 5h = 30 V 6h = 32.5 V 7h = 35 V
3	MAX_VM_MODE	R/W	0h	Overvoltage Fault Recovery Mode 0h = Latch on Overvoltage 1h = Automatic clear if voltage in bounds
2-0	AUTO_RETRY_TIMES	R/W	0h	Automatic retry attempts 0h = No Limit 1h = 2 2h = 3 3h = 5 4h = 7 5h = 10 6h = 15 7h = 20

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7.7.3 Hardware_Configuration Registers

[HARDWARE_CONFIGURATION Registers](#) lists the memory-mapped registers for the Hardware_Configuration registers. All register offset addresses not listed in [HARDWARE_CONFIGURATION Registers](#) should be considered as reserved locations and the register contents should not be modified.

Table 7-33. HARDWARE_CONFIGURATION Registers

Address	Acronym	Register Name	Section
A4h	PIN_CONFIG	Hardware Pin Configuration	Section 7.7.3.1
A6h	DEVICE_CONFIG1	Device configuration1	Section 7.7.3.2
A8h	DEVICE_CONFIG2	Device configuration2	Section 7.7.3.3
ACh	GD_CONFIG1	Gate Driver Configuration1	Section 7.7.3.4
AEh	GD_CONFIG2	Gate Driver Configuration2	Section 7.7.3.5

Complex bit access types are encoded to fit into small table cells. [Hardware_Configuration Access Type Codes](#) shows the codes that are used for access types in this section.

Table 7-34. Hardware_Configuration Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
W1C	W 1C	Write 1 to clear
Reset or Default Value		
-n		Value after reset or the default value

7.7.3.1 PIN_CONFIG Register (Address = A4h) [Reset = 0000000h]

 PIN_CONFIG is shown in [PIN_CONFIG Register](#) and described in [PIN_CONFIG Register Field Descriptions](#).

 Return to the [HARDWARE_CONFIGURATION Registers](#).

Register to configure hardware pins

Figure 7-73. PIN_CONFIG Register

31	30	29	28	27	26	25	24
PARITY		DACOUT1_VAR_ADDR					
R/W-0h		R/W-0h					
23	22	21	20	19	18	17	16
DACOUT1_VAR_ADDR				DACOUT2_VAR_ADDR			
R/W-0h				R/W-0h			
15	14	13	12	11	10	9	8
DACOUT2_VAR_ADDR							
R/W-0h							
7	6	5	4	3	2	1	0
DACOUT2_VAR_ADDR			BRAKE_PIN_M ODE	ALIGN_BRAKE _ANGLE_SEL	BRAKE_INPUT		ANA_PWM_SP D_SET
R/W-0h			R/W-0h	R/W-0h	R/W-0h		R/W-0h

Table 7-35. PIN_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-19	DACOUT1_VAR_ADDR	R/W	0h	12-bit address of variable to be monitored
18-5	DACOUT2_VAR_ADDR	R/W	0h	14-bit address of variable to be monitored
4	BRAKE_PIN_MODE	R/W	0h	Brake Pin Mode 0h = Low side Brake 1h = Align Brake
3	ALIGN_BRAKE_ANGLE_SEL	R/W	0h	Align Brake Angle Select 0h = Use last commutation angle before entering align braking 1h = Use ALIGN_ANGLE configuration for align braking
2-1	BRAKE_INPUT	R/W	0h	Brake pin override 0h = Hardware Pin BRAKE 1h = Override pin and brake / align according to BRAKE_PIN_MODE 2h = Override pin and do not brake / align 3h = Hardware Pin BRAKE
0	ANA_PWM_SPD_SET	R/W	0h	Configure either Analog or PWM based speed Input 0h = Analog mode speed Input 1h = PWM Mode Speed Input

7.7.3.2 DEVICE_CONFIG1 Register (Address = A6h) [Reset = X]

DEVICE_CONFIG1 is shown in [DEVICE_CONFIG1 Register](#) and described in [DEVICE_CONFIG1 Register Field Descriptions](#).

Return to the [HARDWARE_CONFIGURATION Registers](#).

Register to configure device

Figure 7-74. DEVICE_CONFIG1 Register

31	30	29	28	27	26	25	24
PARITY	PIN_38_CONFIG		SPEED_PIN_CONFIG	PIN_36_37_CONFIG	RESERVED		
R/W-0h	R/W-0h		R/W-0h	R/W-0h	R/W-X		
23	22	21	20	19	18	17	16
RESERVED				RESERVED			
R/W-X				R/W-X			
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED			RESERVED			BUS_VOLT	
R/W-X			R/W-0h			R/W-0h	

Table 7-36. DEVICE_CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-29	PIN_38_CONFIG	R/W	0h	Pin 38 configuration 0h = DACOUT2 1h = SOA 2h = SOB 3h = SOC
28	SPEED_PIN_CONFIG	R/W	0h	Speed Pin Configuration 0h = Speed pin used to set SPEED_CMD 1h = Speed pin is used to wake up device from sleep, it doesn't affect speed command
27	PIN_36_37_CONFIG	R/W	0h	Pin 36 and Pin 37 configuration 0h = Pin 36 as X1 and Pin 37 as X2 1h = Pin 36 as DACOUT1 and PIN37 as DACOUT2
26-20	RESERVED	R/W	X	Reserved
19-5	RESERVED	R/W	X	Reserved
4-2	RESERVED	R/W	0h	Reserved
1-0	BUS_VOLT	R/W	0h	Maximum Bus Voltage Configuration 0h = 15 V 1h = 30 V 2h = 60 V 3h = Not defined

7.7.3.3 DEVICE_CONFIG2 Register (Address = A8h) [Reset = 0000000h]

DEVICE_CONFIG2 is shown in [DEVICE_CONFIG2 Register](#) and described in [DEVICE_CONFIG2 Register Field Descriptions](#).

Return to the [HARDWARE_CONFIGURATION Registers](#).

Register to configure device

Figure 7-75. DEVICE_CONFIG2 Register

31	30	29	28	27	26	25	24
PARITY		RESERVED					
R/W-0h		R/W-0h					
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED		DYNAMIC_CSA_GAIN_EN	DYNAMIC_VOLTAGE_GAIN_EN	DEV_MODE	SPD_RANGE_SELECT	CLK_SEL	
R/W-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
RESERVED	EXT_CLK_EN	EXT_CLK_CONFIG			RESERVED		
R/W-0h	R/W-0h	R/W-0h			R/W-0h		

Table 7-37. DEVICE_CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-14	RESERVED	R/W	0h	Reserved
13	DYNAMIC_CSA_GAIN_EN	R/W	0h	Adjust CSA gain at 1ms rate for optimal current resolution at all current levels 0h = Disable 1h = Enable
12	DYNAMIC_VOLTAGE_GAIN_EN	R/W	0h	Adjust voltage gain at 1ms rate for optimal voltage resolution at all voltage levels 0h = Dynamic Voltage Gain is Disabled 1h = Dynamic Voltage Gain is Enabled
11	DEV_MODE	R/W	0h	Device mode select 0h = Standby Mode 1h = Sleep Mode
10	SPD_RANGE_SELECT	R/W	0h	Speed range selection flag 0h = 100Hz to 100KHz speed PWM input 1h = 10Hz to 10KHz speed PWM input
9-8	CLK_SEL	R/W	0h	Clock Source 0h = Internal Oscillator 1h = Crude Oscillator -- WDT 2h = Crystal Oscillator 3h = External Clock input
7	RESERVED	R/W	0h	Reserved
6	EXT_CLK_EN	R/W	0h	Enable External Clock mode 0h = Disable 1h = Enable

Table 7-37. DEVICE_CONFIG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-3	EXT_CLK_CONFIG	R/W	0h	External Clock Configuration 0h = 8 kHz 1h = 16 kHz 2h = 32 kHz 3h = 64 kHz 4h = 128 kHz 5h = 256 kHz 6h = 512 kHz 7h = 1024 kHz
2-0	RESERVED	R/W	0h	Reserved

7.7.3.4 GD_CONFIG1 Register (Address = ACh) [Reset = 10228100h]

 GD_CONFIG1 is shown in [GD_CONFIG1 Register](#) and described in [GD_CONFIG1 Register Field Descriptions](#).

 Return to the [HARDWARE_CONFIGURATION Registers](#).

Register to configure gated driver settings1

Figure 7-76. GD_CONFIG1 Register

31	30	29	28	27	26	25	24
PARITY	RESERVED		RESERVED	SLEW_RATE		RESERVED	
R/W-0h	R/W-0h		R/W-1h	R/W-0h		R/W-0h	
23	22	21	20	19	18	17	16
RESERVED	RESERVED	RESERVED	RESERVED	OVP_SEL	OVP_EN	RESERVED	OTW_REP
R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h
15	14	13	12	11	10	9	8
RESERVED	RESERVED	RESERVED		TRETRY	OCP_LVL	OCP_MODE	
R/W-1h	R/W-0h	R/W-0h		R/W-0h	R/W-0h	R/W-1h	
7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	CSA_GAIN	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	

Table 7-38. GD_CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-29	RESERVED	R/W	0h	Reserved
28	RESERVED	R/W	1h	Reserved
27-26	SLEW_RATE	R/W	0h	Slew Rate Settings 0h = Slew rate is 25 V/μs 1h = Slew rate is 50 V/μs 2h = Slew rate is 125 V/μs 3h = Slew rate is 200 V/μs
25-24	RESERVED	R/W	0h	Reserved
23	RESERVED	R/W	0h	Reserved
22	RESERVED	R/W	0h	Reserved
21	RESERVED	R/W	1h	Reserved
20	RESERVED	R/W	0h	Reserved
19	OVP_SEL	R/W	0h	Overvoltage Level Setting 0h = VM overvoltage level is 32-V 1h = VM overvoltage level is 20-V
18	OVP_EN	R/W	0h	Overvoltage Enable Bit 0h = Overvoltage protection is disabled 1h = Overvoltage protection is enabled
17	RESERVED	R/W	1h	Reserved
16	OTW_REP	R/W	0h	Overtemperature Warning Reporting Bit 0h = Over temperature reporting on nFAULT is disabled 1h = Over temperature reporting on nFAULT is enabled
15	RESERVED	R/W	1h	Reserved
14	RESERVED	R/W	0h	Reserved
13-12	RESERVED	R/W	0h	Reserved

Table 7-38. GD_CONFIG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	TRETRY	R/W	0h	OCP Retry Time Settings 0h = OCP retry time is 5 ms 1h = OCP retry time is 500 ms
10	OCP_LVL	R/W	0h	Overcurrent Level Setting 0h = OCP level is 16 A (Typical) 1h = OCP level is 24 A (Typical)
9-8	OCP_MODE	R/W	1h	OCP Fault Options 0h = Overcurrent causes a latched fault 1h = Overcurrent causes an automatic retrying fault 2h = Overcurrent is report only but no action is taken 3h = Overcurrent is not reported and no action is taken
7	RESERVED	R/W	0h	Reserved
6	RESERVED	R/W	0h	Reserved
5	RESERVED	R/W	0h	Reserved
4	RESERVED	R/W	0h	Reserved
3	RESERVED	R/W	0h	Reserved
2	RESERVED	R/W	0h	Reserved
1-0	CSA_GAIN	R/W	0h	Current Sense Amplifier's Gain Settings (Used only if DYNAMIC_CSA_GAIN_EN = 0) 0h = CSA gain is 0.15 V/A 1h = CSA gain is 0.3 V/A 2h = CSA gain is 0.6 V/A 3h = CSA gain is 1.2 V/A

7.7.3.5 GD_CONFIG2 Register (Address = AEh) [Reset = 0120000h]

 GD_CONFIG2 is shown in [GD_CONFIG2 Register](#) and described in [GD_CONFIG2 Register Field Descriptions](#).

 Return to the [HARDWARE_CONFIGURATION Registers](#).

Register to configure gated driver settings2

Figure 7-77. GD_CONFIG2 Register

31	30	29	28	27	26	25	24
PARITY	RESERVED	RESERVED				RESERVED	BUCK_PS_DIS
R/W-0h	R/W-0h	R/W-0h				R/W-0h	R/W1C-1h
23	22	21	20	19	18	17	16
BUCK_CL	BUCK_SEL		RESERVED	RESERVED			
R/W-0h	R/W-1h		R/W-0h	R/W-0h			
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED							
R/W-0h							

Table 7-39. GD_CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30	RESERVED	R/W	0h	Reserved
29-26	RESERVED	R/W	0h	Reserved
25	RESERVED	R/W	0h	Reserved
24	BUCK_PS_DIS	R/W1C	1h	Buck Power Sequencing Disable Bit 0h = Buck power sequencing is enabled 1h = Buck power sequencing is disabled
23	BUCK_CL	R/W	0h	Buck Current Limit Setting 0h = Buck regulator current limit is set to 600 mA 1h = Buck regulator current limit is set to 150 mA
22-21	BUCK_SEL	R/W	1h	Buck Voltage Selection 0h = Buck voltage is 3.3 V 1h = Buck voltage is 5.0 V 2h = Buck voltage is 4.0 V 3h = Buck voltage is 5.7 V
20	RESERVED	R/W	0h	Reserved
19-0	RESERVED	R/W	0h	Reserved

7.8 RAM (Volatile) Register Map

7.8.1 Fault_Status Registers

[FAULT_STATUS Registers](#) lists the memory-mapped registers for the Fault_Status registers. All register offset addresses not listed in [FAULT_STATUS Registers](#) should be considered as reserved locations and the register contents should not be modified.

Table 7-40. FAULT_STATUS Registers

Address	Acronym	Register Name	Section
E0h	GATE_DRIVER_FAULT_STATUS	Fault Status Register	Section 7.8.1.1
E2h	CONTROLLER_FAULT_STATUS	Fault Status Register	Section 7.8.1.2

Complex bit access types are encoded to fit into small table cells. [Fault_Status Access Type Codes](#) shows the codes that are used for access types in this section.

Table 7-41. Fault_Status Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Reset or Default Value		
-n		Value after reset or the default value

7.8.1.1 GATE_DRIVER_FAULT_STATUS Register (Address = E0h) [Reset = 0000000h]

GATE_DRIVER_FAULT_STATUS is shown in [GATE_DRIVER_FAULT_STATUS Register](#) and described in [GATE_DRIVER_FAULT_STATUS Register Field Descriptions](#).

Return to the [FAULT_STATUS Registers](#).

Status of various gate driver faults

Figure 7-78. GATE_DRIVER_FAULT_STATUS Register

31	30	29	28	27	26	25	24
DRIVER_FAULT	BK_FLT	RESERVED	OCP	NPOR	OVP	OT	RESERVED
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
23	22	21	20	19	18	17	16
OTW	OTS	OCP_HC	OCP_LC	OCP_HB	OCP_LB	OCP_HA	OCP_LA
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
15	14	13	12	11	10	9	8
RESERVED	OTP_ERR	BUCK_OCP	BUCK_UV	VCP_UV	RESERVED		
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h		
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 7-42. GATE_DRIVER_FAULT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DRIVER_FAULT	R	0h	Logic OR of FAULT status registers. Mirrors nFAULT pin.

Table 7-42. GATE_DRIVER_FAULT_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
30	BK_FLT	R	0h	Buck Fault Bit 0h = No buck regulator fault condition is detected 1h = Buck regulator fault condition is detected
29	RESERVED	R	0h	Reserved
28	OCP	R	0h	Over Current Protection Status Bit 0h = No overcurrent condition is detected 1h = Overcurrent condition is detected
27	NPOR	R	0h	Supply Power On Reset Bit 0h = Power on reset condition is detected on VM 1h = No power-on-reset condition is detected on VM
26	OVP	R	0h	Supply Overvoltage Protection Status Bit 0h = No overvoltage condition is detected on VM 1h = Overvoltage condition is detected on VM
25	OT	R	0h	Overtemperature Fault Status Bit 0h = No overtemperature warning / shutdown is detected 1h = Overtemperature warning / shutdown is detected
24	RESERVED	R	0h	Reserved
23	OTW	R	0h	Overtemperature Warning Status Bit 0h = No overtemperature warning is detected 1h = Overtemperature warning is detected
22	OTS	R	0h	Overtemperature Shutdown Status Bit 0h = No overtemperature shutdown is detected 1h = Overtemperature shutdown is detected
21	OCP_HC	R	0h	Overcurrent Status on High-side switch of OUTC 0h = No overcurrent detected on high-side switch of OUTC 1h = Overcurrent detected on high-side switch of OUTC
20	OCP_LC	R	0h	Overcurrent Status on Low-side switch of OUTC 0h = No overcurrent detected on low-side switch of OUTC 1h = Overcurrent detected on low-side switch of OUTC
19	OCP_HB	R	0h	Overcurrent Status on High-side switch of OUTB 0h = No overcurrent detected on high-side switch of OUTB 1h = Overcurrent detected on high-side switch of OUTB
18	OCP_LB	R	0h	Overcurrent Status on Low-side switch of OUTB 0h = No overcurrent detected on low-side switch of OUTB 1h = Overcurrent detected on low-side switch of OUTB
17	OCP_HA	R	0h	Overcurrent Status on High-side switch of OUTA 0h = No overcurrent detected on high-side switch of OUTA 1h = Overcurrent detected on high-side switch of OUTA
16	OCP_LA	R	0h	Overcurrent Status on Low-side switch of OUTA 0h = No overcurrent detected on low-side switch of OUTA 1h = Overcurrent detected on low-side switch of OUTA
15	RESERVED	R	0h	Reserved
14	OTP_ERR	R	0h	One Time Programmability Error 0h = No OTP error is detected 1h = OTP Error is detected
13	BUCK_OCP	R	0h	Buck Regulator Overcurrent Status Bit 0h = No buck regulator overcurrent is detected 1h = Buck regulator overcurrent is detected

Table 7-42. GATE_DRIVER_FAULT_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	BUCK_UV	R	0h	Buck Regulator Undervoltage Status Bit 0h = No buck regulator undervoltage is detected 1h = Buck regulator undervoltage is detected
11	VCP_UV	R	0h	Charge Pump Undervoltage Status Bit 0h = No charge pump undervoltage is detected 1h = Charge pump undervoltage is detected
10-0	RESERVED	R	0h	Reserved

7.8.1.2 CONTROLLER_FAULT_STATUS Register (Address = E2h) [Reset = 0000000h]

CONTROLLER_FAULT_STATUS is shown in [CONTROLLER_FAULT_STATUS Register](#) and described in [CONTROLLER_FAULT_STATUS Register Field Descriptions](#).

Return to the [FAULT_STATUS Registers](#).

Status of various controller faults

Figure 7-79. CONTROLLER_FAULT_STATUS Register

31	30	29	28	27	26	25	24
CONTROLLER_FAULT	OTW_CONTROLLER	IPD_FREQ_FAULT	IPD_T1_FAULT	IPD_T2_FAULT	BUS_CURRENT_LIMIT_STATUS	MPET_IPD_FAULT	MPET_BEMF_FAULT
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
23	22	21	20	19	18	17	16
ABN_SPEED	ABN_BEMF	NO_MTR	MTR_LCK	LOCK_LIMIT	HW_LOCK_LIMIT	MTR_UNDER_VOLTAGE	MTR_OVER_VOLTAGE
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
15	14	13	12	11	10	9	8
SPEED_LOOP_SATURATION	CURRENT_LOOP_SATURATION	RESERVED					
R-0h	R-0h	R-0h					
7	6	5	4	3	2	1	0
RESERVED					RESERVED	RESERVED	APP_RESET
R-0h					R-0h	R-0h	R-0h

Table 7-43. CONTROLLER_FAULT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CONTROLLER_FAULT	R	0h	Logic OR of Controller FAULT status registers
30	OTW_CONTROLLER	R	0h	Indicates overtemperature controller
29	IPD_FREQ_FAULT	R	0h	Indicates IPD frequency fault
28	IPD_T1_FAULT	R	0h	Indicates IPD T1 fault
27	IPD_T2_FAULT	R	0h	Indicates IPD T2 fault
26	BUS_CURRENT_LIMIT_STATUS	R	0h	Indicates status of Bus Current limit
25	MPET_IPD_FAULT	R	0h	Indicates error during resistance and inductance measurement
24	MPET_BEMF_FAULT	R	0h	Indicates error during BEMF constant measurement
23	ABN_SPEED	R	0h	Indicates Abnormal speed motor lock condition
22	ABN_BEMF	R	0h	Indicates Abnormal BEMF motor lock condition
21	NO_MTR	R	0h	Indicates No Motor fault

Table 7-43. CONTROLLER_FAULT_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	MTR_LCK	R	0h	Indicates when one of the motor lock is triggered
19	LOCK_LIMIT	R	0h	Indicates Lock llimit fault
18	HW_LOCK_LIMIT	R	0h	Indicates Hardware Lock llimit fault
17	MTR_UNDER_VOLTAGE	R	0h	Indicates Motor Undervoltage fault
16	MTR_OVER_VOLTAGE	R	0h	Indicates Motor Over voltage fault
15	SPEED_LOOP_SATURAT ION	R	0h	Indicates speed loop saturation
14	CURRENT_LOOP_SATU RATION	R	0h	Indicates current loop saturation
13-3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1	RESERVED	R	0h	Reserved
0	APP_RESET	R	0h	App Reset

7.8.2 System_Status Registers

[SYSTEM_STATUS Registers](#) lists the memory-mapped registers for the System_Status registers. All register offset addresses not listed in [SYSTEM_STATUS Registers](#) should be considered as reserved locations and the register contents should not be modified.

Table 7-44. SYSTEM_STATUS Registers

Address	Acronym	Register Name	Section
E4h	ALGO_STATUS	System Status Register	Section 7.8.2.1
E6h	MTR_PARAMS	System Status Register	Section 7.8.2.2
E8h	ALGO_STATUS_MPET	System Status Register	Section 7.8.2.3

Complex bit access types are encoded to fit into small table cells. [System_Status Access Type Codes](#) shows the codes that are used for access types in this section.

Table 7-45. System_Status Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Reset or Default Value		
-n		Value after reset or the default value

7.8.2.1 ALGO_STATUS Register (Address = E4h) [Reset = 0000000h]

ALGO_STATUS is shown in [ALGO_STATUS Register](#) and described in [ALGO_STATUS Register Field Descriptions](#).

Return to the [SYSTEM_STATUS Registers](#).

Status of various system and algorithm parameters

Figure 7-80. ALGO_STATUS Register

31	30	29	28	27	26	25	24
VOLT_MAG							
R-0h							
23	22	21	20	19	18	17	16

Figure 7-80. ALGO_STATUS Register (continued)

VOLT_MAG							
R-0h							
15	14	13	12	11	10	9	8
DUTY_CMD							
R-0h							
7	6	5	4	3	2	1	0
DUTY_CMD				SLEEP_STATU S	SYS_INIT_DON E	SYS_ENABLE_ FLAG	RESERVED
R-0h				R-0h	R-0h	R-0h	R-0h

Table 7-46. ALGO_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	VOLT_MAG	R	0h	16-bit value indicating applied voltage magnitude. Voltage magnitude applied = VOLT_MAG * 100 / 32768 %
15-4	DUTY_CMD	R	0h	12-bit value indicating decoded speed command in PWM/Analog mode DUTY_CMD (%) = DUTY_CMD/4096 * 100%.
3	SLEEP_STATUS	R	0h	Sleep mode status 0h = Device is in sleep mode 1h = Device is in active mode
2	SYS_INIT_DONE	R	0h	1 indicates device is ready for GUI control 0 indicates firmware is still copying EEPROM to shadow memory
1	SYS_ENABLE_FLAG	R	0h	1 indicates GUI can control the register 0 indicates GUI is still copying default parameters from shadow memory
0	RESERVED	R	0h	Reserved

7.8.2.2 MTR_PARAMS Register (Address = E6h) [Reset = 0000000h]

MTR_PARAMS is shown in [MTR_PARAMS Register](#) and described in [MTR_PARAMS Register Field Descriptions](#).

Return to the [SYSTEM_STATUS Registers](#).

Status of various motor parameters

Figure 7-81. MTR_PARAMS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MOTOR_R								MOTOR_BEMF_CONST							
R-0h								R-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOTOR_L								RESERVED							
R-0h								R-0h							

Table 7-47. MTR_PARAMS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	MOTOR_R	R	0h	8-bit value indicating measured Motor Resistance
23-16	MOTOR_BEMF_CONST	R	0h	8-bit value indicating measured BEMF constant
15-8	MOTOR_L	R	0h	8-bit value indicating measured Motor Inductance
7-0	RESERVED	R	0h	Reserved

7.8.2.3 ALGO_STATUS_MPET Register (Address = E8h) [Reset = 0000000h]

ALGO_STATUS_MPET is shown in [ALGO_STATUS_MPET Register](#) and described in [ALGO_STATUS_MPET Register Field Descriptions](#).

Return to the [SYSTEM_STATUS Registers](#).

Status of various MPET parameters

Figure 7-82. ALGO_STATUS_MPET Register

31	30	29	28	27	26	25	24
MPET_R_STAT US	MPET_L_STAT US	MPET_KE_STA TUS	MPET_MECH_ STATUS	MPET_PWM_FREQ			
R-0h	R-0h	R-0h	R-0h	R-0h			
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 7-48. ALGO_STATUS_MPET Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MPET_R_STATUS	R	0h	Indicates status of Resistance measurement
30	MPET_L_STATUS	R	0h	Indicates status of Inductance measurement
29	MPET_KE_STATUS	R	0h	Indicates status of BEMF constant measurement
28	MPET_MECH_STATUS	R	0h	Indicates status of mechanical parameter measurement
27-24	MPET_PWM_FREQ	R	0h	4-bit value indicating PWM frequency used during BEMF constant measurement
23-0	RESERVED	R	0h	Reserved

7.8.3 Control Registers

[CONTROL Registers](#) lists the memory-mapped registers for the Control registers. All register offset addresses not listed in [CONTROL Registers](#) should be considered as reserved locations and the register contents should not be modified.

Table 7-49. CONTROL Registers

Address	Acronym	Register Name	Section
EAh	ALGO_CTRL1	Device Control Register	Section 7.8.3.1

Complex bit access types are encoded to fit into small table cells. [Control Access Type Codes](#) shows the codes that are used for access types in this section.

Table 7-50. Control Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write

Table 7-50. Control Access Type Codes (continued)

Access Type	Code	Description
Reset or Default Value		
-n		Value after reset or the default value

7.8.3.1 ALGO_CTRL1 Register (Address = EAh) [Reset = 00073800h]

ALGO_CTRL1 is shown in [ALGO_CTRL1 Register](#) and described in [ALGO_CTRL1 Register Field Descriptions](#).

Return to the [CONTROL Registers](#).

Control settings

Figure 7-83. ALGO_CTRL1 Register

31	30	29	28	27	26	25	24
EEPROM_WRT	EEPROM_READ	CLR_FLT	CLR_FLT_RETRY_COUNT	RESERVED			
R/W-0h	R/W-0h	W-0h	W-0h	W-0h			
23	22	21	20	19	18	17	16
RESERVED				DACOUT2_SCALING			
W-0h				W-7h			
15	14	13	12	11	10	9	8
DACOUT2_UNIPOLAR	DACOUT1_SCALING				DACOUT1_UNIPOLAR	FORCED_ALIGN_ANGLE	
W-0h	W-7h				W-0h	W-0h	
7	6	5	4	3	2	1	0
FORCED_ALIGN_ANGLE							RESERVED
W-0h							W-0h

Table 7-51. ALGO_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EEPROM_WRT	R/W	0h	Write the configuration to EEPROM
30	EEPROM_READ	R/W	0h	Read the default configuration from EEPROM
29	CLR_FLT	W	0h	Clears all faults
28	CLR_FLT_RETRY_COUNT	W	0h	Clears fault retry count
27-20	RESERVED	W	0h	Reserved

Table 7-51. ALGO_CTRL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19-16	DACOUT2_SCALING	W	7h	<p>Scaling factor for DACOUT2</p> <p>Algorithm Variable extracted from the address contained in DACOUT2_VAR_ADDR scaled with DACOUT2_SCALING / 16. Actual voltage depends on DACOUT2_UNIPOLAR.</p> <p>If DACOUT2_UNIPOLAR = 1, 0V == 0pu of algorithmVariable * DACOUT2_SCALING / 16, 3V == 1pu of algorithmVariable * DACOUT2_SCALING / 16</p> <p>If DACOUT2_UNIPOLAR = 0, 0V == -1pu of algorithmVariable * DACOUT2_SCALING / 16, 3V == 1pu of algorithmVariable * DACOUT2_SCALING / 16</p> <p>0h = Disabled</p> <p>1h = 1 / 16</p> <p>2h = 2 / 16</p> <p>3h = 3 / 16</p> <p>4h = 4 / 16</p> <p>5h = 5 / 16</p> <p>6h = 6 / 16</p> <p>7h = 7 / 16</p> <p>8h = 8 / 16</p> <p>9h = 9 / 16</p> <p>Ah = 10 / 16</p> <p>Bh = 11 / 16</p> <p>Ch = 12 / 16</p> <p>Dh = 13 / 16</p> <p>Eh = 14 / 16</p> <p>Fh = 15 / 16</p>
15	DACOUT2_UNIPOLAR	W	0h	<p>Configures output of DACOUT2</p> <p>If DACOUT2_UNIPOLAR = 1, 0V == 0pu of algorithmVariable * DACOUT2_SCALING / 16, 3V == 1pu of algorithmVariable * DACOUT2_SCALING / 16</p> <p>If DACOUT2_UNIPOLAR = 0, 0V == -1pu of algorithmVariable * DACOUT2_SCALING / 16, 3V == 1pu of algorithmVariable * DACOUT2_SCALING / 16</p> <p>0h = Bipolar (Offset of 1.5 V)</p> <p>1h = Unipolar (No Offset)</p>

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Table 7-51. ALGO_CTRL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14-11	DACOUT1_SCALING	W	7h	Scaling factor for DACOUT1 Algorithm Variable extracted from the address contained in DACOUT1_VAR_ADDR scaled with DACOUT1_SCALING / 16. Actual voltage depends on DACOUT1_UNIPOLAR. If DACOUT1_UNIPOLAR = 1, 0V == 0pu of algorithmVariable * DACOUT1_SCALING / 16, 3V == 1pu of algorithmVariable * DACOUT1_SCALING / 16 If DACOUT1_UNIPOLAR = 0, 0V == -1pu of algorithmVariable * DACOUT1_SCALING / 16, 3V == 1pu of algorithmVariable * DACOUT1_SCALING / 16 0h = Disabled 1h = 1 / 16 2h = 2 / 16 3h = 3 / 16 4h = 4 / 16 5h = 5 / 16 6h = 6 / 16 7h = 7 / 16 8h = 8 / 16 9h = 9 / 16 Ah = 10 / 16 Bh = 11 / 16 Ch = 12 / 16 Dh = 13 / 16 Eh = 14 / 16 Fh = 15 / 16
10	DACOUT1_UNIPOLAR	W	0h	Configures output of DACOUT1 If DACOUT1_UNIPOLAR = 1, 0V == 0pu of algorithmVariable * DACOUT1_SCALING / 16, 3V == 1pu of algorithmVariable * DACOUT1_SCALING / 16 If DACOUT1_UNIPOLAR = 0, 0V == -1pu of algorithmVariable * DACOUT1_SCALING / 16, 3V == 1pu of algorithmVariable * DACOUT1_SCALING / 16 0h = Bipolar (Offset of 1.5 V) 1h = Unipolar (No Offset)
9-1	FORCED_ALIGN_ANGLE	W	0h	9-bit value (in degrees) used during forced Align state (FORCE_ALIGN_EN = 1) Angle applied = FORCED_ALIGN_ANGLE % 360deg
0	RESERVED	W	0h	Reserved

7.8.4 Algorithm_Control Registers

[ALGORITHM_CONTROL Registers](#) lists the memory-mapped registers for the Algorithm_Control registers. All register offset addresses not listed in [ALGORITHM_CONTROL Registers](#) should be considered as reserved locations and the register contents should not be modified.

Table 7-52. ALGORITHM_CONTROL Registers

Address	Acronym	Register Name	Section
ECh	ALGO_DEBUG1	Algorithm Control Register	Section 7.8.4.1
Eh	ALGO_DEBUG2	Algorithm Control Register	Section 7.8.4.2
F0h	CURRENT_PI	Current PI Controller used	Section 7.8.4.3
F2h	SPEED_PI	Speed PI controller used	Section 7.8.4.4

Complex bit access types are encoded to fit into small table cells. [Algorithm_Control Access Type Codes](#) shows the codes that are used for access types in this section.

Table 7-53. Algorithm_Control Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.8.4.1 ALGO_DEBUG1 Register (Address = ECh) [Reset = 0000000h]

ALGO_DEBUG1 is shown in [ALGO_DEBUG1 Register](#) and described in [ALGO_DEBUG1 Register Field Descriptions](#).

Return to the [ALGORITHM_CONTROL Registers](#).

Algorithm control register for debug

Figure 7-84. ALGO_DEBUG1 Register

31	30	29	28	27	26	25	24
OVERRIDE		DIGITAL_SPEED_CTRL					
W-0h		W-0h					
23	22	21	20	19	18	17	16
DIGITAL_SPEED_CTRL				CURRENT_LO OP_DIS	CLOSED_LOO P_DIS	FORCE_ALIGN _EN	
W-0h				W-0h	W-0h	W-0h	
15	14	13	12	11	10	9	8
FORCE_SLOW _FIRST_CYCL E_EN	FORCE_IPD_E N	FORCE_ISD_E N	FORCE_ALIGN _ANGLE_SRC_ SEL	FORCE_IQ_REF_SPEED_LOOP_DIS			
W-0h	W-0h	W-0h	W-0h	W-0h			
7	6	5	4	3	2	1	0
FORCE_IQ_REF_SPEED_LOOP_DIS						RESERVED	
W-0h						W-0h	

Table 7-54. ALGO_DEBUG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	OVERRIDE	W	0h	Use to control the SPD_CTRL bits. If OVERRIDE = '1', speed command can be written by the user through serial interface. 0h = SPEED_CMD using Analog/PWM mode 1h = SPEED_CMD using DIGITAL_SPEED_CTRL
30-19	DIGITAL_SPEED_CTRL	W	0h	Digital Speed Control If OVERRIDE = 0b1, then SPEED_CMD is control using DIGITAL_SPEED_CTRL
18	CURRENT_LOOP_DIS	W	0h	Use to control the FORCE_VD_CURRENT_LOOP_DIS and FORCE_VQ_CURRENT_LOOP_DIS. If CURRENT_LOOP_DIS = '1', Current loop and speed loop is disabled 0h = Enable Current Loop 1h = Disable Current Loop

Table 7-54. ALGO_DEBUG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	CLOSED_LOOP_DIS	W	0h	Use to disable Closed loop 0h = Enable Closed Loop 1h = Disable Closed loop, motor commutation in open loop
16	FORCE_ALIGN_EN	W	0h	Force Align State Enable 0h = Disable Force Align state, device comes out of align state if MTR_STARTUP is selected as ALIGN or DOUBLE ALIGN 1h = Enable Force Align state, device stays in align state if MTR_STARTUP is selected as ALIGN or DOUBLE ALIGN
15	FORCE_SLOW_FIRST_CYCLE_EN	W	0h	Force Slow First Cycle Enable 0h = Disable Force Slow First Cycle state, device comes out of slow first cycle state if MTR_STARTUP is selected as SLOW FIRST CYCLE 1h = Enable Force Slow First Cycle state, device stays in slow first cycle state if MTR_STARTUP is selected as SLOW FIRST CYCLE
14	FORCE_IPD_EN	W	0h	Force IPD Enable 0h = Disable Force IPD state, device comes out of IPD state if MTR_STARTUP is selected as IPD 1h = Enable Force IPD state, device stays in IPD state if MTR_STARTUP is selected as IPD
13	FORCE_ISD_EN	W	0h	Force ISD enable 0h = Disable Force ISD state, device comes out of ISD state if ISD_EN is set 1h = Enable Force ISD state, device stays in ISD state if ISD_EN is set
12	FORCE_ALIGN_ANGLE_SRC_SEL	W	0h	Force Align Angle State Source Select 0h = Force Align Angle defined by ALIGN_ANGLE 1h = Force Align Angle defined by FORCED_ALIGN_ANGLE
11-2	FORCE_IQ_REF_SPEED_LOOP_DIS	W	0h	Sets IQ Ref (% of BASE_CURRENT) when speed loop is disabled Formula: FORCE_IQ_REF_SPEED_LOOP_DIS / 10 * BASE_CURRENT If SPEED_LOOP_DIS = 0b1, then Iq_ref is control using IQ_REF_SPEED_LOOP_DIS $iqRef = (FORCE_IQ_REF_SPEED_LOOP_DIS / 500) * BASE_CURRENT$ if FORCE_IQ_REF_SPEED_LOOP_DIS < 500 $-(FORCE_IQ_REF_SPEED_LOOP_DIS - 512) / 500 * BASE_CURRENT$ if FORCE_IQ_REF_SPEED_LOOP_DIS > 512 Valid values are 0 to 500 and 512 to 1000
1-0	RESERVED	W	0h	Reserved

7.8.4.2 ALGO_DEBUG2 Register (Address = EEh) [Reset = 0000000h]

ALGO_DEBUG2 is shown in [ALGO_DEBUG2 Register](#) and described in [ALGO_DEBUG2 Register Field Descriptions](#).

Return to the [ALGORITHM_CONTROL Registers](#).

Algorithm control register for debug

Figure 7-85. ALGO_DEBUG2 Register

31	30	29	28	27	26	25	24
RESERVED						FORCE_VD_CURRENT_LOOP_DIS	
W-0h						W-0h	
23	22	21	20	19	18	17	16

Figure 7-85. ALGO_DEBUG2 Register (continued)

FORCE_VD_CURRENT_LOOP_DIS							
W-0h							
15	14	13	12	11	10	9	8
FORCE_VQ_CURRENT_LOOP_DIS							
W-0h							
7	6	5	4	3	2	1	0
FORCE_VQ_CURRENT_LOOP_DIS	MPET_CMD	MPET_R	MPET_L	MPET_KE	MPET_MECH	MPET_WRITE_SHADOW	
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

Table 7-55. ALGO_DEBUG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	W	0h	Reserved
25-16	FORCE_VD_CURRENT_LOOP_DIS	W	0h	Sets Vd when current loop speed loop are disabled If CURRENT_LOOP_DIS = 0b1, then Vd is control using FORCE_VD_CURRENT_LOOP_DIS $mdRef = (FORCE_VD_CURRENT_LOOP_DIS / 500)$ if $FORCE_VD_CURRENT_LOOP_DIS < 500$ $-(FORCE_VD_CURRENT_LOOP_DIS - 512)/500$ if $FORCE_VD_CURRENT_LOOP_DIS > 512$ Valid values: 0 to 500 and 512 to 1000
15-6	FORCE_VQ_CURRENT_LOOP_DIS	W	0h	Sets Vq when current loop speed loop are disabled If CURRENT_LOOP_DIS = 0b1, then Vq is control using FORCE_VQ_CURRENT_LOOP_DIS $mqRef = (FORCE_VQ_CURRENT_LOOP_DIS / 500)$ if $FORCE_VQ_CURRENT_LOOP_DIS < 500$ $-(FORCE_VQ_CURRENT_LOOP_DIS - 512)/500$ if $FORCE_VQ_CURRENT_LOOP_DIS > 512$ Valid values: 0 to 500 and 512 to 1000
5	MPET_CMD	W	0h	Initiates motor parameter measurement routine when set to 1
4	MPET_R	W	0h	Enables motor resistance measurement during motor parameter measurement routine 0h = Disables Motor Resistance measurement during motor parameter measurement routine 1h = Enable Motor Resistance measurement during motor parameter measurement routine
3	MPET_L	W	0h	Enables motor inductance measurement during motor parameter measurement routine 0h = Disables Motor Inductance measurement during motor parameter measurement routine 1h = Enable Motor Inductance measurement during motor parameter measurement routine
2	MPET_KE	W	0h	Enables motor BEMF constant measurement during motor parameter measurement routine 0h = Disables Motor BEMF constant measurement during motor parameter measurement routine 1h = Enable Motor BEMF constant measurement during motor parameter measurement routine
1	MPET_MECH	W	0h	Enables motor mechanical parameter measurement during motor parameter measurement routine 0h = Disables Motor mechanical parameter measurement during motor parameter measurement routine 1h = Enable Motor mechanical parameter measurement during motor parameter measurement routine

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Table 7-55. ALGO_DEBUG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	MPET_WRITE_SHADOW	W	0h	Write measured parameters to shadow register when set to 1

7.8.4.3 CURRENT_PI Register (Address = F0h) [Reset = 0000000h]

CURRENT_PI is shown in [CURRENT_PI Register](#) and described in [CURRENT_PI Register Field Descriptions](#).
Return to the [ALGORITHM_CONTROL Registers](#).

Current PI controller used

Figure 7-86. CURRENT_PI Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CURRENT_LOOP_KP										CURRENT_LOOP_KI					
R-0h										R-0h					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CURRENT_LOOP_KI					RESERVED										
R-0h					R-0h										

Table 7-56. CURRENT_PI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	CURRENT_LOOP_KP	R	0h	10 bit for current loop kp Same Scaling as CURR_LOOP_KP
21-12	CURRENT_LOOP_KI	R	0h	10 bit for current loop ki Same Scaling as CURR_LOOP_KI
11-0	RESERVED	R	0h	Reserved

7.8.4.4 SPEED_PI Register (Address = F2h) [Reset = 0000000h]

SPEED_PI is shown in [SPEED_PI Register](#) and described in [SPEED_PI Register Field Descriptions](#).
Return to the [ALGORITHM_CONTROL Registers](#).

Speed PI controller used

Figure 7-87. SPEED_PI Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SPEED_LOOP_KP										SPEED_LOOP_KI					
R-0h										R-0h					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPEED_LOOP_KI					RESERVED										
R-0h					R-0h										

Table 7-57. SPEED_PI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	SPEED_LOOP_KP	R	0h	10 bit for speed loop kp Same Scaling as SPD_LOOP_KP
21-12	SPEED_LOOP_KI	R	0h	10 bit for speed loop ki Same Scaling as SPD_LOOP_KI
11-0	RESERVED	R	0h	Reserved

7.8.5 Algorithm_Variables Registers

[ALGORITHM_VARIABLES Registers](#) lists the memory-mapped registers for the Algorithm_Variables registers. All register offset addresses not listed in [ALGORITHM_VARIABLES Registers](#) should be considered as reserved locations and the register contents should not be modified.

Table 7-58. ALGORITHM_VARIABLES Registers

Address	Acronym	Register Name	Section
20Eh	ALGORITHM_STATE	Current Algorithm State Register	Section 7.8.5.1
410h	BUS_CURRENT	Calculated Supply Current Register	Section 7.8.5.2
440h	PHASE_CURRENT_A	Measured current on Phase A Register	Section 7.8.5.3
442h	PHASE_CURRENT_B	Measured current on Phase B Register	Section 7.8.5.4
444h	PHASE_CURRENT_C	Measured current on Phase C Register	Section 7.8.5.5
468h	CSA_GAIN_FEEDBACK	CSA Gain Register	Section 7.8.5.6
478h	VOLTAGE_GAIN_FEEDBACK	Voltage Gain Register	Section 7.8.5.7
47Ah	VM_VOLTAGE	VM Voltage Register	Section 7.8.5.8
47Eh	PHASE_VOLTAGE_VA	Phase Voltage Register	Section 7.8.5.9
480h	PHASE_VOLTAGE_VB	Phase Voltage Register	Section 7.8.5.10
482h	PHASE_VOLTAGE_VC	Phase Voltage Register	Section 7.8.5.11
4BAh	SIN_COMMUTATION_ANGLE	Sine of Commutation Angle	Section 7.8.5.12
4BCCh	COS_COMMUTATION_ANGLE	Cosine of Commutation Angle	Section 7.8.5.13
4D2h	IALPHA	IALPHA Current Register	Section 7.8.5.14
4D4h	IBETA	IBETA Current Register	Section 7.8.5.15
4D6h	VALPHA	VALPHA Voltage Register	Section 7.8.5.16
4D8h	VBETA	VBETA Voltage Register	Section 7.8.5.17
4E2h	ID	Measured d-axis Current Register	Section 7.8.5.18
4E4h	IQ	Measured q-axis Current Register	Section 7.8.5.19
4E6h	VD	VD Voltage Register	Section 7.8.5.20
4E8h	VQ	VQ Voltage Register	Section 7.8.5.21
522h	IQ_REF_ROTOR_ALIGN	Align Current Reference	Section 7.8.5.22
538h	SPEED_REF_OPEN_LOOP	Open Loop Speed Register	Section 7.8.5.23
546h	IQ_REF_OPEN_LOOP	Open Loop Current Reference	Section 7.8.5.24
5C8h	SPEED_REF_CLOSED_LOOP	Speed Reference Register	Section 7.8.5.25
5EEh	ID_REF_CLOSED_LOOP	Reference for Current Loop Register	Section 7.8.5.26
5F0h	IQ_REF_CLOSED_LOOP	Reference for Current Loop Register	Section 7.8.5.27
668h	ISD_STATE	ISD state Register	Section 7.8.5.28
672h	ISD_SPEED	ISD Speed Register	Section 7.8.5.29
69Ah	IPD_STATE	IPD state Register	Section 7.8.5.30
6DEh	IPD_ANGLE	Calculated IPD Angle Register	Section 7.8.5.31
724h	EQ	Estimated BEMF EQ Register	Section 7.8.5.32
726h	ED	Estimated BEMF ED Register	Section 7.8.5.33
734h	SPEED_FDBK	Speed Feedback Register	Section 7.8.5.34
736h	THETA_EST	Estimated motor position Register	Section 7.8.5.35

Complex bit access types are encoded to fit into small table cells. [Algorithm_Variables Access Type Codes](#) shows the codes that are used for access types in this section.

Table 7-59. Algorithm_Variables Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Reset or Default Value		
-n		Value after reset or the default value

7.8.5.1 ALGORITHM_STATE Register (Address = 20Eh) [Reset = 0000h]

ALGORITHM_STATE is shown in [ALGORITHM_STATE Register](#) and described in [ALGORITHM_STATE Register Field Descriptions](#).

Return to the [ALGORITHM_VARIABLES Registers](#).

Current Algorithm State Register

Figure 7-88. ALGORITHM_STATE Register

15	14	13	12	11	10	9	8
ALGORITHM_STATE							
R-0h							
7	6	5	4	3	2	1	0
ALGORITHM_STATE							
R-0h							

Table 7-60. ALGORITHM_STATE Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	ALGORITHM_STATE	R	0h	16-bit value indicating current state of device 0h = MOTOR_IDLE 1h = MOTOR_ISD 2h = MOTOR_TRISTATE 3h = MOTOR_BRAKE_ON_START 4h = MOTOR_IPD 5h = MOTOR_SLOW_FIRST_CYCLE 6h = MOTOR_ALIGN 7h = MOTOR_OPEN_LOOP 8h = MOTOR_CLOSED_LOOP_UNALIGNED 9h = MOTOR_CLOSED_LOOP_ALIGNED Ah = MOTOR_CLOSED_LOOP_ACTIVE_BRAKING Bh = MOTOR_SOFT_STOP Ch = MOTOR_RECIRCULATE_STOP Dh = MOTOR_BRAKE_ON_STOP Eh = MOTOR_FAULT Fh = MOTOR_MPET_MOTOR_STOP_CHECK 10h = MOTOR_MPET_MOTOR_STOP_WAIT 11h = MOTOR_MPET_MOTOR_BRAKE 12h = MOTOR_MPET_ALGORITHM_PARAMETERS_INIT 13h = MOTOR_MPET_RL_MEASURE 14h = MOTOR_MPET_KE_MEASURE 15h = MOTOR_MPET_STALL_CURRENT_MEASURE 16h = MOTOR_MPET_TORQUE_MODE 17h = MOTOR_MPET_DONE 18h = MOTOR_MPET_FAULT

7.8.5.2 BUS_CURRENT Register (Address = 410h) [Reset = 00000000h]

BUS_CURRENT is shown in [BUS_CURRENT Register](#) and described in [BUS_CURRENT Register Field Descriptions](#).

Return to the [ALGORITHM_VARIABLES Registers](#).

Calculated Supply Current Register

Figure 7-89. BUS_CURRENT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BUS_CURRENT																															
R-0h																															

Table 7-61. BUS_CURRENT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BUS_CURRENT	R	0h	32-bit value indicating bus current $i_{Bus} = (BUS_CURRENT / 2^{27}) * Base_Current/8$

7.8.5.3 PHASE_CURRENT_A Register (Address = 440h) [Reset = 0000000h]

PHASE_CURRENT_A is shown in [PHASE_CURRENT_A Register](#) and described in [PHASE_CURRENT_A Register Field Descriptions](#).

Return to the [ALGORITHM_VARIABLES Registers](#).

Measured current on Phase A Register

Figure 7-90. PHASE_CURRENT_A Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHASE_CURRENT_A																															
R-0h																															

Table 7-62. PHASE_CURRENT_A Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHASE_CURRENT_A	R	0h	32-bit value indicating measured current on Phase A $i_A = (PHASE_CURRENT_A / 2^{27}) * Base_Current/8$

7.8.5.4 PHASE_CURRENT_B Register (Address = 442h) [Reset = 0000000h]

PHASE_CURRENT_B is shown in [PHASE_CURRENT_B Register](#) and described in [PHASE_CURRENT_B Register Field Descriptions](#).

Return to the [ALGORITHM_VARIABLES Registers](#).

Measured current on Phase B Register

Figure 7-91. PHASE_CURRENT_B Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHASE_CURRENT_B																															
R-0h																															

Table 7-63. PHASE_CURRENT_B Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHASE_CURRENT_B	R	0h	32-bit value indicating measured current on Phase B $i_B = (PHASE_CURRENT_B / 2^{27}) * Base_Current/8$

7.8.5.5 PHASE_CURRENT_C Register (Address = 444h) [Reset = 0000000h]

PHASE_CURRENT_C is shown in [PHASE_CURRENT_C Register](#) and described in [PHASE_CURRENT_C Register Field Descriptions](#).

Return to the [ALGORITHM_VARIABLES Registers](#).

Measured current on Phase C Register

Figure 7-92. PHASE_CURRENT_C Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHASE_CURRENT_C																															
R-0h																															

Table 7-64. PHASE_CURRENT_C Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHASE_CURRENT_C	R	0h	32-bit value indicating measured current on Phase C $i_C = (\text{PHASE_CURRENT_C} / 2^{27}) * \text{Base_Current}/8$

7.8.5.6 CSA_GAIN_FEEDBACK Register (Address = 468h) [Reset = 0000h]

CSA_GAIN_FEEDBACK is shown in [CSA_GAIN_FEEDBACK Register](#) and described in [CSA_GAIN_FEEDBACK Register Field Descriptions](#).

Return to the [ALGORITHM_VARIABLES Registers](#).

VM Voltage Register

Figure 7-93. CSA_GAIN_FEEDBACK Register

15	14	13	12	11	10	9	8
CSA_GAIN_FEEDBACK							
R-0h							
7	6	5	4	3	2	1	0
CSA_GAIN_FEEDBACK							
R-0h							

Table 7-65. CSA_GAIN_FEEDBACK Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	CSA_GAIN_FEEDBACK	R	0h	16-bit value indicating current sense gain 0h = MAX_CSA_GAIN * 8 1h = MAX_CSA_GAIN * 4 2h = MAX_CSA_GAIN * 2 3h = MAX_CSA_GAIN * 1

7.8.5.7 VOLTAGE_GAIN_FEEDBACK Register (Address = 478h) [Reset = 0000h]

VOLTAGE_GAIN_FEEDBACK is shown in [VOLTAGE_GAIN_FEEDBACK Register](#) and described in [VOLTAGE_GAIN_FEEDBACK Register Field Descriptions](#).

Return to the [ALGORITHM_VARIABLES Registers](#).

Voltage Gain Register

Figure 7-94. VOLTAGE_GAIN_FEEDBACK Register

15	14	13	12	11	10	9	8
VOLTAGE_GAIN_FEEDBACK							
R-0h							
7	6	5	4	3	2	1	0
VOLTAGE_GAIN_FEEDBACK							
R-0h							

Table 7-66. VOLTAGE_GAIN_FEEDBACK Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	VOLTAGE_GAIN_FEEDBACK	R	0h	16-bit value indicating voltage gain 0h = 60V 1h = 30V 2h = 15V

7.8.5.8 VM_VOLTAGE Register (Address = 47Ah) [Reset = 0000000h]

 VM_VOLTAGE is shown in [VM_VOLTAGE Register](#) and described in [VM_VOLTAGE Register Field Descriptions](#).

 Return to the [ALGORITHM_VARIABLES Registers](#).

Supply voltage register

Figure 7-95. VM_VOLTAGE Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VM_VOLTAGE																															
R-0h																															

Table 7-67. VM_VOLTAGE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VM_VOLTAGE	R	0h	32-bit value indicating dc bus voltage DC Bus Voltage = VM_VOLTAGE * 60 / 2 ²⁷

7.8.5.9 PHASE_VOLTAGE_VA Register (Address = 47Eh) [Reset = 0000000h]

 PHASE_VOLTAGE_VA is shown in [PHASE_VOLTAGE_VA Register](#) and described in [PHASE_VOLTAGE_VA Register Field Descriptions](#).

 Return to the [ALGORITHM_VARIABLES Registers](#).

Phase Voltage Register

Figure 7-96. PHASE_VOLTAGE_VA Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHASE_VOLTAGE_VA																															
R-0h																															

Table 7-68. PHASE_VOLTAGE_VA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHASE_VOLTAGE_VA	R	0h	32-bit value indicating Phase Voltage Va during ISD Phase A voltage = PHASE_VOLTAGE_VA * 60 / (sqrt(3) * 2 ²⁷)

7.8.5.10 PHASE_VOLTAGE_VB Register (Address = 480h) [Reset = 0000000h]

 PHASE_VOLTAGE_VB is shown in [PHASE_VOLTAGE_VB Register](#) and described in [PHASE_VOLTAGE_VB Register Field Descriptions](#).

 Return to the [ALGORITHM_VARIABLES Registers](#).

Phase Voltage Register

Figure 7-97. PHASE_VOLTAGE_VB Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHASE_VOLTAGE_VB																															

Figure 7-97. PHASE_VOLTAGE_VB Register (continued)

R-0h

Table 7-69. PHASE_VOLTAGE_VB Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHASE_VOLTAGE_VB	R	0h	32-bit value indicating Phase Voltage Vb during ISD Phase B voltage = PHASE_VOLTAGE_VB * 60 / (sqrt(3) * 2 ²⁷)

7.8.5.11 PHASE_VOLTAGE_VC Register (Address = 482h) [Reset = 0000000h]

PHASE_VOLTAGE_VC is shown in [PHASE_VOLTAGE_VC Register](#) and described in [PHASE_VOLTAGE_VC Register Field Descriptions](#).

Return to the [ALGORITHM_VARIABLES Registers](#).

Phase Voltage Register

Figure 7-98. PHASE_VOLTAGE_VC Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHASE_VOLTAGE_VC																															
R-0h																															

Table 7-70. PHASE_VOLTAGE_VC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHASE_VOLTAGE_VC	R	0h	32-bit value indicating Phase Voltage Vc during ISD Phase C voltage = PHASE_VOLTAGE_VC * 60 / (sqrt(3) * 2 ²⁷)

7.8.5.12 SIN_COMMUTATION_ANGLE Register (Address = 4BAh) [Reset = 0000000h]

SIN_COMMUTATION_ANGLE is shown in [SIN_COMMUTATION_ANGLE Register](#) and described in [SIN_COMMUTATION_ANGLE Register Field Descriptions](#).

Return to the [ALGORITHM_VARIABLES Registers](#).

Sine of Commutation Angle

Figure 7-99. SIN_COMMUTATION_ANGLE Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIN_COMMUTATION_ANGLE																															
R-0h																															

Table 7-71. SIN_COMMUTATION_ANGLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SIN_COMMUTATION_ANGLE	R	0h	32-bit value indicating sine of commutation Angle sinCommutationAngle = (SIN_COMMUTATION_ANGLE / 2 ²⁷)

7.8.5.13 COS_COMMUTATION_ANGLE Register (Address = 4BCh) [Reset = 0000000h]

COS_COMMUTATION_ANGLE is shown in [COS_COMMUTATION_ANGLE Register](#) and described in [COS_COMMUTATION_ANGLE Register Field Descriptions](#).

Return to the [ALGORITHM_VARIABLES Registers](#).

Cosine of Commutation Angle

Figure 7-100. COS_COMMUTATION_ANGLE Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COS_COMMUTATION_ANGLE																															
R-0h																															

Table 7-72. COS_COMMUTATION_ANGLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COS_COMMUTATION_ANGLE	R	0h	32-bit value indicating cosine of commutation Angle $\text{cosCommutationAngle} = (\text{COS_COMMUTATION_ANGLE} / 2^{27})$

7.8.5.14 IALPHA Register (Address = 4D2h) [Reset = 0000000h]

IALPHA is shown in [IALPHA Register](#) and described in [IALPHA Register Field Descriptions](#).

Return to the [ALGORITHM_VARIABLES Registers](#).

IALPHA Current Register

Figure 7-101. IALPHA Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IALPHA																															
R-0h																															

Table 7-73. IALPHA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	IALPHA	R	0h	32-bit value indicating calculated IALPHA $i\text{Alpha} = (\text{IALPHA} / 2^{27}) * \text{Base_Current}/8$

7.8.5.15 IBETA Register (Address = 4D4h) [Reset = 0000000h]

IBETA is shown in [IBETA Register](#) and described in [IBETA Register Field Descriptions](#).

Return to the [ALGORITHM_VARIABLES Registers](#).

IBETA Current Register

Figure 7-102. IBETA Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IBETA																															
R-0h																															

Table 7-74. IBETA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	IBETA	R	0h	32-bit value indicating calculated IBETA $i\text{Beta} = (\text{IBETA} / 2^{27}) * \text{Base_Current}/8$

7.8.5.16 VALPHA Register (Address = 4D6h) [Reset = 0000000h]

VALPHA is shown in [VALPHA Register](#) and described in [VALPHA Register Field Descriptions](#).

Return to the [ALGORITHM_VARIABLES Registers](#).

VALPHA Voltage Register

Figure 7-103. VALPHA Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	---	---	---	---	---	---	---	---	---	---

Figure 7-103. VALPHA Register (continued)

VALPHA
R-0h

Table 7-75. VALPHA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VALPHA	R	0h	32-bit value indicating calculated VALPHA $vAlpha = (VALPHA / 2^{27}) * 60 / \sqrt{3}$

7.8.5.17 VBETA Register (Address = 4D8h) [Reset = 00000000h]

VBETA is shown in [VBETA Register](#) and described in [VBETA Register Field Descriptions](#).

Return to the [ALGORITHM_VARIABLES Registers](#).

VBETA Voltage Register

Figure 7-104. VBETA Register

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
VBETA
R-0h

Table 7-76. VBETA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VBETA	R	0h	32-bit value indicating calculated VBETA $vBeta = (VBETA / 2^{27}) * 60 / \sqrt{3}$

7.8.5.18 ID Register (Address = 4E2h) [Reset = 00000000h]

ID is shown in [ID Register](#) and described in [ID Register Field Descriptions](#).

Return to the [ALGORITHM_VARIABLES Registers](#).

Measured d-axis Current Register

Figure 7-105. ID Register

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID
R-0h

Table 7-77. ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ID	R	0h	32-bit value indicating estimated Id $id = (ID / 2^{27}) * Base_Current/8$

7.8.5.19 IQ Register (Address = 4E4h) [Reset = 00000000h]

IQ is shown in [IQ Register](#) and described in [IQ Register Field Descriptions](#).

Return to the [ALGORITHM_VARIABLES Registers](#).

Measured q-axis Current Register

Figure 7-106. IQ Register

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
IQ

Figure 7-106. IQ Register (continued)

R-0h

Table 7-78. IQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	IQ	R	0h	32-bit value indicating estimated Iq $iq = (IQ / 2^{27}) * Base_Current/8$

7.8.5.20 VD Register (Address = 4E6h) [Reset = 0000000h]

VD is shown in [VD Register](#) and described in [VD Register Field Descriptions](#).

Return to the [ALGORITHM_VARIABLES](#) Registers.

VD Voltage Register

Figure 7-107. VD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VD																															
R-0h																															

Table 7-79. VD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VD	R	0h	32-bit value indicating applied Vd $vd = (VD / 2^{27}) * 60 / \text{sqrt}(3)$

7.8.5.21 VQ Register (Address = 4E8h) [Reset = 0000000h]

VQ is shown in [VQ Register](#) and described in [VQ Register Field Descriptions](#).

Return to the [ALGORITHM_VARIABLES](#) Registers.

VQ Voltage Register

Figure 7-108. VQ Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VQ																															
R-0h																															

Table 7-80. VQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VQ	R	0h	32-bit value indicating applied Vq $vq = (VQ / 2^{27}) * 60 / \text{sqrt}(3)$

7.8.5.22 IQ_REF_ROTOR_ALIGN Register (Address = 522h) [Reset = 0000000h]

IQ_REF_ROTOR_ALIGN is shown in [IQ_REF_ROTOR_ALIGN Register](#) and described in [IQ_REF_ROTOR_ALIGN Register Field Descriptions](#).

Return to the [ALGORITHM_VARIABLES](#) Registers.

Align Current Reference

Figure 7-109. IQ_REF_ROTOR_ALIGN Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IQ_REF_ROTOR_ALIGN																															

Figure 7-109. IQ_REF_ROTOR_ALIGN Register (continued)

R-0h

Table 7-81. IQ_REF_ROTOR_ALIGN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	IQ_REF_ROTOR_ALIGN	R	0h	32-bit value indicating Align Current Reference $iqRefRotorAlign = (IQ_REF_ROTOR_ALIGN / 2^{27}) * Base_Current/8$

7.8.5.23 SPEED_REF_OPEN_LOOP Register (Address = 538h) [Reset = 0000000h]

SPEED_REF_OPEN_LOOP is shown in [SPEED_REF_OPEN_LOOP Register](#) and described in [SPEED_REF_OPEN_LOOP Register Field Descriptions](#).

Return to the [ALGORITHM_VARIABLES Registers](#).

Speed at which motor transitions to close loop

Figure 7-110. SPEED_REF_OPEN_LOOP Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPEED_REF_OPEN_LOOP																															
R-0h																															

Table 7-82. SPEED_REF_OPEN_LOOP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SPEED_REF_OPEN_LOOP	R	0h	32-bit value indicating Open Loop Speed $openLoopSpeedRef = (SPEED_REF_OPEN_LOOP / 2^{27}) * max_Speed - In\ Hz$

7.8.5.24 IQ_REF_OPEN_LOOP Register (Address = 546h) [Reset = 0000000h]

IQ_REF_OPEN_LOOP is shown in [IQ_REF_OPEN_LOOP Register](#) and described in [IQ_REF_OPEN_LOOP Register Field Descriptions](#).

Return to the [ALGORITHM_VARIABLES Registers](#).

Open Loop Current Reference

Figure 7-111. IQ_REF_OPEN_LOOP Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IQ_REF_OPEN_LOOP																															
R-0h																															

Table 7-83. IQ_REF_OPEN_LOOP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	IQ_REF_OPEN_LOOP	R	0h	32-bit value indicating Open Loop Current Reference $iqRefOpenLoop = (IQ_REF_OPEN_LOOP / 2^{27}) * Base_Current/8$

7.8.5.25 SPEED_REF_CLOSED_LOOP Register (Address = 5C8h) [Reset = 0000000h]

SPEED_REF_CLOSED_LOOP is shown in [SPEED_REF_CLOSED_LOOP Register](#) and described in [SPEED_REF_CLOSED_LOOP Register Field Descriptions](#).

Return to the [ALGORITHM_VARIABLES Registers](#).

Speed Reference Register

Figure 7-112. SPEED_REF_CLOSED_LOOP Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPEED_REF_CLOSED_LOOP																															
R-0h																															

Table 7-84. SPEED_REF_CLOSED_LOOP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SPEED_REF_CLOSED_LOOP	R	0h	32-bit value indicating reference for speed loop Speed Reference in closed loop (Hz) = (SPEED_REF_CLOSED_LOOP / 2 ²⁷) * max_Speed - ln Hz

7.8.5.26 ID_REF_CLOSED_LOOP Register (Address = 5EEh) [Reset = 0000000h]

ID_REF_CLOSED_LOOP is shown in [ID_REF_CLOSED_LOOP Register](#) and described in [ID_REF_CLOSED_LOOP Register Field Descriptions](#).

Return to the [ALGORITHM_VARIABLES Registers](#).

Reference for Current Loop Register

Figure 7-113. ID_REF_CLOSED_LOOP Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID_REF_CLOSED_LOOP																															
R-0h																															

Table 7-85. ID_REF_CLOSED_LOOP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ID_REF_CLOSED_LOOP	R	0h	32-bit value indicating Id_ref for flux loop idRefClosedLoop = (ID_REF_CLOSED_LOOP / 2 ²⁷) * Base_Current/8

7.8.5.27 IQ_REF_CLOSED_LOOP Register (Address = 5F0h) [Reset = 0000000h]

IQ_REF_CLOSED_LOOP is shown in [IQ_REF_CLOSED_LOOP Register](#) and described in [IQ_REF_CLOSED_LOOP Register Field Descriptions](#).

Return to the [ALGORITHM_VARIABLES Registers](#).

Reference for Current Loop Register

Figure 7-114. IQ_REF_CLOSED_LOOP Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IQ_REF_CLOSED_LOOP																															
R-0h																															

Table 7-86. IQ_REF_CLOSED_LOOP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	IQ_REF_CLOSED_LOOP	R	0h	32-bit value indicating Iq_ref for torque loop iqRefClosedLoop = (IQ_REF_CLOSED_LOOP / 2 ²⁷) * Base_Current/8

7.8.5.28 ISD_STATE Register (Address = 668h) [Reset = 0000h]

ISD_STATE is shown in [ISD_STATE Register](#) and described in [ISD_STATE Register Field Descriptions](#).

Return to the [ALGORITHM_VARIABLES Registers](#).

ISD state Register

Figure 7-115. ISD_STATE Register

15	14	13	12	11	10	9	8
ISD_STATE							
R-0h							
7	6	5	4	3	2	1	0
ISD_STATE							
R-0h							

Table 7-87. ISD_STATE Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	ISD_STATE	R	0h	16-bit value indicating current ISD state 0h = ISD_INIT 1h = ISD_MOTOR_STOP_CHECK 2h = ISD_MOTOR_DIRECTION_CHECK 3h = ISD_COMPLETE 4h = ISD_FAULT

7.8.5.29 ISD_SPEED Register (Address = 672h) [Reset = 0000000h]

ISD_SPEED is shown in [ISD_SPEED Register](#) and described in [ISD_SPEED Register Field Descriptions](#).

Return to the [ALGORITHM_VARIABLES Registers](#).

ISD Speed Register

Figure 7-116. ISD_SPEED Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ISD_SPEED																															
R-0h																															

Table 7-88. ISD_SPEED Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ISD_SPEED	R	0h	32-bit value indicating calculated speed during ISD state $isdSpeed = (ISD_SPEED / 2^{27}) * max_Speed - In\ Hz$

7.8.5.30 IPD_STATE Register (Address = 69Ah) [Reset = 0000h]

IPD_STATE is shown in [IPD_STATE Register](#) and described in [IPD_STATE Register Field Descriptions](#).

Return to the [ALGORITHM_VARIABLES Registers](#).

IPD state Register

Figure 7-117. IPD_STATE Register

15	14	13	12	11	10	9	8
IPD_STATE							
R-0h							
7	6	5	4	3	2	1	0
IPD_STATE							
R-0h							

Figure 7-117. IPD_STATE Register (continued)

Table 7-89. IPD_STATE Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	IPD_STATE	R	0h	16-bit value indicating current IPD state 0h = IPD_INIT 1h = IPD_VECTOR_CONFIG 2h = IPD_RUN 3h = IPD_SLOW_RISE_CLOCK 4h = IPD_SLOW_FALL_CLOCK 5h = IPD_WAIT_CURRENT_DECAY 6h = IPD_GET_TIMES 7h = IPD_SET_NEXT_VECTOR 8h = IPD_CALC_SECTOR_RISE 9h = IPD_CALC_ROTOR_POSITION Ah = IPD_CALC_ANGLE Bh = IPD_COMPLETE Ch = IPD_FAULT

7.8.5.31 IPD_ANGLE Register (Address = 6DEh) [Reset = 0000000h]

IPD_ANGLE is shown in [IPD_ANGLE Register](#) and described in [IPD_ANGLE Register Field Descriptions](#).

Return to the [ALGORITHM_VARIABLES Registers](#).

Calculated IPD Angle Register

Figure 7-118. IPD_ANGLE Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IPD_ANGLE																															
R-0h																															

Table 7-90. IPD_ANGLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	IPD_ANGLE	R	0h	32-bit value indicating measured IPD angle $ipdAngle = (IPD_ANGLE / 2^{27}) * 360$ (Degree)

7.8.5.32 EQ Register (Address = 724h) [Reset = 0000000h]

EQ is shown in [EQ Register](#) and described in [EQ Register Field Descriptions](#).

Return to the [ALGORITHM_VARIABLES Registers](#).

Estimated BEMF EQ Register

Figure 7-119. EQ Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EQ																															
R-0h																															

Table 7-91. EQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	EQ	R	0h	32-bit value indicating estimated EQ $Eq = (EQ / 2^{27}) * 60 / \sqrt{3}$

7.8.5.33 ED Register (Address = 726h) [Reset = 0000000h]

ED is shown in [ED Register](#) and described in [ED Register Field Descriptions](#).

Return to the [ALGORITHM_VARIABLES Registers](#).

Estimated BEMF ED Register

Figure 7-120. ED Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ED																															
R-0h																															

Table 7-92. ED Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ED	R	0h	32-bit value indicating estimated ED $Ed = (ED / 2^{27}) * 60 / \text{sqrt}(3)$

7.8.5.34 SPEED_FDBK Register (Address = 734h) [Reset = 0000000h]

SPEED_FDBK is shown in [SPEED_FDBK Register](#) and described in [SPEED_FDBK Register Field Descriptions](#).

Return to the [ALGORITHM_VARIABLES Registers](#).

Speed Feedback Register

Figure 7-121. SPEED_FDBK Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPEED_FDBK																															
R-0h																															

Table 7-93. SPEED_FDBK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SPEED_FDBK	R	0h	32-bit value indicating estimated rotor speed $\text{estimatedSpeed} = (\text{SPEED_FDBK} / 2^{27}) * 360$ (Degree)

7.8.5.35 THETA_EST Register (Address = 736h) [Reset = 0000000h]

THETA_EST is shown in [THETA_EST Register](#) and described in [THETA_EST Register Field Descriptions](#).

Return to the [ALGORITHM_VARIABLES Registers](#).

Estimated motor position Register

Figure 7-122. THETA_EST Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
THETA_EST																															
R-0h																															

Table 7-94. THETA_EST Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	THETA_EST	R	0h	32-bit value indicating estimated rotor angle $\text{estimatedAngle} = (\text{THETA_EST} / 2^{27}) * 360$ (Degree)

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The MCF8316A device is used in sensorless 3-phase BLDC motor control. The driver provides a high performance, high-reliability and flexible solution for appliances, fans, pumps, residential and living fans, seat cooling fans, automotive fans and blowers. The following section shows a common application of the MCF8316A device.

8.2 Typical Applications

Figure 8-1 shows the typical schematic of MCF8316A

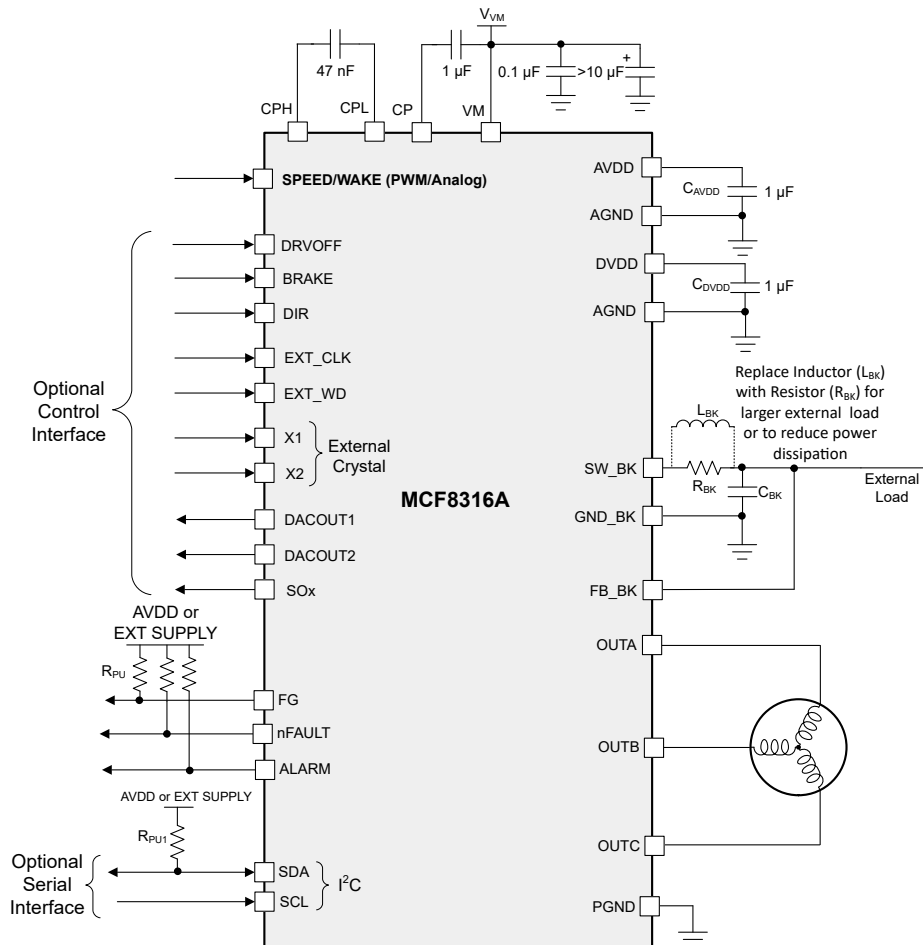


Figure 8-1. Primary Application Schematics

Table 8-1 lists the recommended values of the external components.

Table 8-1. MCF8316A External Components

COMPONENTS	PIN 1	PIN 2	RECOMMENDED
C _{VM1}	VM	PGND	X5R or X7R, 0.1-μF, TI recommends a capacitor voltage rating at least twice the normal operating voltage of the device
C _{VM2}	VM	PGND	≥ 10-μF, TI recommends a capacitor voltage rating at least twice the normal operating voltage of the device
C _{CP}	CP	VM	X5R or X7R, 16-V, 1-μF capacitor
C _{FLY}	CPH	CPL	X5R or X7R, 47-nF, TI recommends a capacitor voltage rating at least twice the normal operating voltage of the pin
C _{AVDD}	AVDD	AGND	X5R or X7R, 1-μF, ≥ 6.3-V. In order for AVDD to accurately regulate output voltage, capacitor should have effective capacitance between 0.7-μF to 1.3-μF at 3.3-V across operating temperature.
C _{DVDD}	AVDD	AGND	X5R or X7R, 1-μF, ≥ 4-V. In order for DVDD to accurately regulate output voltage, capacitor should have effective capacitance between 0.6-μF to 1.3-μF at 1.5-V across operating temperature.
C _{BK}	SW_BK	GND_BK	X5R or X7R, buck-output rated capacitor
L _{BK}	SW_BK	FB_BK	Output inductor
R _{ALARM}	1.8 to 5-V Supply	ALARM	5.1-kΩ, Pullup resistor
R _{FG}	1.8 to 5-V Supply	FG	5.1-kΩ, Pullup resistor
R _{nFAULT}	1.8 to 5-V Supply	nFAULT	5.1-kΩ, Pullup resistor
R _{SDA}	1.8 to 3.3-V Supply	SDA	5.1-kΩ, Pullup resistor

Table 8-2. Recommended Application Range

Parameter	Min	Max	Unit
Motor Voltage	4.5	35	V
Back-EMF constant (see Motor Back-EMF constant)	0.6	2000	mV/Hz
Motor Resistance (see Motor Resistance)	0.010	20	Ω
Motor Inductance (see Motor Inductance)	0.020	20	mH
Motor Electrical Speed	-	1300	Hz
Winding Current	-	8	A

Default EEPROM Configuration for MCF8316A is listed in [Table 8-3](#). Default values are chosen for reliable motor startup and closed loop operation. Refer to [MCF8316A tuning guide](#) which provides step by step procedure to tune a 3-phase BLDC motor in closed loop, conform to use-case and explore features in the device.

Table 8-3. Recommended Default Values

Address Name	Address	Recommended Value
ISD_CONFIG	0x00000080	0x44638C20
REV_DRIVE_CONFIG	0x00000082	0x283AF064
MOTOR_STARTUP1	0x00000084	0x0B6807D0
MOTOR_STARTUP2	0x00000086	0x23066004
CLOSED_LOOP1	0x00000088	0x0D3201B0
CLOSED_LOOP2	0x0000008A	0x1AAD0000
CLOSED_LOOP3	0x0000008C	0x00000000
CLOSED_LOOP4	0x0000008E	0x0000012C
SPEED_PROFILES1	0x00000094	0x00000000

Table 8-3. Recommended Default Values (continued)

Address Name	Address	Recommended Value
SPEED_PROFILES2	0x00000096	0x00000000
SPEED_PROFILES3	0x00000098	0x00000000
SPEED_PROFILES4	0x0000009A	0x00000000
SPEED_PROFILES5	0x0000009C	0x00000000
SPEED_PROFILES6	0x0000009E	0x00000000
FAULT_CONFIG1	0x00000090	0x5FE8820E
FAULT_CONFIG2	0x00000092	0x74C08000
PIN_CONFIG	0x000000A4	0x2DD0E480
DEVICE_CONFIG1	0x000000A6	0x08000000
DEVICE_CONFIG2	0x000000A8	0x00003000
PERI_CONFIG1	0x000000AA	0x40000000
GD_CONFIG1	0x000000AC	0x1C400100
GD_CONFIG2	0x000000AE	0x00200000
ALGO_CTRL1	0x000000EA	0x00000000
INT_ALGO_1	0x000000A0	0x04B3407D
INT_ALGO_2	0x000000A2	0x000001A7

Once the device EEPROM is programmed with the desired configuration, device can be operated stand-alone and I²C serial interface is not required anymore. Speed can be commanded using SPEED pin.

Below are the two essential parameters that are required to spin the motor in closed loop.

1. Maximum motor speed.
2. Current limit for torque PI loop.

8.2.1 Application Curves

8.2.1.1 Motor startup

Figure 8-2 shows the FG waveform and the phase current waveform at different motor operations.

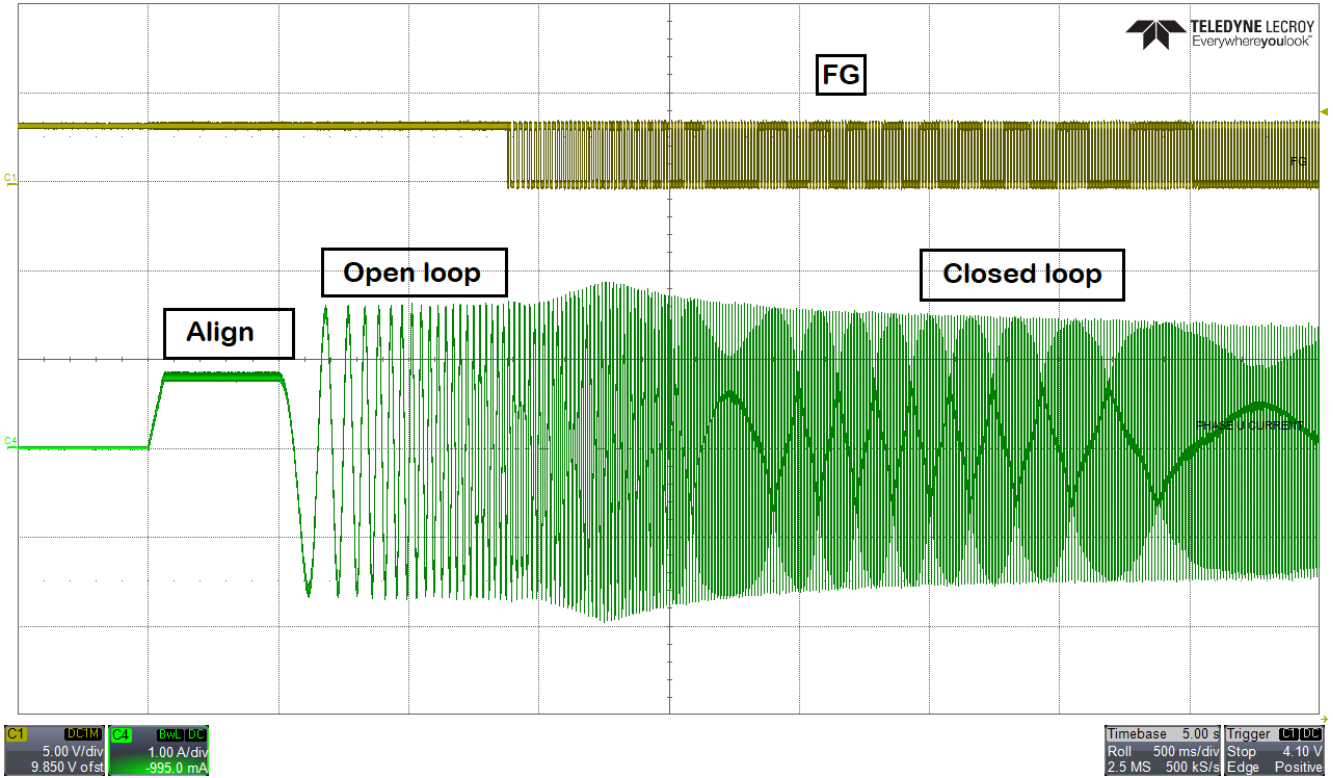


Figure 8-2. Motor Startup - FG and Phase current

8.2.1.2 MPET

Figure 8-3 shows the phase current waveform during motor parameter measurement. Figure 8-4 shows the IPD current waveform during R, L and K_e measurement. Bottom half of Figure 8-4 shows the IPD current waveform during R and L measurement. R is measured during the rising of phase current and L is measured during the falling of phase current. After R and L measurement, motor spins in open loop. Once the speed reaches MPET open loop speed reference [MPET_OPEN_LOOP_SPEED_REF], motor is coasted. BEMF voltage of all three phases are measured and K_e is calculated.

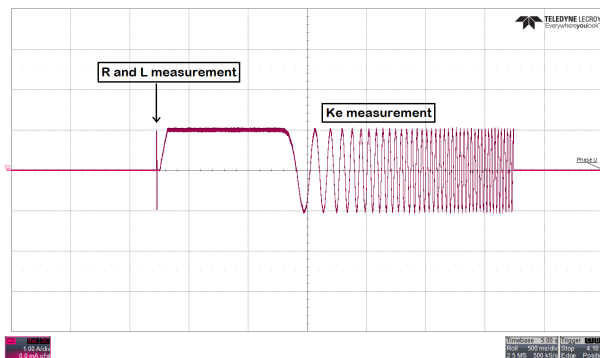


Figure 8-3. MPET - Phase current

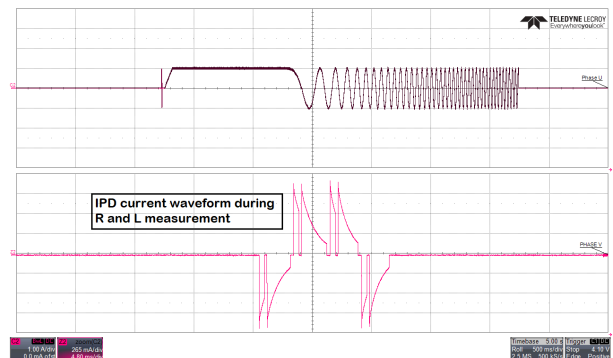


Figure 8-4. IPD current waveform during R and L measurement

8.2.1.3 Dead time compensation

Figure 8-5 shows the phase current waveform when dead time compensation is disabled. Fundamental frequency of phase current is 40 Hz. Fast Fourier transform (FFT) of phase current plot shows harmonics at

160 Hz and 220 Hz. **Figure 8-6** shows the phase current waveform when dead time compensation is enabled. Phase current looks more sinusoidal and the FFT of phase current plot does not have any harmonics.

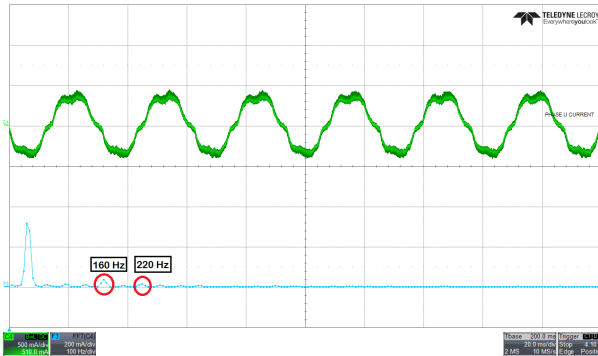


Figure 8-5. Phase current and FFT - Dead time compensation disabled

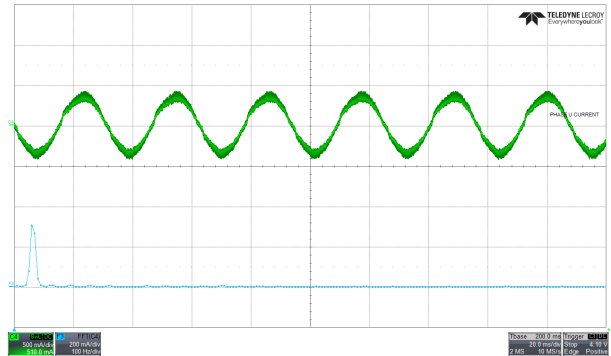


Figure 8-6. Phase current and FFT - Dead time compensation enabled

8.2.1.4 Auto Handoff

Figure 8-7 shows the auto handoff feature in MCF8316A where the motor transitions seamlessly from open loop to closed loop.

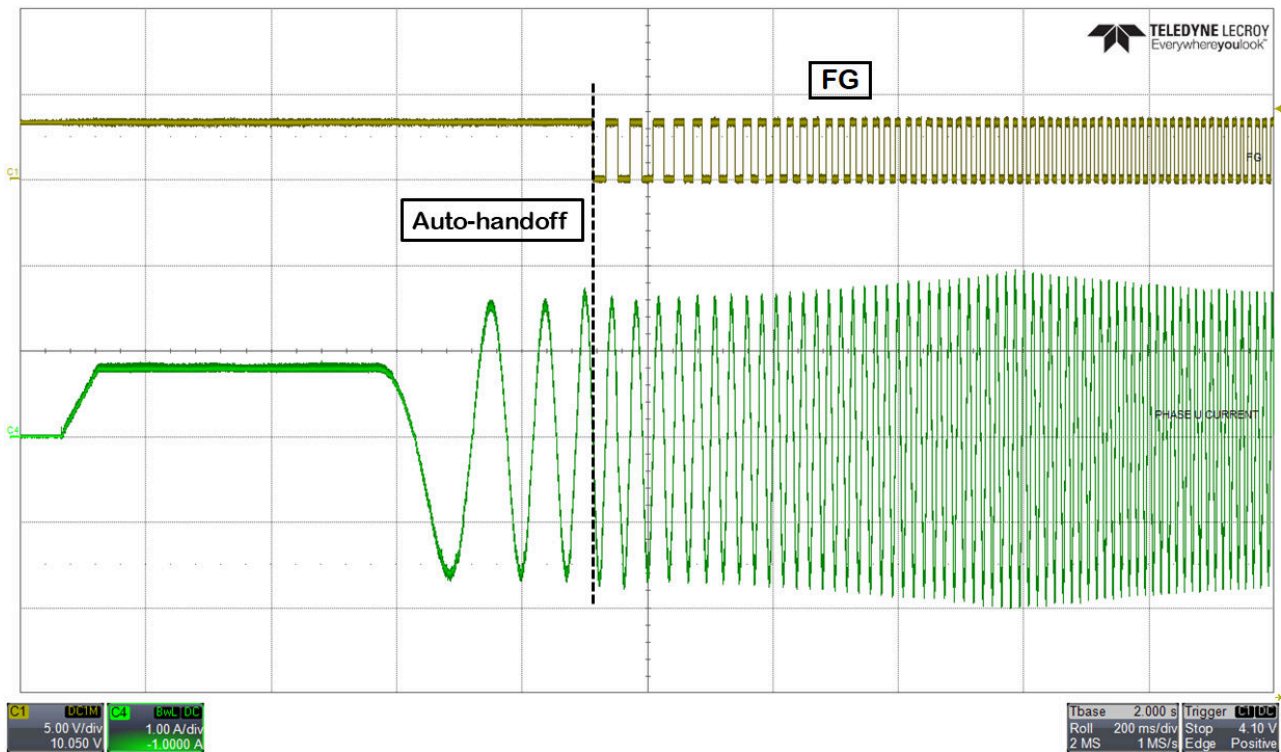


Figure 8-7. Auto-handoff

8.2.1.5 Motor stop – Recirculation mode

Figure 8-8 shows the supply voltage and phase current waveform after stopping the motor. Recirculation mode in MCF8316A prevents the supply voltage from overshoots.

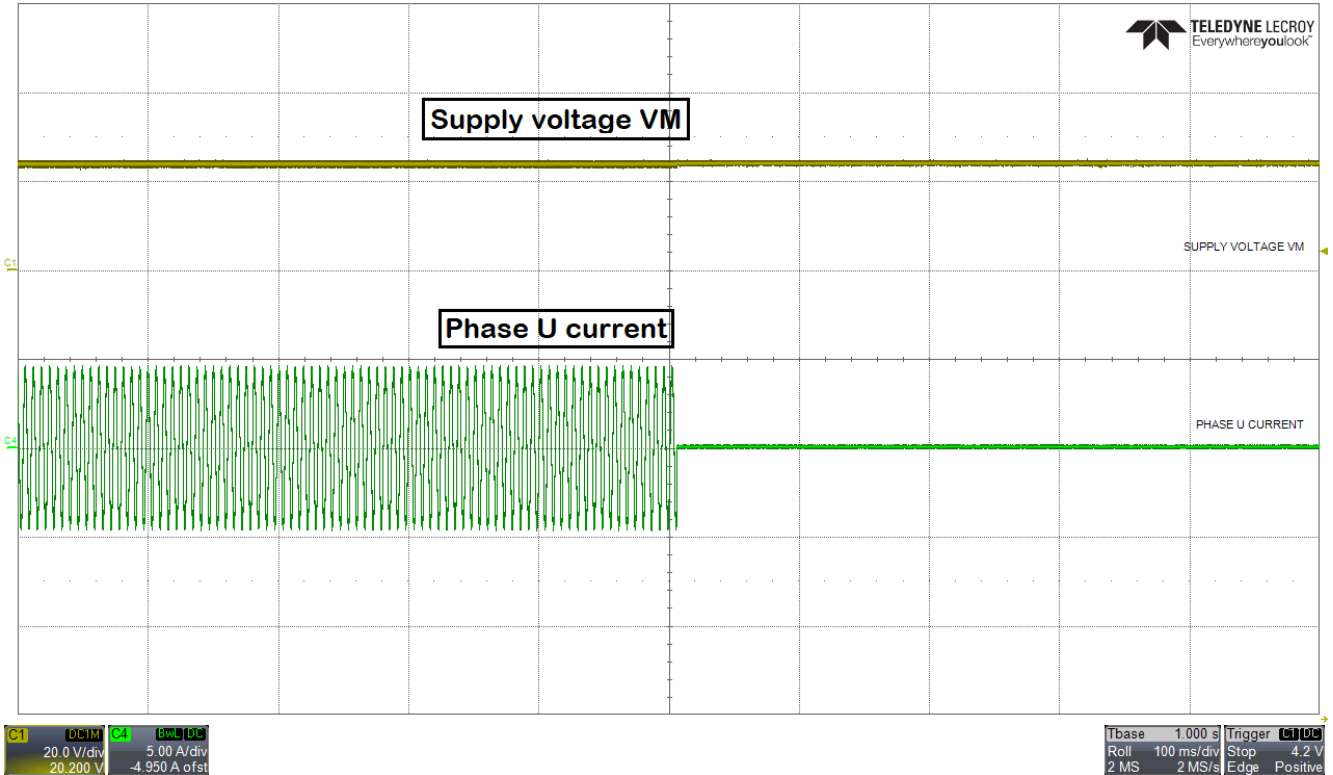


Figure 8-8. Motor stop - recirculation mode

8.2.1.6 Anti voltage surge (AVS)

When motor speed decelerates at very high deceleration rate, mechanical energy from the motor returns to the power supply which could result in pumping up the supply voltage V_m . Figure 8-9 shows overshoot in power supply voltage when AVS is disabled. Motor decelerates from 100% duty cycle to 10% duty cycle at a deceleration rate of 70,000 Hz/sec. Figure 8-10 shows no overshoot in power supply voltage when AVS is enabled.

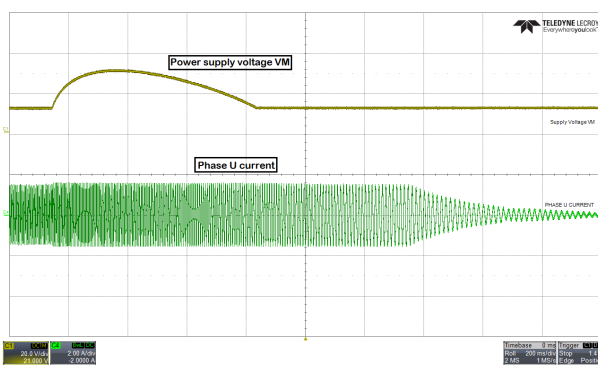


Figure 8-9. Power Supply voltage and phase current waveform when AVS is disabled

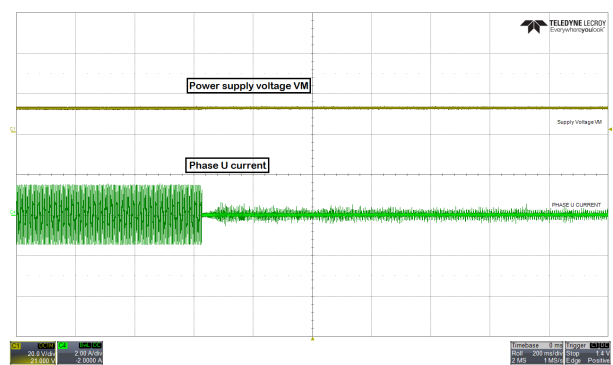


Figure 8-10. Power Supply voltage and phase current waveform when AVS is enabled

8.2.1.7 Real time variable tracking using DACOUT

MCF8316A has two 12-bit DAC which outputs analog voltage equivalent of digital variables on DACOUT1 and DACOUT2 pins with resolution of 12 bits and max voltage of 3V. Signals available on DACOUT pins can be used for tuning speed controller or other driver configuration or bus current monitoring. Check algorithm variable registers in datasheet for list of all algorithm variables.

The addresses for variables for DACOUT1 and DACOUT2 are configured using register bits DACOUT1_VAR_ADDR and DACOUT2_VAR_ADDR. This is useful in applications which require tracking algorithm variables in real time without having any delay from the communication bus. Pin 37 and 38 should be configured as DACOUT1 and DACOUT2.

For example, if the user wants to read phase A current from pin 37, configure pin 37 as DACOUT1 and program the phase A current register address (0x00000440) in Hex in [DACOUT1_VAR_ADDR]. If the user wants to read estimated rotor angle from pin 38, configure pin 38 as DACOUT2 and program the estimated rotor angle register address (0x00000736) in Hex in [DACOUT2_VAR_ADDR].

Figure 8-11 shows the outputs of DACOUT1 and DACOUT2. DACOUT1 is configured to read phase A current and DACOUT2 is configured to read estimated rotor angle.

ADVANCE INFORMATION

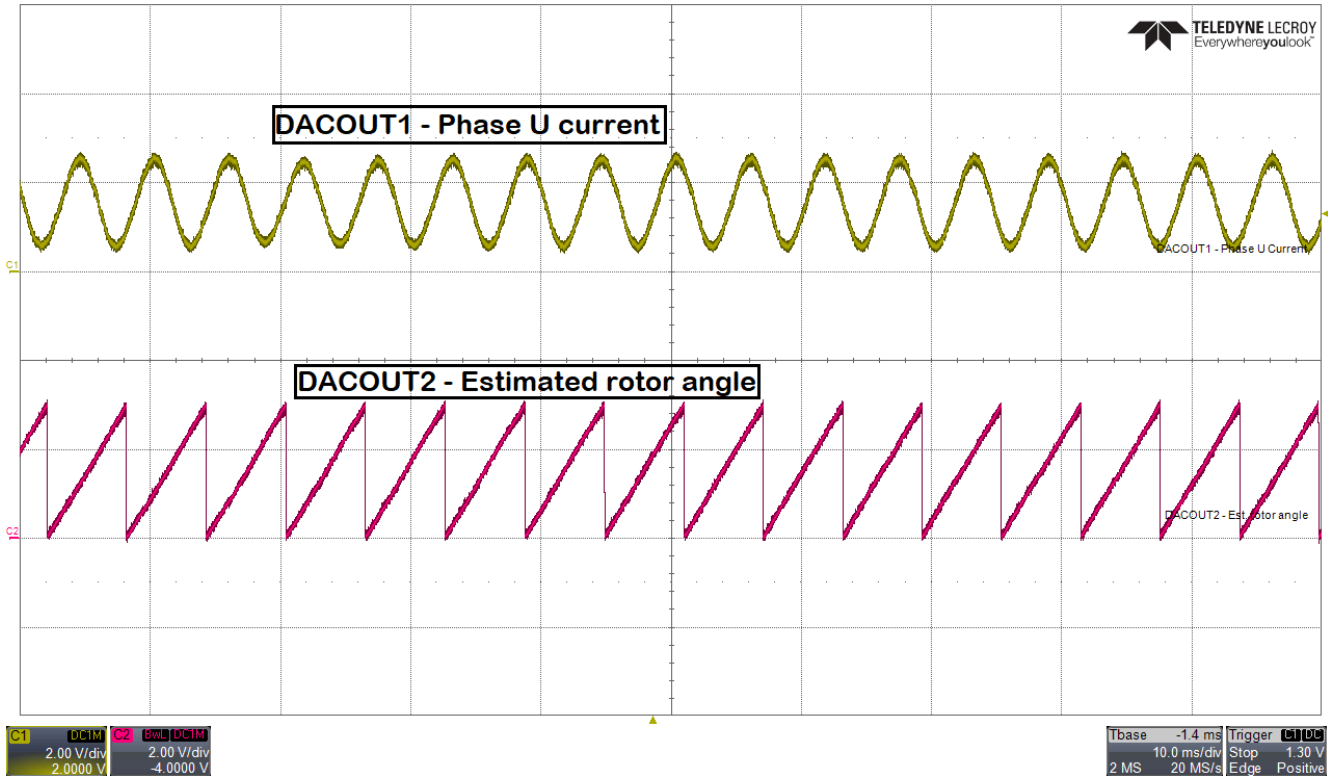


Figure 8-11. DACOUT1 and DACOUT2

9 Power Supply Recommendations

9.1 Bulk Capacitance

Having an appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The capacitance and current capability of the power supply
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed dc, brushless DC, stepper)
- The motor braking method

The inductance between the power supply and the motor drive system limits the rate current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

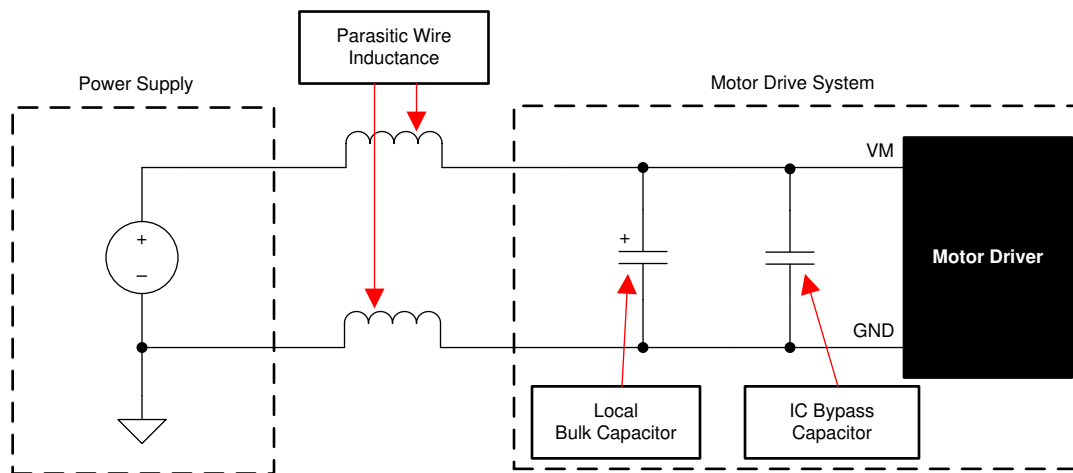


Figure 9-1. Example Setup of Motor Drive System With External Power Supply

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

10 Layout

10.1 Layout Guidelines

The bulk capacitor should be placed to minimize the distance of the high-current path through the motor driver device. The connecting metal trace widths should be as wide as possible, and numerous vias should be used when connecting PCB layers. These practices minimize inductance and allow the bulk capacitor to deliver high current.

Small-value capacitors should be ceramic, and placed closely to device pins.

The high-current device outputs should use wide metal traces.

To reduce noise coupling and EMI interference from large transient currents into small-current signal paths, grounding should be partitioned between PGND and AGND. TI recommends connecting all non-power stage circuitry (including the thermal pad) to AGND to reduce parasitic effects and improve power dissipation from the device. Optionally, GND_BK can be split. Ensure grounds are connected through net-ties or wide resistors to reduce voltage offsets and maintain gate driver performance.

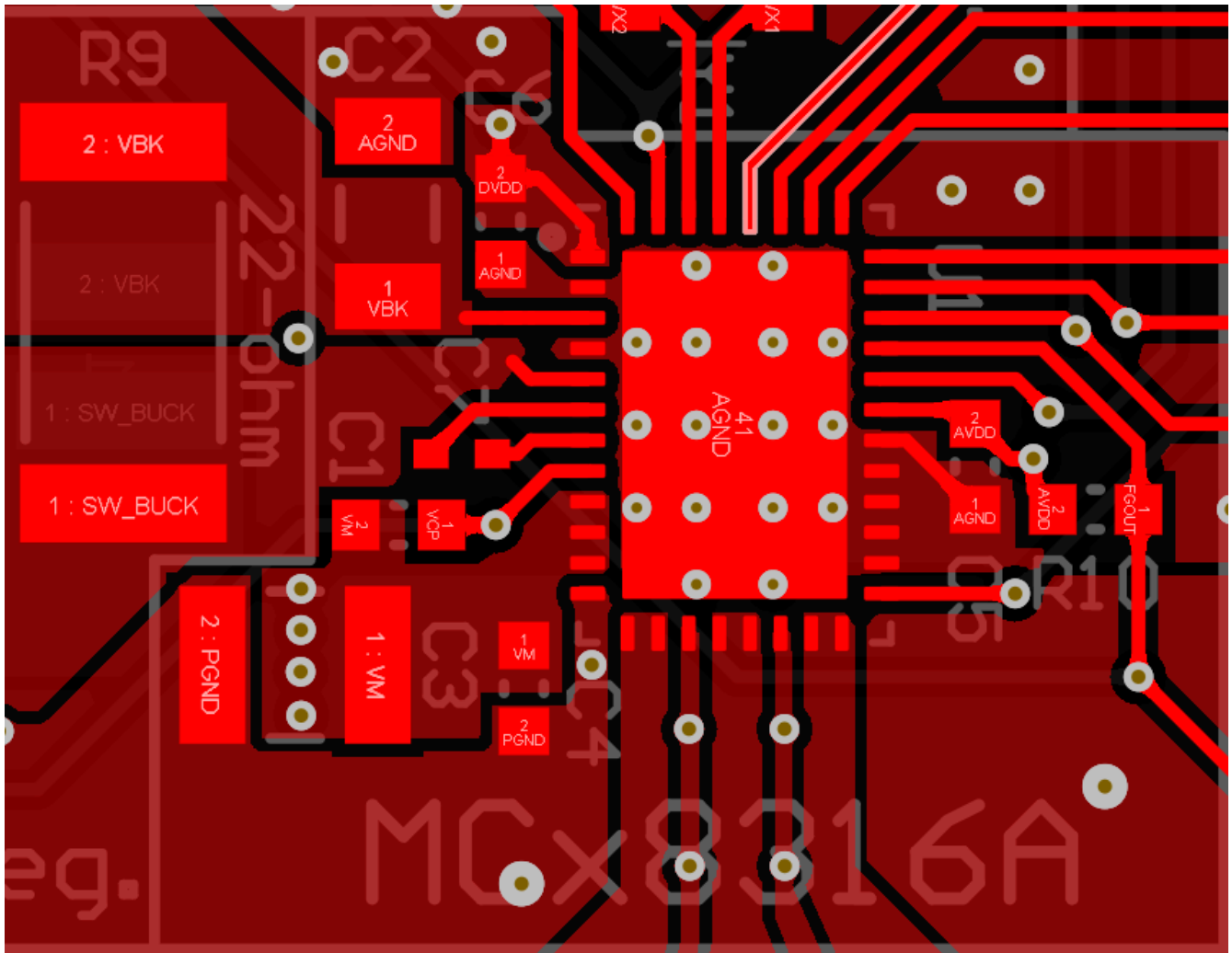
The device thermal pad should be soldered to the PCB top-layer ground plane. Multiple vias should be used to connect to a large bottom-layer ground plane. The use of large metal planes and multiple vias helps dissipate the $I^2 \times r_{DS(on)}$ heat that is generated in the device.

To improve thermal performance, maximize the ground area that is connected to the thermal pad ground across all possible layers of the PCB. Using thick copper pours can lower the junction-to-air thermal resistance and improve thermal dissipation from the die surface.

Separate the SW_BUCK and FB_BUCK traces with ground separation to reduce buck switching from coupling as noise into the buck outer feedback loop. Widen the FB_BUCK trace as much as possible to allow for faster load switching.

Figure 10-1 shows a layout example for the MCF8316A. Also for layout example refer to [MCF8316A EVM](#).

10.2 Layout Example



ADVANCE INFORMATION

Figure 10-1. Recommended Layout Example

10.3 Thermal Considerations

The has thermal shutdown (TSD) as previously described. A die temperature in excess of 150°C (minimally) disables the device until the temperature drops to a safe level.

Any tendency of the device to enter thermal shutdown is an indication of excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

10.3.1 Power Dissipation

The power dissipated in the output FET resistance, or $r_{DS(on)}$ dominates power dissipation in the MCF8316. A rough estimate of average power dissipation of each half-H-bridge when running a static load is:

At start-up and fault conditions, this current is much higher than normal running current; remember to take these peak currents and their duration into consideration.

The total device dissipation is the power dissipated in each of the three half-H-bridges added together.

The maximum amount of power that the device can dissipate depends on ambient temperature and heatsinking.

Note that $r_{DS(on)}$ increases with temperature, so as the device heats, the power dissipation increases. Take this into consideration when sizing the heatsink.

11 Device and Documentation Support

11.1 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

11.2 Trademarks

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11.3 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.4 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

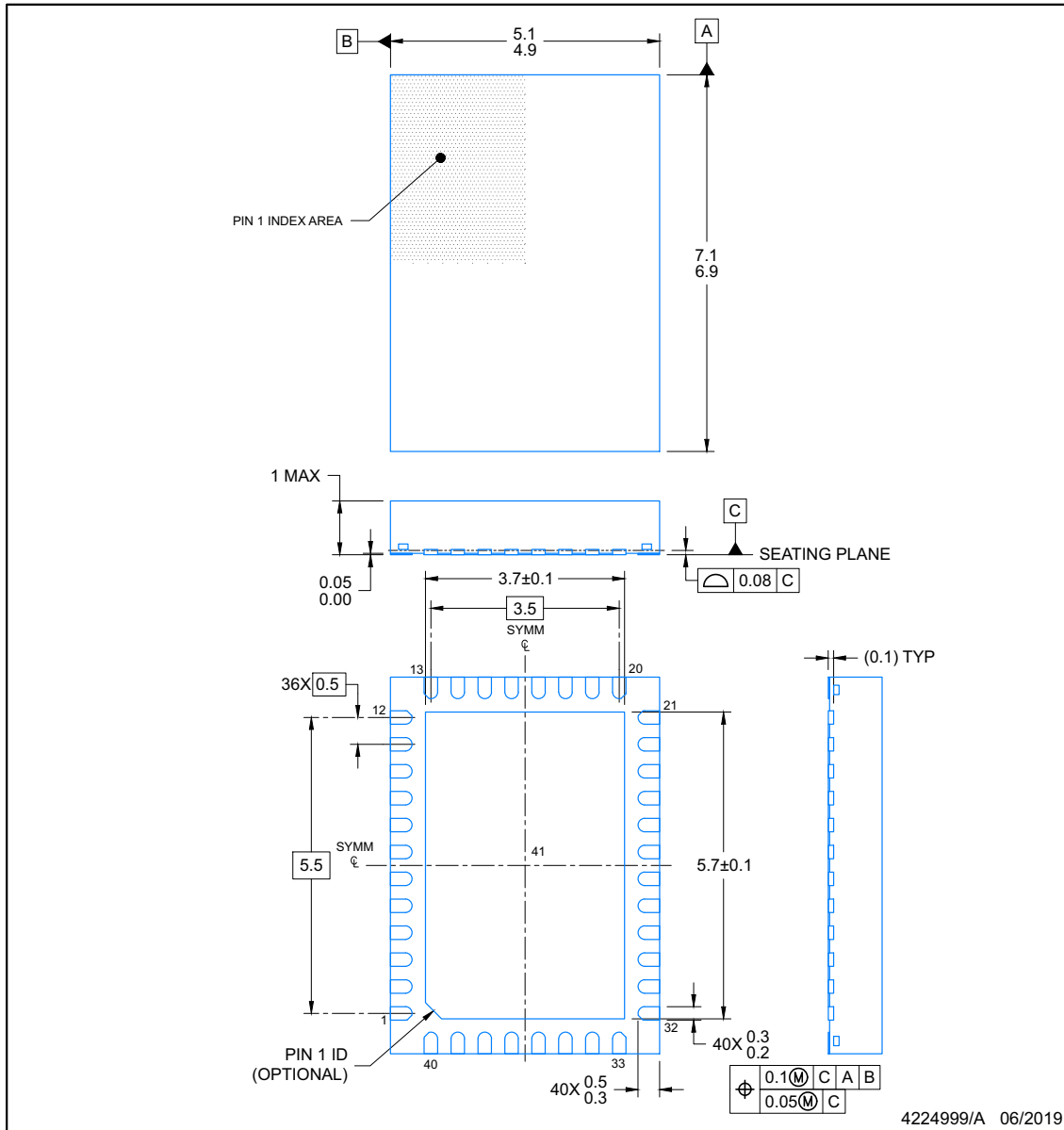
The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

RGF0040E

PACKAGE OUTLINE
VQFN - 1 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD

ADVANCE INFORMATION



4224999/A 06/2019

NOTES:

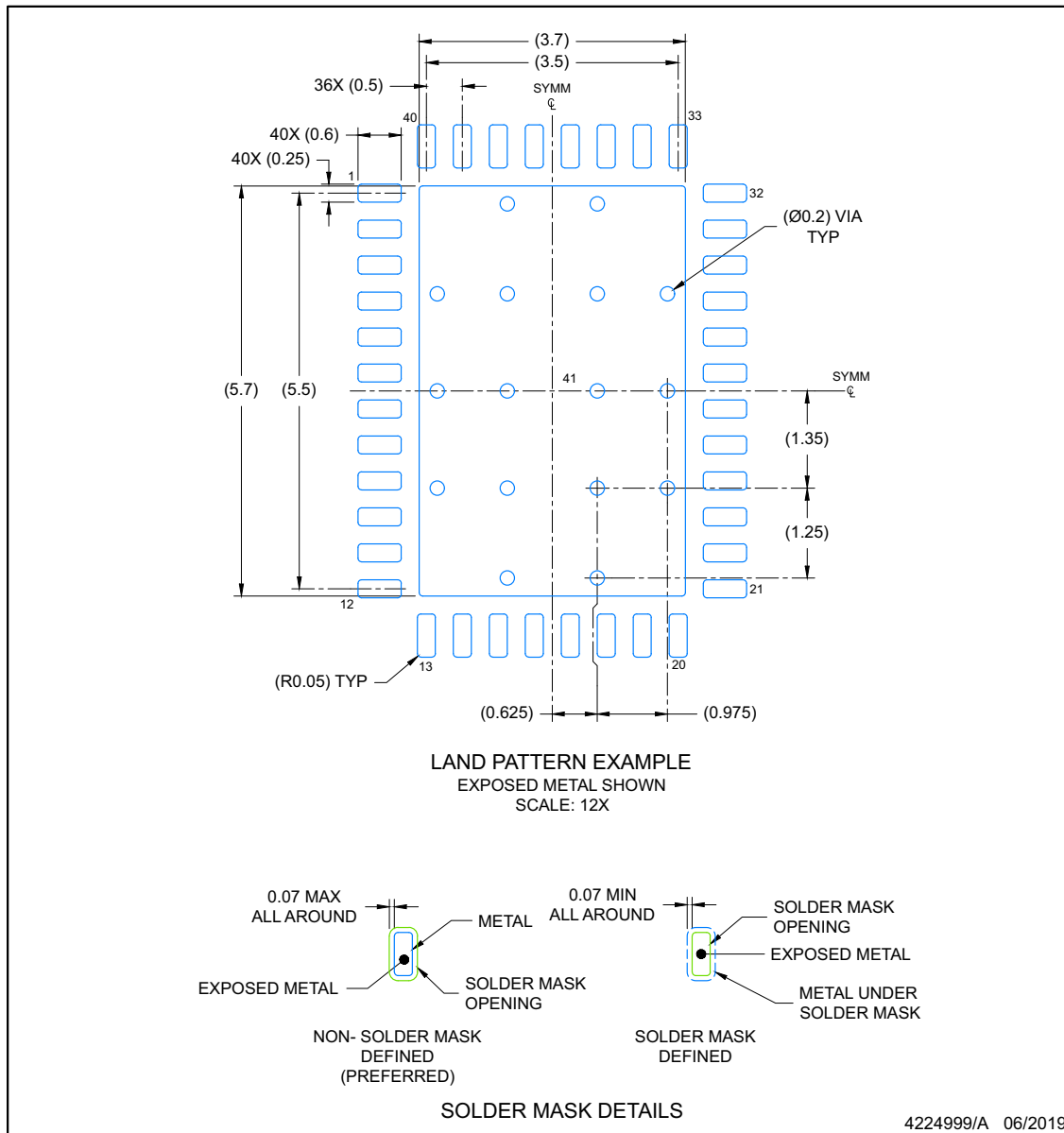
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RGF0040E

VQFN - 1 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

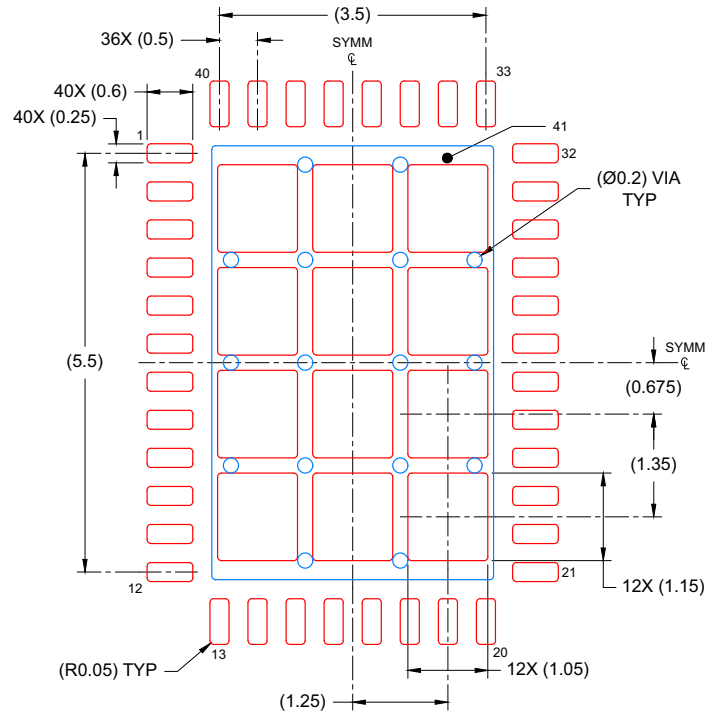
ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

RGF0040E

VQFN - 1 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
 69% PRINTED COVERAGE BY AREA
 SCALE: 12X

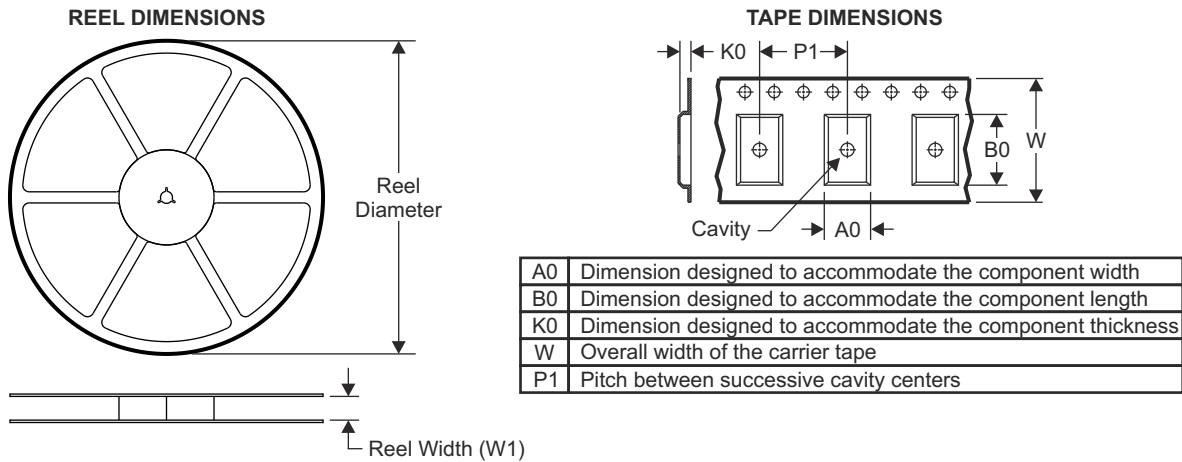
4224999/A 06/2019

NOTES: (continued)

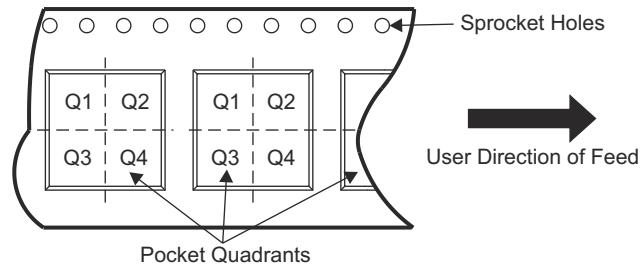
- 6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

ADVANCE INFORMATION

12.1 Tape and Reel Information

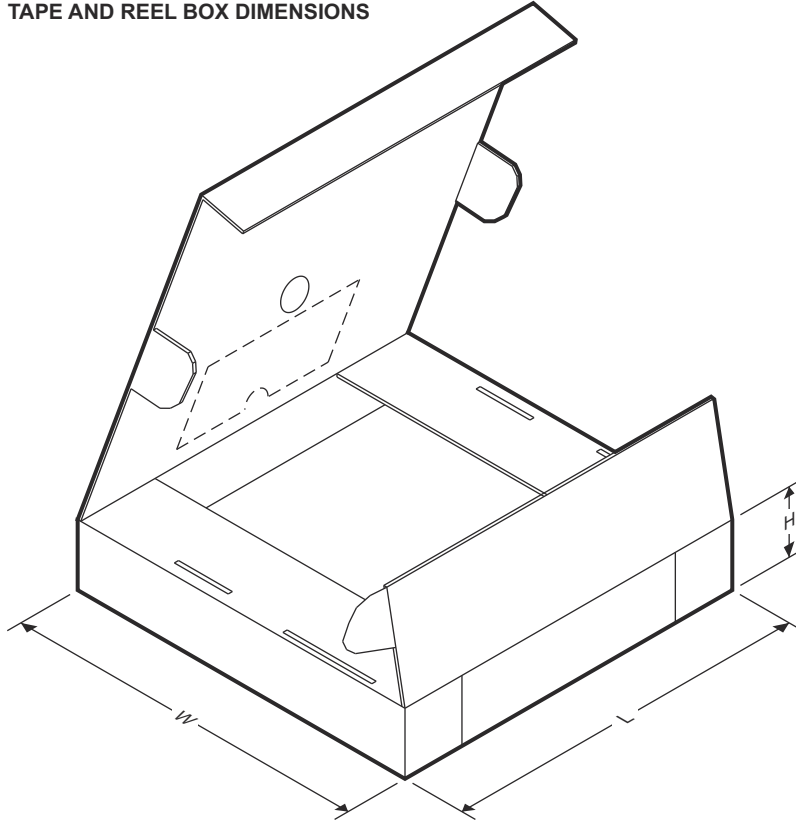


QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MCF8316A1VRGFR	VQFN	RGF	40	3000	330.0	16.4	5.25	7.25	1.45	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MCF8316A1VRGFR	VQFN	RGF	40	3000	367.0	367.0	38.0

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PMCF8316A1VRGFR	ACTIVE	VQFN	RGF	40	3000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

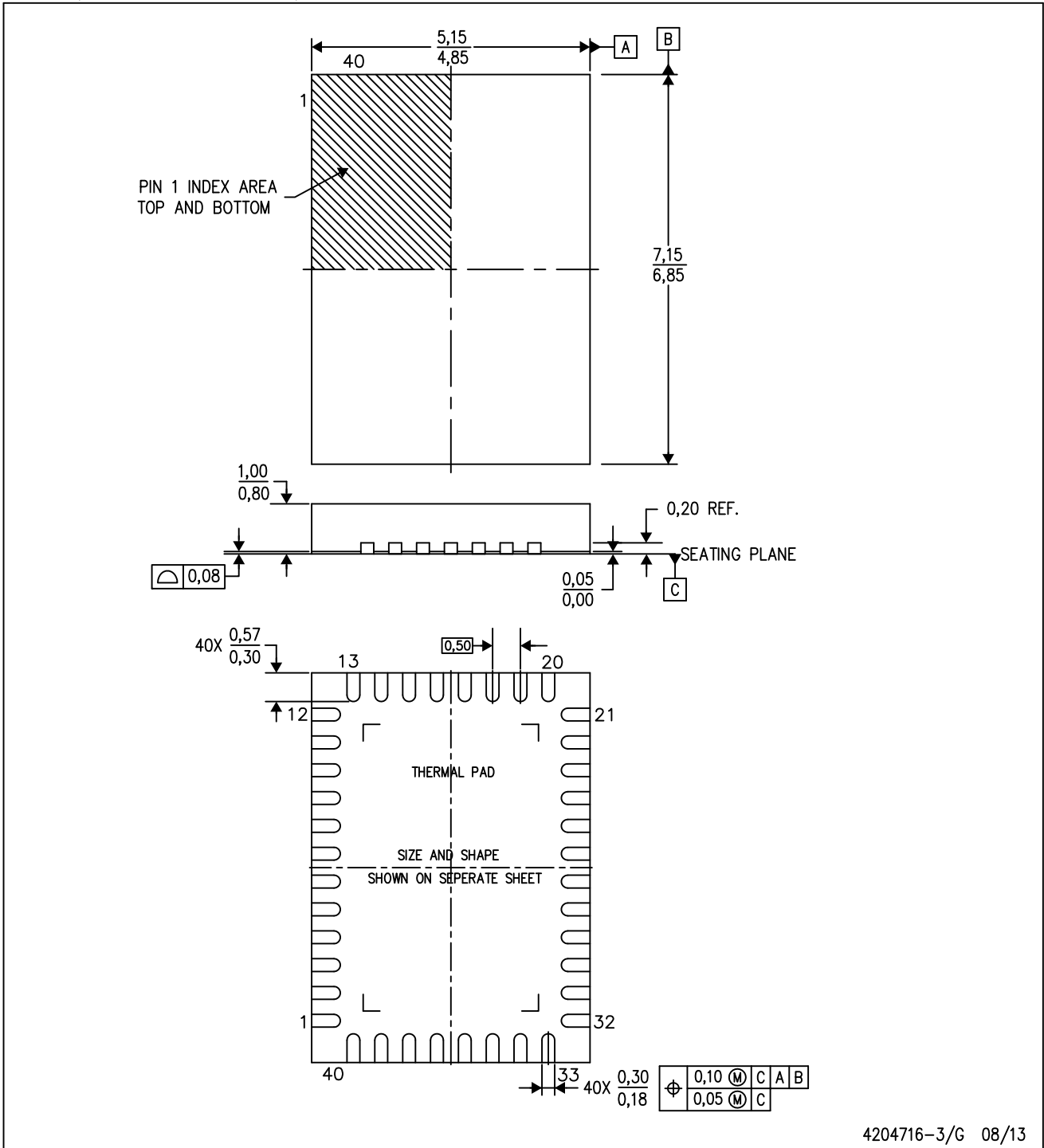
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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RGF (R-PVQFN-N40)

PLASTIC QUAD FLATPACK NO-LEAD



4204716-3/G 08/13

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
 - B. This drawing is subject to change without notice.
 - C. Quad Flatpack, No-leads (QFN) package configuration.
 - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - E. See the additional figure in the Product Data Sheet for details regarding lands and the exposed thermal pad features and dimensions.
 - F. Falls within JEDEC MO-220.

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