Am186™ER and Am188™ER

High-Performance, 80C186- and 80C188-Compatible, 16-Bit Embedded Microcontrollers with RAM

DISTINCTIVE CHARACTERISTICS

- **E86™ family 80C186- and 80C188-compatible microcontrollers with enhanced bus interface**
  - — Lower system cost with high performance
  - — 3.3-V ± 0.3-V operation with 5-V tolerant I/O
- **Memory integration**
  - — 32 Kbyte of internal SRAM
  - — Internal SRAM provides same performance as zero-wait-state external memory
- **High performance**
  - — 25-, 33-, 40- and 50-MHz operating frequencies
  - — Supports zero-wait-state operation at 50 MHz with 55-ns external memory
  - — 1-Mbyte memory address space
  - — 64-Kbyte I/O space
- **Enhanced features provide faster access to memory and various clock input modes**
  - — Nonmultiplexed address bus provides glueless interface to external RAM and ROM
  - — Phase-locked loop (PLL) enables processor to operate at up to four times clock input frequency
- **Enhanced integrated peripherals**
  - — Thirty-two programmable I/O (PIO) pins
  - — Asynchronous serial port allows full-duplex, 7-bit or 8-bit data transfers
  - — DMA to and from asynchronous serial port
  - — Synchronous serial interface allows half-duplex, bidirectional data transfer to and from ASICs
  - — Reset configuration register
  - — Additional external interrupts
  - — Hardware watchdog timer can generate NMI or system reset
  - — Pseudo static RAM (PSRAM) controller includes auto refresh capability
- **Familiar 80C186 peripherals with enhanced functionality**
  - — Two independent DMA channels
  - — Programmable interrupt controller with six external interrupts
  - — Three programmable 16-bit timers
  - — Programmable memory and peripheral chip-select logic
  - — Programmable wait state generator
  - — Power-save clock mode
- **Software-compatible with the 80C186 and 80C188 microcontrollers**
- **Widely available native development tools, applications, and system software**
- **Available in the following packages:**
  - — 100-pin, thin quad flat pack (TQFP)
  - — 100-pin, plastic quad flat pack (PQFP)

GENERAL DESCRIPTION

The Am186™ER and Am188™ER microcontrollers are part of the AMD E86™ family of embedded microcontrollers and microprocessors based on the x86 architecture. The Am186ER and Am188ER microcontrollers are the ideal upgrade for designs requiring 80C186/80C188 microcontroller compatibility, increased performance, serial communications, a direct bus interface, and integrated memory.

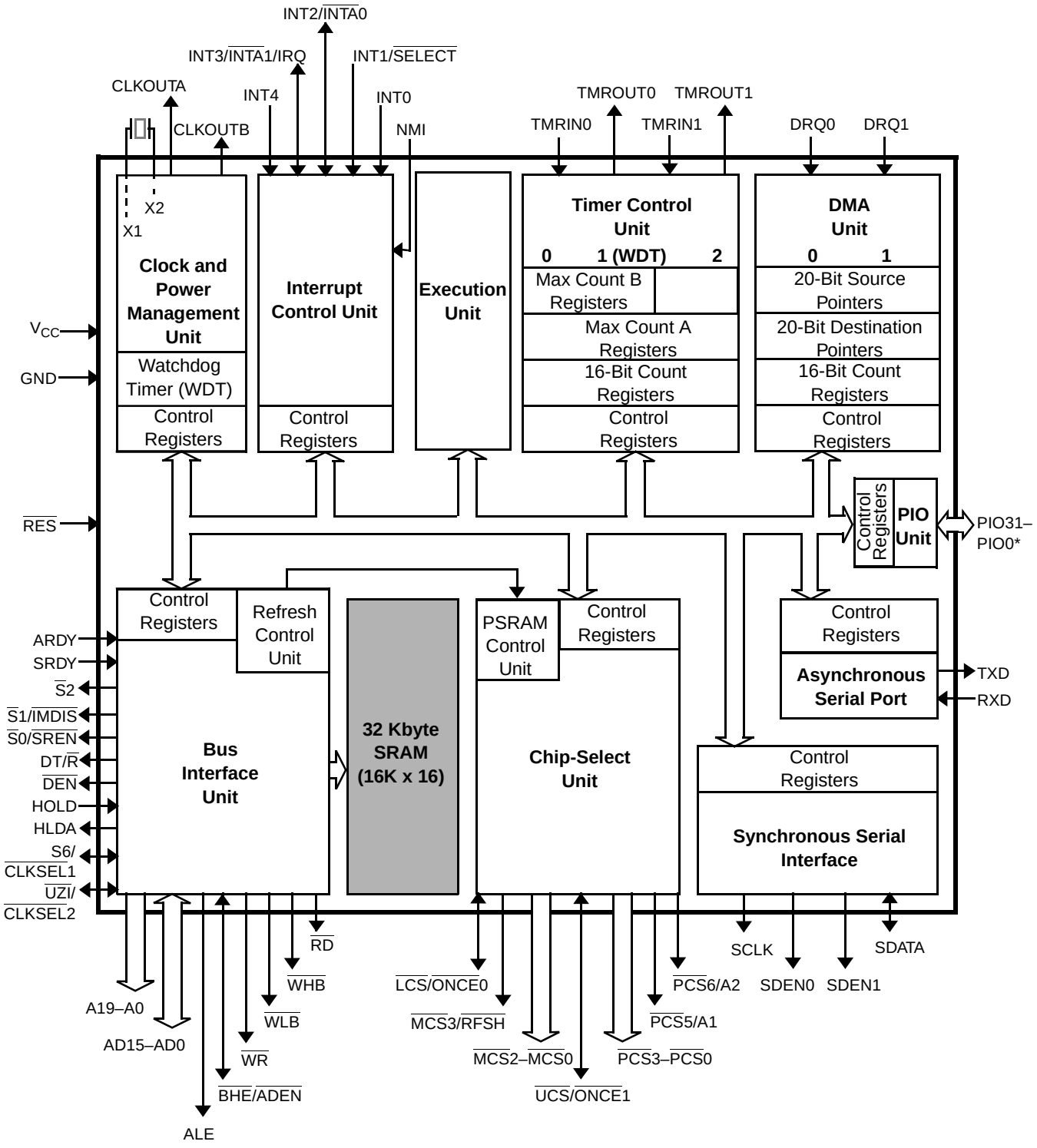
The Am186ER and Am188ER microcontrollers integrate memory and the functions of the CPU, nonmultiplexed address bus, timers, chip selects, interrupt controller, DMA controller, PSRAM controller, watchdog timer, asynchronous serial port, synchronous serial interface, and programmable I/O (PIO) pins on one chip. Compared to the 80C186/80C188 microcontrollers, the Am186ER and Am188ER microcontrollers enable designers to reduce the size, power consumption, and cost of embedded systems, while increasing functionality and performance.

The Am186ER and Am188ER microcontrollers have been designed to meet the most common requirements of embedded products developed for the communications, office automation, mass storage, and general embedded markets. Specific applications include feature phones, cellular phones, PBXs, multiplexers, modems, disk drives, hand-held terminals and desktop terminals, fax machines, printers, photocopiers, and industrial controls.

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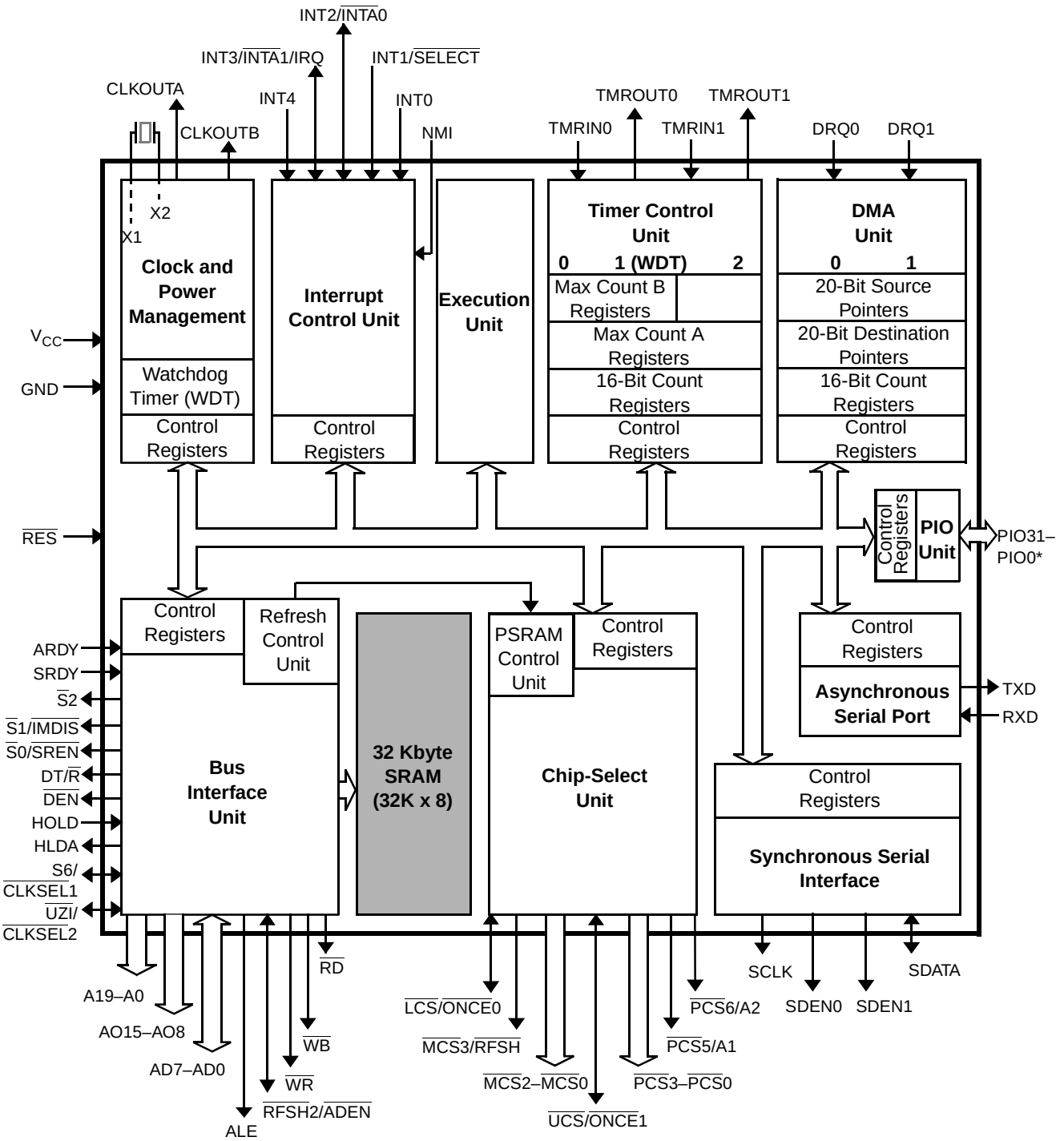
Publication# **20732** Rev: **D** Amendment/**0**
Issue Date: **June 2000**

Am186™ER MICROCONTROLLER BLOCK DIAGRAM



Note:
** All PIO signals are shared with other physical pins. See the pin descriptions beginning on page 30 and Table 3 on page 36 for information on shared functions.*

Am188™ER MICROCONTROLLER BLOCK DIAGRAM



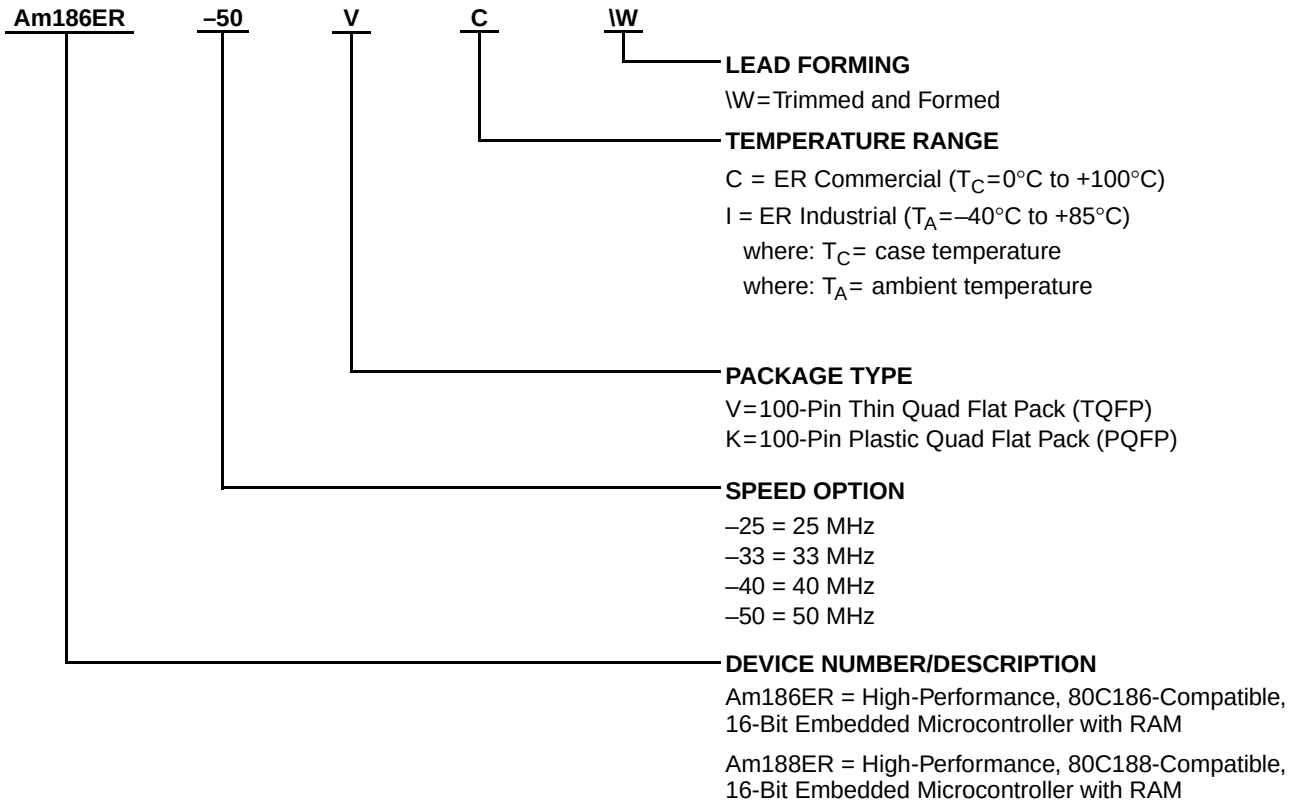
Notes:

** All PIO signals are shared with other physical pins. See the pin descriptions beginning on page 30 and Table 3 on page 36 for information on shared functions.*

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order numbers (valid combinations) are formed by a combination of the elements below.



Valid Combinations	
Am186ER–25 Am186ER–33 Am186ER–40 Am186ER–50	VC\W or KC\W
Am188ER–25 Am188ER–33 Am188ER–40 Am188ER–50	VC\W or KC\W
Am186ER–25 Am186ER–33 Am186ER–40 Am186ER–50	KI\W or VI\W
Am188ER–25 Am188ER–33 Am188ER–40 Am188ER–50	KI\W or VI\W

Valid Combinations

Valid combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

TABLE OF CONTENTS

Distinctive Characteristics 1
General Description 1
Am186™ER Microcontroller Block Diagram 2
Am188™ER Microcontroller Block Diagram 3
Ordering Information 4
List of Figures 9
List of Tables 9
Revision History 10
E86™ Family of Embedded Microprocessors and Microcontrollers 12
Related Documents 13
Demonstration Board Products 13
Third-Party Development Support Products 13
Customer Service 13
Key Features and Benefits 14
Application Considerations 14
Comparison of the Am186™ER and 80C186 Microcontrollers 15
TQFP Connection Diagram and Pinouts—Am186™ER Microcontroller 16
TQFP Pin Assignments—Am186™ER Microcontroller (Sorted by Pin Number) 17
TQFP Pin Assignments—Am186™ER Microcontroller (Sorted by Pin Name) 18
TQFP Connection Diagram and Pinouts—Am188™ER Microcontroller 19
TQFP Pin Assignments—Am188™ER Microcontroller (Sorted by Pin Number) 20
TQFP Pin Assignments—Am188™ER Microcontroller (Sorted by Pin Name) 21
PQFP Connection Diagram and Pinouts—Am186™ER Microcontroller 22
PQFP Pin Assignments—Am186™ER Microcontroller (Sorted by Pin Number) 23
PQFP Pin Assignments—Am186™ER Microcontroller (Sorted by Pin Name) 24
PQFP Connection Diagram and Pinouts—Am188™ER Microcontroller 25
PQFP Pin Assignments—Am188™ER Microcontroller (Sorted by Pin Number) 26
PQFP Pin Assignments—Am188™ER Microcontroller (Sorted by Pin Name) 27
Logic Symbol—Am186™ER Microcontroller 28
Logic Symbol—Am188™ER Microcontroller 29
Pin Descriptions 30
Pins Used by Emulators 30
A19–A0 (A19/PIO9, A18/PIO8, A17/PIO7) 30
AD7–AD0 30
AD15–AD8 (Am186™ER Microcontroller) 30
AO15–AO8 (Am188™ER Microcontroller) 30
ALE 31
$\overline{\text{ARDY}}$ 31
$\overline{\text{BHE}}$/ADEN (Am186™ER Microcontroller Only) 31
CLKOUTA 31
$\overline{\text{CLKOUTB}}$ 31
DEN/PIO5 31
DRQ1–DRQ0 (DRQ1/PIO13, DRQ0/PIO12) 32
DT/$\overline{\text{R}}$/PIO4 32
GND 32
HLDA 32
HOLD 32
INT0 32
INT1/$\overline{\text{SELECT}}$ 32
INT2/$\overline{\text{INTA}}$0/PIO31 33
INT3/INTA1/IRQ 33
INT4/PIO30 33

LCS/ONCE0 33
MCS3/RFSH/PIO25 33
MCS2–MCS0 (MCS2/PIO24, MCS1/PIO15, MCS0/PIO14) 34
NMI 34
PCS3–PCS0 (PCS3/PIO19, PCS2/PIO18, PCS1/PIO17, PCS0/PIO16) 34
PCS5/A1/PIO3 34
PCS6/A2/PIO2 34
PIO31–PIO0 (Shared) 35
RD 35
RES 35
RFSH2/ADEN (Am188™ER Microcontroller Only) 35
RXD/PIO28 35
S2 35
S1/IMDIS 37
S0/SREN 37
S6/CLKSEL1/PIO29 37
SCLK/PIO20 37
SDATA/PIO21 37
SDEN1/PIO23, SDEN0/PIO22 37
SRDY/PIO6 38
TMRIN0/PIO11 38
TMRIN1/PIO0 38
TMROUT0/PIO10 38
TMROUT1/PIO1 38
TXD/PIO27 38
UCS/ONCE1 38
UZI/CLKSEL2/PIO26 38
V_{CC} 39
WHB (Am186™ER Microcontroller Only) 39
WLB (Am186™ER Microcontroller Only) 39
WB (Am188™ER Microcontroller Only) 39
WR 39
X1 39
X2 39
Functional Description 40
Memory Organization 40
I/O Space 40
Bus Operation 41
Bus Interface Unit 41
Nonmultiplexed Address Bus 41
Byte Write Enables 41
Output Enable 41
Pseudo Static RAM (PSRAM) Support 44
Peripheral Control Block (PCB) 44
Reading and Writing the PCB 44
Clock and Power Management 44
Phase-Locked Loop (PLL) 44
Crystal-Driven Clock Source 45
External Source Clock 45
System Clocks 48
Power-Save Operation 48
Initialization and Processor Reset 48
Reset Configuration Register 48

Chip-Select Unit 49
Chip-Select Timing 49
Ready and Wait-State Programming 49
Memory Maps 50
Chip-Select Overlap 51
Upper Memory Chip Select 51
Low Memory Chip Select 51
Midrange Memory Chip Selects 51
Peripheral Chip Selects 52
Internal Memory 52
Interaction with External RAM 52
Emulator and Debug Modes 52
Refresh Control Unit 53
Interrupt Control Unit 53
Programming the Interrupt Control Unit 53
Timer Control Unit 53
Watchdog Timer 54
Direct Memory Access 54
DMA Operation 55
Asynchronous Serial Port/DMA Transfers 55
DMA Channel Control Registers 55
DMA Priority 55
Asynchronous Serial Port 56
DMA Transfers through the Serial Port 56
Synchronous Serial Interface 56
Four-Pin Interface 57
Programmable I/O (PIO) Pins 57
Low-Voltage Operation 59
Low-Voltage Standard 59
Power Savings 59
Input/Output Circuitry 59
Absolute Maximum Ratings 60
Operating Ranges 60
DC Characteristics Over Commercial and Industrial Operating Ranges 60
Thermal Characteristics 61
TQFP Package 61
Typical Ambient Temperatures 62
Commercial and Industrial Switching Characteristics and Waveforms 67
Key to Switching Waveforms 67
Alphabetical Key to Switching Parameter Symbols 68
Numerical Key to Switching Parameter Symbols 69
Switching Characteristics over Commercial and Industrial Operating Ranges, Read Cycle (25 MHz and 33 MHz) 70
Switching Characteristics over Commercial and Industrial Operating Ranges, Read Cycle (40 MHz and 50 MHz) 71
Read Cycle Waveforms 72
Switching Characteristics over Commercial and Industrial Operating Ranges, Write Cycle (25 MHz and 33 MHz) 73
Switching Characteristics over Commercial and Industrial Operating Ranges, Write Cycle (40 MHz and 50 MHz) 74
Write Cycle Waveforms 75
Switching Characteristics over Commercial and Industrial Operating Ranges, Internal RAM Show Read Cycle (25 MHz and 33 MHz) 76

Switching Characteristics over Commercial and Industrial Operating Ranges, Internal RAM Show Read Cycle (40 MHz and 50 MHz) 76
Internal RAM Show Read Cycle Waveform 77
Switching Characteristics over Commercial and Industrial Operating Ranges, PSRAM Read Cycle (25 MHz and 33 MHz) 78
Switching Characteristics over Commercial and Industrial Operating Ranges, PSRAM Read Cycle (40 MHz and 50 MHz) 79
PSRAM Read Cycle Waveforms 80
Switching Characteristics over Commercial and Industrial Operating Ranges, PSRAM Write Cycle (25 MHz and 33 MHz) 81
Switching Characteristics over Commercial and Industrial Operating Ranges, PSRAM Write Cycle (40 MHz and 50 MHz) 82
PSRAM Write Cycle Waveforms 83
Switching Characteristics over Commercial and Industrial Operating Ranges, PSRAM Refresh Cycle (25 MHz and 33 MHz) 84
Switching Characteristics over Commercial and Industrial Operating Ranges, PSRAM Refresh Cycle (40 MHz and 50 MHz) 85
PSRAM Refresh Cycle Waveforms 86
Switching Characteristics over Commercial and Industrial Operating Ranges, Interrupt Acknowledge Cycle (25 MHz and 33 MHz) 87
Switching Characteristics over Commercial Operating Ranges, Interrupt Acknowledge Cycle (40 MHz and 50 MHz) 88
Interrupt Acknowledge Cycle Waveforms 89
Switching Characteristics over Commercial and Industrial Operating Ranges, Software Halt Cycle (25 MHz and 33 MHz) 90
Switching Characteristics over Commercial and Industrial Operating Ranges, Software Halt Cycle (40 MHz and 50 MHz) 90
Software Halt Cycle Waveforms 91
Switching Characteristics over Commercial and Industrial Operating Ranges, Clock (25 MHz) 92
Switching Characteristics over Commercial and Industrial Operating Ranges, Clock (33 MHz) 93
Switching Characteristics over Commercial and Industrial Operating Ranges, Clock (40 MHz and 50 MHz) 94
Clock Waveforms—Active Mode 95
Clock Waveforms—Power-Save Mode 95
Switching Characteristics over Commercial and Industrial Operating Ranges, Ready and Peripheral Timing (25 MHz and 33 MHz) 96
Switching Characteristics over Commercial and Industrial Operating Ranges, Ready and Peripheral Timing (40 MHz and 50 MHz) 96
Synchronous Ready Waveforms 97
Asynchronous Ready Waveforms 97
Peripheral Waveforms 98
Switching Characteristics over Commercial and Industrial Operating Ranges, Reset and Bus Hold (25 MHz and 33 MHz) 99
Switching Characteristics over Commercial and Industrial Operating Ranges, Reset and Bus Hold (40 MHz and 50 MHz) 99
Reset Waveforms 100
Signals Related to Reset Waveforms 100
Bus Hold Waveforms—Entering 101
Bus Hold Waveforms—Leaving 101
Switching Characteristics over Commercial and Industrial Operating Ranges, Synchronous Serial Interface (SSI) (25 MHz and 33 MHz) 102

Switching Characteristics over Commercial and Industrial Operating Ranges, Synchronous Serial Interface (SSI) (40 MHz and 50 MHz) 102
Synchronous Serial Interface (SSI) Waveforms 103
TQFP Physical Dimensions 104
PQFP Physical Dimensions 105
Index Index-1

LIST OF FIGURES

Figure 1. Am186ER 50-MHz Example System Design 15
Figure 2. Typical 80C186 System Design 15
Figure 3. Two-Component Address Example 40
Figure 4. Am186™ER Microcontroller Address Bus—Normal Operation 42
Figure 5. Am186™ER Microcontroller—Address Bus Disable in Effect 42
Figure 6. Am188™ER Microcontroller Address Bus—Normal Operation 43
Figure 7. Am188™ER Microcontroller—Address Bus Disable in Effect 43
Figure 8. Am186™ER and Am188™ER Microcontrollers Oscillator Configurations 45
Figure 9. Peripheral Control Block Register Map 46
Figure 10. Clock Organization 48
Figure 11. ARDY and SRDY Synchronization Logic Diagram 49
Figure 12. Example Memory Maps 50
Figure 13. DMA Unit Block Diagram 56
Figure 14. Synchronous Serial Interface Multiple Write 58
Figure 15. Synchronous Serial Interface Multiple Read 58
Figure 16. Thermal Resistance (°C/Watt) 61
Figure 17. Thermal Characteristics Equations 61
Figure 18. Typical Ambient Temperatures for PQFP with Two-Layer Board 63
Figure 19. Typical Ambient Temperatures for TQFP with Two-Layer Board 64
Figure 20. Typical Ambient Temperatures for PQFP with Four-Layer to Six-Layer Board 65
Figure 21. Typical Ambient Temperatures for TQFP with Four-Layer to Six-Layer Board 66

LIST OF TABLES

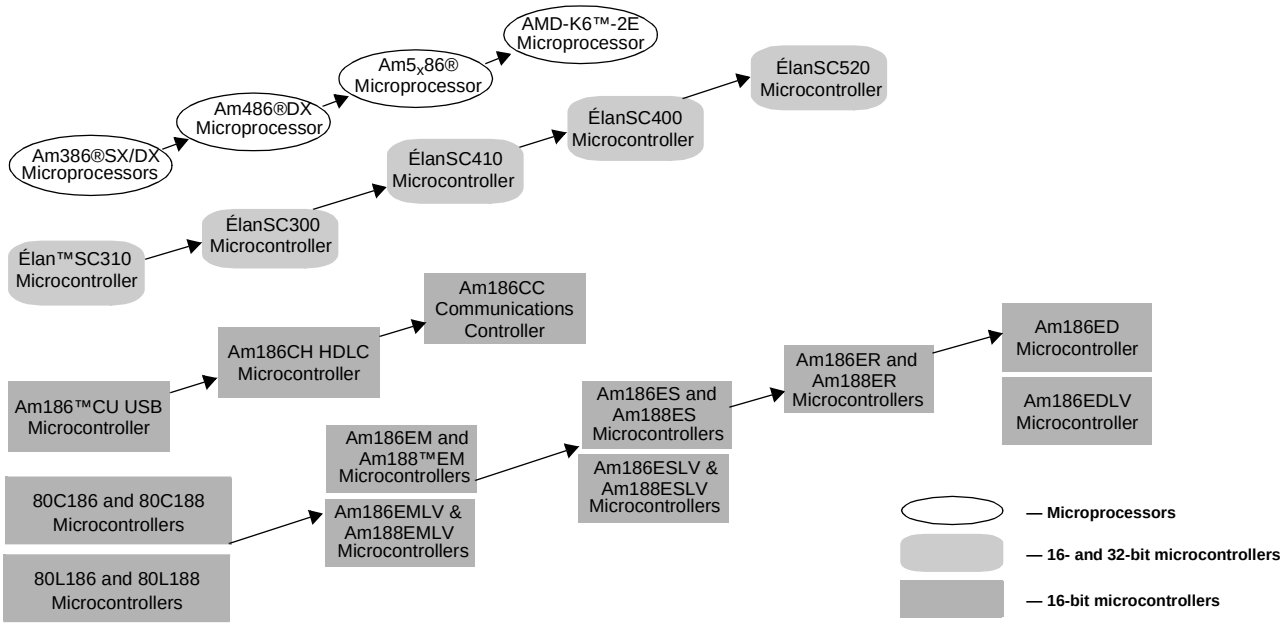
Table 1. Related AMD Products—E86™ Family Devices 12
Table 2. Data Byte Encoding 31
Table 3. Numeric PIO Pin Assignments 36
Table 4. Alphabetic PIO Pin Assignments 36
Table 5. Bus Cycle Encoding 37
Table 6. Clocking Modes 39
Table 7. Segment Register Selection Rules 40
Table 8. Maximum and Minimum Clock Frequencies 44
Table 9. Am186ER Microcontroller Maximum DMA Transfer Rates 55
Table 10. Thermal Characteristics (°C/Watt) 61
Table 11. Typical Power Consumption Calculation 62
Table 12. Junction Temperature Calculation 62
Table 13. Typical Ambient Temperatures for PQFP with Two-Layer Board 63
Table 14. Typical Ambient Temperatures for TQFP with Two-Layer Board 64
Table 15. Typical Ambient Temperatures for PQFP with Four-Layer to Six-Layer Board 65
Table 16. Typical Ambient Temperatures for TQFP with Four-Layer to Six-Layer Board 66

REVISION HISTORY

Date	Rev	Description
Feb. 2000	D	Replaced block diagrams on page 2 and page 3 with updated diagrams showing that the internal data bus interfaces via the BIU and not RAM.
Feb. 2000	D	Added new industrial parts for “Ordering Information” on page 4.
Feb. 2000	D	Updated product listings and customer service matter on page 12 and page 13.
Feb. 2000	D	Replaced Figure 8 on page 45 (microcontroller oscillator configurations) with updated figure.
Feb. 2000	D	Updated several references to watchdog timer on page 54 to reflect that the WDT is inactive after reset, not active).
Feb. 2000	D	Provided a value for the TBD in the table entitled, “DC Characteristics Over Commercial and Industrial Operating Ranges” on page 60.
Feb. 2000	D	Updated table title and "Min" values for No. 66 in the switching characteristics table, “Read Cycle (40 MHz and 50 MHz)” on page 71.
Feb. 2000	D	Updated table title and "Max" values for No. 87 in the switching characteristics table, “Write Cycle (40 MHz and 50 MHz)” on page 74.
Feb. 2000	D	Updated table title and "Min" value for No. 9 (50 MHz) in the switching characteristics table, “Internal RAM Show Read Cycle (40 MHz and 50 MHz)” on page 76.
Feb. 2000	D	Updated table title and "Min" values for No. 66 in the switching characteristics table, “PSRAM Read Cycle (40 MHz and 50 MHz)” on page 79.
Feb. 2000	D	Updated table title and "Max" value for No. 68 (40 MHz) in the switching characteristics table, “PSRAM Write Cycle (40 MHz and 50 MHz)” on page 82.
Feb. 2000	D	Updated table title in the switching characteristics table, “PSRAM Refresh Cycle (40 MHz and 50 MHz)” on page 85.
Feb. 2000	D	Updated table title in the switching characteristics table, “Software Halt Cycle (40 MHz and 50 MHz)” on page 90.
Feb. 2000	D	Updated "Min" and "Max" values in the switching characteristics table, “Clock (33 MHz)” on page 93.
Feb. 2000	D	Updated table title in the switching characteristics table, “Clock (40 MHz and 50 MHz)” on page 94.
Feb. 2000	D	Updated table title in the switching characteristics table, “Ready and Peripheral Timing (40 MHz and 50 MHz)” on page 96.
Feb. 2000	D	Updated table title in the switching characteristics table, “Reset and Bus Hold (40 MHz and 50 MHz)” on page 99.
Feb. 2000	D	Updated table title in the switching characteristics table, “Synchronous Serial Interface (SSI) (40 MHz and 50 MHz)” on page 102.
Feb. 2000	D	In the table "Switching Characteristics over Commercial and Industrial Operating Ranges Read Cycle (40 MHz and 50 MHz)", row 9, column "50 MHz" - "Min", the "0" is deleted.
Feb. 2000	D	In the table "Switching Characteristics over Commercial and Industrial Operating Ranges Read Cycle (40 MHz and 50 MHz)", row 66, column "40 MHz" - "Min", the value is changed.
Feb. 2000	D	In the table "Switching Characteristics over Commercial and Industrial Operating Ranges Read Cycle (40 MHz and 50 MHz)", row 66, column "50 MHz" - "Min", the value is changed.
Feb. 2000	D	In the table "Switching Characteristics over Commercial and Industrial Operating Ranges PSRAM Write Cycle (40 MHz and 50 MHz)", row 68, column "40 MHz" - "Max", the value is changed.
May 2000	D	Under “Key Features and Benefits” on page 14, in the third bullet "Enhanced functionality," the feature, "a PSRAM controller" was added.
May 2000	D	Under “HOLD” on page 32, the sentence, "A HOLD request is second only to DRAM or PSRAM refresh requests in priority of activity requests received by the processor." is changed.

Date	Rev	Description
May 2000	D	Under “SRDY/PIO6” on page 38, the following sentence was added: "When SRDY is configured as P106, the internal SRDY signal is driven Low."
May 2000	D	In Table 8, “Maximum and Minimum Clock Frequencies,” on page 44, the values are changed in the cell of row "Divide by 2" and column "X1/X2 Min" and in the cell of row "Divide by 2" and column "CLKOUTA Min".
May 2000	D	In “Switching Characteristics over Commercial and Industrial Operating Ranges” on page 93, Max value in the number "36" row was changed to "33."
May 2000	D	In “Switching Characteristics over Commercial and Industrial Operating Ranges” on page 94, the value in "40 MHz Max" for row number 36 was changed to "33."
May 2000	D	In “Synchronous Ready Waveforms” on page 97, the diagram was changed.
May 2000	D	In “Asynchronous Ready Waveforms” on page 97, the diagram was changed.
May 2000	D	In "$\overline{\text{BHE}}$/$\overline{\text{ADEN}}$", on page 31, the second paragraph under $\overline{\text{ADEN}}$ was changed.
May 2000	D	In "$\overline{\text{UZI}}$/$\overline{\text{CLKSEL2}}$/PIO26", on page 38, the paragraph description of $\overline{\text{UZI}}$ was changed.
May 2000	D	In “Read Cycle Waveforms” on page 72, the UZI line in the diagram was changed.
May 2000	D	In “Write Cycle Waveforms” on page 75, the UZI line in the diagram was changed.
May 2000	D	Added the diagram, Table 11, “ARDY and SRDY Synchronization Logic Diagram,” on page 49.
May 2000	D	Added an index.

E86™ FAMILY OF EMBEDDED MICROPROCESSORS AND MICROCONTROLLERS



E86™ Family of Embedded Microprocessors and Microcontrollers

Table 1. Related AMD Products—E86™ Family Devices

Device[1]	Description
80C186/80C188	16-bit microcontroller
80L186/80L188	Low-voltage, 16-bit microcontroller
Am186™EM/Am188™EM	High-performance, 16-bit embedded microcontroller
Am186EMLV/Am188EMLV	High-performance, 16-bit embedded microcontroller
Am186ES/Am188ES	High-performance, 16-bit embedded microcontroller
Am186ESLV/Am188ESLV	High-performance, 16-bit embedded microcontroller
Am186ED	High-performance, 80C186- and 80C188-compatible, 16-bit embedded microcontroller with 8- or 16-bit external data bus
Am186EDLV	High-performance, 80C186- and 80C188-compatible, low-voltage, 16-bit embedded microcontroller with 8- or 16-bit external data bus
Am186ER/Am188ER	High-performance, low-voltage, 16-bit embedded microcontroller with 32 Kbyte of internal SRAM
Am186CC	High-performance, 16-bit embedded communications controller
Am186CH	High-performance, 16-bit embedded HDLC microcontroller
Am186CU	High-performance, 16-bit embedded USB microcontroller
ÉlanSC300	High-performance, highly integrated, low-voltage, 32-bit embedded microcontroller
ÉlanSC310	High-performance, single-chip, 32-bit embedded PC/AT-compatible microcontroller
ÉlanSC400	High-performance, single-chip, low-power, PC/AT-compatible microcontroller
ÉlanSC410	High-performance, single-chip, PC/AT-compatible microcontroller
ÉlanSC520	High-performance, single-chip, 32-bit embedded microcontroller
Am386®SX	High-performance, 32-bit embedded microprocessor with 16-bit external data bus
Am386®DX	High-performance, 32-bit embedded microprocessor with 32-bit external data bus
Am486®DX	High-performance, 32-bit embedded microprocessor with 32-bit external data bus
Am5$_x$86®	High-performance, 32-bit embedded microprocessor with 32-bit external data bus
AMD-K6™-2E	High-performance, 32-bit embedded microprocessor with 64-bit external data bus and 3DNow!™ technology

Notes:

1. 186 = 16-bit microcontroller and 80C186-compatible (except where noted otherwise); 188 = 16-bit microcontroller with 8-bit external data bus and 80C188-compatible (except where noted otherwise); LV = low voltage

Related Documents

The following documents provide additional information regarding the Am186ER and Am188ER microcontrollers.

- *Am186ER and Am188ER Microcontrollers User's Manual*, order #21684
- *FusionE86℠ Catalog*, order #19255
- *Making the Most of the Am186™ER or Am188™ER Microcontroller Application Note*, order #21046
- *Using the 3.3-V Am186™ER or Am188™ER Microcontroller in a 5-V System Application Note,* order #21045
- *Comparing the Am186™EM and Am186ER Microcontrollers* Technical Bulletin (Available only at **www.amd.com/products/epd/techdocs.**)
- *The Advantages of Integrated RAM* Technical Bulletin (Available only at **www.amd.com/products/epd/techdocs.**)

A full description of the Am186ER and Am188ER microcontrollers' registers and instructions is included in the *Am186ER and Am188ER Microcontrollers User's Manual* listed above.

To order literature, contact the nearest AMD sales office or call the literature center at one of the numbers listed on the back cover of this manual. In addition, all these documents are available in PDF form on the AMD web site. To access the AMD home page, go to www.amd.com. Then follow the Embedded Processor link for information about E86 microcontrollers.

Demonstration Board Products

The SD186ER demonstration board product is a standalone, low-cost evaluation platform for the Am186ER microcontroller.

The SD186ER board demonstrates the basic processor functionality and features of the Am186ER microcontroller and the simplicity of its system design. The SD186ER demonstration board is designed with the Am186/Am188 expansion interface that provides access to the Am186ER microcontroller signals. The 104-pin expansion interface facilitates prototyping by enabling the demonstration board to be used as the minimal system core of a design. Contact your local AMD sales office for more information on demonstration board availability and pricing.

Third-Party Development Support Products

The FusionE86 Program of Partnerships for Application Solutions provides the customer with an array of products designed to meet critical time-to-market needs. Products and solutions available from the AMD FusionE86 partners include protocol stacks, emulators, hardware and software debuggers, board-level products, and software development tools, among others.

In addition, mature development tools and applications for the x86 platform are widely available in the general marketplace.

Customer Service

The AMD customer service network includes U.S. offices, international offices, and a customer training center. Expert technical assistance is available from the AMD worldwide staff of field application engineers and factory support staff to answer E86 and Comm86 family hardware and software development questions.

Hotline and World Wide Web Support

For answers to technical questions, AMD provides e-mail support as well as a toll-free number for direct access to our corporate applications hotline.

Note: *The support telephone numbers listed below are subject to change. For current telephone numbers, refer to* **www.amd.com/support/literature**.

The AMD World Wide Web home page provides the latest product information, including technical information and data on upcoming product releases. In addition, EPD CodeKit software on the Web site provides tested source code example applications.

Corporate Applications Hotline

(800) 222-9323	Toll-free for U.S. and Canada
44-(0) 1276-803-299	U.K. and Europe hotline

Additional contact information is listed on the back of this datasheet. For technical support questions on all E86 and Comm86 products, send e-mail to **epd.support@amd.com**.

World Wide Web Home Page

To access the AMD home page go to: **www.amd.com**. Then follow the **Embedded Processors** link for information about E86 family and Comm86™ products.

Questions, requests, and input concerning AMD's WWW pages can be sent via e-mail to **webmaster@amd.com**.

Documentation and Literature

Free information such as data books, user's manuals, data sheets, application notes, the <Italics>E86™ Family Products and Development Tools CD, order #21058, and other literature is available with a simple phone call. Internationally, contact your local AMD sales office for product literature. Additional contact information is listed on the back of this data sheet.

Literature Ordering

(800) 222-9323	Toll-free for U.S. and Canada

KEY FEATURES AND BENEFITS

The Am186ER and Am188ER microcontrollers are higher-performance, highly integrated versions of the 80C186/80C188 microprocessors, offering a migration path that was previously unavailable. New peripherals, on-chip system interface logic, and 32 Kbyte of internal memory on the Am186ER microcontroller reduce the cost of existing 80C186/80C188 designs. Upgrading to the Am186ER microcontroller is an attractive solution for several reasons:

- **Integrated SRAM**—32 Kbyte of internal SRAM ensures a low-cost supply of memory and a smaller form factor for system designs. The internal memory provides the same performance as external zero-wait-state SRAM devices.
- **3.3-V operation with 5-V-tolerant I/O**—3.3-V operation provides much lower power consumption when compared to existing 5-V designs. Plus, the Am186ER and Am188ER controllers accommodate current 5-V designs with 5-V-tolerant I/O drivers.
- **x86 software compatibility**—80C186/80C188-compatible and upward-compatible with the other members of the AMD E86 family.
- **Enhanced performance**—The Am186ER and Am188ER microcontrollers increase the performance of 80C186/80C188 systems, and the nonmultiplexed address bus offers faster, unbuffered access to commodity-speed, external memory.
- **Enhanced functionality**—Enhanced on-chip peripherals include an asynchronous serial port, up to 32 PIOs, a hardware watchdog timer, an additional interrupt pin, a synchronous serial interface, a PSRAM controller, a 16-bit reset configuration register, and enhanced chip-select functionality.

Application Considerations

The integration enhancements of the Am186ER microcontroller provide a high-performance, low-system-cost solution for 16-bit embedded microcontroller designs. Both multiplexed and nonmultiplexed address buses are available on the Am186ER and Am188ER microcontrollers. The nonmultiplexed address bus eliminates system-support logic ordinarily needed to interface with external memory devices, while the multiplexed address/data bus maintains the value of previously engineered, customer-specific peripherals and circuits within the upgraded design. Figure 1 on page 15 illustrates an example system design that uses the integrated peripheral set to achieve high performance with reduced system cost.

Internal Memory

The 32-Kbyte internal RAM fulfills the memory requirements for many embedded systems. These systems can take advantage of the increased reliability, smaller system form factor, decreased system power, stable RAM supply, and lower system cost compared with buying external SRAM. The integrated RAM also ensures that an entire embedded system will not require requalification based on the short life cycles of external SRAM. Additionally, for those systems using more RAM than required because of the granularity of external RAM, the Am186ER microcontroller provides a closer system match.

Clock Generation

The integrated clock generation circuitry of the Am186ER and Am188ER microcontrollers enables the processors to operate at up to four times the crystal frequency. The design in Figure 1 achieves 50-MHz CPU operation while using a 12.5-MHz crystal. The clocking frequency function is controlled by an internal PLL. The following modes are available (see Figure 10 on page 48):

- Divide by Two—The frequency of the fundamental clock is half the frequency of the crystal with the PLL disabled.
- Times One—The frequency of the fundamental clock will be the same as the external crystal with the PLL enabled.
- Times Four—The frequency of the fundamental clock is four times the frequency of the crystal with the PLL enabled.

The default mode is Times Four.

Memory Interface

The integrated memory controller logic of the Am186ER and Am188ER microcontrollers provides a direct address bus to memory devices. Using an external address latch controlled by the address latch enable (ALE) signal is no longer necessary. Individual byte-write-enable signals on the Am186ER and Am188ER microcontrollers eliminate the need for external high/low byte-write-enable circuitry. The maximum bank size programmable for the memory chip-select signals is increased to facilitate the use of high-density memory devices.

The improved memory timing specifications for the Am186ER and Am188ER microcontrollers facilitate the use of external memory devices with 55-ns access times at 50-MHz CPU operation. As a result, overall system cost is significantly reduced as system designers are able to use commonly available memory technology.

Direct Memory Interface Example

Figure 1 illustrates the direct interface to memory of the Am186ER microcontroller. The A19–A0 bus connects to the memory address inputs, the AD bus connects to the data inputs and outputs, and the chip selects connect to the memory chip-select inputs.

Figure 1 also shows an implementation of an RS-232 console or modem communications port. The RS-232-to-CMOS voltage-level converter is required for the electrical interface with the external device.

COMPARISON OF THE Am186™ER AND 80C186 MICROCONTROLLERS

Figure 1 shows an example system using a 50-MHz Am186ER microcontroller. Figure 2 shows a comparable system implementation with an 80C186 microcontroller. Because of its superior integration, the Am186ER system does not require the support devices required on the 80C186 example system. In addition, the Am186ER microcontroller provides significantly better performance with its 50-MHz clock rate.

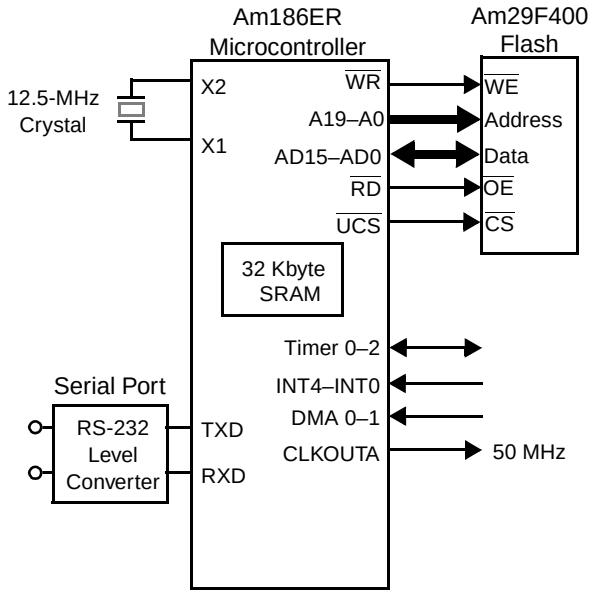


Figure 1. Am186™ER 50-MHz Example System Design

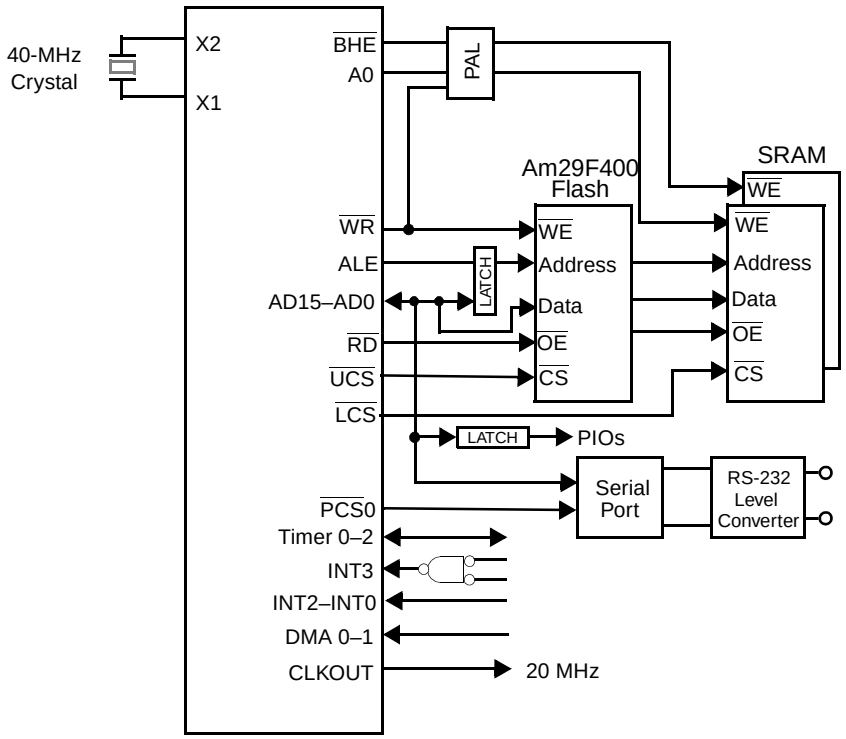
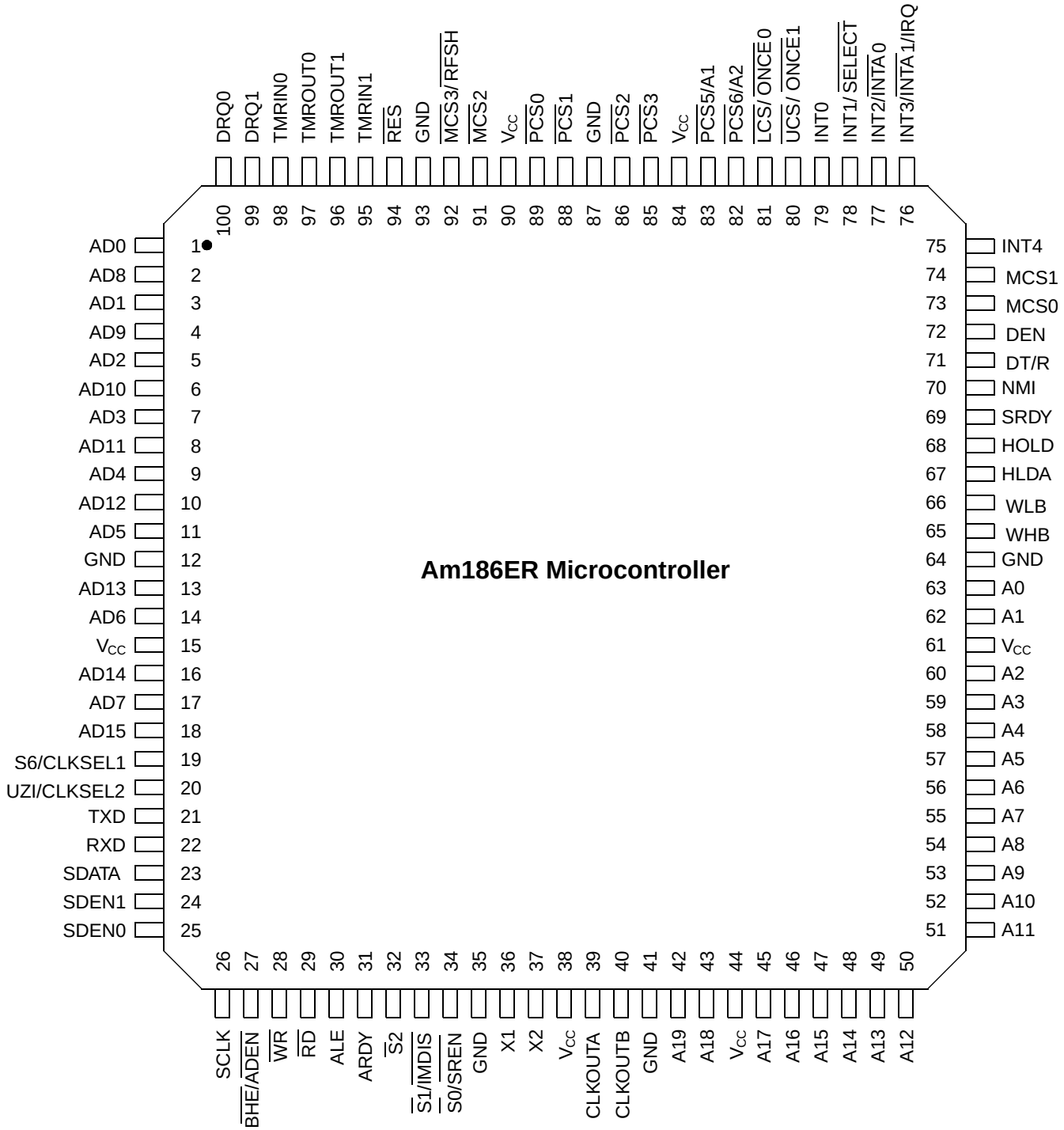


Figure 2. Typical 80C186 System Design

TQFP CONNECTION DIAGRAM AND PINOUTS—Am186™ER MICROCONTROLLER

Top Side View—100-Pin Thin Quad Flat Pack (TQFP)



Notes:

Pin 1 is marked for orientation.

TQFP PIN ASSIGNMENTS—Am186™ER MICROCONTROLLER (Sorted by Pin Number)

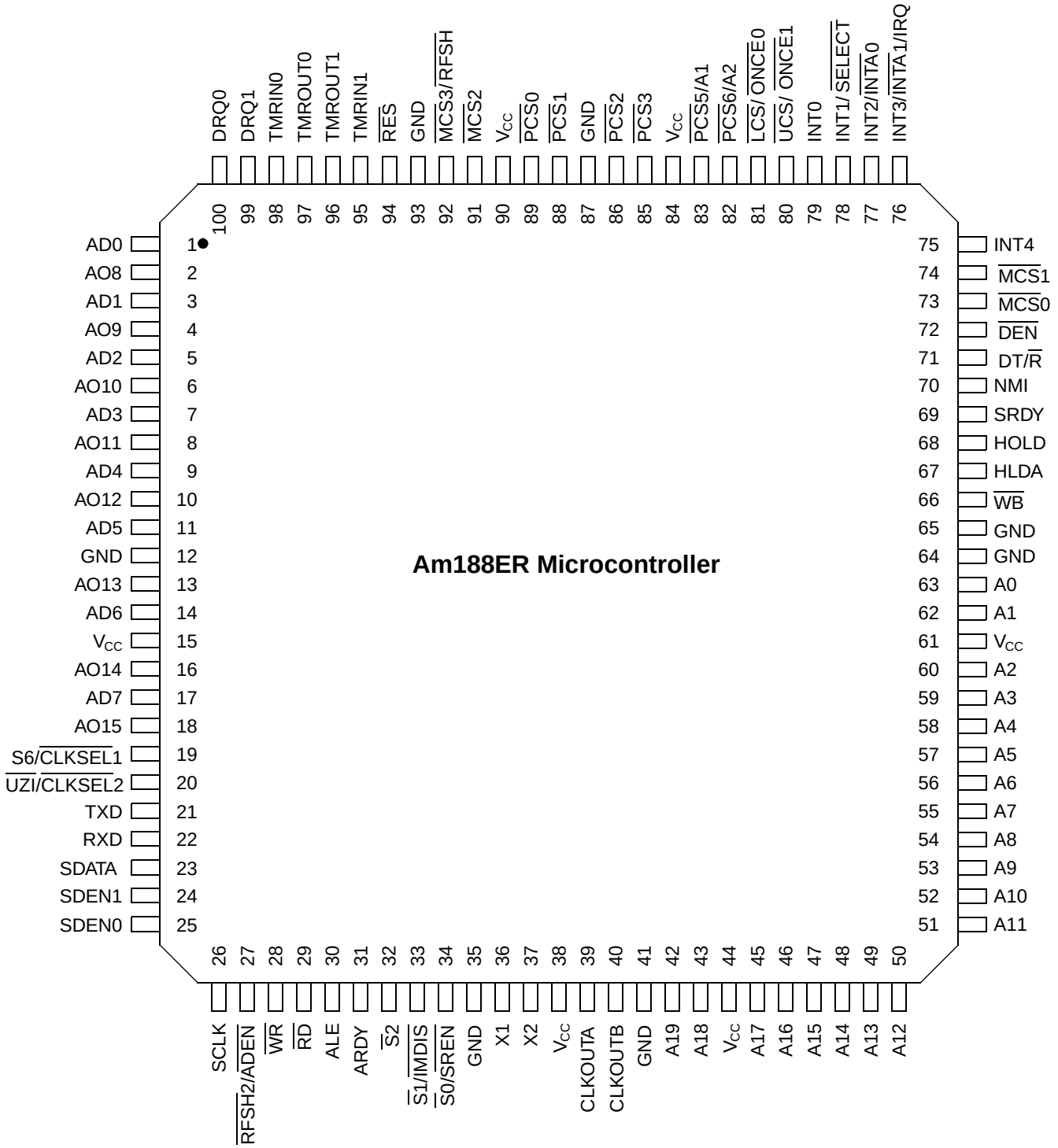
Pin No.	Name	Pin No.	Name	Pin No.	Name	Pin No.	Name
1	AD0	26	SCLK/PIO20	51	A11	76	INT3/$\overline{\text{INTA}}$1/IRQ
2	AD8	27	$\overline{\text{BHE}}$/$\overline{\text{ADEN}}$	52	A10	77	INT2/$\overline{\text{INTA}}$0
3	AD1	28	$\overline{\text{WR}}$	53	A9	78	INT1/$\overline{\text{SELECT}}$
4	AD9	29	$\overline{\text{RD}}$	54	A8	79	INT0
5	AD2	30	ALE	55	A7	80	UCS/$\overline{\text{ONCE}}$1
6	AD10	31	ARDY	56	A6	81	$\overline{\text{LCS}}$/$\overline{\text{ONCE}}$0
7	AD3	32	$\overline{\text{S}}$2	57	A5	82	$\overline{\text{PCS}}$6/A2/PIO2
8	AD11	33	$\overline{\text{S}}$1/$\overline{\text{IMDIS}}$	58	A4	83	$\overline{\text{PCS}}$5/A1/PIO3
9	AD4	34	$\overline{\text{S}}$0/$\overline{\text{SREN}}$	59	A3	84	V_{CC}
10	AD12	35	GND	60	A2	85	$\overline{\text{PCS}}$3/PIO19
11	AD5	36	X1	61	V_{CC}	86	$\overline{\text{PCS}}$2/PIO18
12	GND	37	X2	62	A1	87	GND
13	AD13	38	V_{CC}	63	A0	88	$\overline{\text{PCS}}$1/PIO17
14	AD6	39	CLKOUTA	64	GND	89	$\overline{\text{PCS}}$0/PIO16
15	V_{CC}	40	CLKOUTB	65	$\overline{\text{WHB}}$	90	V_{CC}
16	AD14	41	GND	66	$\overline{\text{WLB}}$	91	$\overline{\text{MCS}}$2
17	AD7	42	A19/PIO9	67	HLDA	92	$\overline{\text{MCS}}$3/$\overline{\text{RFSH}}$
18	AD15	43	A18/PIO8	68	HOLD	93	GND
19	S6/$\overline{\text{CKLSEL}}$1/PIO29	44	V_{CC}	69	SRDY/PIO6	94	$\overline{\text{RES}}$
20	$\overline{\text{UZI}}$/$\overline{\text{CLKSEL}}$2/PIO26	45	A17/PIO7	70	NMI	95	TMRIN1/PIO0
21	TXD	46	A16	71	DT/$\overline{\text{R}}$/PIO4	96	TMROUT1/PIO1
22	RXD	47	A15	72	$\overline{\text{DEN}}$/PIO5	97	TMROUT0/PIO10
23	SDATA/PIO21	48	A14	73	$\overline{\text{MCS}}$0/PIO14	98	TMRIN0/PIO11
24	SDEN1/PIO23	49	A13	74	$\overline{\text{MCS}}$1/PIO15	99	DRQ1/PIO13
25	SDEN0/PIO22	50	A12	75	INT4	100	DRQ0/PIO12

TQFP PIN ASSIGNMENTS—Am186™ER MICROCONTROLLER
(Sorted by Pin Name)

Pin Name	No.	Pin Name	No.	Pin Name	No.	Pin Name	No.
A0	63	AD5	11	GND	93	$\overline{S2}$	32
A1	62	AD6	14	HLDA	67	S6/$\overline{CLKSEL1}$/PIO29	19
A2	60	AD7	17	HOLD	68	SCLK/PIO20	26
A3	59	AD8	2	INT0	79	SDATA/PIO21	23
A4	58	AD9	4	INT1/$\overline{SELECT}$	78	SDEN0/PIO22	25
A5	57	AD10	6	INT2/$\overline{INTA}$0	77	SDEN1/PIO23	24
A6	56	AD11	8	INT3/$\overline{INTA}$1/IRQ	76	SRDY/PIO6	69
A7	55	AD12	10	INT4	75	TMRIN0/PIO11	98
A8	54	AD13	13	$\overline{LCS}$/$\overline{ONCE}$0	81	TMRIN1/PIO0	95
A9	53	AD14	16	$\overline{MCS}$0/PIO14	73	TMROUT0/PIO10	97
A10	52	AD15	18	$\overline{MCS}$1/PIO15	74	TMROUT1/PIO1	96
A11	51	ALE	30	$\overline{MCS}$2	91	TXD	21
A12	50	ARDY	31	$\overline{MCS}$3/$\overline{RFSH}$	92	$\overline{UCS}$/$\overline{ONCE}$1	80
A13	49	$\overline{BHE}$/$\overline{ADEN}$	27	NMI	70	$\overline{UZI}$/$\overline{CLKSEL}$2/PIO26	20
A14	48	CLKOUTA	39	$\overline{PCS}$0/PIO16	89	V_{CC}	15
A15	47	CLKOUTB	40	$\overline{PCS}$1/PIO17	88	V_{CC}	38
A16	46	$\overline{DEN}$/PIO5	72	$\overline{PCS}$2/PIO18	86	V_{CC}	44
A17/PIO7	45	DRQ0/PIO12	100	$\overline{PCS}$3/PIO19	85	V_{CC}	61
A18/PIO8	43	DRQ1/PIO13	99	$\overline{PCS}$5/A1/PIO3	83	V_{CC}	84
A19/PIO9	42	DT/$\overline{R}$/PIO4	71	$\overline{PCS}$6/A2/PIO2	82	V_{CC}	90
AD0	1	GND	12	$\overline{RD}$	29	$\overline{WHB}$	65
AD1	3	GND	35	$\overline{RES}$	94	$\overline{WLB}$	66
AD2	5	GND	41	RXD	22	$\overline{WR}$	28
AD3	7	GND	64	$\overline{S0}$/$\overline{SREN}$	34	X1	36
AD4	9	GND	87	$\overline{S1}$/$\overline{IMDIS}$	33	X2	37

TQFP CONNECTION DIAGRAM AND PINOUTS—Am188™ER MICROCONTROLLER

Top Side View—100-Pin Thin Quad Flat Pack (TQFP)



Notes:

Pin 1 is marked for orientation.

TQFP PIN ASSIGNMENTS—Am188™ER MICROCONTROLLER
(Sorted by Pin Number)

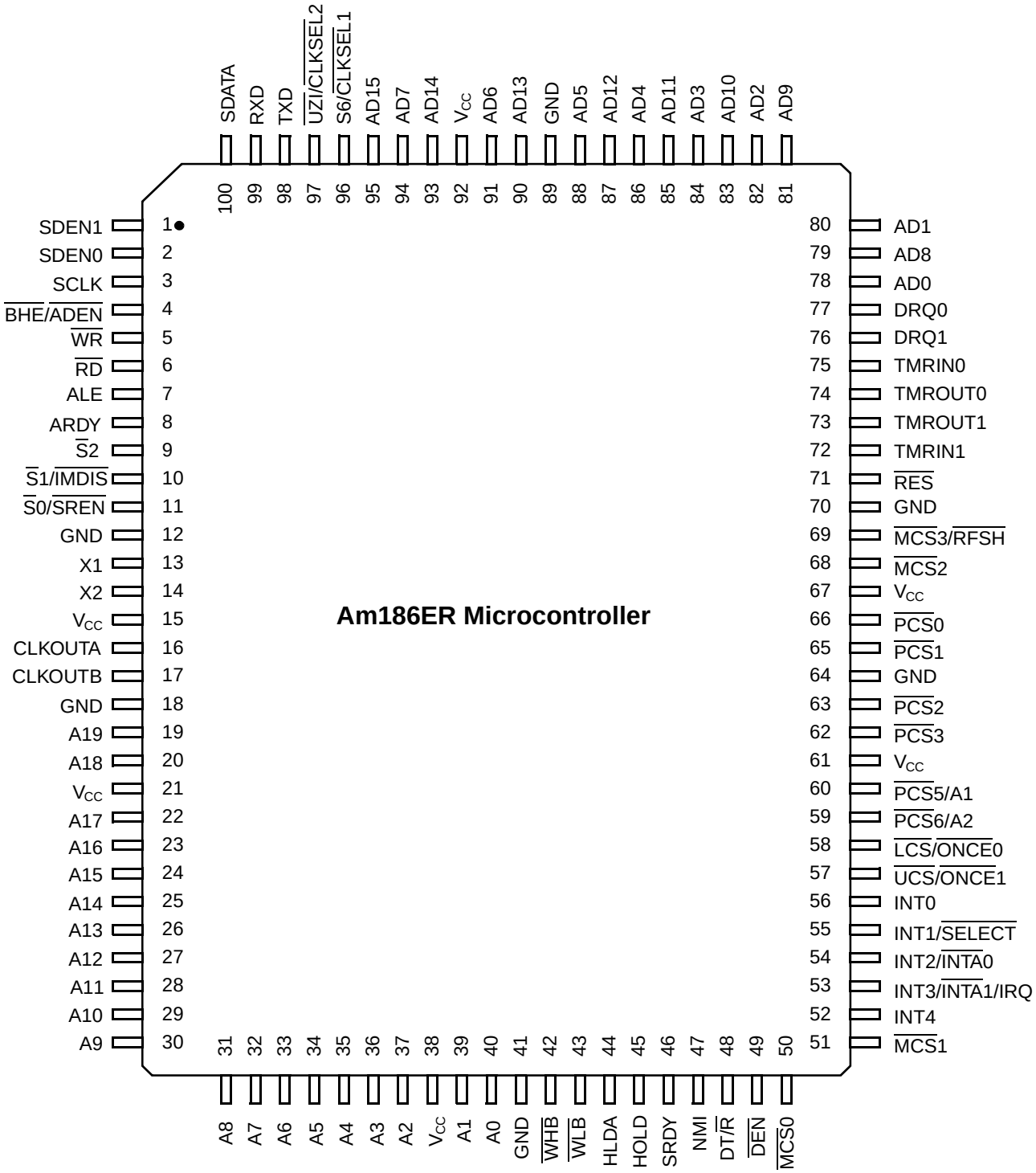
Pin No.	Name	Pin No.	Name	Pin No.	Name	Pin No.	Name
1	AD0	26	SCLK/PIO20	51	A11	76	INT3/$\overline{\text{INTA}}$1/IRQ
2	AO8	27	$\overline{\text{RFSH}}$2/$\overline{\text{ADEN}}$	52	A10	77	INT2/$\overline{\text{INTA}}$0/PIO31
3	AD1	28	$\overline{\text{WR}}$	53	A9	78	INT1/$\overline{\text{SELECT}}$
4	AO9	29	$\overline{\text{RD}}$	54	A8	79	INT0
5	AD2	30	ALE	55	A7	80	$\overline{\text{UCS}}$/$\overline{\text{ONCE}}$1
6	AO10	31	ARDY	56	A6	81	$\overline{\text{LCS}}$/$\overline{\text{ONCE}}$0
7	AD3	32	$\overline{\text{S}}$2	57	A5	82	$\overline{\text{PCS}}$6/A2/PIO2
8	AO11	33	$\overline{\text{S}}$1/$\overline{\text{IMDIS}}$	58	A4	83	$\overline{\text{PCS}}$5/A1/PIO3
9	AD4	34	$\overline{\text{S}}$0/$\overline{\text{SREN}}$	59	A3	84	V_{CC}
10	AO12	35	GND	60	A2	85	$\overline{\text{PCS}}$3/PIO19
11	AD5	36	X1	61	V_{CC}	86	$\overline{\text{PCS}}$2/PIO18
12	GND	37	X2	62	A1	87	GND
13	AO13	38	V_{CC}	63	A0	88	$\overline{\text{PCS}}$1/PIO17
14	AD6	39	CLKOUTA	64	GND	89	$\overline{\text{PCS}}$0/PIO16
15	V_{CC}	40	CLKOUTB	65	GND	90	V_{CC}
16	AO14	41	GND	66	$\overline{\text{WB}}$	91	$\overline{\text{MCS}}$2/PIO24
17	AD7	42	A19/PIO9	67	HLDA	92	$\overline{\text{MCS}}$3/$\overline{\text{RFSH}}$/PIO25
18	AO15	43	A18/PIO8	68	HOLD	93	GND
19	S6/$\overline{\text{CLKSEL}}$1/PIO29	44	V_{CC}	69	SRDY/PIO6	94	$\overline{\text{RES}}$
20	$\overline{\text{UZI}}$/$\overline{\text{CLKSEL}}$2/PIO26	45	A17/PIO7	70	NMI	95	TMRIN1/PIO0
21	TXD/PIO27	46	A16	71	DT/$\overline{\text{R}}$/PIO4	96	TMROUT1/PIO1
22	RXD/PIO28	47	A15	72	$\overline{\text{DEN}}$/PIO5	97	TMROUT0/PIO10
23	SDATA/PIO21	48	A14	73	$\overline{\text{MCS}}$0/PIO14	98	TMRIN0/PIO11
24	SDEN1/PIO23	49	A13	74	$\overline{\text{MCS}}$1/PIO15	99	DRQ1/PIO13
25	SDEN0/PIO22	50	A12	75	INT4/PIO30	100	DRQ0/PIO12

TQFP PIN ASSIGNMENTS—Am188™ER MICROCONTROLLER
(Sorted by Pin Name)

Pin Name	No.	Pin Name	No.	Pin Name	No.	Pin Name	No.
A0	63	AD5	11	GND	93	$\overline{S}$1/$\overline{IMDIS}$	33
A1	62	AD6	14	HLDA	67	$\overline{S}$2	32
A2	60	AD7	17	HOLD	68	S6/$\overline{CLKSEL}$1/PIO29	19
A3	59	ALE	30	INT0	79	SCLK/PIO20	26
A4	58	AO8	2	INT1/$\overline{SELECT}$	78	SDATA/PIO21	23
A5	57	AO9	4	INT2/$\overline{INTA}$0/PIO31	77	SDEN0/PIO22	25
A6	56	AO10	6	INT3/$\overline{INTA}$1/IRQ	76	SDEN1/PIO23	24
A7	55	AO11	8	INT4/PIO30	75	SRDY/PIO6	69
A8	54	AO12	10	$\overline{LCS}$/$\overline{ONCE}$0	81	TMRIN0/PIO11	98
A9	53	AO13	13	$\overline{MCS}$0/PIO14	73	TMRIN1/PIO0	95
A10	52	AO14	16	$\overline{MCS}$1/PIO15	74	TMROUT0/PIO10	97
A11	51	AO15	18	$\overline{MCS}$2/PIO24	91	TMROUT1/PIO1	96
A12	50	ARDY	31	$\overline{MCS}$3/$\overline{RFSH}$/PIO25	92	TXD/PIO27	21
A13	49	CLKOUTA	39	NMI	70	$\overline{UCS}$/$\overline{ONCE}$1	80
A14	48	CLKOUTB	40	$\overline{PCS}$0/PIO16	89	$\overline{UZI}$/$\overline{CLKSEL}$2	20
A15	47	$\overline{DEN}$/PIO5	72	$\overline{PCS}$1/PIO17	88	V_{CC}	15
A16	46	DRQ0/PIO12	100	$\overline{PCS}$2/PIO18	86	V_{CC}	38
A17/PIO7	45	DRQ1/PIO13	99	$\overline{PCS}$3/PIO19	85	V_{CC}	44
A18/PIO8	43	DT/$\overline{R}$/PIO4	71	$\overline{PCS}$5/A1/PIO3	83	V_{CC}	61
A19/PIO9	42	GND	12	$\overline{PCS}$6/A2/PIO2	82	V_{CC}	84
AD0	1	GND	35	$\overline{RD}$	29	V_{CC}	90
AD1	3	GND	41	$\overline{RES}$	94	$\overline{WB}$	66
AD2	5	GND	64	$\overline{RFSH}$2/$\overline{ADEN}$	27	$\overline{WR}$	28
AD3	7	GND	65	RXD/PIO28	22	X1	36
AD4	9	GND	87	$\overline{S}$0/$\overline{SREN}$	34	X2	37

PQFP CONNECTION DIAGRAM AND PINOUTS—Am186™ER MICROCONTROLLER

Top Side View—100-Pin Plastic Quad Flat Pack (PQFP)



Notes:
Pin 1 is marked for orientation.

PQFP PIN ASSIGNMENTS—Am186™ER MICROCONTROLLER
(Sorted by Pin Number)

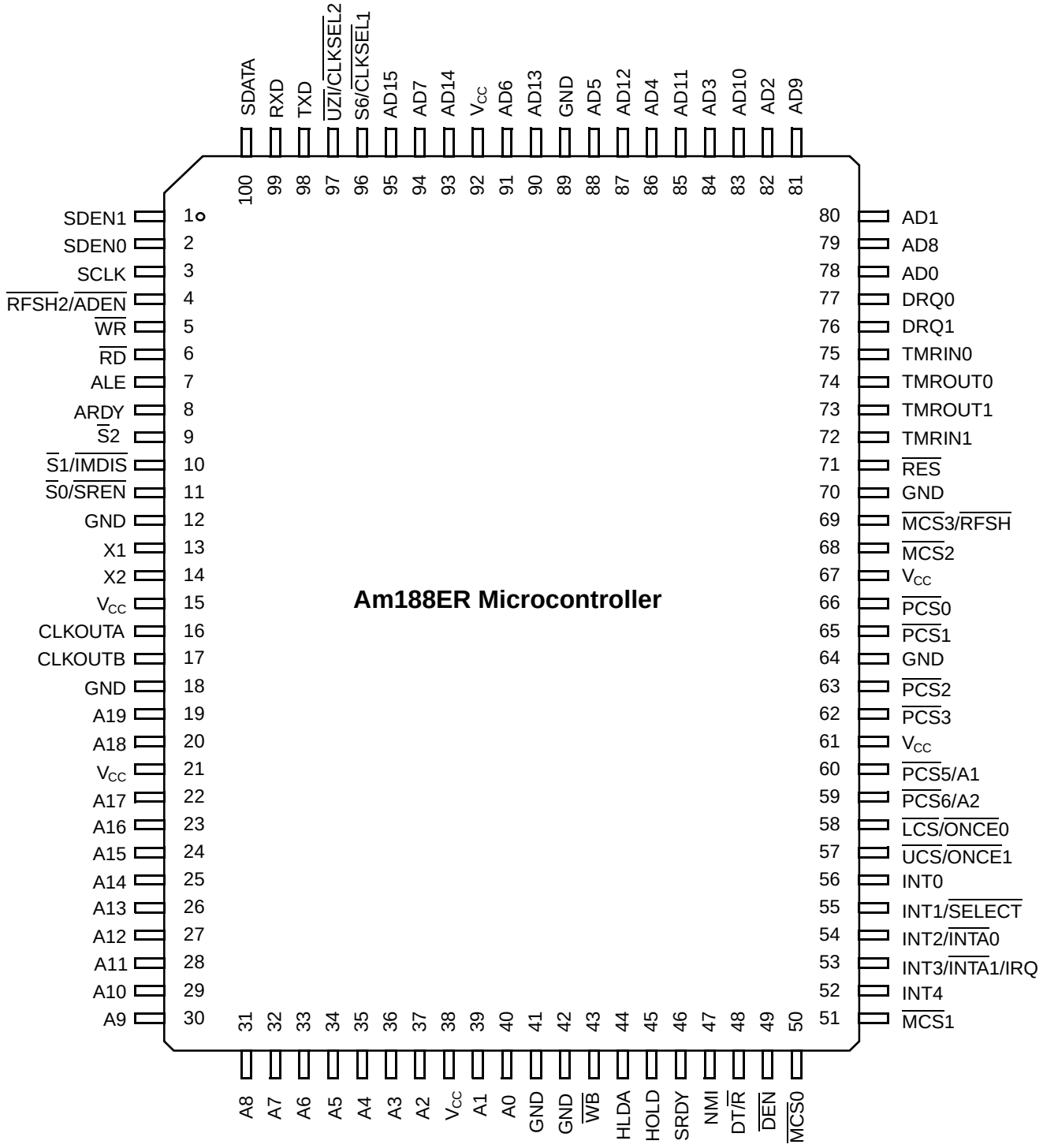
Pin No.	Name	Pin No.	Name	Pin No.	Name	Pin No.	Name
1	SDEN1/PIO23	26	A13	51	$\overline{\text{MCS}}$1/PIO15	76	DRQ1/PIO13
2	SDEN0/PIO22	27	A12	52	INT4/PIO30	77	DRQ0/PIO12
3	SCLK/PIO20	28	A11	53	INT3/$\overline{\text{INTA}}$1/IRQ	78	AD0
4	$\overline{\text{BHE}}$/$\overline{\text{ADEN}}$	29	A10	54	INT2/$\overline{\text{INTA}}$0/PIO31	79	AD8
5	$\overline{\text{WR}}$	30	A9	55	INT1/$\overline{\text{SELECT}}$	80	AD1
6	$\overline{\text{RD}}$	31	A8	56	INT0	81	AD9
7	ALE	32	A7	57	$\overline{\text{UCS}}$/$\overline{\text{ONCE}}$1	82	AD2
8	ARDY	33	A6	58	$\overline{\text{LCS}}$/$\overline{\text{ONCE}}$0	83	AD10
9	$\overline{\text{S}}$2	34	A5	59	$\overline{\text{PCS}}$6/A2/PIO2	84	AD3
10	$\overline{\text{S}}$1/$\overline{\text{IMDIS}}$	35	A4	60	$\overline{\text{PCS}}$5/A1/PIO3	85	AD11
11	$\overline{\text{S}}$0/$\overline{\text{SREN}}$	36	A3	61	V_{CC}	86	AD4
12	GND	37	A2	62	$\overline{\text{PCS}}$3/PIO19	87	AD12
13	X1	38	V_{CC}	63	$\overline{\text{PCS}}$2/PIO18	88	AD5
14	X2	39	A1	64	GND	89	GND
15	V_{CC}	40	A0	65	$\overline{\text{PCS}}$1/PIO17	90	AD13
16	CLKOUTA	41	GND	66	$\overline{\text{PCS}}$0/PIO16	91	AD6
17	CLKOUTB	42	$\overline{\text{WHB}}$	67	V_{CC}	92	V_{CC}
18	GND	43	$\overline{\text{WLB}}$	68	$\overline{\text{MCS}}$2/PIO24	93	AD14
19	A19/PIO9	44	HLDA	69	$\overline{\text{MCS}}$3/$\overline{\text{RFSH}}$/PIO25	94	AD7
20	A18/PIO8	45	HOLD	70	GND	95	AD15
21	V_{CC}	46	SRDY/PIO6	71	$\overline{\text{RES}}$	96	S6/$\overline{\text{CLKSEL}}$1/PIO29
22	A17/PIO7	47	NMI	72	TMRIN1/PIO0	97	$\overline{\text{UZI}}$/$\overline{\text{CLKSEL}}$2/PIO26
23	A16	48	DT/$\overline{\text{R}}$/PIO4	73	TMROUT1/PIO1	98	TXD/PIO27
24	A15	49	$\overline{\text{DEN}}$/PIO5	74	TMROUT0/PIO10	99	RXD/PIO28
25	A14	50	$\overline{\text{MCS}}$0/PIO14	75	TMRIN0/PIO11	100	SDATA/PIO21

PQFP PIN ASSIGNMENTS—Am186™ER MICROCONTROLLER
(Sorted by Pin Name)

Pin Name	No.	Pin Name	No.	Pin Name	No.	Pin Name	No.
A0	40	AD5	88	GND	89	$\overline{S2}$	9
A1	39	AD6	91	HLDA	44	S6/$\overline{CLKSEL1}$/PIO29	96
A2	37	AD7	94	HOLD	45	SCLK/PIO20	3
A3	36	AD8	79	INT0	56	SDATA/PIO21	100
A4	35	AD9	81	INT1/$\overline{SELECT}$	55	SDEN0/PIO22	2
A5	34	AD10	83	INT2/$\overline{INTA}$0/PIO31	54	SDEN1/PIO23	1
A6	33	AD11	85	INT3/$\overline{INTA}$1/IRQ	53	SRDY/PIO6	46
A7	32	AD12	87	INT4/PIO30	52	TMRIN0/PIO11	75
A8	31	AD13	90	$\overline{LCS}$/$\overline{ONCE}$0	58	TMRIN1/PIO0	72
A9	30	AD14	93	$\overline{MCS}$0/PIO14	50	TMROUT0/PIO10	74
A10	29	AD15	95	$\overline{MCS}$1/PIO15	51	TMROUT1/PIO1	73
A11	28	ALE	7	$\overline{MCS}$2/PIO24	68	TXD/PIO27	98
A12	27	ARDY	8	$\overline{MCS}$3/$\overline{RFSH}$/PIO25	69	$\overline{UCS}$/$\overline{ONCE}$1	57
A13	26	$\overline{BHE}$/$\overline{ADEN}$	4	NMI	47	$\overline{UZI}$/$\overline{CLKSEL}$2/PIO26	97
A14	25	CLKOUTA	16	$\overline{PCS}$0/PIO16	66	V_{CC}	15
A15	24	CLKOUTB	17	$\overline{PCS}$1/PIO17	65	V_{CC}	21
A16	23	$\overline{DEN}$/PIO5	49	$\overline{PCS}$2/PIO18	63	V_{CC}	38
A17/PIO7	22	DRQ0/PIO12	77	$\overline{PCS}$3/PIO19	62	V_{CC}	61
A18/PIO8	20	DRQ1/PIO13	76	$\overline{PCS}$5/A1/PIO3	60	V_{CC}	67
A19/PIO9	19	DT/$\overline{R}$/PIO4	48	$\overline{PCS}$6/A2/PIO2	59	V_{CC}	92
AD0	78	GND	12	$\overline{RD}$	6	$\overline{WHB}$	42
AD1	80	GND	18	$\overline{RES}$	71	$\overline{WLB}$	43
AD2	82	GND	41	RXD/PIO28	99	$\overline{WR}$	5
AD3	84	GND	64	$\overline{S0}$/$\overline{SREN}$	11	X1	13
AD4	86	GND	70	$\overline{S1}$/$\overline{IMDIS}$	10	X2	14

PQFP CONNECTION DIAGRAM AND PINOUTS—Am188™ER MICROCONTROLLER

Top Side View—100-Pin Plastic Quad Flat Pack (PQFP)



Notes:
Pin 1 is marked for orientation.

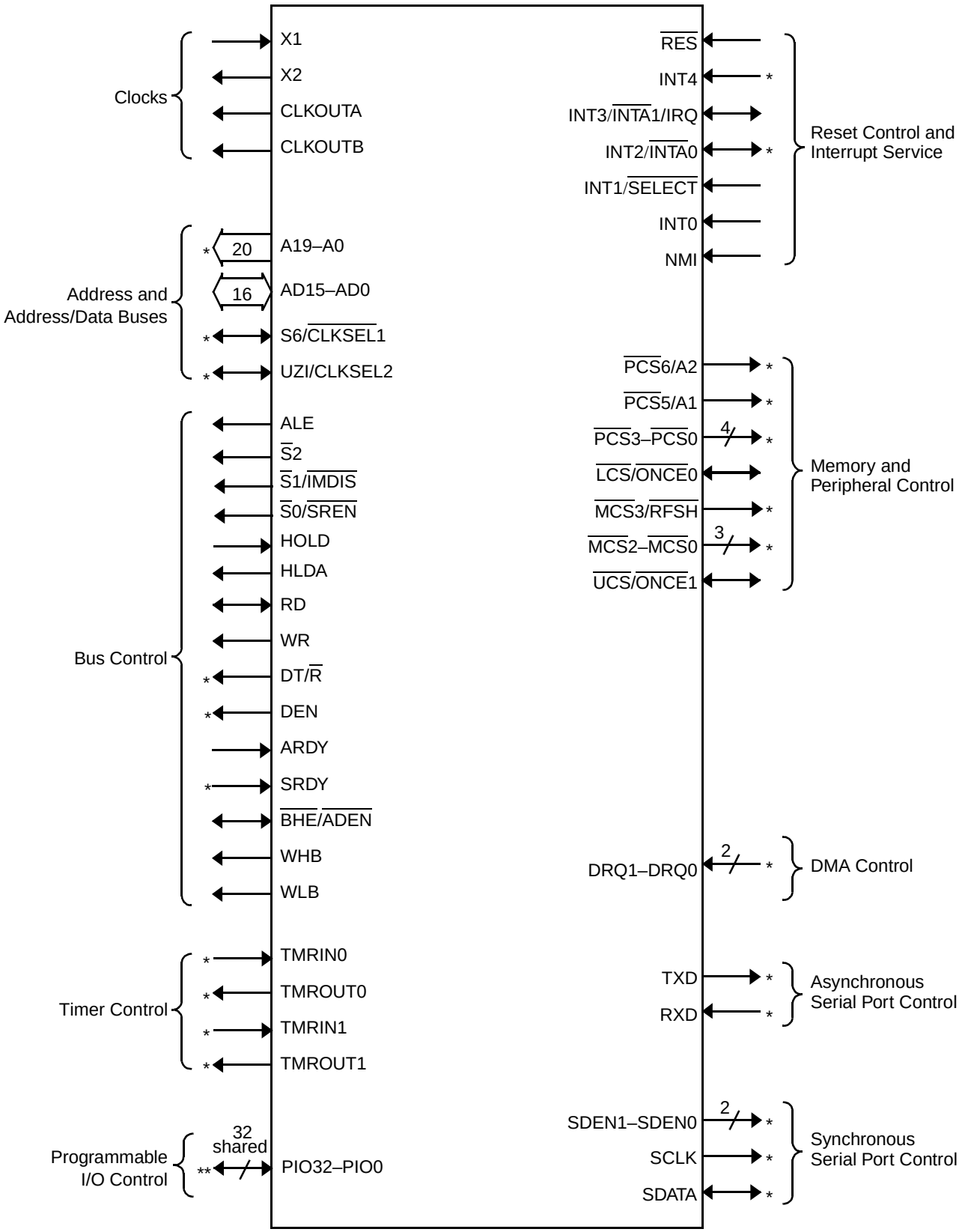
PQFP PIN ASSIGNMENTS—Am188™ER MICROCONTROLLER
(Sorted by Pin Number)

Pin No.	Name	Pin No.	Name	Pin No.	Name	Pin No.	Name
1	SDEN1/PIO23	26	A13	51	$\overline{\text{MCS}}$1/PIO15	76	DRQ1/PIO13
2	SDEN0/PIO22	27	A12	52	INT4/PIO30	77	DRQ0/PIO12
3	SCLK/PIO20	28	A11	53	INT3/$\overline{\text{INTA}}$1/IRQ	78	AD0
4	$\overline{\text{RFSH}}$2/$\overline{\text{ADEN}}$	29	A10	54	INT2/$\overline{\text{INTA}}$0/PIO31	79	AO8
5	$\overline{\text{WR}}$	30	A9	55	INT1/$\overline{\text{SELECT}}$	80	AD1
6	$\overline{\text{RD}}$	31	A8	56	INT0	81	AO9
7	ALE	32	A7	57	$\overline{\text{UCS}}$/$\overline{\text{ONCE}}$1	82	AD2
8	ARDY	33	A6	58	$\overline{\text{LCS}}$/$\overline{\text{ONCE}}$0	83	AO10
9	$\overline{\text{S}}$2	34	A5	59	$\overline{\text{PCS}}$6/A2/PIO2	84	AD3
10	$\overline{\text{S}}$1/$\overline{\text{IMDIS}}$	35	A4	60	$\overline{\text{PCS}}$5/A1/PIO3	85	AO11
11	$\overline{\text{S}}$0/$\overline{\text{SREN}}$	36	A3	61	V_{CC}	86	AD4
12	GND	37	A2	62	$\overline{\text{PCS}}$3/PIO19	87	AO12
13	X1	38	V_{CC}	63	$\overline{\text{PCS}}$2/PIO18	88	AD5
14	X2	39	A1	64	GND	89	GND
15	V_{CC}	40	A0	65	$\overline{\text{PCS}}$1/PIO17	90	AO13
16	CLKOUTA	41	GND	66	$\overline{\text{PCS}}$0/PIO16	91	AD6
17	CLKOUTB	42	GND	67	V_{CC}	92	V_{CC}
18	GND	43	$\overline{\text{WB}}$	68	$\overline{\text{MCS}}$2/PIO24	93	AO14
19	A19/PIO9	44	HLDA	69	$\overline{\text{MCS}}$3/$\overline{\text{RFSH}}$/PIO25	94	AD7
20	A18/PIO8	45	HOLD	70	GND	95	AO15
21	V_{CC}	46	SRDY/PIO6	71	$\overline{\text{RES}}$	96	S6/$\overline{\text{CLKSEL}}$1/PIO29
22	A17/PIO7	47	NMI	72	TMRIN1/PIO0	97	$\overline{\text{UZI}}$/$\overline{\text{CLKSEL}}$2/PIO26
23	A16	48	DT/$\overline{\text{R}}$/PIO4	73	TMROUT1/PIO1	98	TXD/PIO27
24	A15	49	$\overline{\text{DEN}}$/PIO5	74	TMROUT0/PIO10	99	RXD/PIO28
25	A14	50	$\overline{\text{MCS}}$0/PIO14	75	TMRIN0/PIO11	100	SDATA/PIO21

PQFP PIN ASSIGNMENTS—Am188™ER MICROCONTROLLER
(Sorted by Pin Name)

Pin Name	No.	Pin Name	No.	Pin Name	No.	Pin Name	No.
A0	40	AD5	88	GND	89	$\overline{S1}/\overline{IMDIS}$	10
A1	39	AD6	91	HLDA	44	$\overline{S2}$	9
A2	37	AD7	94	HOLD	45	S6/$\overline{CLKSEL1}$/PIO29	96
A3	36	ALE	7	INT0	56	SCLK/PIO20	3
A4	35	AO8	79	INT1/$\overline{SELECT}$	55	SDATA/PIO21	100
A5	34	AO9	81	INT2/$\overline{INTA0}$/PIO31	54	SDEN0/PIO22	2
A6	33	AO10	83	INT3/$\overline{INTA1}$/IRQ	53	SDEN1/PIO23	1
A7	32	AO11	85	INT4/PIO30	52	SRDY/PIO6	46
A8	31	AO12	87	$\overline{LCS}/\overline{ONCE0}$	58	TMRIN0/PIO11	75
A9	30	AO13	90	$\overline{MCS0}$/PIO14	50	TMRIN1/PIO0	72
A10	29	AO14	93	$\overline{MCS1}$/PIO15	51	TMROUT0/PIO10	74
A11	28	AO15	95	$\overline{MCS2}$/PIO24	68	TMROUT1/PIO1	73
A12	27	ARDY	8	$\overline{MCS3}/\overline{RFSH}$/PIO25	69	TXD/PIO27	98
A13	26	CLKOUTA	16	NMI	47	$\overline{UCS}/\overline{ONCE1}$	57
A14	25	CLKOUTB	17	$\overline{PCS0}$/PIO16	66	$\overline{UZI}/\overline{CLKSEL2}$/PIO26	97
A15	24	$\overline{DEN}$/PIO5	49	$\overline{PCS1}$/PIO17	65	V_{CC}	15
A16	23	DRQ0/PIO12	77	$\overline{PCS2}$/PIO18	63	V_{CC}	21
A17/PIO7	22	DRQ1/PIO13	76	$\overline{PCS3}$/PIO19	62	V_{CC}	38
A18/PIO8	20	DT/$\overline{R}$/PIO4	48	$\overline{PCS5}$/A1/PIO3	60	V_{CC}	61
A19/PIO9	19	GND	12	$\overline{PCS6}$/A2/PIO2	59	V_{CC}	67
AD0	78	GND	18	$\overline{RD}$	6	V_{CC}	92
AD1	80	GND	41	$\overline{RES}$	71	$\overline{WB}$	43
AD2	82	GND	42	$\overline{RFSH2}/\overline{ADEN}$	4	$\overline{WR}$	5
AD3	84	GND	64	RXD/PIO28	99	X1	13
AD4	86	GND	70	$\overline{S0}/\overline{SREN}$	11	X2	14

LOGIC SYMBOL—Am186™ER MICROCONTROLLER

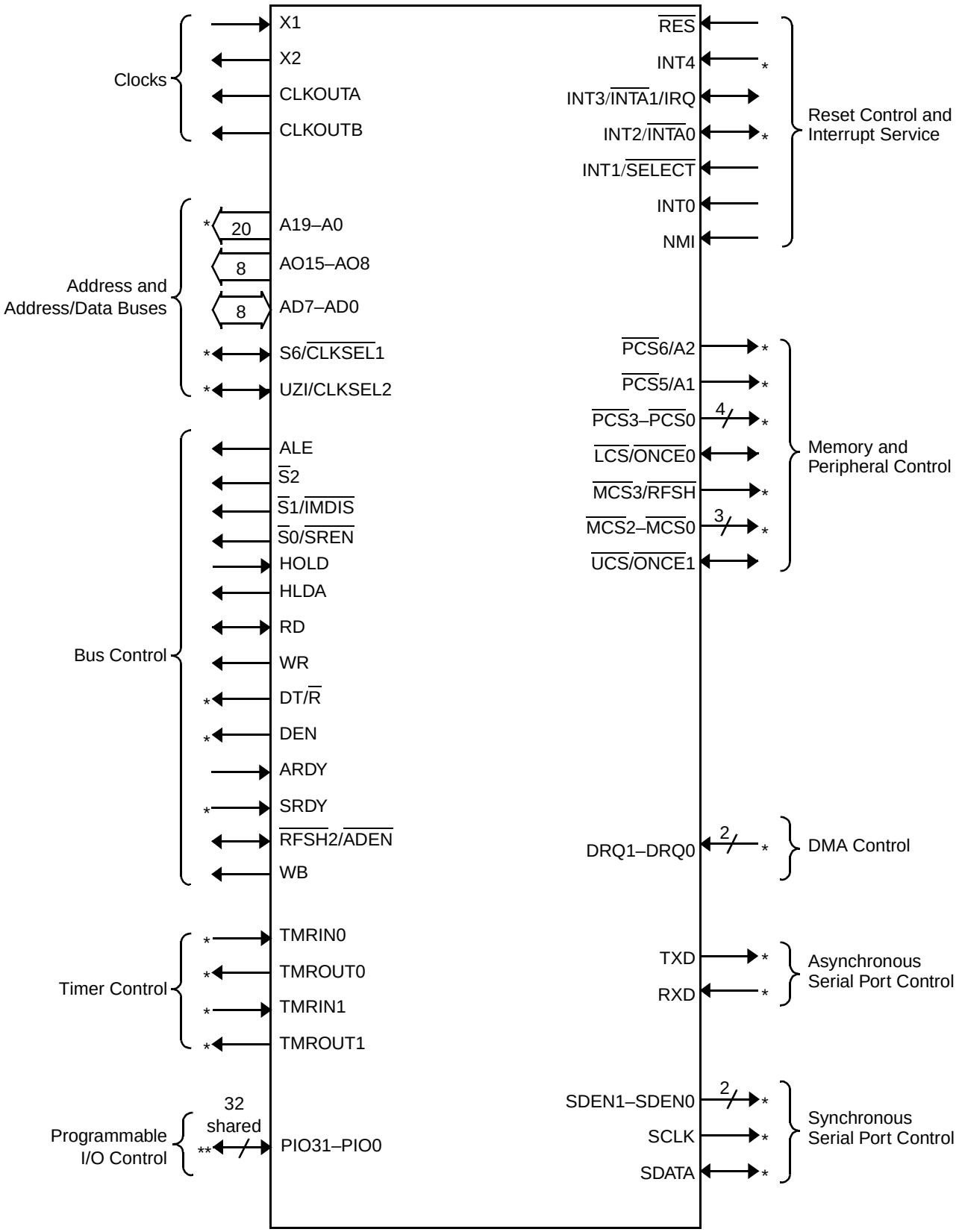


Notes:

** These signals are the normal function of a pin that can be used as a PIO. See the pin descriptions beginning on page 30 and Table 3 on page 36 for information on shared function.*

*** All PIO signals are shared with other physical pins.*

LOGIC SYMBOL—Am188™ER MICROCONTROLLER



Notes:

** These signals are the normal function of a pin that can be used as a PIO. See the pin descriptions beginning on page 30 and Table 3 on page 36 for information on shared function.*

*** All PIO signals are shared with other physical pins.*

PIN DESCRIPTIONS

Pins Used by Emulators

The following pins are used by emulators: A19–A0, AO15–AO8, AD7–AD0, ALE, BHE/ADEN (on the Am186ER microcontroller), CLKOUTA, RFSH2/ADEN (on the Am188ER microcontroller), RD, S2, S1/IMDIS, S0/SREN, S6/CLKSEL1, and UZI/CLKSEL2.

Emulators require that S6/CLKSEL1 and UZI/CLKSEL2 be configured in their normal functionality, that is, as S6 and UZI. If BHE/ADEN (on the Am186ER microcontroller) or RFSH2/ADEN (on the Am188ER microcontroller) is held Low during the rising edge of RES, S6 and UZI are configured in their normal functionality and cannot be programmed as PIOs.

A19–A0 (A19/PIO9, A18/PIO8, A17/PIO7)

Address Bus (output, three-state, synchronous)

These pins supply nonmultiplexed memory or I/O addresses to the system one-half of a CLKOUTA period earlier than the multiplexed address and data bus (AD15–AD0 on the Am186ER microcontroller or AO15–AO8 and AD7–AD0 on the Am188ER microcontroller). During a bus hold or reset condition, the address bus is in a high-impedance state.

AD7–AD0

Address and Data Bus (input/output, three-state, synchronous, level-sensitive)

These time-multiplexed pins supply partial memory or I/O addresses, as well as data, to the system. AD7–AD0 supply the low-order 8 bits of an address to the system during the first period of a bus cycle (t_1). On a write, these pins supply data to the system during the remaining periods of that cycle (t_2, t_3, and t_4). On a read, these pins latch data at the end of t_3.

Also, if S0/SREN (show read enable) was pulled Low during reset or if the SR bit is set in the Internal Memory Chip Select (IMCS) Register, these pins supply the data read from internal memory during t_3 and t_4.

On the Am186ER microcontroller, AD7–AD0 combine with AD15–AD8 to form a complete multiplexed address and 16-bit data bus.

On the Am188ER microcontroller, AD7–AD0 combine with AO15–AO8 to form a complete multiplexed address bus while AD7–AD0 is the 8-bit data bus.

The address phase of these pins can be disabled. See the ADEN description with the BHE/ADEN pin. When WLB is negated, these pins are three-stated during t_2, t_3, and t_4.

During a bus hold or reset condition, the address and data bus are in a high-impedance state.

During a power-on reset, the address and data bus pins (AD15–AD0 for the Am186ER microcontroller, AO15–AO8 and AD7–AD0 for the Am188ER microcontroller) can also be used to load system configuration information into the internal reset configuration register. The system information is latched on the rising edge of RES.

AD15–AD8 (Am186™ER Microcontroller)

Address and Data Bus (input/output, three-state, synchronous, level-sensitive)

These time-multiplexed pins supply partial memory or I/O addresses, as well as data, to the system. AD15–AD8 supply the high-order 8 bits of an address to the system during the first period of a bus cycle (t_1). On a write, these pins supply data to the system during the remaining periods of that cycle (t_2, t_3, and t_4). On a read, these pins latch data at the end of t_3.

Also, if S0/SREN (show read enable) was pulled Low during reset or if the SR bit is set in the Internal Memory Chip Select (IMCS) Register, these pins supply the data read from internal memory during t_3 and t_4.

On the Am186ER microcontroller, AD15–AD8 combine with AD7–AD0 to form a complete multiplexed address and 16-bit data bus.

The address phase of these pins can be disabled. See the ADEN description with the BHE/ADEN pin. When WHB is negated, these pins are three-stated during t_2, t_3, and t_4.

During a bus hold or reset condition, the address and data bus is in a high-impedance state.

During a power-on reset, the address and data bus pins (AD15–AD0 for the Am186ER microcontroller, AO15–AO8 and AD7–AD0 for the Am188ER microcontroller) can also be used to load system configuration information into the internal reset configuration register. The system information is latched on the rising edge of RES.

AO15–AO8 (Am188™ER Microcontroller)

Address-Only Bus (output, three-state, synchronous, level-sensitive)

On the Am188ER microcontroller, the address-only bus (AO15–AO8) contains valid high-order address bits from bus cycles t_1–t_4. These outputs are three-stated during a bus hold or reset.

On the Am188ER microcontroller, AO15–AO8 combine with AD7–AD0 to form a complete multiplexed address bus while AD7–AD0 is the 8-bit data bus.

On the Am188ER microcontroller during a power-on reset, the AO15–AO8 and AD7–AD0 pins can also be used to load system configuration information into an internal register for later use.

ALE

Address Latch Enable (output, synchronous)

This pin indicates to the system that an address appears on the address and data bus (AD15–AD0 for the Am186ER microcontroller or AO15–AO8 and AD7–AD0 for the Am188ER microcontroller). The address is guaranteed valid on the trailing edge of ALE. This pin is three-stated during ONCE mode.

ARDY

Asynchronous Ready (input, asynchronous, level-sensitive)

This pin indicates to the microcontroller that the addressed memory space or I/O device will complete a data transfer. The ARDY pin accepts a rising edge that is asynchronous to CLKOUTA and is active High. The falling edge of ARDY must be synchronized to CLKOUTA. To always assert the ready condition to the microcontroller, tie ARDY High. If the system does not use ARDY, tie the pin Low to yield control to SRDY.

BHE/ADEN (Am186™ER Microcontroller Only)

Bus High Enable (three-state, output, synchronous) Address Enable (input, internal pullup)

BHE—During a memory access, this pin and the least-significant address bit (AD0 or A0) indicate to the system which bytes of the data bus (upper, lower, or both) participate in a bus cycle. The BHE/ADEN and AD0 pins are encoded as shown in Table 2.

BHE is asserted during t_1 and remains asserted through t_3 and t_W. BHE does not need to be latched. BHE is three-stated during bus hold and reset conditions.

On the Am186ER microcontroller, WLB and WHB implement the functionality of BHE and AD0 for high and low byte write enables.

Table 2. Data Byte Encoding

BHE	AD0	Type of Bus Cycle
0	0	Word Transfer
0	1	High Byte Transfer (Bits 15–8)
1	0	Low Byte Transfer (Bits 7–0)
1	1	Refresh

BHE/ADEN also signals DRAM refresh cycles when using the multiplexed address and data (AD) bus. A refresh cycle is indicated when both BHE/ADEN and AD0 are High. During refresh cycles, the A bus and the AD bus are not guaranteed to provide the same address during the address phase of the AD bus cycle. For this reason, the A0 signal cannot be used in place of the AD0 signal to determine refresh cycles. PSRAM refreshes also provide an additional RFSH signal (see the MCS3/RFSH pin description on page 33).

ADEN—If BHE/ADEN is held High or left floating during power-on reset, the address portion of the AD bus (AD15–AD0) is enabled or disabled during LCS and UCS bus cycles based on the DA bit in the LMCS and UMCS registers. If the DA bit is set, the memory address is accessed on the A19–A0 pins. This mode of operation reduces power consumption. For more information, see the Bus Operation section on page 41. There is a weak internal pullup resistor on BHE/ADEN so no external pullup is required.

If BHE/ADEN is held Low on power-on reset, the AD bus drives both addresses and data. Changing the DA bit of the LMCS and UMCS registers will have no effect. (S6 and UZI also assume their normal functionality in this instance. The PIO Mode and Direction registers cannot reconfigure these pins as PIOs. See Table 3 on page 36.) The pin is sampled within three crystal clock cycles after the rising edge of RES. BHE/ADEN is three-stated during bus holds and ONCE mode.

Note: *Once the above modes are set, they can be changed only by resetting the processor.*

CLKOUTA

Clock Output A (output, synchronous)

This pin supplies the internal clock to the system. Depending on the value of the Power-Save Control Register (PDCON), CLKOUTA operates at either the CPU fundamental frequency (which varies with the divide by two, times one, and times four clocking modes), the power-save frequency, or is three-stated (see Figure 10 on page 48). CLKOUTA remains active during reset and bus hold conditions.

CLKOUTB

Clock Output B (output, synchronous)

This pin supplies a clock to the system. Depending on the value of the Power-Save Control Register (PDCON), CLKOUTB operates at either the CPU fundamental frequency (which varies with the divide by two, times one, and times four clocking modes), the power-save frequency, or is three-stated (see Figure 10 on page 48). CLKOUTB remains active during reset and bus hold conditions.

DEN/PIO5

Data Enable (output, three-state, synchronous)

This pin supplies an output enable to an external data-bus transceiver. DEN is asserted during memory, I/O, and interrupt acknowledge cycles. DEN is deasserted when DT/R changes state. DEN is three-stated during a bus hold or reset condition.

DRQ1–DRQ0 (DRQ1/PIO13, DRQ0/PIO12)

DMA Requests (input, synchronous, level-sensitive)

These pins indicate to the microcontroller that an external device is ready for DMA channel 1 or channel 0 to perform a transfer. DRQ1–DRQ0 are level-triggered and internally synchronized.

The DRQ signals are not latched and must remain active until serviced.

DT/$\overline{R}$/PIO4

Data Transmit or Receive (output, three-state, synchronous)

This pin indicates which direction data should flow through an external data-bus transceiver. When DT/$\overline{R}$ is asserted High, the microcontroller transmits data. When this pin is deasserted Low, the microcontroller receives data. DT/$\overline{R}$ is three-stated during a bus hold or reset condition.

GND

Ground

The ground pins connect the system ground to the microcontroller.

HLDA

Bus Hold Acknowledge (output, synchronous)

When an external bus master requests control of the local bus (by asserting HOLD), the microcontroller completes the bus cycle in progress and then relinquishes control of the bus to the external bus master by asserting HLDA and floating $\overline{DEN}$, $\overline{RD}$, $\overline{WR}$, $\overline{S2}$–$\overline{S0}$, AD15–AD0, S6, A19–A0, $\overline{BHE}$, $\overline{WHB}$, $\overline{WLB}$, and DT/$\overline{R}$, and then driving the chip selects $\overline{UCS}$, $\overline{LCS}$, $\overline{MCS3}$–$\overline{MCS0}$, $\overline{PCS6}$–$\overline{PCS5}$, and $\overline{PCS3}$–$\overline{PCS0}$ High.

When the external bus master has finished using the local bus, it indicates this to the microcontroller by deasserting HOLD. The microcontroller responds by deasserting HLDA.

If the microcontroller requires access to the bus (that is, for refresh), it will deassert HLDA before the external bus master deasserts HOLD. The external bus master must be able to deassert HOLD and allow the microcontroller access to the bus. See the timing diagrams for bus hold on page 101. This pin is three-stated during ONCE mode.

HOLD

Bus Hold Request (input, synchronous, level-sensitive)

This pin indicates to the microcontroller that an external bus master needs control of the local bus. For more information, see the HLDA pin description.

The Am186ER and Am188ER microcontrollers' HOLD latency time, the time between HOLD request and HOLD acknowledge, is a function of the activity occurring in the processor when the HOLD request is received. A HOLD request is second only to DRAM or PSRAM refresh requests in priority of activity requests received by the processor. This implies that if a HOLD request is received just as a DMA transfer begins, the HOLD latency can be as great as four bus cycles. This occurs if a DMA word transfer operation is taking place (Am186ER microcontroller only) from an odd address to an odd address. This is a total of 16 clock cycles or more if wait states are required. In addition, if locked transfers are performed, the HOLD latency time is increased by the length of the locked transfer.

INT0

Maskable Interrupt Request 0 (input, asynchronous)

This pin indicates to the microcontroller that an interrupt request has occurred. If the INT0 pin is not masked, the microcontroller transfers program execution to the location specified by the INT0 vector in the microcontroller interrupt vector table.

Interrupt requests are synchronized internally and can be edge-triggered or level-triggered. To guarantee interrupt recognition, the requesting device must continue asserting INT0 until the request is acknowledged.

INT1/$\overline{SELECT}$

Maskable Interrupt Request 1 (input, asynchronous)
Slave Select (input, asynchronous)

INT1—This pin indicates to the microcontroller that an interrupt request has occurred. If INT1 is not masked, the microcontroller transfers program execution to the location specified by the INT1 vector in the microcontroller interrupt vector table.

Interrupt requests are synchronized internally and can be edge-triggered or level-triggered. To guarantee interrupt recognition, the requesting device must continue asserting INT1 until the request is acknowledged.

SELECT—When the microcontroller interrupt control unit is operating as a slave to an external master interrupt controller, this pin indicates to the microcontroller that an interrupt type appears on the address and data bus. The INT0 pin must indicate to the microcontroller that an interrupt has occurred before the $\overline{SELECT}$ pin indicates to the microcontroller that the interrupt type appears on the bus.

INT2/INTA0/PIO31

Maskable Interrupt Request 2 (input, asynchronous)
Interrupt Acknowledge 0 (output, synchronous)

INT2—This pin indicates to the microcontroller that an interrupt request has occurred. If the INT2 pin is not masked, the microcontroller transfers program execution to the location specified by the INT2 vector in the microcontroller interrupt vector table.

Interrupt requests are synchronized internally and can be edge-triggered or level-triggered. To guarantee interrupt recognition, the requesting device must continue asserting INT2 until the request is acknowledged. INT2 becomes INTA0 when INT0 is configured in cascade mode.

INTA0—When the microcontroller interrupt control unit is operating in cascade mode, this pin indicates to the system that the microcontroller needs an interrupt type to process the interrupt request on INT0. The peripheral issuing the interrupt request must provide the microcontroller with the corresponding interrupt type.

INT3/INTA1/IRQ

Maskable Interrupt Request 3 (input, asynchronous)
Interrupt Acknowledge 1 (output, synchronous)
Slave Interrupt Request (output, synchronous)

INT3—This pin indicates to the microcontroller that an interrupt request has occurred. If the INT3 pin is not masked, the microcontroller then transfers program execution to the location specified by the INT3 vector in the microcontroller interrupt vector table.

Interrupt requests are synchronized internally, and can be edge-triggered or level-triggered. To guarantee interrupt recognition, the requesting device must continue asserting INT3 until the request is acknowledged. INT3 becomes INTA1 when INT1 is configured in cascade mode.

INTA1—When the microcontroller interrupt control unit is operating in cascade mode, this pin indicates to the system that the microcontroller needs an interrupt type to process the interrupt request on INT1. The peripheral issuing the interrupt request must provide the microcontroller with the corresponding interrupt type.

IRQ—When the microcontroller interrupt control unit is operating as a slave to an external master interrupt controller, this pin lets the microcontroller issue an interrupt request to the external master interrupt controller.

INT4/PIO30

Maskable Interrupt Request 4 (input, asynchronous)

This pin indicates to the microcontroller that an interrupt request has occurred. If the INT4 pin is not masked, the microcontroller then transfers program execution to the location specified by the INT4 vector in the microcontroller interrupt vector table.

Interrupt requests are synchronized internally and can be edge-triggered or level-triggered. To guarantee interrupt recognition, the requesting device must continue asserting INT4 until the request is acknowledged.

LCS/ONCE0

Lower Memory Chip Select (output, synchronous, internal pullup)
ONCE Mode Request 0 (input)

LCS—This pin indicates to the system that a memory access is in progress to the lower memory block. The size of the lower memory block is programmable up to 512 Kbyte. LCS is held High during a bus hold condition.

ONCE0—During reset, this pin and ONCE1 indicate to the microcontroller the mode in which it should operate. ONCE0 and ONCE1 are sampled on the rising edge of RES. If both pins are asserted Low, the microcontroller enters ONCE mode; otherwise, it operates normally.

In ONCE mode, all pins assume a high-impedance state and remain in that state until a subsequent reset occurs. To guarantee that the microcontroller does not inadvertently enter ONCE mode, ONCE0 has a weak internal pullup resistor that is active only during reset.

MCS3/RFSH/PIO25

Midrange Memory Chip Select 3 (output, synchronous, internal pullup)
Automatic Refresh (output, synchronous)

MCS3—This pin indicates to the system that a memory access is in progress to the fourth region of the midrange memory block. The base address and size of the midrange memory block are programmable. MCS3 is held High during a bus hold condition. In addition, this pin has a weak internal pullup resistor that is active during reset.

RFSH—This pin provides a signal timed for auto refresh to PSRAM devices. It is only enabled to function as a refresh pulse when the PSRAM mode bit is set in the LMCS Register. An active Low pulse is generated for 1.5 clock cycles with an adequate deassertion period to ensure that overall auto refresh cycle time is met.

MCS2–MCS0 (MCS2/PIO24, MCS1/PIO15, MCS0/PIO14)

Midrange Memory Chip Selects (output, synchronous, internal pullup)

These pins indicate to the system that a memory access is in progress to the corresponding region of the midrange memory block. The base address and size of the midrange memory block are programmable. MCS2–MCS0 are held High during a bus hold condition. In addition, they have weak internal pullup resistors that are active during reset. Unlike the UCS and LCS chip selects, the MCS outputs assert with the multiplexed AD address bus.

NMI

Nonmaskable Interrupt (input, synchronous, edge-sensitive)

This pin indicates to the microcontroller that an interrupt request has occurred. The NMI signal is the highest priority hardware interrupt and, unlike the INT4–INT0 pins, cannot be masked. The microcontroller always transfers program execution to the location specified by the nonmaskable interrupt vector in the microcontroller interrupt vector table when NMI is asserted.

Although NMI is the highest priority interrupt source, it does not participate in the priority resolution process of the maskable interrupts. There is no bit associated with NMI in the interrupt in-service or interrupt request registers. This means that a new NMI request can interrupt an executing NMI interrupt service routine. As with all hardware interrupts, the IF (interrupt flag) is cleared when the processor takes the interrupt, disabling the maskable interrupt sources. However, if maskable interrupts are reenabled by software in the NMI interrupt service routine, via the STI instruction for example, an NMI currently in service will not have any effect on the priority resolution of maskable interrupt requests. For this reason, it is strongly advised that the interrupt service routine for NMI does not enable the maskable interrupts.

An NMI transition from Low to High is latched and synchronized internally, and it initiates the interrupt at the next instruction boundary. To guarantee that the interrupt is recognized, the NMI pin must be asserted for at least one CLKOUTA period. Because NMI is rising edge sensitive, holding the pin High during reset has no effect on program execution.

PCS3–PCS0 (PCS3/PIO19, PCS2/PIO18, PCS1/PIO17, PCS0/PIO16)

Peripheral Chip Selects (output, synchronous)

These pins indicate to the system that a memory access is in progress to the corresponding region of the peripheral memory block (either I/O or memory address space). The base address of the peripheral memory block is programmable. PCS3–PCS0 are held High during a bus hold condition. They are also held High during reset.

PCS4 is not available on the Am186ER and Am188ER microcontrollers.

Unlike the UCS/LCS chip selects, the PCS outputs assert with the multiplexed AD address bus. Note also that each peripheral chip select asserts over a 256-byte address range, which is twice the address range covered by peripheral chip selects in the 80C186/80C188 microcontrollers.

PCS5/A1/PIO3

Peripheral Chip Select 5 (output, synchronous) Latched Address Bit 1 (output, synchronous)

PCS5—This pin indicates to the system that a memory access is in progress to the sixth region of the peripheral memory block (either I/O or memory address space). The base address of the peripheral memory block is programmable. PCS5 is held High during a bus hold condition. It is also held High during reset.

Unlike the UCS and LCS chip selects, the PCS outputs assert with the multiplexed AD address bus. Note also that each peripheral chip select asserts over a 256-byte address range, which is twice the address range covered by peripheral chip selects in the 80C186 and 80C188 microcontrollers.

A1—When the EX bit in the MCS and PCS auxiliary register is 0, this pin supplies an internally latched address bit 1 to the system. During a bus hold condition, A1 retains its previously latched value.

PCS6/A2/PIO2

Peripheral Chip Select 6 (output, synchronous) Latched Address Bit 2 (output, synchronous)

PCS6—This pin indicates to the system that a memory access is in progress to the seventh region of the peripheral memory block (either I/O or memory address space). The base address of the peripheral memory block is programmable. PCS6 is held High during a bus hold condition or reset.

Unlike the UCS and LCS chip selects, the PCS outputs assert with the multiplexed AD address bus. Note also that each peripheral chip select asserts over a 256-byte address range, which is twice the address range covered by peripheral chip selects in earlier generations of the Am186/Am188 microcontrollers.

A2—When the EX bit in the MCS and PCS auxiliary register is 0, this pin supplies an internally latched address bit 2 to the system. During a bus hold condition, A2 retains its previously latched value.

PIO31–PIO0 (Shared)

Programmable I/O Pins (input/output, asynchronous, open-drain)

The Am186ER and Am188ER microcontrollers provide 32 individually programmable I/O pins. Each PIO can be programmed with the following attributes: PIO function (enabled/disabled), direction (input/output), and weak pullup or pulldown.

On the Am186ER and Am188ER microcontrollers, the internal pullup resistor has a value of approximately 100 kohms. The internal pulldown resistor has a value of approximately 100 kohms.

The pins that are multiplexed with PIO31–PIO0 are listed in Table 3 and Table 4 on page 36.

After power-on reset, the PIO pins default to various configurations. The column titled *Power-On Reset Status* in Table 3 and Table 4 lists the defaults for the PIOs. The system initialization code must reconfigure any PIOs as required.

If PIO29 (S6/CLKSEL1) is to be used in input mode, the input device must not drive PIO29 Low during power-on reset. The pin defaults to a PIO input with pullup, so it does not need to be driven High externally.

The A19–A17 address pins default to normal operation on power-on reset, allowing the processor to correctly begin fetching instructions at the boot address FFFF0h. The DT/R, DEN, and SRDY pins also default to normal operation on power-on reset.

RD

Read Strobe (output, synchronous, three-state)

This pin indicates to the system that the microcontroller is performing a memory or I/O read cycle. RD is guaranteed not to be asserted before the address and data bus is floated during the address-to-data transition. RD is three-stated during bus holds and ONCE mode.

RES

Reset (input, asynchronous, level-sensitive)

This pin requires the microcontroller to perform a reset. When RES is asserted, the microcontroller immediately terminates its present activity, clears its internal logic, and CPU control is transferred to the reset address FFFF0h.

RES must be held Low for at least 1 ms.

RES can be asserted asynchronously to CLKOUTA because RES is synchronized internally. For proper initialization, V_{CC} must be within specifications, and CLKOUTA must be stable for more than four CLKOUTA periods during which RES is asserted.

The microcontroller begins fetching instructions approximately 6.5 CLKOUTA periods after RES is deasserted. This input is provided with a Schmitt trigger to facilitate power-on RES generation via an RC network.

RFSH2/ADEN (Am188™ER Microcontroller Only)

Refresh 2 (three-state, output, synchronous) Address Enable (input, internal pullup)

RFSH2—Asserted Low to signify a DRAM refresh bus cycle. The use of RFSH2/ADEN to signal a refresh is not valid when PSRAM mode is selected. Instead, the MCS3/RFSH signal is provided to the PSRAM. During reset, this pin is a pullup. This pin is three-stated during bus holds and ONCE mode.

ADEN—If RFSH2/ADEN is held High or left floating on power-on reset, the AD bus (AO15–AO8 and AD7–AD0) is enabled or disabled during the address portion of LCS and UCS bus cycles based on the DA bit in the LMCS and UMCS registers. If the DA bit is set, the memory address is accessed on the A19–A0 pins. This mode of operation reduces power consumption. For more information, see the Bus Operation section on page 41. There is a weak internal pullup resistor on RFSH2/ADEN so no external pullup is required.

If RFSH2/ADEN is held Low on power-on reset, the AD bus drives both addresses and data. Changing the DA bit of the LMCS and UMCS registers will have no effect. (S6 and UZI also assume their normal functionality in this instance. The PIO Mode and Direction registers cannot reconfigure these pins as PIOs. See Table 3 and Table 4 on page 36.) The pin is sampled within three crystal clock cycles after the rising edge of RES. RFSH2/ADEN is three-stated during bus holds and ONCE mode.

Note: *Once the above modes are set, they can be changed only by resetting the processor.*

RXD/PIO28

Receive Data (input, asynchronous)

This pin supplies asynchronous serial receive data from the system to the internal UART of the microcontroller.

S2

Bus Cycle Status (output, three-state, synchronous)

S2—This pin indicates to the system the type of bus cycle in progress. S2 can be used as a logical memory or I/O indicator. S2–S0 are three-stated during bus holds, hold acknowledges, and ONCE mode. During reset, these pins are pullups. The S2–S0 pins are encoded as shown in Table 5 on page 37.

Table 3. Numeric PIO Pin Assignments

PIO No.	Associated Pin	Power-On Reset Status
0	TMRIN1	Input with pullup
1	TMROUT1	Input with pulldown
2	$\overline{\text{PCS}}$6/A2	Input with pullup
3	$\overline{\text{PCS}}$5/A1	Input with pullup
4	DT/$\overline{\text{R}}$	Normal operation(3)
5	$\overline{\text{DEN}}$	Normal operation(3)
6	SRDY	Normal operation(4)
7(1)	A17	Normal operation(3)
8(1)	A18	Normal operation(3)
9(1)	A19	Normal operation(3)
10	TMROUT0	Input with pulldown
11	TMRIN0	Input with pullup
12	DRQ0	Input with pullup
13	DRQ1	Input with pullup
14	$\overline{\text{MCS}}$0	Input with pullup
15	$\overline{\text{MCS}}$1	Input with pullup
16	$\overline{\text{PCS}}$0	Input with pullup
17	$\overline{\text{PCS}}$1	Input with pullup
18	$\overline{\text{PCS}}$2	Input with pullup
19	$\overline{\text{PCS}}$3	Input with pullup
20	SCLK	Input with pullup
21	SDATA	Input with pullup
22	SDEN0	Input with pulldown
23	SDEN1	Input with pulldown
24	$\overline{\text{MCS}}$2	Input with pullup
25	$\overline{\text{MCS}}$3/$\overline{\text{RFSH}}$	Input with pullup
26(1,2)	$\overline{\text{UZI}}$/$\overline{\text{CLKSEL}}$2	Input with pullup
27	TXD	Input with pullup
28	RXD	Input with pullup
29(1,2)	S6/$\overline{\text{CLKSEL}}$1	Input with pullup
30	INT4	Input with pullup
31	INT2	Input with pullup

Notes:

1. *These pins are used by emulators. (Emulators also use $\overline{S2}$–$\overline{S0}$, $\overline{RES}$, NMI, CLKOUTA, $\overline{BHE}$, ALE, AD15–AD0, and A16–A0.)*
2. *These pins revert to normal operation if $\overline{BHE}$/$\overline{ADEN}$ (Am186ER microcontroller) or $\overline{RFSH2}$/$\overline{ADEN}$ (Am188ER microcontroller) is held Low during power-on reset.*
3. *When used as a PIO, input with pullup option available.*
4. *When used as a PIO, input with pulldown option available.*

Table 4. Alphabetic PIO Pin Assignments

Associated Pin	PIO No.	Power-On Reset Status
A17(1)	7	Normal operation(3)
A18(1)	8	Normal operation(3)
A19(1)	9	Normal operation(3)
DEN	5	Normal operation(3)
DRQ0	12	Input with pullup
DRQ1	13	Input with pullup
DT/$\overline{\text{R}}$	4	Normal operation(3)
INT2	31	Input with pullup
INT4	30	Input with pullup
$\overline{\text{MCS}}$0	14	Input with pullup
$\overline{\text{MCS}}$1	15	Input with pullup
$\overline{\text{MCS}}$2	24	Input with pullup
$\overline{\text{MCS}}$3/$\overline{\text{RFSH}}$	25	Input with pullup
$\overline{\text{PCS}}$0	16	Input with pullup
$\overline{\text{PCS}}$1	17	Input with pullup
$\overline{\text{PCS}}$2	18	Input with pullup
$\overline{\text{PCS}}$3	19	Input with pullup
$\overline{\text{PCS}}$5/A1	3	Input with pullup
$\overline{\text{PCS}}$6/A2	2	Input with pullup
RXD	28	Input with pullup
S6/$\overline{\text{CLKSEL}}$1(1,2)	29	Input with pullup
SCLK	20	Input with pullup
SDATA	21	Input with pullup
SDEN0	22	Input with pulldown
SDEN1	23	Input with pulldown
SRDY	6	Normal operation(4)
TMRIN0	11	Input with pullup
TMRIN1	0	Input with pullup
TMROUT0	10	Input with pulldown
TMROUT1	1	Input with pulldown
TXD	27	Input with pullup
$\overline{\text{UZI}}$/$\overline{\text{CLKSEL}}$2(1,2)	26	Input with pullup

Notes:

1. *These pins are used by emulators. (Emulators also use $\overline{S2}$–$\overline{S0}$, $\overline{RES}$, NMI, CLKOUTA, $\overline{BHE}$, ALE, AD15–AD0, and A16–A0.)*
2. *These pins revert to normal operation if $\overline{BHE}$/$\overline{ADEN}$ (Am186ER microcontroller) or $\overline{RFSH2}$/$\overline{ADEN}$ (Am188ER microcontroller) is held Low during power-on reset.*
3. *When used as a PIO, input with pullup option available.*
4. *When used as a PIO, input with pulldown option available.*

$\overline{S1}$/$\overline{IMDIS}$

Bus Cycle Status (output, three-state, synchronous)
Internal Memory Disable (input, internal pullup)

$\overline{S1}$—This pin indicates to the system the type of bus cycle in progress. $\overline{S1}$ can be used as a data transmit or receive indicator. $\overline{S2}$–$\overline{S0}$ are three-stated during bus holds, hold acknowledges, and ONCE mode. During reset, these pins are pullups. The $\overline{S2}$–$\overline{S0}$ pins are encoded as shown in Table 5.

$\overline{IMDIS}$—If asserted during reset, this pin disables internal memory. Internal memory disable mode is provided for emulation and debugging purposes.

$\overline{S0}$/$\overline{SREN}$

Bus Cycle Status (output, three-state, synchronous)

Show Read Enable (input, internal pullup)

S0—This pin indicates to the system the type of bus cycle in progress. $\overline{S2}$–$\overline{S0}$ are three-stated during bus holds, hold acknowledges, and ONCE mode. During reset, these pins are pullups. The $\overline{S2}$–$\overline{S0}$ pins are encoded as shown in Table 5.

$\overline{SREN}$—If asserted during reset, this pin enables data read from internal memory to be shown/driven on the AD15–AD0 bus. Note that if a byte read is being shown, the unused byte will also be driven on the AD15–AD0 bus.This mode is provided for emulation and debugging purposes.

Table 5. Bus Cycle Encoding

$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	Bus Cycle
0	0	0	Interrupt acknowledge
0	0	1	Read data from I/O
0	1	0	Write data to I/O
0	1	1	Halt
1	0	0	Instruction fetch
1	0	1	Read data from memory
1	1	0	Write data to memory
1	1	1	None (passive)

S6/$\overline{CLKSEL1}$/PIO29

Bus Cycle Status Bit 6 (output, synchronous)
Clock Select 1 (input, internal pullup)

S6—During the second and remaining periods of a cycle (t_2, t_3, and t_4), this pin is asserted High to indicate a DMA-initiated bus cycle. During a bus hold or reset condition, S6 is three-stated.

$\overline{CLKSEL1}$—The clocking mode of the Am186ER and Am188ER microcontrollers is controlled by UZI/CLKSEL2/PIO26 and S6/$\overline{CLKSEL1}$/PIO29. Both CLKSEL2 and $\overline{CLKSEL1}$ are held High during power-on reset because of an internal pullup resistor. This is the default clocking mode—Times Four. If $\overline{CLKSEL1}$ is held Low during power-on reset, the chip enters the Divide by Two clocking mode where the fundamental clock is derived by dividing the external clock input by 2. If Divide by Two mode is selected, the PLL is disabled. This pin is latched within three crystal clock cycles after the rising edge of $\overline{RES}$. Refer to Reset Waveforms on page 100 and Signals Related to Reset Waveforms on page 100 to determine signal hold times. See Table 6 on page 39 for more information on the clocking modes.

If S6 is used as PIO29 in input mode, the device driving PIO29 must not drive the pin Low during power-on reset. S6/$\overline{CLKSEL1}$/PIO29 defaults to a PIO input with pullup, so the pin does not need to be driven High externally.

SCLK/PIO20

Serial Clock (output, synchronous)

This pin supplies the synchronous serial interface (SSI) clock to a slave device, allowing transmit and receive operations to be synchronized between the microcontroller and the slave. SCLK is derived from the microcontroller internal clock and then divided by 2, 4, 8, or 16 depending on register settings.

An access to any of the SSR or SSD registers activates SCLK for eight SCLK cycles (see Figure 14 and Figure 15 on page 58). When SCLK is inactive, it is held High by the microcontroller. SCLK is three-stated during ONCE mode.

SDATA/PIO21

Serial Data (input/output, synchronous)

This pin transmits and receives synchronous serial interface (SSI) data to and from a slave device. When SDATA is inactive, a weak keeper holds the last value of SDATA on the pin.

SDEN1/PIO23, SDEN0/PIO22

Serial Data Enables (output, synchronous)

These pins enable data transfers on port 1 and port 0 of the synchronous serial interface (SSI). The microcontroller asserts either SDEN1 or SDEN0 at the beginning of a transfer and deasserts it after the transfer is complete. When SDEN1–SDEN0 are inactive, they are held Low by the microcontroller. SDEN1–SDEN0 are three-stated during ONCE mode.

SRDY/PIO6

Synchronous Ready (input, synchronous, level-sensitive)

This pin indicates to the microcontroller that the addressed memory space or I/O device will complete a data transfer. The SRDY pin accepts an active High input synchronized to CLKOUTA.

Using SRDY instead of ARDY allows a relaxed system timing because of the elimination of the one-half clock period required to internally synchronize ARDY. To always assert the ready condition to the microcontroller, tie SRDY High. If the system does not use SRDY, tie the pin Low to yield control to ARDY. When SRDY is configured as P106, the internal SRDY signal is driven low.

TMRIN0/PIO11

Timer Input 0 (input, synchronous, edge-sensitive)

This pin supplies a clock or control signal to the internal microcontroller timer 0. After internally synchronizing a Low-to-High transition on TMRIN0, the microcontroller increments the timer. TMRIN0 must be tied High if not being used.

TMRIN1/PIO0

Timer Input 1 (input, synchronous, edge-sensitive)

This pin supplies a clock or control signal to the internal microcontroller timer 1. After internally synchronizing a Low-to-High transition on TMRIN1, the microcontroller increments the timer. TMRIN1 must be tied High if not being used.

TMROUT0/PIO10

Timer Output 0 (output, synchronous)

This pin supplies the system with either a single pulse or a continuous waveform with a programmable duty cycle.

TMROUT1/PIO1

Timer Output 1 (output, synchronous)

This pin supplies the system with either a single pulse or a continuous waveform with a programmable duty cycle.

TXD/PIO27

Transmit Data (output, asynchronous)

This pin supplies asynchronous serial transmit data to the system from the internal UART of the microcontroller.

$\overline{\text{UCS}}$/$\overline{\text{ONCE1}}$

Upper Memory Chip Select (output, synchronous)
ONCE Mode Request 1 (input, internal pullup)

$\overline{\text{UCS}}$—This pin indicates to the system that a memory access is in progress to the upper memory block. The base address and size of the upper memory block are programmable up to 512 Kbyte. $\overline{\text{UCS}}$ is held High during a bus hold condition.

After power-on reset, $\overline{\text{UCS}}$ is asserted because the microcontroller begins executing at FFFF0h and the default configuration for the $\overline{\text{UCS}}$ chip select is 64 Kbyte from F0000h to FFFFFh.

$\overline{\text{ONCE1}}$—During reset, this pin and $\overline{\text{ONCE0}}$ indicate to the microcontroller the mode in which it should operate. $\overline{\text{ONCE0}}$ and $\overline{\text{ONCE1}}$ are sampled on the rising edge of $\overline{\text{RES}}$. If both pins are asserted Low, the microcontroller enters ONCE mode. Otherwise, it operates normally. In ONCE mode, all pins assume a high-impedance state and remain in that state until a subsequent reset occurs. To guarantee the microcontroller does not inadvertently enter ONCE mode, $\overline{\text{ONCE1}}$ has a weak internal pullup resistor that is active only during a reset.

$\overline{\text{UZI}}$/$\overline{\text{CLKSEL2}}$/PIO26

Upper Zero Indicate (output, synchronous)

$\overline{\text{UZI}}$—This pin lets the designer determine if an access to the interrupt vector table is in progress by ORing it with bits 15–10 of the address and data bus (AD15–AD10 on the Am186ER microcontroller and AO15–AO10 on the Am188ER microcontroller). $\overline{\text{UZI}}$ is the logical AND of the inverted A19–A16 bits. $\overline{\text{UZI}}$ is not held throughout the cycle. $\overline{\text{UZI}}$ is asserted in the first period and deasserted in the second period of a bus cycle. $\overline{\text{UZI}}$/$\overline{\text{CLKSEL2}}$ is three-stated during bus holds and ONCE mode.

$\overline{\text{CLKSEL2}}$—The clocking mode of the Am186ER and Am188ER microcontrollers is controlled by $\overline{\text{UZI}}$/$\overline{\text{CLKSEL2}}$/PIO26 and S6/$\overline{\text{CLKSEL1}}$/PIO29 during reset. Both $\overline{\text{CLKSEL2}}$ and $\overline{\text{CLKSEL1}}$ are held High during power-on reset because of an internal pullup resistor. This is the default clocking mode—Times Four, which is used if neither clock select is asserted Low during reset.

If $\overline{\text{CLKSEL2}}$ is held Low during power-on reset, the microcontroller enters Times One mode.

This pin is latched within three crystal clock cycles after the rising edge of $\overline{\text{RES}}$. Refer to Reset Waveforms on page 100 and Signals Related to Reset Waveforms on page 100 to determine signal hold times. Note that clock selection must be stable four clock cycles prior to exiting reset (that is, $\overline{\text{RES}}$ going High). See Table 6 on page 39 for specifics on the clocking modes and how to specify them. $\overline{\text{UZI}}$/$\overline{\text{CLKSEL2}}$ is three-stated during bus holds and ONCE mode.

Table 6. Clocking Modes

$\overline{\text{CLKSEL2}}$	$\overline{\text{CLKSEL1}}$	Clocking Mode
H	H	Times Four
H	L	Divide by Two
L	H	Times One
L	L	Reserved[1]

Notes:

1. The reserved clocking mode should not be used. Entering the reserved clocking mode may cause unpredictable system behavior.

V_{CC}

Power Supply (input)

These pins supply power (+3.3 V) to the microcontroller.

$\overline{\text{WHB}}$ (Am186™ER Microcontroller Only)

Write High Byte (output, three-state, synchronous)

This pin and $\overline{\text{WLB}}$ indicate to the system which bytes of the data bus (upper, lower, or both) participate in a write cycle. In 80C186 designs, this information is provided by $\overline{\text{BHE}}$, AD0, and $\overline{\text{WR}}$. However, by using $\overline{\text{WHB}}$ and $\overline{\text{WLB}}$, the standard system interface logic and external address latch that were required are eliminated.

$\overline{\text{WHB}}$ is asserted with AD15–AD8. $\overline{\text{WHB}}$ is the logical OR of $\overline{\text{BHE}}$ and $\overline{\text{WR}}$. During reset, this pin is a pullup. This pin is three-stated during bus holds and ONCE mode.

$\overline{\text{WLB}}$ (Am186™ER Microcontroller Only) $\overline{\text{WB}}$ (Am188™ER Microcontroller Only)

Write Low Byte (output, three-state, synchronous)
Write Byte (output, three-state, synchronous)

$\overline{\text{WLB}}$—This pin and $\overline{\text{WHB}}$ indicate to the system which bytes of the data bus (upper, lower, or both) participate in a write cycle. In 80C186 designs, this information is provided by $\overline{\text{BHE}}$, AD0, and $\overline{\text{WR}}$. However, by using $\overline{\text{WHB}}$ and $\overline{\text{WLB}}$, the standard system interface logic and external address latch that were required are eliminated.

$\overline{\text{WLB}}$ is asserted with AD7–AD0. $\overline{\text{WLB}}$ is the logical OR of A0 and $\overline{\text{WR}}$. This pin is three-stated during bus holds and ONCE mode.

$\overline{\text{WB}}$—On the Am188ER microcontroller, this pin indicates a write to the bus. $\overline{\text{WB}}$ uses the same early timing as the nonmultiplexed address bus. $\overline{\text{WB}}$ is associated with AD7–AD0. This pin is three-stated during bus holds and ONCE mode.

$\overline{\text{WR}}$

Write Strobe (output, synchronous)

This pin indicates to the system that the data on the bus is to be written to a memory or I/O device. $\overline{\text{WR}}$ is three-stated during a bus hold or reset condition.

X1

Crystal Input (input)

This pin and the X2 pin provide connections for a fundamental mode crystal used by the internal oscillator circuit. If providing an external clock source, connect the source to X1 and leave X2 unconnected. Unlike the rest of the pins on the Am186ER and Am188ER microcontrollers, X1 is not 5-V tolerant and has a maximum input equal to V_{CC}.

X2

Crystal Output (output)

This pin and the X1 pin provide connections for a fundamental mode crystal used by the internal oscillator circuit. If providing an external clock source, connect the source to X1 and leave X2 unconnected. Unlike the rest of the pins on the Am186ER and Am188ER microcontrollers, X2 is not 5-V tolerant.

FUNCTIONAL DESCRIPTION

The Am186ER and Am188ER microcontrollers are based on the architecture of the original Am186 and Am188 microcontrollers and they function in the enhanced mode of the Am186 and Am188 microcontrollers. Enhanced mode includes system features such as power-save control.

Each of the 8086, 8088, 80186, and 80188 microcontrollers contains the same basic set of registers, instructions, and addressing modes. The Am186ER and Am188ER microcontrollers are backward compatible with the 80C186/80C188 and Am186/Am188 microcontrollers.

A full description of the Am186ER and Am188ER microcontrollers' registers and instructions is included in the *Am186ER and Am188ER Microcontrollers User's Manual*, order #21684.

Memory Organization

Memory is organized in sets of segments. Each segment is a linear contiguous sequence of 64K (2^{16}) 8-bit bytes. Memory is addressed using a two-component address consisting of a 16-bit segment value and a 16-bit offset. The 16-bit segment values are contained in one of four internal segment registers (CS, DS, SS, or ES). The physical address is calculated by shifting the segment value left by 4 bits and adding the 16-bit offset value to yield a 20-bit physical address (see Figure 3). This allows for a 1-Mbyte physical address size.

All instructions that address operands in memory must specify the segment value and the 16-bit offset value. For speed and compact instruction encoding, the segment register used for physical address generation is implied by the addressing mode used (see Table 7).

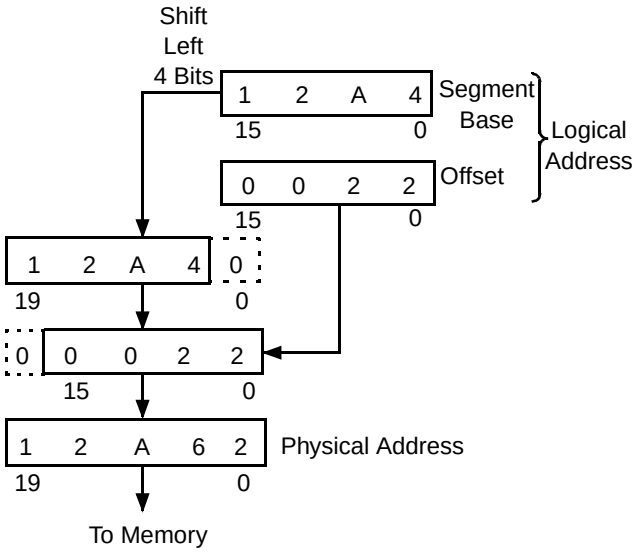


Figure 3. Two-Component Address Example

I/O Space

The I/O space consists of 64K 8-bit or 32K 16-bit ports. Separate instructions (IN, INS and OUT, OUTS) address the I/O space with either an 8-bit port address specified in the instruction, or a 16-bit port address in the DX register. Eight-bit port addresses are zero-extended such that A15–A8 are Low.

Table 7. Segment Register Selection Rules

Memory Reference Needed	Segment Register Used	Implicit Segment Selection Rule
Instructions	Code (CS)	Instructions (including immediate data)
Local Data	Data (DS)	All data references
Stack	Stack (SS)	All stack pushes and pops; any memory references that use BP Register
External Data (Global)	Extra (ES)	All string instruction references that use the DI Register as an index

BUS OPERATION

The industry-standard 80C186/80C188 microcontrollers use a multiplexed address and data (AD) bus. The address is present on the AD bus only during the t_1 clock phase. The Am186ER and Am188ER microcontrollers continue to provide the multiplexed AD bus and, in addition, provide a nonmultiplexed address (A) bus. The A bus provides an address to the system for the complete bus cycle (t_1–t_4).

For systems where power consumption is a concern, the address can be disabled from being driven on the AD bus on the Am186ER microcontroller and on the AD and AO buses on the Am188ER microcontroller during the normal address portion of the bus cycle for accesses to UCS and/or LCS address spaces. In this mode, the affected bus is placed in a high-impedance state during the address portion of the bus cycle. This feature is enabled through the DA bits in the UMCS and LMCS registers. When address disable is in effect, the number of signals that assert on the bus during all normal bus cycles to the associated address space is reduced, thus decreasing power consumption, reducing processor switching noise, and preventing bus contention with memory devices and peripherals when operating at high clock rates. On the Am188ER microcontroller, the address is driven on A015–A08 during the data portion of the bus cycle, regardless of the setting of the DA bits.

If the $\overline{\text{ADEN}}$ pin is pulled Low during processor reset, the value of the DA bits in the UMCS and LMCS registers is ignored and the address is driven on the AD bus for all accesses, thus preserving the industry-standard 80C186 and 80C188 microcontrollers' multiplexed address bus and providing support for existing emulation tools.

Figure 4 on page 42 shows the affected signals during a normal read or write operation for an Am186ER microcontroller. The address and data will be multiplexed onto the AD bus.

Figure 5 on page 42 shows an Am186ER microcontroller bus cycle when address bus disable is in effect. This results in having the AD bus operate in a nonmultiplexed data-only mode. The A bus will have the address during a read or write operation.

Figure 6 on page 43 shows the affected signals during a normal read or write operation for an Am188ER microcontroller. The multiplexed address/data mode is compatible with the 80C188 microcontrollers and might be used to take advantage of existing logic or peripherals.

Figure 7 on page 43 shows an Am188ER microcontroller bus cycle when address bus disable is in effect. The address and data is not multiplexed. The AD7–AD0 signals will have only data on the bus, while the A bus will have the address during a read or write operation. The AO bus will also have the address during t_2–t_4.

BUS INTERFACE UNIT

The bus interface unit controls all accesses to external peripherals and memory devices. External accesses include those to memory devices, as well as those to memory-mapped and I/O-mapped peripherals and the peripheral control block. The Am186ER and Am188ER microcontrollers provide an enhanced bus interface unit with the following features:

- A nonmultiplexed address bus
- Separate byte write enables for high and low bytes on the Am186ER microcontroller and a write enable on the Am188ER microcontroller
- Pseudo Static RAM (PSRAM) support

The standard 80C186/80C188 multiplexed address and data bus requires system interface logic and an external address latch. On the Am186ER and Am188ER microcontrollers, new byte write enables, PSRAM control logic, and a new nonmultiplexed address bus can reduce design costs by eliminating this external logic.

Nonmultiplexed Address Bus

The nonmultiplexed address bus (A19–A0) is valid one-half CLKOUTA cycle in advance of the address on the AD bus. When used in conjunction with the modified $\overline{\text{UCS}}$ and $\overline{\text{LCS}}$ outputs and the byte write enable signals, the A19–A0 bus provides a seamless interface to external SRAM, PSRAM, and Flash/EPROM memory systems.

Byte Write Enables

The Am186ER microcontroller provides the $\overline{\text{WHB}}$ (Write High Byte) and $\overline{\text{WLB}}$ (Write Low Byte) signals which act as byte write enables. The Am188ER microcontroller provides the WB (Write Byte) signal which acts as a write enable.

$\overline{\text{WHB}}$ is the logical AND of $\overline{\text{BHE}}$ and $\overline{\text{WR}}$. $\overline{\text{WHB}}$ is Low when both $\overline{\text{BHE}}$ and $\overline{\text{WR}}$ are Low. $\overline{\text{WLB}}$ is the logical AND of A0 and $\overline{\text{WR}}$. $\overline{\text{WLB}}$ is Low when A0 and $\overline{\text{WR}}$ are both Low. $\overline{\text{WB}}$ is Low whenever a byte is written by the Am188ER microcontroller.

The byte write enables are driven in conjunction with the nonmultiplexed address bus as required for the write timing requirements of common SRAMs.

Output Enable

The Am186ER and Am188ER microcontrollers provide the $\overline{\text{RD}}$ (Read) signal which acts as an output enable.

The $\overline{\text{RD}}$ signal is Low when a word or byte is read by the Am186ER or Am188ER microcontroller.

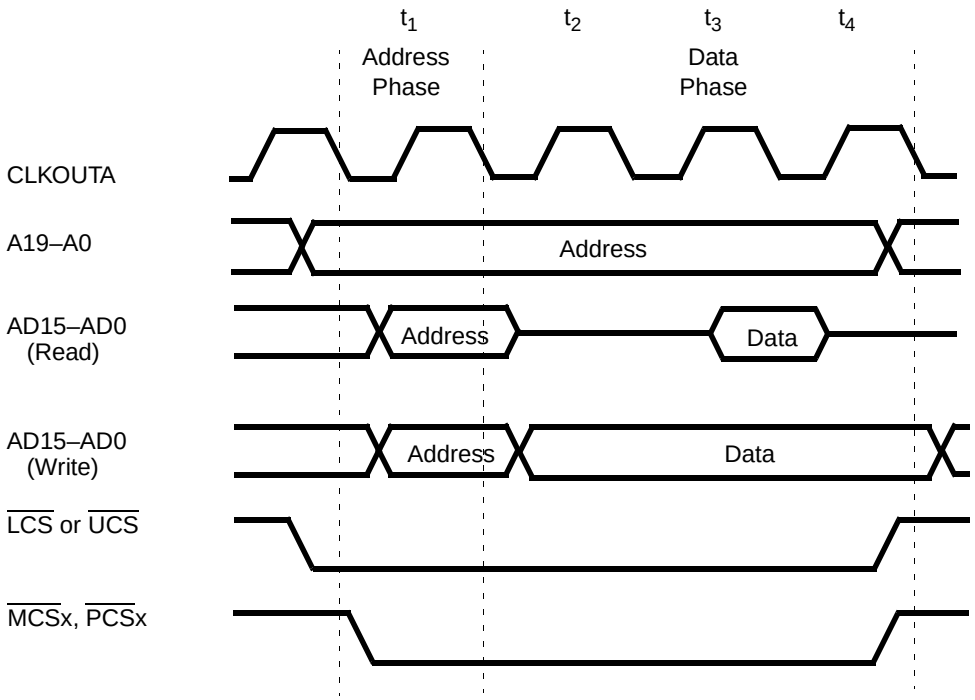


Figure 4. Am186™ER Microcontroller Address Bus—Normal Operation

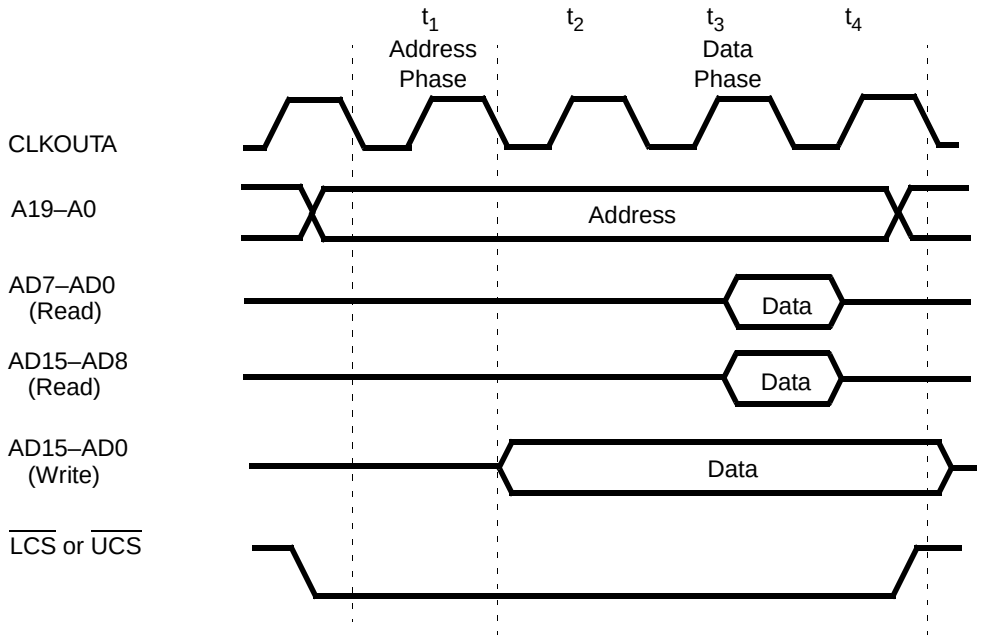


Figure 5. Am186™ER Microcontroller—Address Bus Disable in Effect

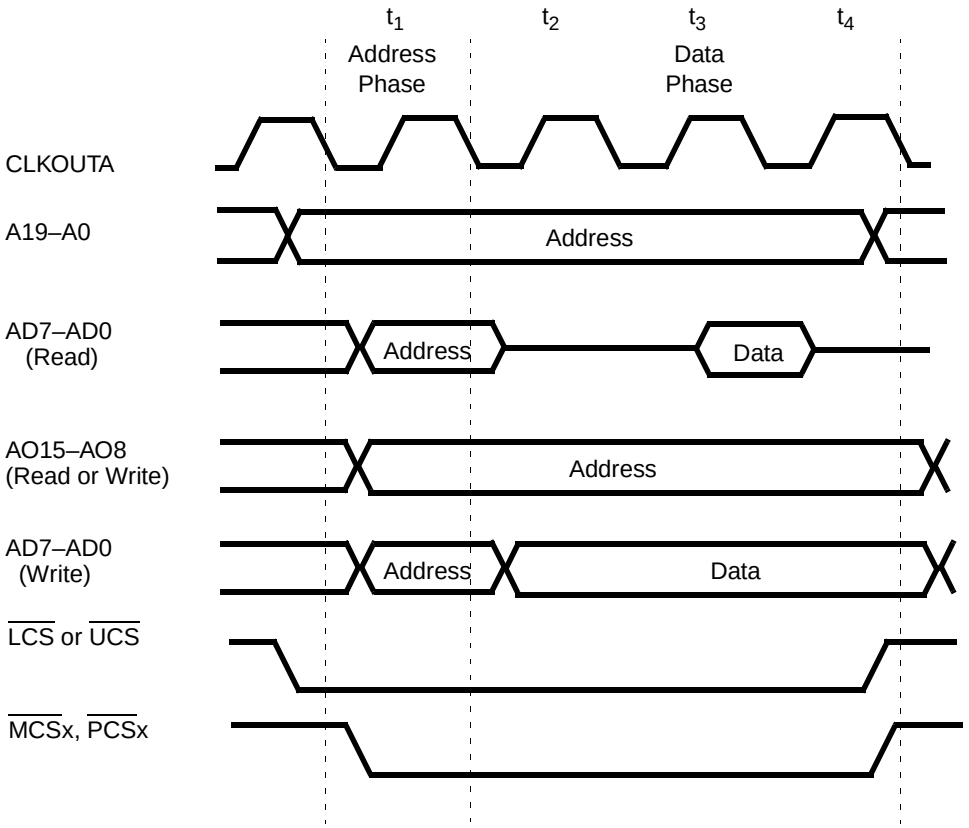


Figure 6. Am188™ER Microcontroller Address Bus—Normal Operation

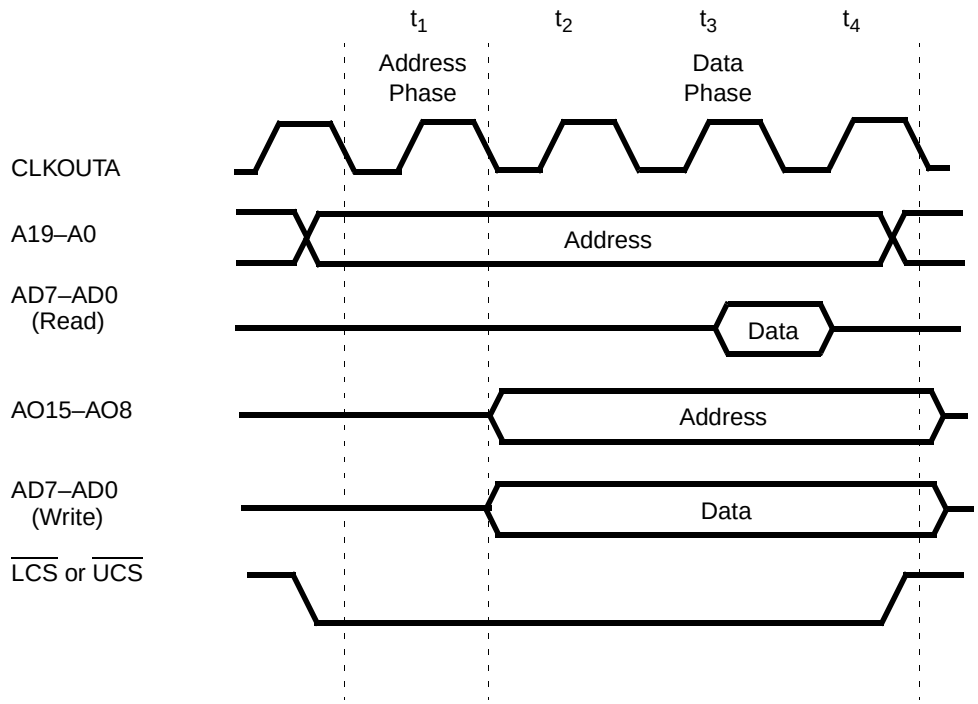


Figure 7. Am188™ER Microcontroller—Address Bus Disable in Effect

Pseudo Static RAM (PSRAM) Support

The Am186ER and Am188ER microcontrollers support the use of PSRAM devices in low memory chip-select (LCS) space only. When PSRAM mode is enabled, the timing for the LCS signal is modified by the chip-select control unit to provide a CS precharge period during PSRAM accesses. The 50-MHz timing of the Am186ER and Am188ER microcontrollers is appropriate to allow 70-ns PSRAM to run with one wait state. PSRAM mode is enabled through a bit in the Low Memory Chip-Select (LMCS) Register. The PSRAM feature is disabled on CPU reset.

In addition to the LCS timing changes for PSRAM precharge, the PSRAM devices also require periodic refresh of all internal row addresses to retain their data. Although refresh of PSRAM can be accomplished several ways, the Am186ER and Am188ER microcontrollers implement auto refresh only.

The Am186ER and Am188ER microcontrollers generate RFSH, a refresh signal, to the PSRAM devices when PSRAM mode is enabled. No refresh address is required by the PSRAM when using the auto refresh mechanism. The RFSH signal is multiplexed with the MCS3 signal pin. When PSRAM mode is enabled, MCS3 is not available for use as a chip-select signal.

The refresh control unit must be programmed before accessing PSRAM in LCS space. The refresh counter in the Clock Prescaler (CDRAM) Register must be configured with the required refresh interval value. The refresh counter reload value in the CDRAM Register should not be set to less than 18 (12h) in order to provide time for processor cycles between refreshes. The refresh address counter must be set to 000000h to prevent the MCS3–MCS0 or PCS6–PCS0 chip selects from asserting. UCS may randomly assert during a PSRAM refresh.

LCS is held High and the A bus is not used during refresh cycles. The LMCS Register must be configured to external ready ignored (R2 = 1) with one wait state (R1–R0 = 01b), and the PSRAM mode enable bit (SE) must be set. The ending address of LCS space in the LMCS Register must also be programmed.

PERIPHERAL CONTROL BLOCK (PCB)

The integrated peripherals of the Am186ER and Am188ER microcontrollers are controlled by 16-bit read/write registers. The peripheral registers are contained within an internal 256-byte control block. The registers are physically located in the peripheral devices they control, but they are addressed as a single 256-byte block. Figure 9 on page 46 shows a map of these registers.

Reading and Writing the PCB

Code intended to execute on the Am188ER microcontroller should perform all writes to the PCB registers as byte writes. These writes will transfer 16 bits of data to the PCB Register even if an 8-bit register is named in the instruction. For example, `out dx, al` results in the ax value being written to the port address in dx. Reads to the PCB should be done as word reads. Code written in this manner will run correctly on the Am188ER and Am186ER microcontrollers.

Unaligned reads and writes to the PCB result in unpredictable behavior on both the Am186ER and Am188ER microcontrollers.

For a complete description of all the registers in the PCB, refer to the *Am186ER and Am188ER Microcontrollers User's Manual*, order #21684.

CLOCK AND POWER MANAGEMENT

The clock and power management unit of the Am186ER and Am188ER microcontrollers includes a phase-locked loop (PLL) and a second programmable system clock output (CLKOUTB).

Phase-Locked Loop (PLL)

In a traditional 80C186/80C188 design, the internal clock frequency is half the frequency of the crystal. Because of the internal PLL on the Am186ER and Am188ER microcontrollers, the internal clock generated by both microcontrollers can operate at up to four times the frequency of the crystal. The Am186ER and Am188ER microcontrollers operate in the following modes:

- Divide by Two—Frequency of the system clock is half the frequency of the crystal with PLL disabled.
- Times One—Frequency of the system clock will be the same as the external crystal with PLL enabled.
- Times Four—Frequency of the system clock is four times the frequency of the crystal with PLL enabled.

The default Times Four mode must be used for processor frequencies above 40 MHz. The Divide by Two mode should be used for frequencies below 16 MHz. The clocking mode is selected using CLKSEL1 and CLKSEL2 on reset. Table 8 provides the maximum and minimum frequencies for X1, X2, and CLKOUTA according to clocking mode.

Table 8. Maximum and Minimum Clock Frequencies

Mode	X1/X2 Max	X1/X2 Min	CLKOUTA Max	CLKOUTA Min
Divide by 2	40 MHz	30 MHz	20 MHz	15 MHz
Times 1	40 MHz	16 MHz	40 MHz	16 MHz
Times 4	12.5 MHz	4 MHz	50 MHz	16 MHz

Crystal-Driven Clock Source

The internal oscillator circuit of the Am186ER and Am188ER microcontrollers is designed to function with a parallel-resonant fundamental mode crystal. Because of the PLL, the crystal frequency can be twice, equal to, or one quarter of the processor frequency. Do not replace a crystal with an LC or RC equivalent. See Figure 8 for a diagram of oscillator configurations.

The X1 and X2 signals are connected to an internal inverting amplifier (oscillator) that provides, along with the external feedback loading, the necessary phase shift. In such a positive feedback circuit, the inverting amplifier has an output signal (X2) 180 degrees out of phase of the input signal (X1).

The external feedback network provides an additional 180-degree phase shift. In an ideal system, the input to X1 will have 360 or zero degrees of phase shift. The external feedback network is designed to be as close to ideal as possible. If the feedback network is not providing necessary phase shift, negative feedback will dampen the output of the amplifier and negatively affect the operation of the clock generator. Values for the loading on X1 and X2 must be chosen to provide the necessary phase shift and crystal operation.

Selecting a Crystal

When selecting a crystal, the load capacitance should always be specified (C_L). This value can cause variance in the oscillation frequency from the desired specified value (resonance). The load capacitance and the loading of the feedback network have the following relationship:

$$C_L = \frac{(C_1 \cdot C_2)}{(C_1 + C_2)} + C_S$$

where C_S is the stray capacitance of the circuit. Placing the crystal and C_L in series across the inverting amplifier and tuning these values (C_1, C_2) allows the crystal to oscillate at resonance. Finally, there is a relationship between C_1 and C_2. To enhance the oscillation of the inverting amplifier, these values need to be offset with the larger load on the output (X2). Equal values of these loads will tend to balance the poles of the inverting amplifier.

The characteristics of the inverting amplifier set limits on the following parameters for crystals:

ESR (Equivalent Series Resistance)60-ohm max

Drive Level ..... 500-mW max

The recommended range of values for C_1 and C_2 are as follows:

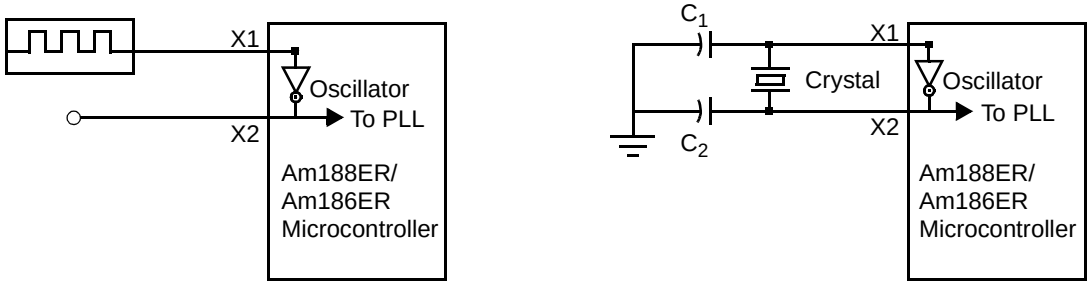
C_1..... 15 pF ± 20%

C_2..... 22 pF ± 20%

The specific values for C_1 and C_2 must be determined by the designer and are dependent on the characteristics of the chosen crystal and board design.

External Source Clock

Alternately, the internal oscillator can be driven by an external clock source. The external clock source should be connected to the input of the inverting amplifier (X1) with the output (X2) left unconnected. X1 and X2 are not 5-V tolerant and X1 has a maximum input equal to V_{CC}.



a. External Clock Configuration

b. Crystal Configuration

Notes:
X1 and X2 are not 5-V tolerant. The X1 maximum input is V_{CC}.

Figure 8. Am186™ER and Am188™ER Microcontrollers Oscillator Configurations

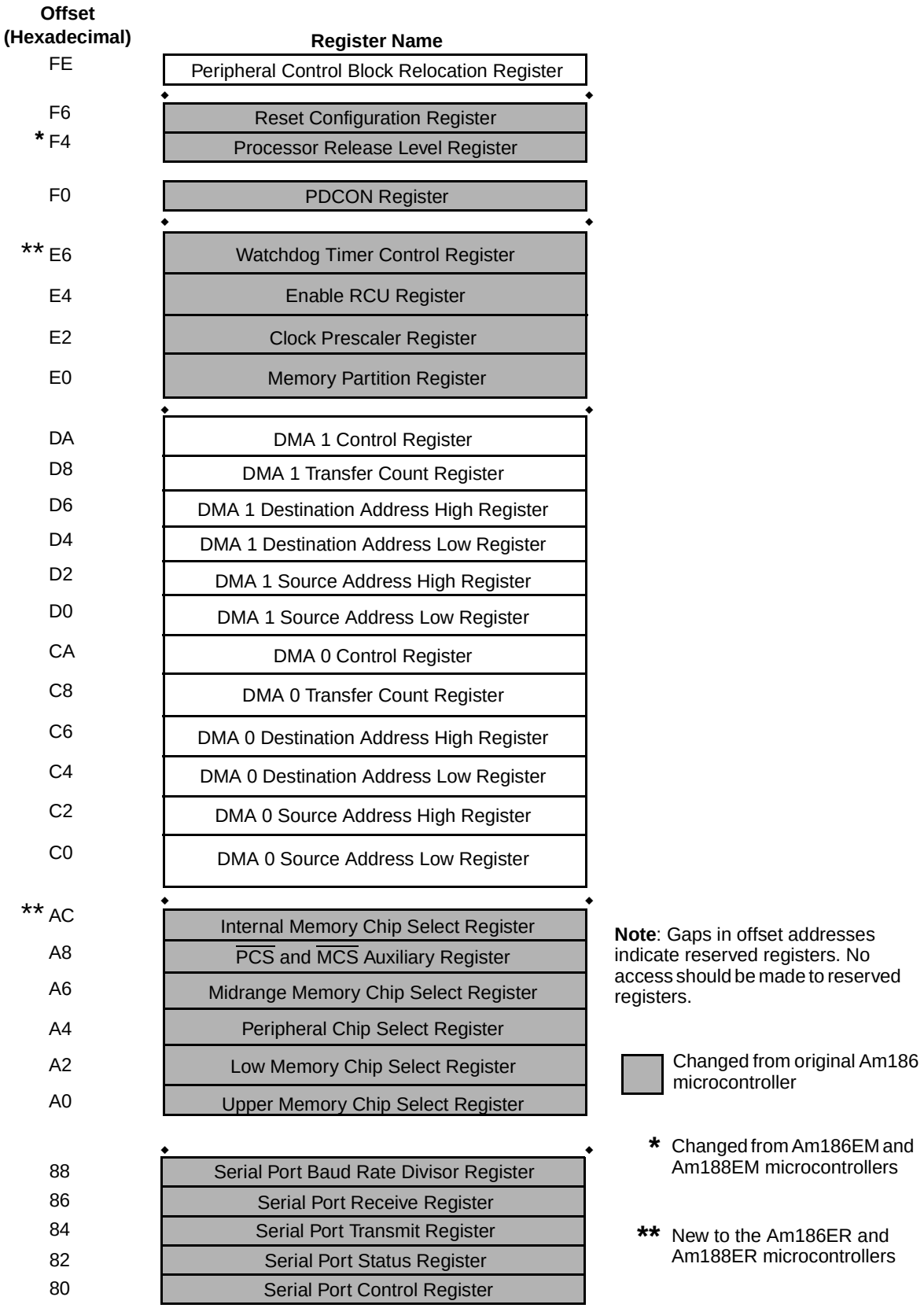


Figure 9. Peripheral Control Block Register Map

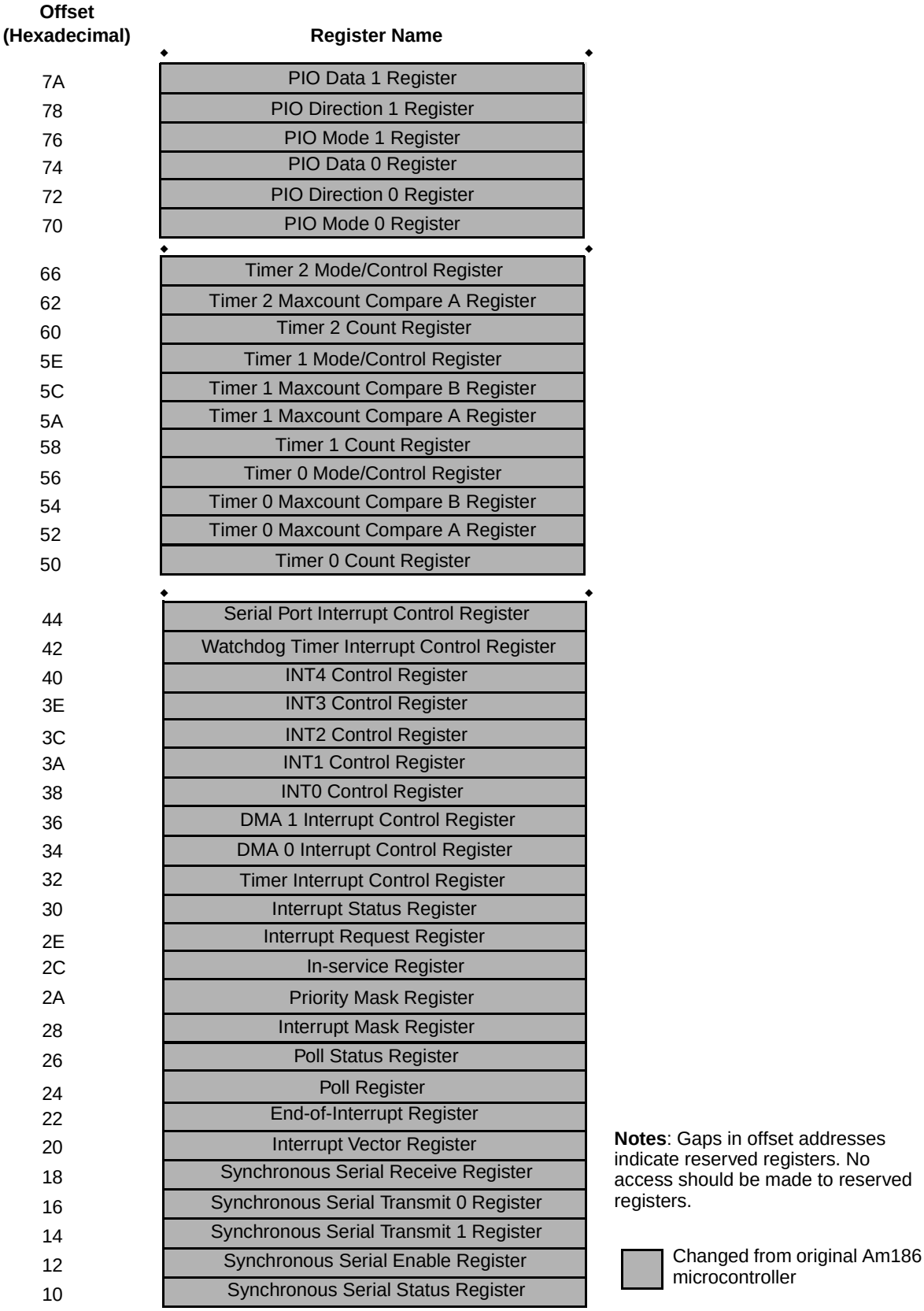
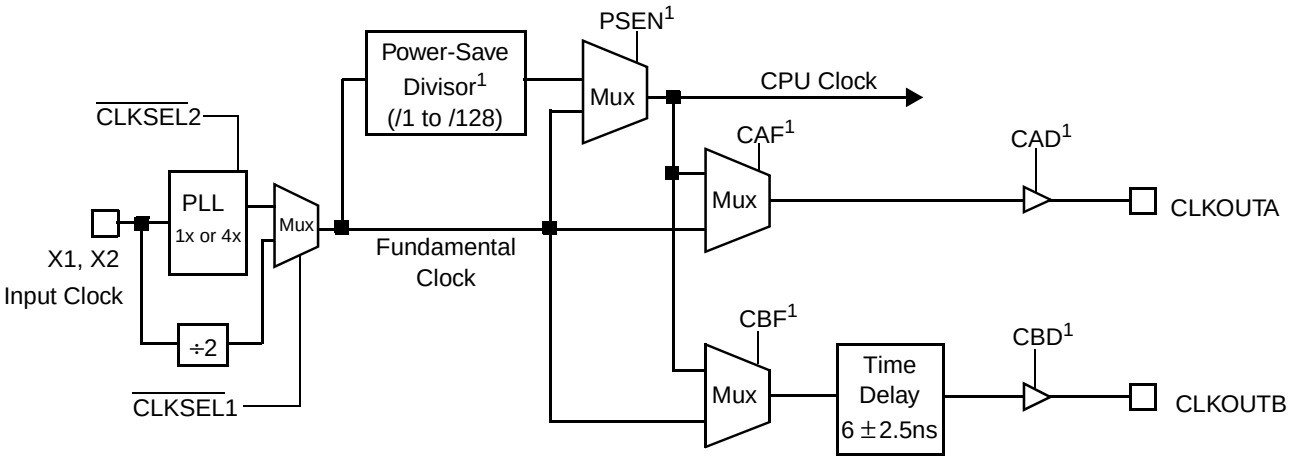


Figure 9. Peripheral Control Block Register Map (Continued)



Notes:
1. Set via PDCON Register

Figure 10. Clock Organization

System Clocks

The base system clock of the original Am186/Am188 microcontrollers is renamed CLKOUTA and the additional output is called CLKOUTB. CLKOUTA and CLKOUTB operate at either the fundamental processor frequency or the CPU clock (power-save) frequency. Figure 10 shows the organization of the clocks.

The second clock output (CLKOUTB) allows one clock to run at the fundamental frequency and the other clock to run at the CPU (power-save) frequency. Individual drive enable bits allow selective enabling of just one, or both, of these clock outputs.

Power-Save Operation

The Power-Save mode of the Am186ER and Am188ER microcontrollers reduces power consumption and heat dissipation, thereby extending battery life in portable systems. In Power-Save mode, operation of the CPU and internal peripherals continues at a slower clock frequency. When a hardware interrupt occurs, the microcontroller automatically returns to its normal operating frequency. The microcontroller remains in Power-Save mode for software interrupts and traps.

Note: *Power-save operation requires that clock-dependent peripherals be reprogrammed for clock frequency changes. Software drivers must be aware of clock frequency.*

Initialization and Processor Reset

Processor initialization or startup is accomplished by driving the $\overline{\text{RES}}$ input pin Low. $\overline{\text{RES}}$ must be held Low for 1 ms during power-up to ensure proper device initialization. $\overline{\text{RES}}$ forces the Am186ER and Am188ER microcontrollers to terminate all execution and local bus activity. No instruction or bus activity occurs as long as $\overline{\text{RES}}$ is active. After $\overline{\text{RES}}$ becomes inactive and an internal processing interval elapses, the microcontroller begins execution with the instruction at physical location FFFF0h. $\overline{\text{RES}}$ also sets some registers to predefined values. Note that all clock selection (S6/$\overline{\text{CLKSEL1}}$ and $\overline{\text{UZI}}$/$\overline{\text{CLKSEL2}}$) must be stable four clocks prior to the deassertion of $\overline{\text{RES}}$. Activating the PLL will require 1 ms to achieve a stable clock.

Reset Configuration Register

When the $\overline{\text{RES}}$ input is asserted Low, the contents of the address/data bus (AD15–AD0) are written into the Reset Configuration Register. The system can place configuration information on the address/data bus using weak external pullup or pulldown resistors, or using an external driver that is enabled during reset. The processor does not drive the address/data bus during reset.

For example, the Reset Configuration Register could be used to provide the software with the position of a configuration switch in the system. Using weak external pullup and pulldown resistors on the address and data bus, the system would provide the microcontroller with a value corresponding to the position of the jumper during a reset.

The Reset Configuration Register can only be modified during reset. This register is read-only during normal operation.

CHIP-SELECT UNIT

The Am186ER and Am188ER microcontrollers contain logic that provides programmable chip-select generation for both memories and peripherals. The logic can be programmed to provide external ready and wait-state generation and latched address bits A1 and A2. The chip-select lines are active for all memory and I/O cycles in their programmed areas, whether they are generated by the CPU or by the integrated DMA unit.

Chip-Select Timing

The timing for the $\overline{\text{UCS}}$ and $\overline{\text{LCS}}$ outputs is modified from the original Am186 microcontroller. These outputs now assert in conjunction with the nonmultiplexed address bus for normal memory timing. To enable these outputs to be available earlier in the bus cycle, the number of programmable memory size selections has been reduced.

Ready and Wait-State Programming

The Am186ER and Am188ER microcontrollers can be programmed to sense a ready signal for each of the external peripheral or memory chip-select lines. The external ready signal can be either the ARDY or SRDY signal as shown in Figure 11. For diagrams of the synchronous ready waveforms and asynchronous ready waveforms, refer to page 97. Each external chip-select control register (UMCS, LMCS, MMCS, PACS, and MPCS) contains a single-bit field that determines whether the external ready signal is required or ignored. The internal memory ignores the external ready signal.

The number of wait states to be inserted for each access to an external peripheral or memory region is programmable. The chip-select control registers for $\overline{\text{UCS}}$, $\overline{\text{LCS}}$, $\overline{\text{MCS3}}$–$\overline{\text{MCS0}}$, $\overline{\text{PCS6}}$, and $\overline{\text{PCS5}}$ contain a two-bit field that determines the number of wait states from zero to three to be inserted. $\overline{\text{PCS3}}$–$\overline{\text{PCS0}}$ use three bits to provide additional values of 5, 7, 9, and 15 wait states. The chip-select control register for internal memory always specifies no wait states.

When external ready is required, internally programmed wait states will always complete before external ready can terminate or extend a bus cycle. For example, if the internal wait states are set to insert two wait states, the processor samples the external ready pin during the first wait cycle. If external ready is asserted at that time, the access completes after six cycles (four cycles plus two wait states). If external ready is not asserted during the first wait state, the access is extended until ready is asserted, which is followed by one more wait state followed by t_4.

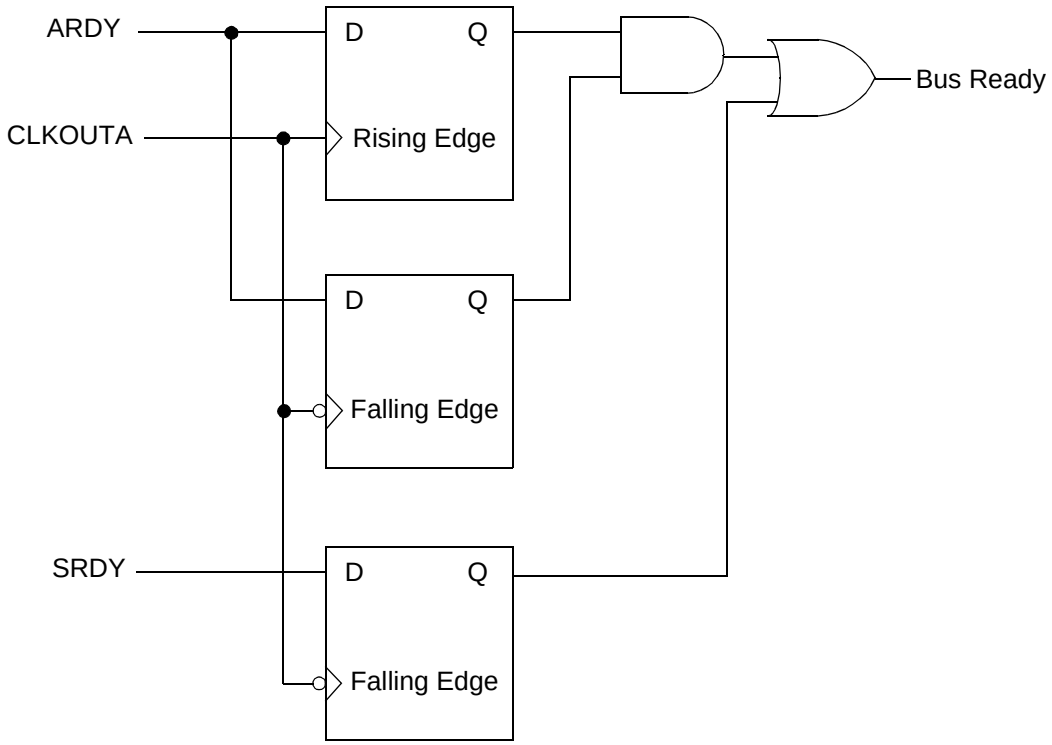


Figure 11. ARDY and SRDY Synchronization Logic Diagram

Memory Maps

There are several possible ways to configure the address space of the Am186ER and Am188ER microcontrollers. Four of the most popular configurations are shown in Figure 12.

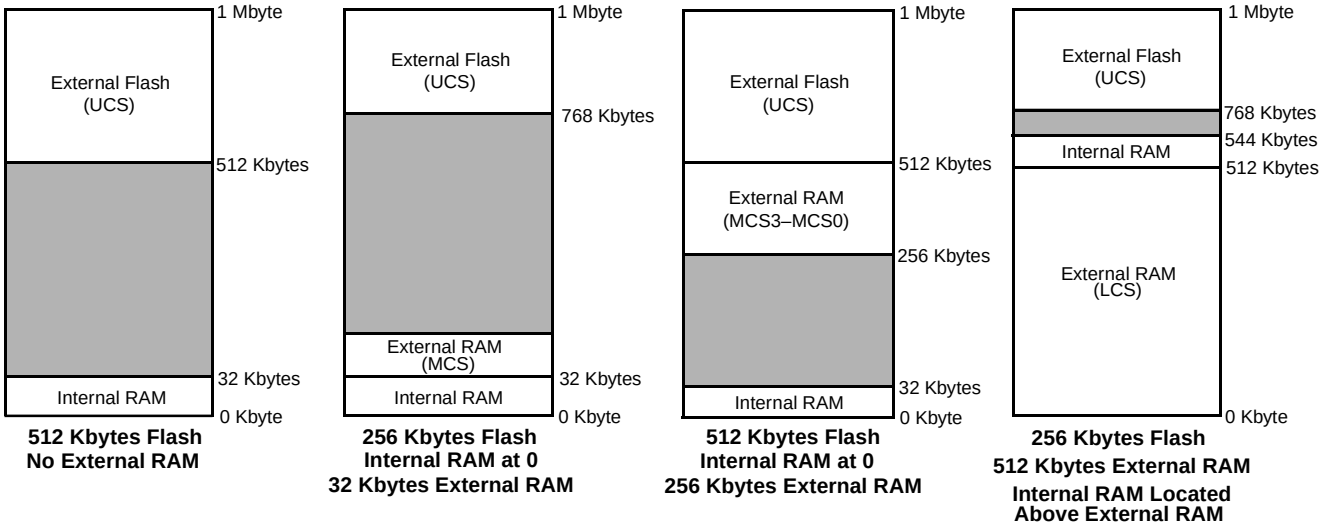


Figure 12. Example Memory Maps

Chip-Select Overlap

Although programming the various chip selects on the Am186ER microcontroller so that multiple chip select signals are asserted for the same physical address is not recommended, it may be unavoidable in some systems. In such systems, the chip selects whose assertions overlap must have the same configuration for ready (external ready required or not required) and the number of wait states to be inserted into the cycle by the processor.

The peripheral control block (PCB) and the internal memory are both accessed using internal signals. These internal signals function as chip selects configured with zero wait states and no external ready. Therefore, the PCB and internal memory can be programmed to addresses that overlap external chip select signals if those external chip selects are programmed to zero wait states with no external ready required.

When overlapping an additional chip select with either the LCS or UCS chip selects, it must be noted that setting the Disable Address (DA) bit in the LMCS or UMCS register will disable the address from being driven on the AD bus for all accesses for which the associated chip select is asserted, including any accesses for which multiple chip selects assert.

The MCS and PCS chip select pins can be configured as either chip selects (normal function) or as PIO inputs or outputs. It should be noted; however, that the ready and wait state generation logic for these chip selects is in effect regardless of their configurations as chip selects or PIOs. This means that if these chip selects are enabled (by a write to the MMCS and MPCS for the MCS chip selects, or by a write to the PACS and MPCS registers for the PCS chip selects), the ready and wait state programming for these signals must agree with the programming for any other chip selects with which their assertion would overlap if they were configured as chip selects.

Although the PCS4 signal is not available on an external pin, the ready and wait state logic for this signal still exists internal to the part. For this reason, the PCS4 address space must follow the rules for overlapping chip selects. The ready and wait-state logic for PCS6–PCS5 is disabled when these signals are configured as address bits A2–A1.

Failure to configure overlapping chip selects with the same ready and wait state requirements may cause the processor to hang with the appearance of waiting for a ready signal. This behavior may occur even in a system in which ready is always asserted (ARDY or SRDY tied High).

Configuring PCS in I/O space with LCS or any other chip select configured for memory address 0 is not considered overlapping of the chip selects. Overlapping chip selects refers to configurations where more than one chip select asserts for the same physical address.

Upper Memory Chip Select

The Am186ER and Am188ER microcontrollers provide a UCS chip select for the top of memory. On reset, the Am186ER and Am188ER microcontrollers begin fetching and executing instructions starting at memory location FFFF0h. Therefore, upper memory is usually used as instruction memory. To facilitate this usage, UCS defaults to active on reset, with a default memory range of 64 Kbyte from F0000h to FFFFFh, with external ready required and three wait states automatically inserted. The UCS memory range always ends at FFFFFh. The lower boundary is programmable. The Upper Memory Chip Select is configured through the Upper Memory Chip Select (UMCS) Register.

During the address phase of a bus cycle when UCS is asserted, the DA bit in the UMCS Register enables or disables the AD15–AD0 bus. If the DA bit is set to 1, AD15–AD0 is not driven during the address phase of a bus cycle when UCS is asserted. If DA is cleared to 0, AD15–AD0 is driven during the address phase of a bus cycle. Disabling AD15–AD0 reduces power consumption and eliminates potential bus conflicts with memory or peripherals at high clock rates. The DA bit in the UMCS Register defaults to 0 at power-on reset.

Low Memory Chip Select

The Am186ER and Am188ER microcontrollers provide an LCS chip select for the bottom of memory. Because the interrupt vector table is located at the bottom of memory starting at 00000h, the LCS pin has traditionally been used to control data memory. The LCS pin is not active on reset. The Am186ER and Am188ER microcontrollers also allow the IMCS Register and internal memory to be programmed to address 0. This would allow the internal memory to be used for the interrupt vector table and data memory.

Midrange Memory Chip Selects

The Am186ER and Am188ER microcontrollers provide four chip selects, MCS3–MCS0, for use in a user-locatable memory block. The base address of the memory block can be located anywhere within the 1-Mbyte memory address space, exclusive of the areas associated with the UCS and LCS chip selects, as well as the address range of the Peripheral Chip Selects, PCS6, PCS5, and PCS3–PCS0, if they are mapped to memory. The MCS address range can overlap the PCS address range if the PCS chip selects are mapped to I/O space.

Unlike the UCS and LCS chip selects, the MCS outputs assert with the multiplexed AD address bus.

Peripheral Chip Selects

The Am186ER and Am188ER microcontrollers provide six chip selects, PCS6–PCS5 and PCS3–PCS0, for use within a user-locatable memory or I/O block. PCS4 is not available on the Am186ER and Am188ER microcontrollers. The base address of the memory block can be located anywhere within the 1-Mbyte memory address space, exclusive of the areas associated with the UCS, LCS, and MCS chip selects, or they can be configured to access the 64-Kbyte I/O space.

The PCS pins are not active on reset. PCS6–PCS5 can have from zero to three wait states. PCS3–PCS0 can have four additional wait-state values—5, 7, 9, and 15.

Unlike the UCS and LCS chip selects, the PCS outputs assert with the multiplexed AD address bus. Note also that each peripheral chip select asserts over a 256-byte address range, which is twice the address range covered by peripheral chip selects in the 80C186 and 80C188 microcontrollers.

INTERNAL MEMORY

The Am186ER and Am188ER microcontrollers provide 32 Kbyte of on-chip RAM. The integration of memory helps to reduce the overall cost, power, and size of system designs. The internal memory also improves reliability with fewer connections and eases inventory management and system qualification because of the integrated supply.

The internal RAM for the Am186ER microcontroller is a 16K x 16-bit-wide array (32 Kbyte) which provides the same performance as 16-bit external zero-wait-state RAM. For the Am188ER microcontroller, the internal RAM is a 32K x 8-bit-wide array (32 Kbyte) that provides the same performance as 8-bit external zero wait-state RAM.

Interaction with External RAM

The Am186ER and Am188ER microcontrollers include an Internal Memory Chip Select (IMCS) Register to control the mapping of the internal RAM. The internal address space can be located at any 32-Kbyte boundary within the 1-Mbyte memory address space, provided that it does not overlap any external chip selects. If an overlap does occur, the external chip select must be set to 0 wait states and to ignore external ready. If the internal and external chip selects overlap, both will be active, but the internal memory data will be used on reads. Writes, with all the corresponding external control signals, will occur to both devices. Special system consideration must be made for show read cycles, since those cycles will drive data out on reads.

If internal and external chip selects overlap and the external chip selects are not set to 0 wait states and to ignore external ready, the results are unpredictable. Because of the many potential problems with overlapping chip selects, this practice is not recommended.

The base address of the internal RAM is determined by the value of bits BA19–BA15 in the IMCS Register. Because the interrupt vector table is located at 00000h, it is not unusual to store the interrupt vector table in the internal RAM for faster access, and thus program the IMCS Register for a base address of 0. However, this scenario may lead to a memory address overlap between the IMCS and low memory chip select (LMCS) registers, as the base address of the LMCS Register is always 0 if activated.

Emulator and Debug Modes

There are two debug modes associated with the internal memory. One mode allows users to disable the internal RAM, and the other mode makes it possible to drive data on the external data bus during internal RAM read cycles.

Normal operation of internal RAM has all control signals for reads and writes and data for writes visible externally. Accesses to internal memory can be detected externally by comparing the address on A19–A0 with the address space of the internal memory.

Internal Memory Disable

When this mode is activated, the internal RAM is disabled and all accesses into the internal memory space are made externally for debugging purposes. This mode is activated by pulling the S1/IMDIS pin Low during reset. To use this debug mode, internal memory space must first be activated via the IMCS Register.

Show Read Enable

When this mode is activated, the data from the internal RAM read cycles are driven on the AD15–AD0 bus. Note that if a byte read is being shown, the unused byte will also be driven on the AD15–AD0 bus. This mode can be activated externally by pulling the S0/SREN pin Low during reset or by setting the SR bit in the IMCS Register. If this feature is activated externally using the SREN pin, the value of the SR bit is ignored. Many emulators assert the SREN pin.

During an internal memory read with show read enabled, the address will be driven on the AD bus during t_1 and t_2. The data being read will be driven on the AD bus during t_3 and t_4 by the Am186ER or Am188ER microcontrollers. Special system care must be taken to avoid bus contention, because normal reads have the AD bus three-stated during t_2, t_3, and t_4. It is best to ensure that no external device overlaps the internal memory space.

REFRESH CONTROL UNIT

The Refresh Control Unit (RCU) automatically generates refresh bus cycles. After a programmable period of time, the RCU generates a memory read request to the bus interface unit. If the address generated during a refresh bus cycle is within the range of a properly programmed chip select, that chip select (with the exception of $\overline{\text{UCS}}$ and $\overline{\text{LCS}}$) is activated when the bus interface unit executes the refresh bus cycle. The ready logic and wait states programmed for the region are also in force. If no chip select is activated, then external ready is required to terminate the refresh bus cycle.

If the HLDA pin is active when a refresh request is generated (indicating a bus hold condition), then the Am186ER and Am188ER microcontrollers deactivate the HLDA pin in order to perform a refresh cycle. The external bus master must remove the HOLD signal for at least one clock in order to allow the refresh cycle to execute. The sequence of HLDA going inactive while HOLD is being held active can be used to signal a pending refresh request.

The Am186ER and Am188ER microcontrollers' HOLD latency time, the period between HOLD request and HOLD acknowledge, is a function of the activity occurring in the processor when the HOLD request is received. A HOLD request is second only to DRAM refresh requests in priority of activity requests received by the processor. For example, in the case of a DMA transfer, the HOLD latency can be as great as four bus cycles. This occurs if a DMA word transfer operation is taking place from an odd address to an odd address (Am186ER microcontroller only). This is a total of 16 or more clock cycles if wait states are required. In addition, if locked transfers are performed, the HOLD latency time is increased by the length of the locked transfer.

INTERRUPT CONTROL UNIT

The Am186ER and Am188ER microcontrollers can receive interrupt requests from a variety of sources, both internal and external. The internal interrupt controller arranges these requests by priority and presents them one at a time to the CPU.

There are six external interrupt sources on the Am186ER/Am188ER microcontrollers—five maskable interrupt pins and one nonmaskable interrupt pin. In addition, there are six total internal interrupt sources—three timers, two DMA channels, and the asynchronous serial port—that are not connected to external pins.

The Am186ER and Am188ER microcontrollers provide three interrupt sources not present on the Am186 and Am188 microcontrollers. The first is an additional external interrupt pin (INT4), which operates much like the already existing interrupt pins (INT3–INT0). The second is an internal maskable watchdog timer interrupt. The third is an internal interrupt from the asynchronous serial port.

The five maskable interrupt request pins can be used as direct interrupt requests. Plus, INT3–INT0 can be cascaded with an 82C59A-compatible external interrupt controller if more inputs are needed. An external interrupt controller can be used as the system master by programming the internal interrupt controller to operate in slave mode. In all cases, nesting can be enabled so that service routines for lower priority interrupts are interrupted by a higher priority interrupt.

Programming the Interrupt Control Unit

The Am186ER and Am188ER microcontrollers provide two methods for masking and unmasking the maskable interrupt sources. Each interrupt source has an interrupt control register (offsets 32h–44h) that contains a mask bit specific to that interrupt. In addition, the Interrupt Mask Register (offset 28h) is provided as a single source to access all of the mask bits. While changing a mask bit in either the mask register or the individual register will change the corresponding mask bit in the other register, there is a difference in exactly how the mask is updated.

If the Interrupt Mask Register is written while interrupts are enabled, it is possible that an interrupt could occur while the register is in an undefined state. This can cause interrupts to be accepted even though they were masked both before and after the write to the Interrupt Mask Register. Therefore, the Interrupt Mask Register should only be written when interrupts are disabled. Mask bits in the individual interrupt control registers can be written while interrupts are enabled, and there will be no erroneous interrupt operation.

TIMER CONTROL UNIT

There are three 16-bit programmable timers in the Am186ER and Am188ER microcontrollers. Timer 0 and timer 1 are connected to four external pins (each has an input and an output). These two timers can be used to count, time external events, or generate nonrepetitive or variable-duty-cycle waveforms. In addition, timer 1 can be configured as a watchdog timer interrupt.

Note that a hardware watchdog timer (WDT) has been added to the Am186ER and Am188ER microcontrollers. Use of the WDT is recommended for applications requiring this reset functionality. To maintain compatibility with previous versions of the Am186ER and Am188ER microcontrollers, Timer 1 can be configured as a watchdog timer and can generate a maskable watchdog timer interrupt. The maskable watchdog timer interrupt provides a mechanism for detecting software crashes or hangs. The TMROUT1 output is internally connected to the watchdog timer interrupt. The TIMER1 Count Register must then be reloaded at intervals less than the TIMER1 max count to assure the watchdog interrupt is not taken.

If the code crashes or hangs, the TIMER1 countdown will cause a watchdog interrupt.

Timer 2 is not connected to any external pins. It can be used for real-time coding and time-delay applications. It can also be used as a prescale to timers 0 and 1, or as a DMA request source.

The timers are controlled by eleven 16-bit registers in the peripheral control block. A timer's timer-count register contains the current value of that timer. The timer-count register can be read or written with a value at any time, whether the timer is running or not. The microcontroller increments the value of the timer-count register each time a timer event occurs.

Each timer also has a maximum-count register that defines the maximum value the timer will reach. When the timer reaches the maximum value, it resets to 0 during the same clock cycle—the value in the maximum-count register is never stored in the timer-count register. Also, timers 0 and 1 have a secondary maximum-count register. Using both the primary and secondary maximum-count registers lets the timer alternate between two maximum values.

If the timer is programmed to use only the primary maximum-count register, the timer output pin switches Low for one clock cycle after the maximum value is reached. If the timer is programmed to use both of its maximum-count registers, the output pin indicates which maximum-count register is currently in control, thereby creating a waveform. The duty cycle of the waveform depends on the values in the maximum-count registers.

Each timer is serviced every fourth clock cycle, so a timer can operate at a speed of up to one-quarter the internal clock frequency. A timer can be clocked externally at this same frequency; however, because of internal synchronization and pipelining of the timer circuitry, the timer output may take up to six clock cycles to respond to the clock or gate input.

WATCHDOG TIMER

The Am186ER/Am188ER microcontrollers provide a hardware watchdog timer. The Watchdog Timer (WDT) can be used to regain control of the system when software fails to respond as expected. The WDT is inactive after reset. It can be modified only once by a keyed sequence of writes to the Watchdog Timer Control Register (WDTCON) following reset. This single write can either disable the timer or modify the timeout period and the action taken upon timeout. A keyed sequence is also required to reset the current WDT count. This behavior ensures that randomly executing code will not prevent a WDT event from occurring.

The WDT supports up to a 1.34-second timeout period in a 50-MHz system.

The WDT can be configured to cause either an NMI interrupt or a system reset upon timeout. If the WDT is configured for NMI, the NMIFLAG in the WDTCON Register is set when the NMI is generated. The NMI interrupt service routine (ISR) should examine this flag to determine if the interrupt was generated by the WDT or by an external source. If the NMIFLAG is set, the ISR should clear the flag by writing the correct keyed sequence to the WDTCON Register. If the NMIFLAG is set when a second WDT timeout occurs, a WDT system reset is generated rather than a second NMI event.

When the processor takes a WDT reset, either because of a single WDT event with the WDT configured to generate resets or due to a WDT event with the NMIFLAG set, the RSTFLAG in the WDTCON Register is set. This allows system initialization code to differentiate between a hardware reset and a WDT reset and take appropriate action. The RSTFLAG is cleared when the WDTCON Register is read or written. The processor does not resample external pins during a WDT reset. This means that the clocking, the Reset Configuration Register, and any other features that are user-selectable during reset do not change when a WDT system reset occurs. PIO Mode and PIO Direction registers are not affected and PIO data is undefined. All other activities are identical to those of a normal system reset.

Note: *The Watchdog Timer (WDT) is inactive after reset.*

DIRECT MEMORY ACCESS

Direct memory access (DMA) permits transfer of data between memory and peripherals without CPU involvement. The DMA unit in the Am186ER and Am188ER microcontrollers, shown in Figure 13, provides two high-speed DMA channels. Data transfers can occur between memory and I/O spaces (e.g., memory to I/O) or within the same space (e.g., memory-to-memory or I/O-to-I/O). Additionally, bytes (also words on the Am186ER microcontroller) can be transferred to or from even or odd addresses. Only two bus cycles (a minimum of eight clocks) are necessary for each data transfer.

Each channel accepts a DMA request from one of the four sources: the channel request pin (DRQ1–DRQ0), Timer 2, a serial port, or system software. The two DMA channels can be programmed with different priorities to resolve simultaneous DMA requests, and transfers on one channel can interrupt the other channel.

The DMA channels can be directly connected to the asynchronous serial port. DMA and serial port transfer is accomplished by programming the DMA controller to perform transfers between a data source in memory or I/O space and a serial port transmit or receive register.

DMA Operation

Each channel has six registers in the peripheral control block that define specific channel operations. The DMA registers consist of a 20-bit source address (two registers), a 20-bit destination address (two registers), a 16-bit transfer count register, and a 16-bit control register.

The DMA transfer count register (DTC) specifies the number of DMA transfers to be performed. Up to 64K transfers can be performed with automatic termination. The DMA control registers define the channel operation. All registers can be modified during any DMA activity. Any changes made to the DMA registers are reflected immediately in DMA operation.

The Am188ER microcontroller's maximum DMA transfer rates are half that of those listed in Table 9 for the Am186ER microcontroller.

Table 9. Am186ER Microcontroller Maximum DMA Transfer Rates

Synchronization Type	Maximum DMA Transfer Rate (Mbyte/s)			
	50 MHz	40 MHz	33 MHz	25 MHz
Unsynchronized	12.5	10	8.25	6.25
Source Synch	12.5	10	8.25	6.25
Destination Synch (CPU needs bus)	8.33	6.6	5.5	4.16
Destination Synch (CPU does not need bus)	10.00	8	6.6	5

Asynchronous Serial Port/DMA Transfers

The enhanced Am186ER/Am188ER microcontrollers can DMA to and from the asynchronous serial port. This is accomplished by programming the DMA controller to perform transfers between a data buffer (located either in memory or I/O space) and an asynchronous serial port data register (SPTD or SPRD). Note that when a DMA channel is in use by the asynchronous serial port, the corresponding external DMA request signal is deactivated.

For DMA *to* the asynchronous serial port, the transmit data register address, either I/O-mapped or memory-mapped, should be specified as a byte destination for the DMA by writing the address of the register into the DMA destination low and DMA destination high registers. The destination address (the address of the transmit data register) should be configured as a constant throughout the DMA operation. The asynchronous serial port transmitter acts as the synchronizing device; therefore, the DMA channel should be configured as destination-synchronized.

For DMA *from* the asynchronous serial port, the receive data register address, either I/O-mapped or memory-mapped, should be specified as a byte source for the DMA by writing the address of the register into the DMA Source and DMA Source High registers. The source address (the address of the receive data register) should be configured as a constant throughout the DMA. The asynchronous serial port receiver acts as the synchronizing device; therefore, the DMA channel should be configured as source- synchronized.

DMA Channel Control Registers

Each DMA control register determines the mode of operation for the particular DMA channel. This register specifies the following:

- Mode of synchronization
- Whether bytes or words are transferred (Am186ER microcontroller only)
- Whether an interrupt is generated after the last transfer
- Whether DMA activity ceases after a programmed number of DMA cycles
- Relative priority of the DMA channel with respect to the other DMA channel
- Whether the source address is incremented, decremented, or maintained constant after each transfer
- Whether the source address addresses memory or I/O space
- Whether the destination address is incremented, decremented, or maintained constant after transfers
- Whether the destination address addresses memory or I/O space

DMA Priority

The DMA channels can be programmed so that one channel is always given priority over the other, or they can be programmed to alternate cycles when both have DMA requests pending. DMA cycles always have priority over internal CPU cycles, except between locked memory accesses or word accesses to odd memory locations. However, an external bus hold takes priority over an internal DMA cycle.

Because an interrupt request, other than an NMI, cannot suspend a DMA operation and the CPU cannot access memory during a DMA cycle, interrupt latency time suffers during sequences of continuous DMA cycles. An NMI request, however, causes all internal DMA activity to halt. This allows the CPU to respond quickly to the NMI request.

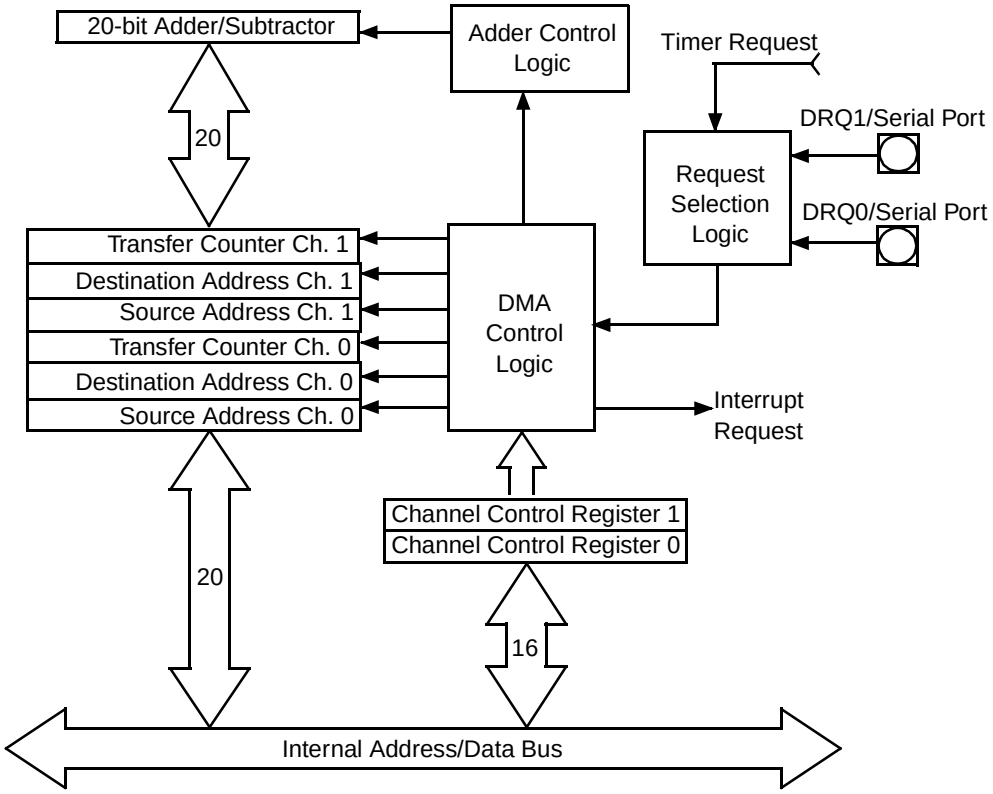


Figure 13. DMA Unit Block Diagram

ASYNCHRONOUS SERIAL PORT

The Am186ER and Am188ER microcontrollers provide an asynchronous serial port. The asynchronous serial port is a two-pin interface that permits full-duplex bidirectional data transfer. The asynchronous serial port supports the following features:

- Full-duplex operation
- 7-bit or 8-bit data transfers
- Odd, even, or no parity
- 1 or 2 stop bits

If additional RS-232 signals are required, they can be created with available PIO pins. The asynchronous serial port transmit and receive sections are double buffered. Break character, framing, parity, and overrun error detection are provided. Exception interrupt generation is programmable by the user.

The transmit/receive clock is based on the internal processor clock, which is divided down internally to the serial port operating frequency. The serial port permits 7-bit and 8-bit data transfers. DMA transfers using the serial port are supported.

The serial port generates one interrupt for any of three serial port events—transmit complete, data received, and receive error.

The serial port can be used in power-save mode, but the software must adjust the transfer rate to correctly reflect the new internal operating frequency and must ensure that the serial port does not receive any information while the frequency is being changed.

DMA Transfers through the Serial Port

The DMA channels can be directly connected to the asynchronous serial port. DMA and serial port transfer is accomplished by programming the DMA controller to perform transfers between a memory or I/O space and a serial port transmit or receive register. For more information see the DMA control register descriptions in the *Am186ER and Am188ER Microcontrollers User's Manual*, order #21684.

SYNCHRONOUS SERIAL INTERFACE

The synchronous serial interface (SSI) enables the Am186ER and Am188ER microcontrollers to communicate with application-specific integrated circuits (ASICs) that require reprogrammability but are short on pins. This four-pin interface permits half-duplex, bidirectional data transfer at speeds of up to 25 Mbit/s.

Unlike the asynchronous serial port, the SSI operates in a master/slave configuration. The Am186ER and Am188ER microcontrollers are the master ports.

The SSI interface provides four pins for communicating with system components: two enables (SDEN0 and SDEN1), a clock (SCLK), and a data pin (SDATA). Five

registers are used to control and monitor the interface. Refer to Figure 14 and Figure 15 on page 58 for diagrams of SSI reads and writes.

Four-Pin Interface

The two enable pins SDEN1–SDEN0 can be used directly as enables for up to two peripheral devices.

Transmit and receive operations are synchronized between the master (Am186ER or Am188ER microcontroller) and slave (peripherals) by means of the SCLK output. SCLK is derived from the internal processor clock and is the processor clock divided by 2, 4, 8, or 16.

PROGRAMMABLE I/O (PIO) PINS

There are 32 pins on the Am186ER and Am188ER microcontrollers that are available as multipurpose signals. Table 3 and Table 4 on page 36 list the PIO pins. Each of these pins can be used as a user-programmable input or output signal if the normal shared function is not needed.

If a pin is enabled to function as a PIO signal, the preassigned signal function is disabled and does not affect the level on the pin. A PIO signal can be configured to operate as an input (with or without a weak pullup or pulldown), as an output, or as an open-drain output. Configuration as an open-drain output is accomplished by keeping the appropriate PDATA bits constant in the PIO data register and writing the data value into its associated bit position in the PIO direction register, so the output is either driving Low or is disabled, depending on the data.

After power-on reset, the PIO pins default to various configurations. The column titled *Power-On Reset Status* in Table 3 and Table 4 on page 36 lists the defaults for the PIOs. The system initialization code must reconfigure the PIOs as required.

Note: *WDT reset does not reset PIO registers.*

The A19–A17 address pins default to normal operation on power-on reset, allowing the processor to correctly begin fetching instructions at the boot address FFFF0h. The DT/$\overline{R}$, $\overline{DEN}$, and SRDY pins also default to normal operation on power-on reset.

Note that emulators use A19, A18, A17, S6, and $\overline{UZI}$. System designers using these signals as PIOs should check with their emulator vendor for limitations on emulator operation.

If the AD15–AD0 bus override is enabled on power-on reset, then S6/$\overline{CLKSEL2}$ and $\overline{UZI}$/$\overline{CLKSEL1}$ revert to normal operation instead of PIO input with pullup. Many emulators assert the $\overline{ADEN}$ override. If $\overline{BHE}$/$\overline{ADEN}$ (Am186ER microcontroller) or $\overline{RFSH2}$/$\overline{ADEN}$ (Am188ER microcontroller) is held Low during power-on reset, the AD15–AD0 bus override is enabled.

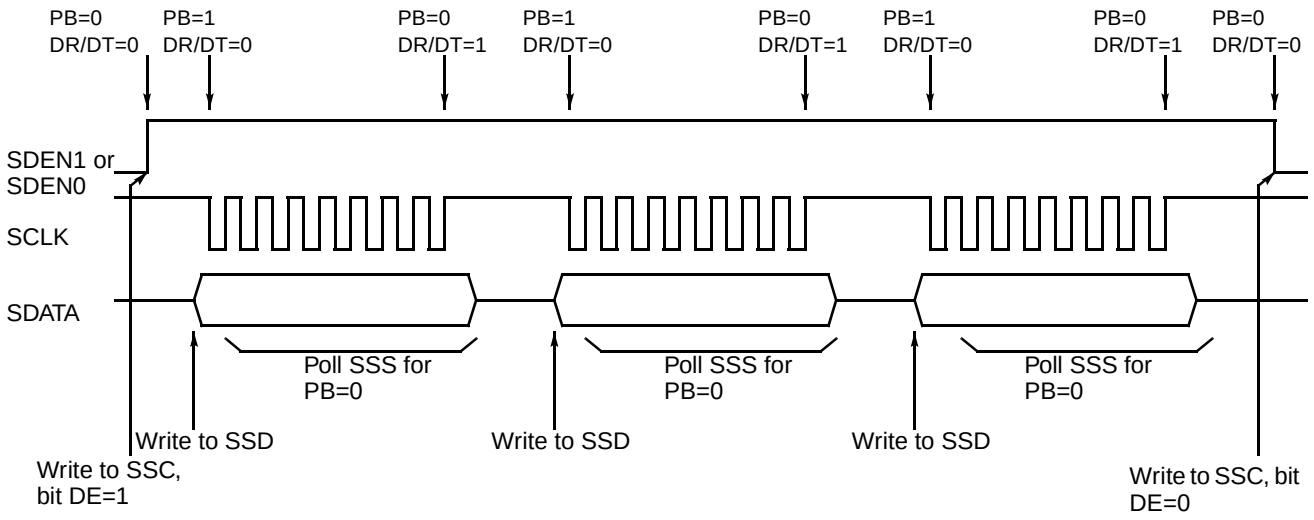


Figure 14. Synchronous Serial Interface Multiple Write

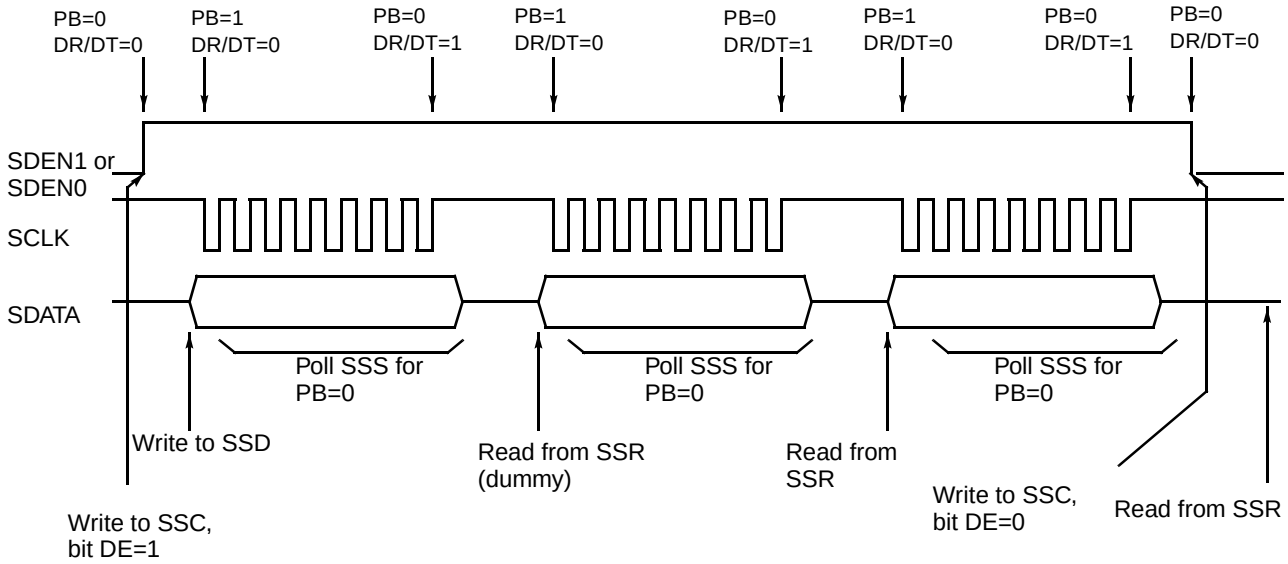


Figure 15. Synchronous Serial Interface Multiple Read

LOW-VOLTAGE OPERATION

The low-voltage operation of the Am186ER and Am188ER microcontrollers is an enabling technology for the design of portable systems with long battery life. This capability, combined with CPU clock management, enables design of very low-power computing systems.

Low-Voltage Standard

Industry standards for low-voltage operation are emerging to facilitate the design of components that will make up a complete low-voltage system. As a guideline, the Am186ER and Am188ER microcontroller specifications follow the first article or regulated version of the JEDEC 8.0 low-voltage proposal. This standard proposal calls for a V_{CC} range of 3.3 V ± 10%.

Power Savings

CMOS dynamic power consumption is proportional to the square of the operating voltage multiplied by capacitance and operating frequency. Static CPU operation can reduce power consumption by enabling the system designer to reduce operating frequency when possible. However, operating voltage is always the dominant factor in power consumption. By reducing the operating voltage from 5 V to 3.3 V for any device, the power consumed is reduced by 56%.

Reduction of CPU and core logic operating voltage dramatically reduces overall system power consumption. Additional power savings can be realized as low-voltage mass storage and peripheral devices become available.

Two basic strategies exist in designing systems containing the Am186ER and Am188ER microcontrollers. The first strategy is to design a homogenous system in which all logic components operate at 3.3 V. This provides the lowest overall power consumption. However, system designers may need to include devices for which 3.3-V versions are not available. In the second strategy, the system designer must then design a mixed 5-V/3.3-V system. This compromise enables the system designer to minimize the core logic power consumption while still including functionality of the 5-V features. The choice of a mixed voltage system design also involves balancing design complexity with the need for the additional features.

Input/Output Circuitry

To accommodate current 5-V systems, the Am186ER and Am188ER microcontrollers have 5-V tolerant I/O drivers. The drivers produce TTL-compatible drive output (minimum 2.4-V logic High) and receive TTL and CMOS levels (up to V_{CC} + 2.6 V). The following are some design issues that should be considered when upgrading an Am186ER microcontroller 5-V design:

- During power-up, if the 3.3-V supply has a significant delay in achieving stable operation relative to 5-V supply, then the 5-V circuitry in the system may start driving the processor's inputs above the maximum levels (V_{CC} + 2.6 V). The system design should ensure that the 5-V supply does not exceed 2.6 V above the 3.3-V supply during a power-on sequence.
- Preferably, all inputs will be driven by sources that can be three-stated during a system reset condition. The system reset condition should persist until stable V_{CC} conditions are met. This should help ensure that the maximum input levels are not exceeded during power-up conditions.
- Preferably, all pullup resistors will be tied to the 3.3-V supply, which will ensure that inputs requiring pullups are not over stressed during power-up.

ABSOLUTE MAXIMUM RATINGS

Temperature under bias:

Commercial (T_C) ..... 0°C to + 100°C

Storage temperature ..... –65°C to + 125°C

Voltage on any pin with respect to ground ..... –0.5 V to V_{CC} + 2.6 V*

Notes:

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

**X1 and X2 are not 5-V-tolerant and have a range of –0.5 V to V_{CC}.*

OPERATING RANGES

T_C (Commercial) ..... 0°C to +100°C

Industrial* (T_A) ..... –40°C to + 85°C

V_{CC} up to 50 MHz ..... 3.3 V ± 0.3 V

Where: T_C = case temperature
T_A = ambient temperature

Notes:

Operating Ranges define those limits between which the functionality of the device is guaranteed.

**Industrial versions of Am186ER and Am188ER microcontrollers are available in 25- and 33-MHz operating frequencies only.*

DC CHARACTERISTICS OVER COMMERCIAL AND INDUSTRIAL OPERATING RANGES

Symbol	Parameter Description	Notes	Preliminary		Unit
			Min	Max	
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 2.6	V
V_{IH}	Clock Input High Voltage (X2, X1)			V_{CC}	V
V_{OL}	Output Low Voltage	I_{OL} = 4.0 mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = –1.0 mA	2.4		V
I_{CC}	Power Supply Current	Note 8		5.0	mA/ MHz
I_{LI}	Input Leakage Current	Note 1 Note 2		±15 ±50	µA
I_{IH}	Input Leakage Current	Note 3		200	µA
I_{IL}	Input Leakage Current	Note 4		–400	µA
I_{LO}	Output Leakage Current	Note 5 Note 6		±15 ±50	µA
C_{IN}	Input Capacitance	F_C=1 MHz (Note 7)		10	pF
C_{OUT}	I/O Capacitance	F_C=1 MHz (Note 7)		14	pF

Notes:

1. *This parameter is for inputs without pullup or pulldown resistors and for which 0 ≤ V_{IN} ≤ V_{CC}.*
2. *This parameter is for inputs without pullup or pulldown resistors and for which 0 ≤ V_{IN} ≤ 5 V.*
3. *This parameter is for inputs with pulldown resistors and for which V_{IH} = 2.4 V.*
4. *This parameter is for inputs with pullup resistors and for which V_{IL} = 0.45 V.*
5. *This parameter is for three-state outputs where V_{EXT} is driven on the three-state output and 0 ≤ V_{EXT} ≤ V_{CC}.*
6. *This parameter is for three-state outputs where V_{EXT} is driven on the three-state output and 0 ≤ V_{EXT} ≤ 5 V.*
7. *This parameter has not been fully tested.*
8. *Current is measured with the device in RESET with X1 and X2 driven and all other non-power pins open but held High or Low.*

THERMAL CHARACTERISTICS

TQFP Package

The Am186ER and Am188ER microcontrollers are specified for operation with case temperature ranges from 0°C to +100°C for a commercial temperature device. Case temperature is measured at the top center of the package as shown in Figure 16. The various temperatures and thermal resistances can be determined using the equations in Figure 17 with information given in Table 10.

θ_{JA} is the sum of θ_{JC} and θ_{CA} . θ_{JC} is the internal thermal resistance of the assembly. θ_{CA} is the case to ambient thermal resistance.

The variable P is power in watts. Typical power supply current (I_{CC}) for the Am186ER and Am188ER microcontrollers is 3.7 mA per MHz of clock frequency.

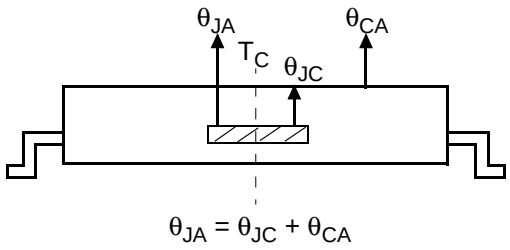


Figure 16. Thermal Resistance (°C/Watt)

$$\theta_{JA} = \theta_{JC} + \theta_{CA}$$
$$P = I_{CC} \cdot \text{freq (MHz)} \cdot V_{CC}$$
$$T_J = T_C + (P \cdot \theta_{JC})$$
$$T_J = T_A + (P \cdot \theta_{JA})$$
$$T_C = T_J - (P \cdot \theta_{JC})$$
$$T_C = T_A + (P \cdot \theta_{CA})$$
$$T_A = T_J - (P \cdot \theta_{JA})$$
$$T_A = T_C - (P \cdot \theta_{CA})$$

Figure 17. Thermal Characteristics Equations

Table 10. Thermal Characteristics (°C/Watt)

Package/Board	Airflow (Linear Feet per Minute)	θ_{JC}	θ_{CA}	θ_{JA}
PQFP/2-Layer	0 fpm	7	38	45
	200 fpm	7	32	39
	400 fpm	7	28	35
	600 fpm	7	26	33
TQFP/2-Layer	0 fpm	10	46	56
	200 fpm	10	36	46
	400 fpm	10	30	40
	600 fpm	10	28	38
PQFP/4-Layer to 6-Layer	0 fpm	5	18	23
	200 fpm	5	16	21
	400 fpm	5	14	19
	600 fpm	5	12	17
TQFP/4-Layer to 6-Layer	0 fpm	6	24	30
	200 fpm	6	22	28
	400 fpm	6	20	26
	600 fpm	6	18	24

Typical Ambient Temperatures

The typical ambient temperature specifications are based on the following assumptions and calculations:

The commercial operating range of the Am186ER and Am188ER microcontrollers is a case temperature T_C of 0 to 100 degrees Centigrade. T_C is measured at the top center of the package. An increase in the ambient temperature causes a proportional increase in T_C.

The 50-MHz microcontroller is specified as 3.3 V, plus or minus 10%. Therefore, 3.6 V is used for calculating typical power consumption on the 50-MHz microcontroller.

Typical power supply current (I_{CC}) in normal usage is estimated at 3.7 mA per MHz of microcontroller clock rate.

Typical power consumption can be calculated using the following formula:

(Watts) = (3.7 mA/MHz) · 50 MHz · (3.6 V/1000)

Table 11 shows the variables that are used to calculate the typical power consumption value for each version of the Am186ER and Am188ER microcontrollers.

Table 11. Typical Power Consumption Calculation

$P = MHz \cdot I_{CC} \cdot Volts / 1000$			Typical Power (P) in Watts
MHz	Typical I_{CC}	Volts	
50	3.7	3.6	0.662
40	3.7	3.6	0.522
33	3.7	3.6	0.432
25	3.7	3.6	0.342

Thermal resistance is a measure of the ability of a package to remove heat from a semiconductor device. A safe operating range for the device can be calculated using the following formulas from Figure 17 and the variables in Table 10.

By using the maximum case rating T_C, the typical power consumption value from Table 11, and θ_{JC} from Table 10, the junction temperature T_J can be calculated by using the following formula from Figure 17.

$T_J = T_C + (P \cdot \theta_{JC})$

Table 12 shows T_J values for the various versions of the Am186ER and Am188ER microcontrollers. The Speed/Pkg/Board column in Table 12 indicates the clock speed in MHz, the type of package (P for PQFP and T for TQFP), and the type of board (2 for 2-layer and 4–6 for 4-layer to 6-layer).

Table 12. Junction Temperature Calculation

Speed/ Pkg/ Board	$T_J = T_C + (P \cdot \theta_{JC})$			
	T_C	P	θ_{JC}	T_J
50/P2	100	0.662	7	104.6
50/T2	100	0.662	10	106.6
50/P4–6	100	0.662	5	103.3
50/T4–6	100	0.662	6	104.0
40/P2	100	0.522	7	103.7
40/T2	100	0.522	10	105.2
40/P4–6	100	0.522	5	102.6
40/T4–6	100	0.522	6	103.1
33/P2	100	0.432	7	103.0
33/T2	100	0.432	10	104.3
33/P4–6	100	0.432	5	102.2
33/T4–6	100	0.432	6	102.6
25/P2	100	0.342	7	102.4
25/T2	100	0.342	10	103.4
25/P4–6	100	0.342	5	101.7
25/T4–6	100	0.342	6	102.1

By using T_J from Table 12, the typical power consumption value from Table 11, and a θ_{JA} value from Table 10, the typical ambient temperature T_A can be calculated using the following formula from Figure 17.

$T_A = T_J – (P \cdot \theta_{JA})$

For example, T_A for a 50-MHz PQFP design with a 2-layer board and 0 fpm airflow is calculated as follows:

$T_A = 104.6 – (0.662 \cdot 45)$
$T_A = 74.81$

In this calculation, T_J comes from Table 12, P comes from Table 11, and θ_{JA} comes from Table 10. See Table 13.

T_A for a 33-MHz TQFP design with a 4-layer to 6-layer board and 200 fpm airflow is calculated as follows:

$T_A = 102.6 – (0.432 \cdot 28)$
$T_A = 90.5$

See Table 16 for the result of this calculation.

Table 13 through Table 16 and Figure 18 through Figure 21 show T_A based on the preceding assumptions and calculations for a range of θ_{JA} values with airflow from 0 linear feet per minute to 600 linear feet per minute.

Table 13 shows typical maximum ambient temperatures in degrees Centigrade for a PQFP package used with a 2-layer board. The typical ambient temperatures are based on a 100-degree Centigrade maximum case temperature. Figure 18 illustrates the typical temperatures in Table 13.

Table 13. Typical Ambient Temperatures for PQFP with Two-Layer Board

Microcontroller Speed	Typical Power (Watts)	Linear Feet per Minute Airflow			
		0 fpm	200 fpm	400 fpm	600 fpm
50 MHz	0.662	74.81	78.8	81.43	82.8
40 MHz	0.522	80.2	83.3	85.4	86.5
33 MHz	0.432	83.56	86.2	87.9	88.7
25 MHz	0.342	87.0	89.1	90.4	91.1

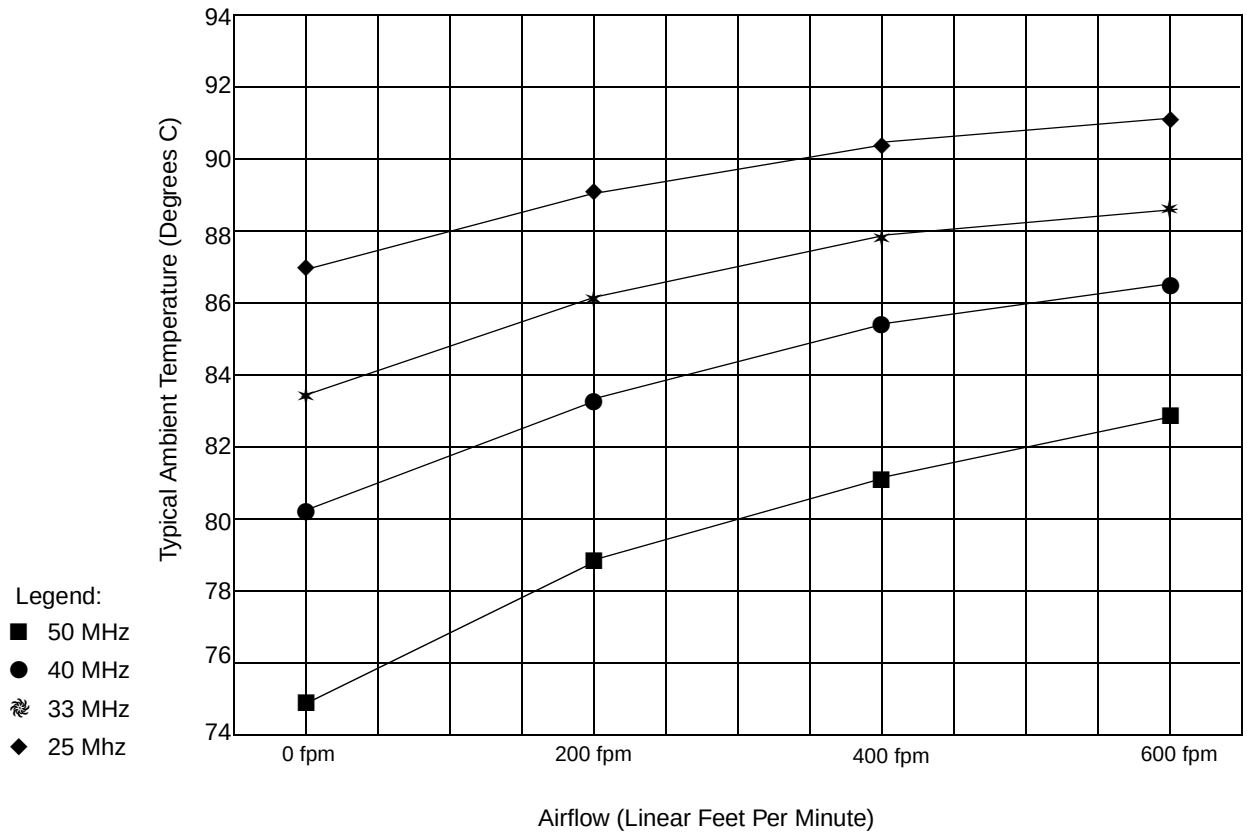


Figure 18. Typical Ambient Temperatures for PQFP with Two-Layer Board

Table 14 shows typical maximum ambient temperatures in degrees Centigrade for a TQFP package used with a 2-layer board. The typical ambient temperatures are based on a 100-degree Centigrade maximum case temperature. Figure 19 illustrates the typical temperatures in Table 14.

Table 14. Typical Ambient Temperatures for TQFP with Two-Layer Board

Microcontroller Speed	Typical Power (Watts)	Linear Feet per Minute Airflow			
		0 fpm	200 fpm	400 fpm	600 fpm
50 MHz	0.662	69.5	76.1	80.1	81.4
40 MHz	0.522	76.0	81.2	84.3	85.4
33 MHz	0.432	80.1	84.4	87.0	87.9
25 MHz	0.342	84.2	87.7	89.7	90.4

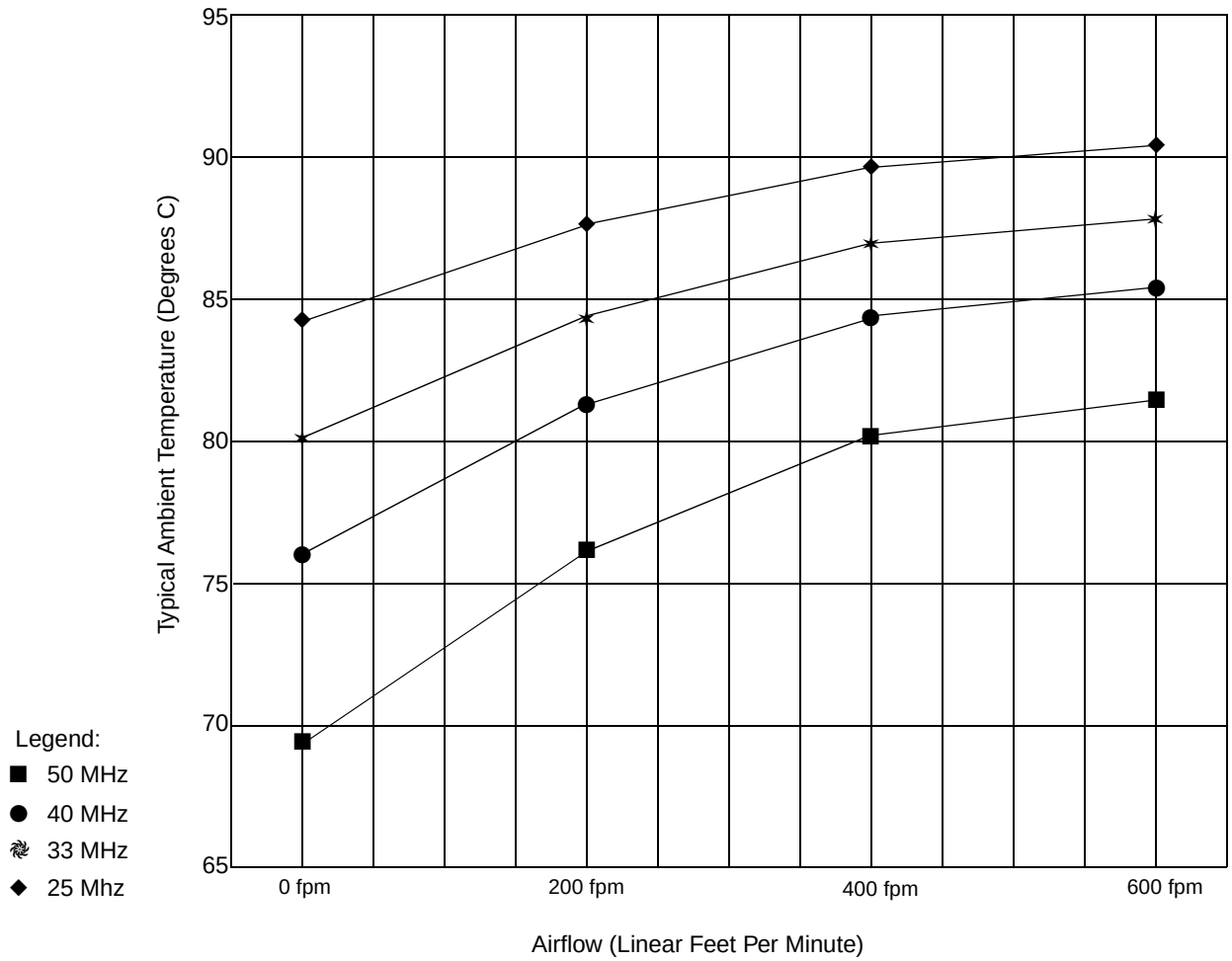


Figure 19. Typical Ambient Temperatures for TQFP with Two-Layer Board

Table 15 shows typical maximum ambient temperatures in degrees Centigrade for a PQFP package used with a 4-layer to 6-layer board. The typical ambient temperatures are based on a 100-degree Centigrade maximum case temperature. Figure 20 illustrates the typical temperatures in Table 15.

Table 15. Typical Ambient Temperatures for PQFP with Four-Layer to Six-Layer Board

Microcontroller Speed	Typical Power (Watts)	Linear Feet per Minute Airflow			
		0 fpm	200 fpm	400 fpm	600 fpm
50 MHz	0.662	88.0	89.4	90.7	92.0
40 MHz	0.522	90.6	91.6	92.7	93.7
33 MHz	0.432	92.3	93.1	93.9	94.9
25 MHz	0.342	93.8	94.5	95.2	95.9

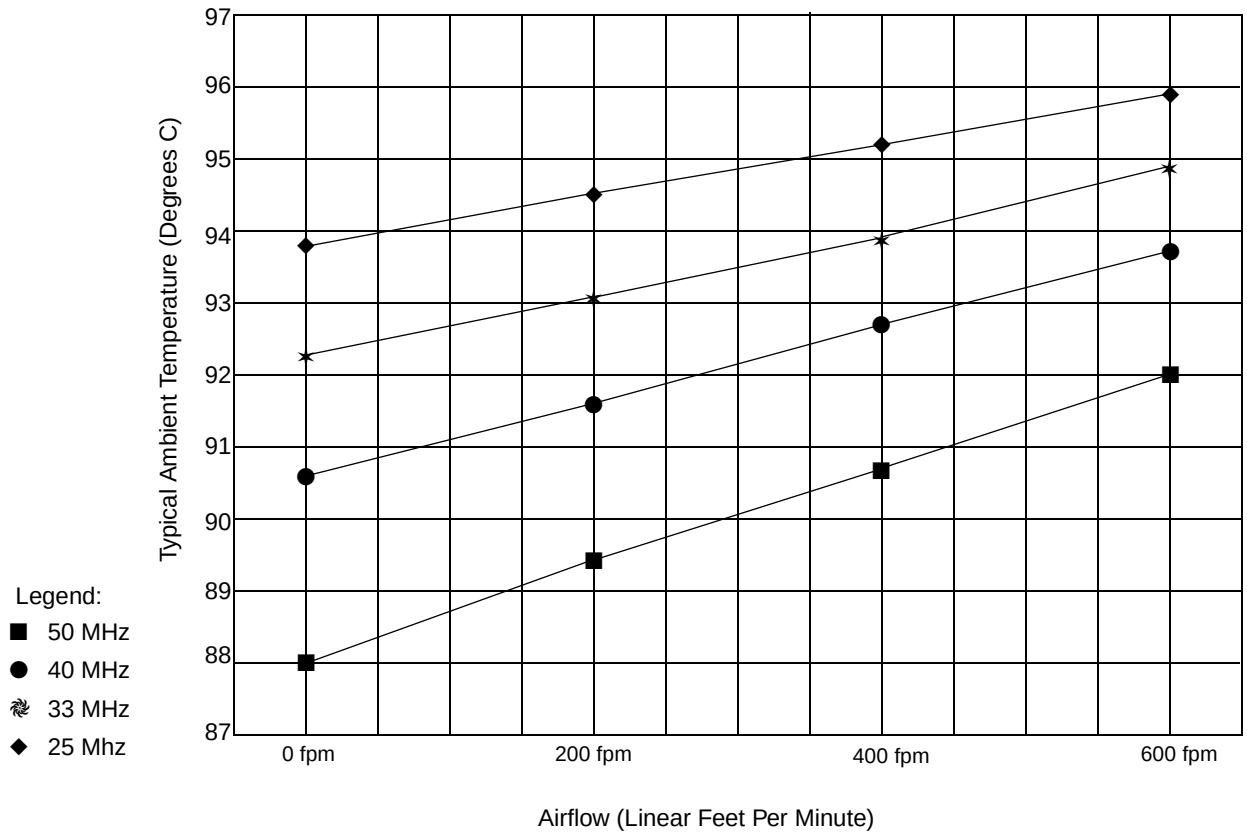


Figure 20. Typical Ambient Temperatures for PQFP with Four-Layer to Six-Layer Board

Table 16 shows typical maximum ambient temperatures in degrees Centigrade for a TQFP package used with a 4-layer to 6-layer board. The typical ambient temperatures are based on a 100-degree Centigrade maximum case temperature. Figure 21 illustrates the typical temperatures in Table 16.

Table 16. Typical Ambient Temperatures for TQFP with Four-Layer to Six-Layer Board

Microcontroller Speed	Typical Power (Watts)	Linear Feet per Minute Airflow			
		0 fpm	200 fpm	400 fpm	600 fpm
50 MHz	0.662	84.1	85.5	86.8	88.1
40 MHz	0.522	87.44	88.5	89.5	90.6
33 MHz	0.432	89.64	90.5	91.4	92.2
25 MHz	0.342	91.84	92.5	93.2	93.9

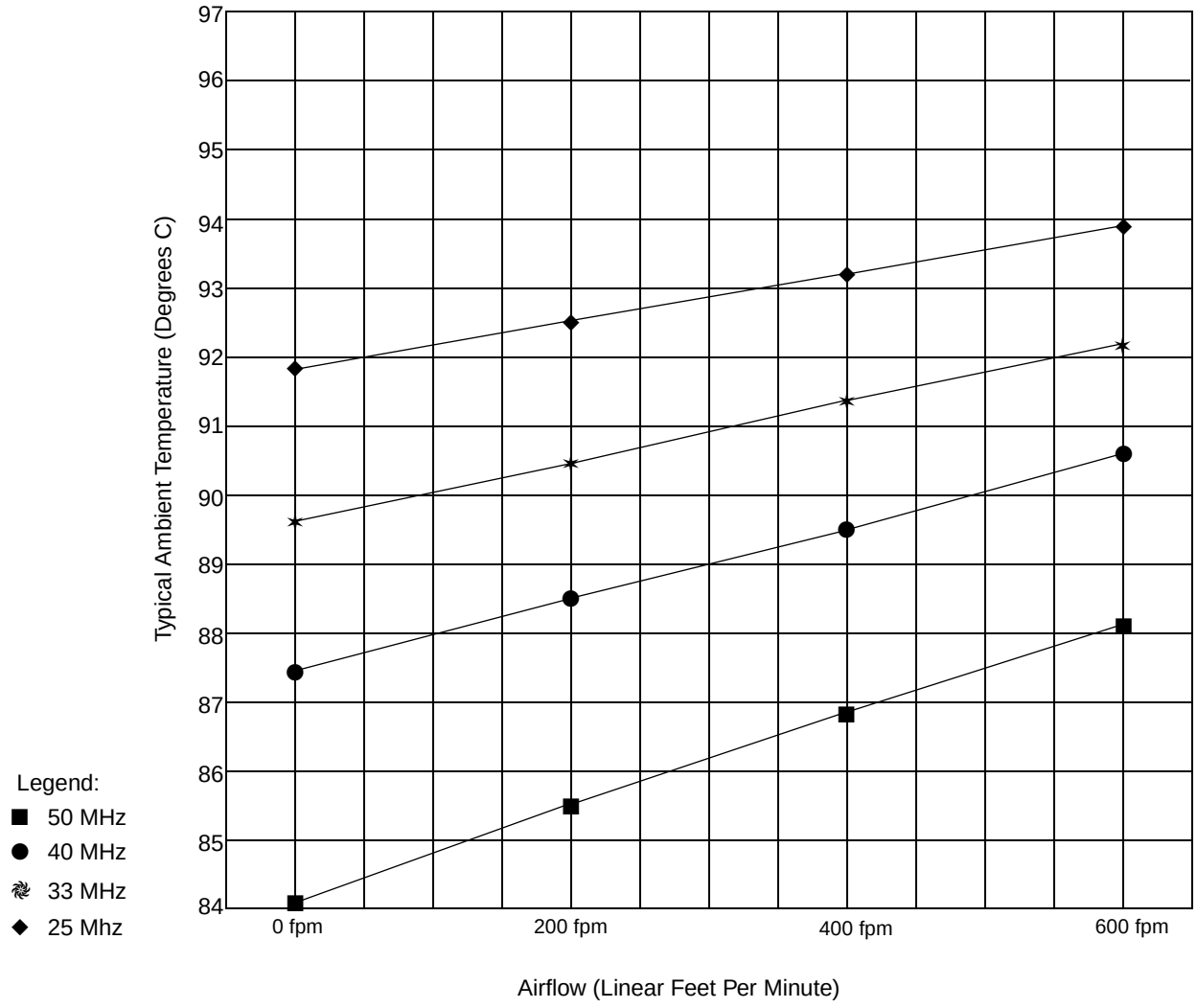


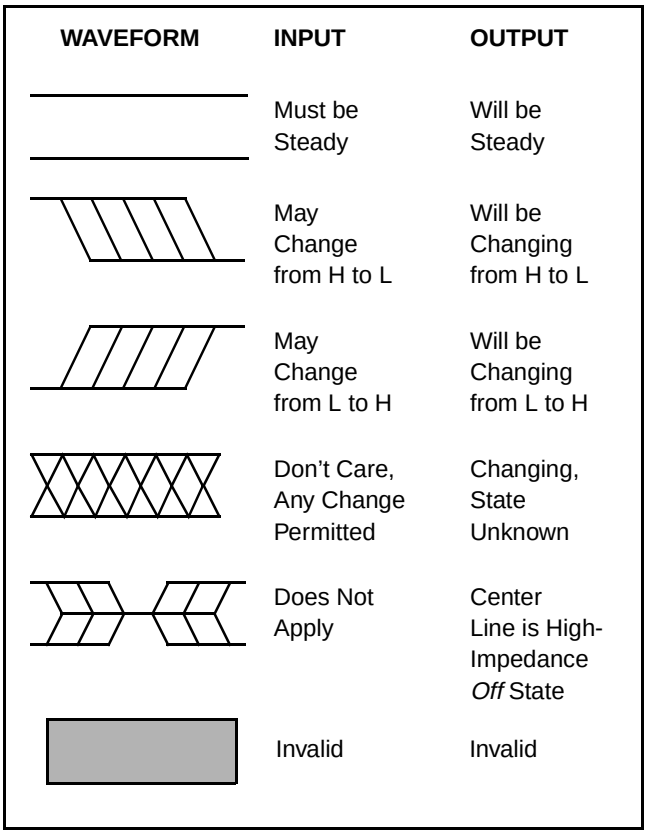
Figure 21. Typical Ambient Temperatures for TQFP with Four-Layer to Six-Layer Board

COMMERCIAL AND INDUSTRIAL SWITCHING CHARACTERISTICS AND WAVEFORMS

In the switching waveforms that follow, several abbreviations are used to indicate the specific periods of a bus cycle. These periods are referred to as time states. A typical bus cycle is composed of four consecutive time states: t_1, t_2, t_3, and t_4. Wait states, which represent multiple t_3 states, are referred to as t_w states. When no bus cycle is pending, an idle (t_i) state occurs.

In the switching parameter descriptions, the *multiplexed* address is referred to as the AD address bus; the *nonmultiplexed* address is referred to as the A address bus.

Key to Switching Waveforms



Alphabetical Key to Switching Parameter Symbols

Parameter Symbol	No.	Description	Parameter Symbol	No.	Description
t_{ARYCH}	49	ARDY Resolution Transition Setup Time	t_{CLDX}	2	Data in Hold
t_{ARYCHL}	51	ARDY Inactive Holding Time	t_{CLEV}	71	CLKOUTA Low to SDEN Valid
t_{ARYLCL}	52	ARDY Setup Time	t_{CLHAV}	62	HLDA Valid Delay
t_{AVBL}	87	A Address Valid to $\overline{WHB}$, $\overline{WLB}$ Low	t_{CLRF}	82	CLKOUTA High to $\overline{RFSH}$ Invalid
t_{AVCH}	14	AD Address Valid to Clock High	t_{CLRH}	27	$\overline{RD}$ Inactive Delay
t_{AVLL}	12	AD Address Valid to ALE Low	t_{CLRL}	25	$\overline{RD}$ Active Delay
t_{AVRL}	66	A Address Valid to $\overline{RD}$ Low	t_{CLSH}	4	Status Inactive Delay
t_{AVWL}	65	A Address Valid to $\overline{WR}$ Low	t_{CLSL}	72	CLKOUTA Low to SCLK Low
t_{AZRL}	24	AD Address Float to $\overline{RD}$ Active	t_{CLSRY}	48	SRDY Transition Hold Time
t_{CH1CH2}	45	CLKOUTA Rise Time	t_{CLTMV}	55	Timer Output Delay
t_{CHAV}	68	CLKOUTA High to A Address Valid	t_{COAOB}	83	CLKOUTA to CLKOUTB Skew
t_{CHCK}	38	X1 High Time	t_{CVCTV}	20	Control Active Delay 1
t_{CHCL}	44	CLKOUTA High Time	t_{CVCTX}	31	Control Inactive Delay
t_{CHCSV}	67	CLKOUTA High to $\overline{LCS}$/$\overline{UCS}$ Valid	t_{CVDEX}	21	$\overline{DEN}$ Inactive Delay
t_{CHCSX}	18	$\overline{MCS}$/$\overline{PCS}$ Inactive Delay	t_{CXCSX}	17	$\overline{MCS}$/$\overline{PCS}$ Hold from Command Inactive
t_{CHCTV}	22	Control Active Delay 2	t_{DVCL}	1	Data in Setup
t_{CHCV}	64	Command Lines Valid Delay (after Float)	t_{DVSH}	75	Data Valid to SCLK High
t_{CHCZ}	63	Command Lines Float Delay	t_{DXDL}	19	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low
t_{CHDX}	8	Status Hold Time	t_{HVCL}	58	HOLD Setup
t_{CHLH}	9	ALE Active Delay	t_{INVCH}	53	Peripheral Setup Time
t_{CHLL}	11	ALE Inactive Delay	t_{INVCL}	54	DRQ Setup Time
t_{CHRFD}	79	CLKOUTA High to $\overline{RFSH}$ Valid	t_{LCRF}	86	$\overline{LCS}$ Inactive to $\overline{RFSH}$ Active Delay
t_{CHSV}	3	Status Active Delay	t_{LHAV}	23	ALE High to Address Valid
t_{CICOA}	69	X1 to CLKOUTA Skew	t_{LHLL}	10	ALE Width
t_{CICOB}	70	X1 to CLKOUTB Skew	t_{LLAX}	13	AD Address Hold from ALE Inactive
t_{CKHL}	39	X1 Fall Time	t_{LOCK}	61	Maximum PLL Lock Time
t_{CKIN}	36	X1 Period	t_{LRLL}	84	$\overline{LCS}$ Precharge Pulse Width
t_{CKLH}	40	X1 Rise Time	t_{RESIN}	57	$\overline{RES}$ Setup Time
t_{CL2CL1}	46	CLKOUTA Fall Time	t_{RFCY}	85	$\overline{RFSH}$ Cycle Time
t_{CLARX}	50	ARDY Active Hold Time	t_{RHAV}	29	$\overline{RD}$ Inactive to AD Address Active
t_{CLAV}	5	AD Address Valid Delay	t_{RHDX}	59	$\overline{RD}$ High to Data Hold on AD Bus
t_{CLAX}	6	Address Hold	t_{RHLH}	28	$\overline{RD}$ Inactive to ALE High
t_{CLAZ}	15	AD Address Float Delay	t_{RLRH}	26	$\overline{RD}$ Pulse Width
t_{CLCH}	43	CLKOUTA Low Time	t_{SHDX}	77	SCLK High to SPI Data Hold
t_{CLCK}	37	X1 Low Time	t_{SLDV}	78	SCLK Low to SPI Data Valid
t_{CLCL}	42	CLKOUTA Period	t_{SRYCL}	47	SRDY Transition Setup Time
t_{CLCLX}	80	$\overline{LCS}$ Inactive Delay	t_{WHDEX}	35	$\overline{WR}$ Inactive to $\overline{DEN}$ Inactive
t_{CLCSL}	81	$\overline{LCS}$ Active Delay	t_{WHDX}	34	Data Hold after $\overline{WR}$
t_{CLCSV}	16	$\overline{MCS}$/$\overline{PCS}$ Active Delay	t_{WHLH}	33	$\overline{WR}$ Inactive to ALE High
t_{CLDOX}	30	Data Hold Time	t_{WLWH}	32	$\overline{WR}$ Pulse Width
t_{CLDV}	7	Data Valid Delay			

Notes:

The following parameters are not defined or used at this time: 41, 56, 60, 73, 74, and 76.

Numerical Key to Switching Parameter Symbols

Number	Parameter Symbol	Description	Number	Parameter Symbol	Description
1	t_{DVCL}	Data in Setup	43	t_{CLCH}	CLKOUTA Low Time
2	t_{CLDX}	Data in Hold	44	t_{CHCL}	CLKOUTA High Time
3	t_{CHSV}	Status Active Delay	45	t_{CH1CH2}	CLKOUTA Rise Time
4	t_{CLSH}	Status Inactive Delay	46	t_{CL2CL1}	CLKOUTA Fall Time
5	t_{CLAV}	AD Address Valid Delay	47	t_{SRYCL}	SRDY Transition Setup Time
6	t_{CLAX}	Address Hold	48	t_{CLSRY}	SRDY Transition Hold Time
7	t_{CLDV}	Data Valid Delay	49	t_{ARYCH}	ARDY Resolution Transition Setup Time
8	t_{CHDX}	Status Hold Time	50	t_{CLARX}	ARDY Active Hold Time
9	t_{CHLH}	ALE Active Delay	51	t_{ARYCHL}	ARDY Inactive Holding Time
10	t_{LHLL}	ALE Width	52	t_{ARYLCL}	ARDY Setup Time
11	t_{CHLL}	ALE Inactive Delay	53	t_{INVCH}	Peripheral Setup Time
12	t_{AVLL}	AD Address Valid to ALE Low	54	t_{INVCL}	DRQ Setup Time
13	t_{LLAX}	AD Address Hold from ALE Inactive	55	t_{CLTMV}	Timer Output Delay
14	t_{AVCH}	AD Address Valid to Clock High	57	t_{RESIN}	$\overline{RES}$ Setup Time
15	t_{CLAZ}	AD Address Float Delay	58	t_{HVCL}	HOLD Setup
16	t_{CLCSV}	$\overline{MCS}$/$\overline{PCS}$ Active Delay	59	t_{RHDX}	$\overline{RD}$ High to Data Hold on AD Bus
17	t_{CXCSX}	$\overline{MCS}$/$\overline{PCS}$ Hold from Command Inactive	61	t_{LOCK}	Maximum PLL Lock Time
18	t_{CHCSX}	$\overline{MCS}$/$\overline{PCS}$ Inactive Delay	62	t_{CLHAV}	HLDA Valid Delay
19	t_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low	63	t_{CHCZ}	Command Lines Float Delay
20	t_{CVCTV}	Control Active Delay 1	64	t_{CHCV}	Command Lines Valid Delay (after Float)
21	t_{CVDEX}	$\overline{DEN}$ Inactive Delay	65	t_{AVWL}	A Address Valid to $\overline{WR}$ Low
22	t_{CHCTV}	Control Active Delay 2	66	t_{AVRL}	A Address Valid to $\overline{RD}$ Low
23	t_{LHAV}	ALE High to Address Valid	67	t_{CHCSV}	CLKOUTA High to $\overline{LCS}$/$\overline{UCS}$ Valid
24	t_{AZRL}	AD Address Float to $\overline{RD}$ Active	68	t_{CHAV}	CLKOUTA High to Address Valid
25	t_{CLRL}	$\overline{RD}$ Active Delay	69	t_{CICOA}	X1 to CLKOUTA Skew
26	t_{RLRH}	$\overline{RD}$ Pulse Width	70	t_{CICOB}	X1 to CLKOUTB Skew
27	t_{CLRH}	$\overline{RD}$ Inactive Delay	71	t_{CLEV}	CLKOUTA Low to SDEN Valid
28	t_{RHLH}	$\overline{RD}$ Inactive to ALE High	72	t_{CLSL}	CLKOUTA Low to SCLK Low
29	t_{RHAV}	$\overline{RD}$ Inactive to AD address Active	75	t_{DVSH}	Data Valid to SCLK High
30	t_{CLDOX}	Data Hold Time	77	t_{SHDX}	SCLK High to SPI Data Hold
31	t_{CVCTX}	Control Inactive Delay	78	t_{SLDV}	SCLK Low to SPI Data Valid
32	t_{WLWH}	$\overline{WR}$ Pulse Width	79	t_{CHRFD}	CLKOUTA High to $\overline{RFSH}$ Valid
33	t_{WHLH}	$\overline{WR}$ Inactive to ALE High	80	t_{CLCLX}	$\overline{LCS}$ Inactive Delay
34	t_{WHDX}	Data Hold after $\overline{WR}$	81	t_{CLCSL}	$\overline{LCS}$ Active Delay
35	t_{WHDEX}	$\overline{WR}$ Inactive to $\overline{DEN}$ Inactive	82	t_{CLRF}	CLKOUTA High to $\overline{RFSH}$ Invalid
36	t_{CKIN}	X1 Period	83	t_{COAOB}	CLKOUTA to CLKOUTB Skew
37	t_{CLCK}	X1 Low Time	84	t_{LRLL}	$\overline{LCS}$ Precharge Pulse Width
38	t_{CHCK}	X1 High Time	85	t_{RFCY}	$\overline{RFSH}$ Cycle Time
39	t_{CKHL}	X1 Fall Time	86	t_{LCRF}	$\overline{LCS}$ Inactive to $\overline{RFSH}$ Active Delay
40	t_{CKLH}	X1 Rise Time	87	t_{AVBL}	A Address Valid to $\overline{WHB}$, $\overline{WLB}$ Low
42	t_{CLCL}	CLKOUTA Period			

Notes:

The following parameters are not defined or used at this time: 41, 56, 60, 73, 74, and 76.

Switching Characteristics over Commercial and Industrial Operating Ranges

Read Cycle (25 MHz and 33 MHz)

Parameter			Preliminary				Unit
			25 MHz		33 MHz		
No.	Symbol	Description	Min	Max	Min	Max	
General Timing Requirements							
1	t_{DVCL}	Data in Setup	10		8		ns
2	t_{CLDX}	Data in Hold(c)	3		3		ns
General Timing Responses							
3	t_{CHSV}	Status Active Delay	0	20	0	15	ns
4	t_{CLSH}	Status Inactive Delay	0	20	0	15	ns
5	t_{CLAV}	AD Address Valid Delay	0	20	0	15	ns
7	t_{CLDV}	Data Valid Delay	0	20	0	15	ns
8	t_{CHDX}	Status Hold Time	0		0		ns
9	t_{CHLH}	ALE Active Delay		20		15	ns
10	t_{LHLL}	ALE Width	$t_{CLCL}-10=30$		$t_{CLCL}-10=20$		ns
11	t_{CHLL}	ALE Inactive Delay		20		15	ns
12	t_{AVLL}	AD Address Valid to ALE Low(a)	t_{CLCH}		t_{CLCH}		ns
13	t_{LLAX}	AD Address Hold from ALE Inactive(a)	t_{CHCL}		t_{CHCL}		ns
14	t_{AVCH}	AD Address Valid to Clock High	0		0		ns
15	t_{CLAZ}	AD Address Float Delay	$t_{CLAX}=0$	20	$t_{CLAX}=0$	15	ns
16	t_{CLCSV}	$\overline{MCS}/\overline{PCS}$ Active Delay	0	20	0	15	ns
17	t_{CXCSX}	$\overline{MCS}/\overline{PCS}$ Hold from Command Inactive(a)	t_{CLCH}		t_{CLCH}		ns
18	t_{CHCSX}	$\overline{MCS}/\overline{PCS}$ Inactive Delay	0	20	0	15	ns
19	t_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low(a)	0		0		ns
20	t_{CVCTV}	Control Active Delay 1(b)	0	20	0	15	ns
21	t_{CVDEX}	$\overline{DEN}$ Inactive Delay	0	20	0	15	ns
22	t_{CHCTV}	Control Active Delay 2(b)	0	20	0	15	ns
23	t_{LHAV}	ALE High to Address Valid	15		10		ns
Read Cycle Timing Responses							
24	t_{AZRL}	AD Address Float to $\overline{RD}$ Active	0		0		ns
25	t_{CLRL}	$\overline{RD}$ Active Delay	0	20	0	15	ns
26	t_{RLRH}	$\overline{RD}$ Pulse Width	$2t_{CLCL}-15=65$		$2t_{CLCL}-15=45$		ns
27	t_{CLRH}	$\overline{RD}$ Inactive Delay	0	20	0	15	ns
28	t_{RHLH}	$\overline{RD}$ Inactive to ALE High(a)	$t_{CLCH}-3$		$t_{CLCH}-3$		ns
29	t_{RHAV}	$\overline{RD}$ Inactive to AD Address Active(a)	$t_{CLCL}-10=30$		$t_{CLCL}-10=20$		ns
59	t_{RHDX}	$\overline{RD}$ High to Data Hold on AD Bus(c)	0		0		ns
66	t_{AVRL}	A Address Valid to $\overline{RD}$ Low	$2t_{CLCL}-15=65$		$2t_{CLCL}-15=45$		ns
67	t_{CHCSV}	CLKOUTA High to $\overline{LCS}/\overline{UCS}$ Valid	0	20	0	15	ns
68	t_{CHAV}	CLKOUTA High to A Address Valid	0	20	0	15	ns

Notes:

All timing parameters are measured at $V_{CC}/2$ with 50 pF loading on CLKOUTA, unless otherwise noted. All output test conditions are with $C_L=50$ pF. For switching tests, $V_{IL}=0.3$ V and $V_{IH}=V_{CC}-0.3$ V.

a Testing is performed with equal loading on referenced pins.

b This parameter applies to the $\overline{DEN}$, $\overline{INTA1}$–$\overline{INTA0}$, $\overline{WR}$, $\overline{WHB}$, and $\overline{WLB}$ signals.

c If either spec 2 or spec 59 is met with respect to data hold time, the part will function correctly.

Switching Characteristics over Commercial and Industrial Operating Ranges

Read Cycle (40 MHz and 50 MHz)

Parameter			Preliminary 40 MHz		50 MHz		Unit
No.	Symbol	Description	Min	Max	Min	Max	
General Timing Requirements							
1	t_{DVCL}	Data in Setup	5		5		ns
2	t_{CLDX}	Data in Hold(c)	2		2		ns
General Timing Responses							
3	t_{CHSV}	Status Active Delay	0	12	0	10	ns
4	t_{CLSH}	Status Inactive Delay	0	12	0	10	ns
5	t_{CLAV}	AD Address Valid Delay	0	12	0	10	ns
7	t_{CLDV}	Data Valid Delay	0	12	0	10	ns
8	t_{CHDX}	Status Hold Time	0		0		ns
9	t_{CHLH}	ALE Active Delay		12		10	ns
10	t_{LHLL}	ALE Width	$t_{CLCL}-5=20$		15		ns
11	t_{CHLL}	ALE Inactive Delay		12		10	ns
12	t_{AVLL}	AD Address Valid to ALE Low(a)	t_{CLCH}		t_{CLCH}		ns
13	t_{LLAX}	AD Address Hold from ALE Inactive(a)	t_{CHCL}		t_{CHCL}		ns
14	t_{AVCH}	AD Address Valid to Clock High	0		0		ns
15	t_{CLAZ}	AD Address Float Delay	$t_{CLAX}=0$	12	0	10	ns
16	t_{CLCSV}	$\overline{MCS}/\overline{PCS}$ Active Delay	0	12	0	10	ns
17	t_{CXCSX}	$\overline{MCS}/\overline{PCS}$ Hold from Command Inactive(a)	t_{CLCH}		t_{CLCH}		ns
18	t_{CHCSX}	$\overline{MCS}/\overline{PCS}$ Inactive Delay	0	12	0	10	ns
19	t_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low(a)	0		0		ns
20	t_{CVCTV}	Control Active Delay 1(b)	0	12	0	10	ns
21	t_{CVDEX}	$\overline{DEN}$ Inactive Delay	0	14	0	14	ns
22	t_{CHCTV}	Control Active Delay 2(b)	0	12	0	10	ns
23	t_{LHAV}	ALE High to Address Valid	7.5		5		ns
Read Cycle Timing Responses							
24	t_{AZRL}	AD Address Float to $\overline{RD}$ Active	0		0		ns
25	t_{CLRL}	$\overline{RD}$ Active Delay	0	10	0	10	ns
26	t_{RLRH}	$\overline{RD}$ Pulse Width	$2t_{CLCL}-10=40$		35		ns
27	t_{CLRH}	$\overline{RD}$ Inactive Delay	0	12	0	10	ns
28	t_{RHLH}	$\overline{RD}$ Inactive to ALE High(a)	$t_{CLCH}-2$		$t_{CLCH}-2$		ns
29	t_{RHAV}	$\overline{RD}$ Inactive to AD Address Active(a)	$t_{CLCL}-5=20$		15		ns
59	t_{RHDX}	$\overline{RD}$ High to Data Hold on AD Bus(c)	0		0		ns
66	t_{AVRL}	A Address Valid to $\overline{RD}$ Low	$2 \cdot t_{CLCL}-10=40$		$2 \cdot t_{CLCL}-10=30$		ns
67	t_{CHCSV}	CLKOUTA High to $\overline{LCS}/\overline{UCS}$ Valid	0	12	0	10	ns
68	t_{CHAV}	CLKOUTA High to A Address Valid	0	10	0	10	ns

Notes:

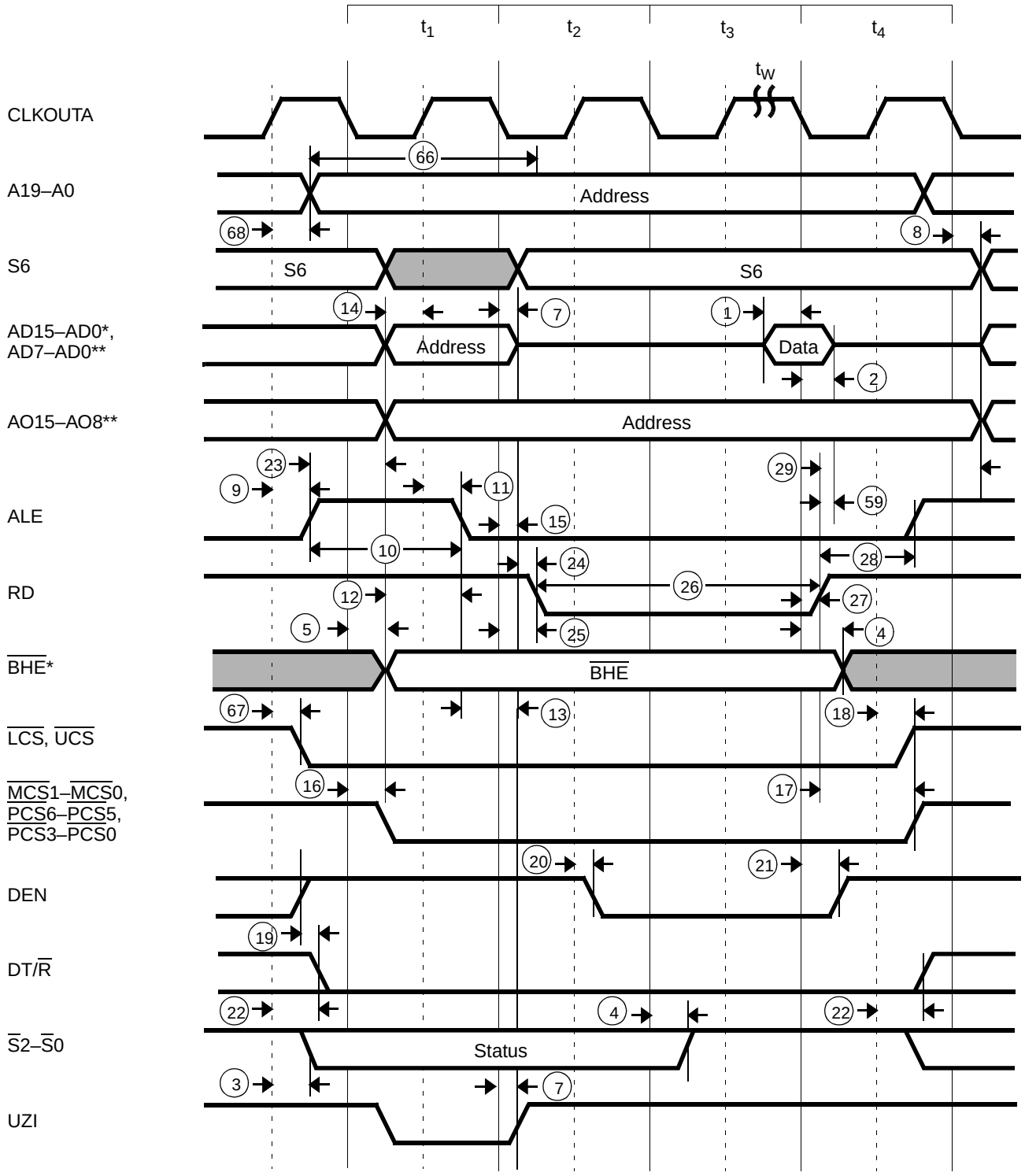
All timing parameters are measured at $V_{CC}/2$ with 50 pF loading on CLKOUTA, unless otherwise noted. All output test conditions are with $C_L=50$ pF. For switching tests, $V_{IL}=0.3$ V and $V_{IH}=V_{CC}-0.3$ V.

a Testing is performed with equal loading on referenced pins.

b This parameter applies to the $\overline{DEN}$, $\overline{INTA1}$–$\overline{INTA0}$, $\overline{WR}$, $\overline{WHB}$, and $\overline{WLB}$ signals.

c If either specification 2 or specification 59 is met with respect to data hold time, the part will function correctly.

Read Cycle Waveforms



Notes:

* *Am186ER microcontroller only*

** *Am188ER microcontroller only*

Switching Characteristics over Commercial and Industrial Operating Ranges

Write Cycle (25 MHz and 33 MHz)

Parameter			Preliminary				Unit
			25 MHz		33 MHz		
No.	Symbol	Description	Min	Max	Min	Max	
General Timing Responses							
3	t_{CHSV}	Status Active Delay	0	20	0	15	ns
4	t_{CLSH}	Status Inactive Delay	0	20	0	15	ns
5	t_{CLAV}	AD Address Valid Delay	0	20	0	15	ns
7	t_{CLDV}	Data Valid Delay	0	20	0	15	ns
8	t_{CHDX}	Status Hold Time	0		0		ns
9	t_{CHLH}	ALE Active Delay		20		15	ns
10	t_{LHLL}	ALE Width	$t_{CLCL}-10=30$		$t_{CLCL}-10=20$		ns
11	t_{CHLL}	ALE Inactive Delay		20		15	ns
12	t_{AVLL}	AD Address Valid to ALE Low[a]	t_{CLCH}		t_{CLCH}		ns
13	t_{LLAX}	AD Address Hold from ALE Inactive[a]	t_{CHCL}		t_{CHCL}		ns
14	t_{AVCH}	AD Address Valid to Clock High	0		0		ns
16	t_{CLCSV}	$\overline{MCS}/\overline{PCS}$ Active Delay	0	20	0	15	ns
17	t_{CXCSX}	$\overline{MCS}/\overline{PCS}$ Hold from Command Inactive[a]	t_{CLCH}		t_{CLCH}		ns
18	t_{CHCSX}	$\overline{MCS}/\overline{PCS}$ Inactive Delay	0	20	0	15	ns
19	t_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low[a]	0		0		ns
20	t_{CVCTV}	Control Active Delay 1[b]	0	20	0	15	ns
23	t_{LHAV}	ALE High to Address Valid	15		10		ns
Write Cycle Timing Responses							
30	t_{CLDOX}	Data Hold Time	0		0		ns
31	t_{CVCTX}	Control Inactive Delay[b]	0	20	0	15	ns
32	t_{WLWH}	$\overline{WR}$ Pulse Width	$2t_{CLCL}-10=70$		$2t_{CLCL}-10=50$		ns
33	t_{WHLH}	$\overline{WR}$ Inactive to ALE High[a]	$t_{CLCH}-2$		$t_{CLCH}-2$		ns
34	t_{WHDX}	Data Hold after $\overline{WR}$[a]	$t_{CLCL}-10=30$		$t_{CLCL}-10=20$		ns
35	t_{WHDEX}	$\overline{WR}$ Inactive to $\overline{DEN}$ Inactive[a]	$t_{CLCH}-3$		$t_{CLCH}-5$		ns
65	t_{AVWL}	A Address Valid to $\overline{WR}$ Low	$t_{CLCL}+t_{CHCL}-3$		$t_{CLCL}+t_{CHCL}-3$		ns
67	t_{CHCSV}	CLKOUTA High to $\overline{LCS}/\overline{UCS}$ Valid	0	20	0	15	ns
68	t_{CHAV}	CLKOUTA High to A Address Valid	0	20	0	15	ns
87	t_{AVBL}	A Address Valid to WHB, WLB Low	$t_{CHCL}-3$	20	$t_{CHCL}-3$	15	ns

Notes:

All timing parameters are measured at $V_{CC}/2$ with 50 pF loading on CLKOUTA, unless otherwise noted. All output test conditions are with $C_L=50$ pF. For switching tests, $V_{IL}=0.3$ V and $V_{IH}=V_{CC}-0.3$ V.

a Testing is performed with equal loading on referenced pins.

b This parameter applies to the $\overline{DEN}$, $\overline{INTA1}$–$\overline{INTA0}$, $\overline{WR}$, $\overline{WHB}$, and $\overline{WLB}$ signals.

Switching Characteristics over Commercial and Industrial Operating Ranges

Write Cycle (40 MHz and 50 MHz)

Parameter			Preliminary				Unit
			40 MHz		50 MHz		
No.	Symbol	Description	Min	Max	Min	Max	
General Timing Responses							
3	t_{CHSV}	Status Active Delay	0	12	0	10	ns
4	t_{CLSH}	Status Inactive Delay	0	12	0	10	ns
5	t_{CLAV}	AD Address Valid Delay	0	12	0	10	ns
7	t_{CLDV}	Data Valid Delay	0	12	0	10	ns
8	t_{CHDX}	Status Hold Time	0		0		ns
9	t_{CHLH}	ALE Active Delay		12		10	ns
10	t_{LHLL}	ALE Width	$t_{CLCL}-5=20$		15		ns
11	t_{CHLL}	ALE Inactive Delay		12		10	ns
12	t_{AVLL}	AD Address Valid to ALE Low[a]	t_{CLCH}		t_{CLCH}		ns
13	t_{LLAX}	AD Address Hold from ALE Inactive[a]	t_{CHCL}		t_{CHCL}		ns
14	t_{AVCH}	AD Address Valid to Clock High	0		0		ns
16	t_{CLCSV}	$\overline{MCS}/\overline{PCS}$ Active Delay	0	12	0	10	ns
17	t_{CXCSX}	$\overline{MCS}/\overline{PCS}$ Hold from Command Inactive[a]	t_{CLCH}		t_{CLCH}		ns
18	t_{CHCSX}	$\overline{MCS}/\overline{PCS}$ Inactive Delay	0	12	0	10	ns
19	t_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low[a]	0		0		ns
20	t_{CVCTV}	Control Active Delay 1[b]	0	12	0	10	ns
23	t_{LHAV}	ALE High to Address Valid	7.5		5		ns
Write Cycle Timing Responses							
30	t_{CLDOX}	Data Hold Time	0		0		ns
31	t_{CVCTX}	Control Inactive Delay[b]	0	12	0	10	ns
32	t_{WLWH}	$\overline{WR}$ Pulse Width	$2t_{CLCL}-10=40$		35		ns
33	t_{WHLH}	$\overline{WR}$ Inactive to ALE High[a]	$t_{CLCH}-2$		$t_{CLCH}-2$		ns
34	t_{WHDX}	Data Hold after $\overline{WR}$[a]	$t_{CLCL}-10=15$		12		ns
35	t_{WHDEX}	$\overline{WR}$ Inactive to $\overline{DEN}$ Inactive[a]	t_{CLCH}		t_{CLCH}		ns
65	t_{AVWL}	A Address Valid to $\overline{WR}$ Low	$t_{CLCL}+t_{CHCL}-1.25$		$t_{CLCL}+t_{CHCL}-1.25$		ns
67	t_{CHCSV}	CLKOUTA High to $\overline{LCS}/\overline{UCS}$ Valid	0	12	0	10	ns
68	t_{CHAV}	CLKOUTA High to A Address Valid	0	10	0	10	ns
87	t_{AVBL}	A Address Valid to WHB, WLB Low	$t_{CHCL}-1.25$	12	$t_{CHCL}-1.25$	10	ns

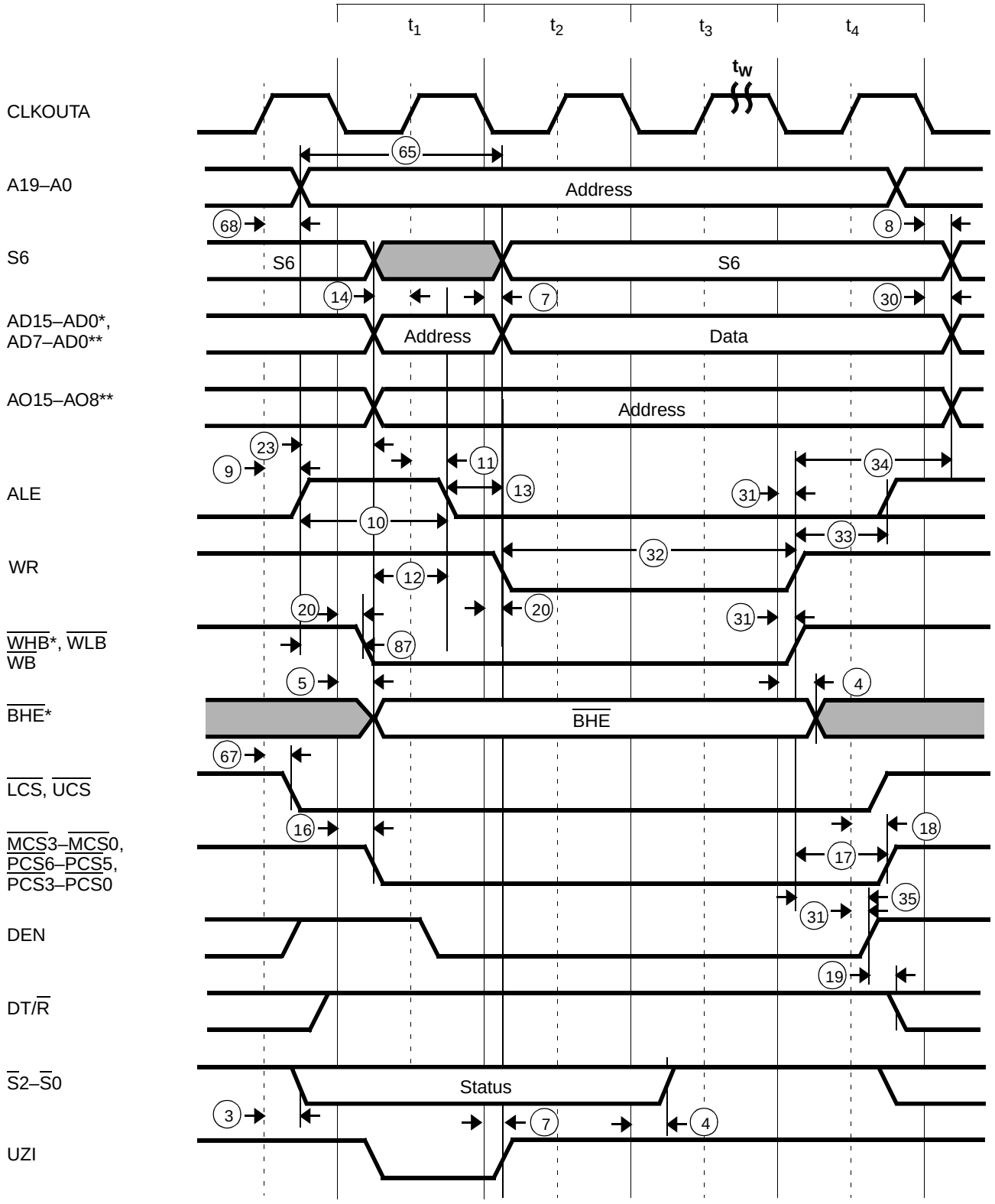
Notes:

All timing parameters are measured at $V_{CC}/2$ with 50 pF loading on CLKOUTA, unless otherwise noted. All output test conditions are with $C_L=50$ pF. For switching tests, $V_{IL}=0.3$ V and $V_{IH}=V_{CC}-0.3$ V.

a Testing is performed with equal loading on referenced pins.

b This parameter applies to the $\overline{DEN}$, $\overline{INTA1}$–$\overline{INTA0}$, $\overline{WR}$, $\overline{WHB}$, and $\overline{WLB}$ signals.

Write Cycle Waveforms



Notes:

* *Am186ER microcontroller only*

** *Am188ER microcontroller only*

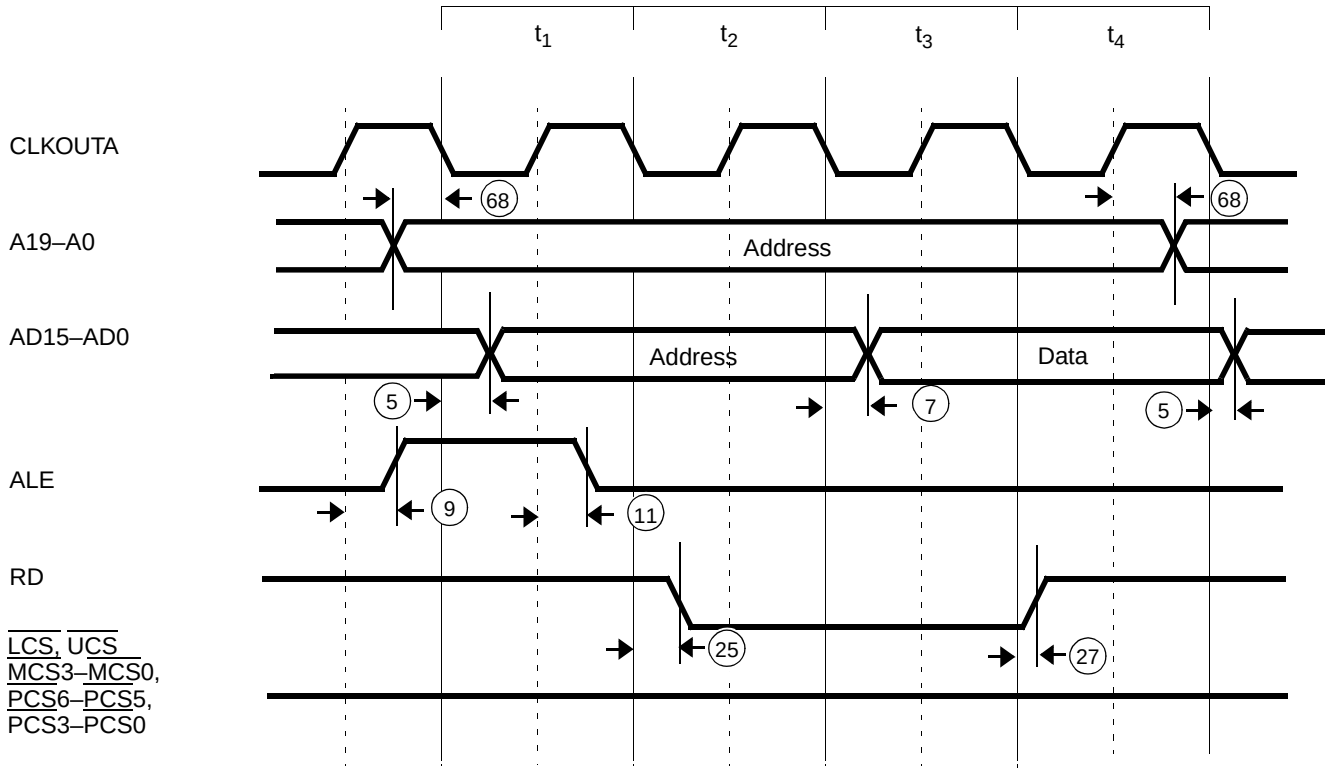
Switching Characteristics over Commercial and Industrial Operating Ranges
Internal RAM Show Read Cycle (25 MHz and 33 MHz)

Parameter			Preliminary				Unit
			25 MHz		33 MHz		
No.	Symbol	Description	Min	Max	Min	Max	
General Timing Responses							
5	t_{CLAV}	AD Address Valid Delay	0	20	0	15	ns
7	t_{CLDV}	Data Valid Delay	0	20	0	15	ns
9	t_{CHLH}	ALE Active Delay		20		15	ns
11	t_{CHLL}	ALE Inactive Delay		20		15	ns
Read Cycle Timing Responses							
25	t_{CLRL}	$\overline{RD}$ Active Delay	0	20	0	15	ns
27	t_{CLRH}	$\overline{RD}$ Inactive Delay	0	20	0	15	ns
68	t_{CHAV}	CLKOUTA High to A Address Valid	0	20	0	15	ns

Switching Characteristics over Commercial and Industrial Operating Ranges
Internal RAM Show Read Cycle (40 MHz and 50 MHz)

Parameter			Preliminary				Unit
			40 MHz		50 MHz		
No.	Symbol	Description	Min	Max	Min	Max	
General Timing Responses							
5	t_{CLAV}	AD Address Valid Delay	0	12	0	10	ns
7	t_{CLDV}	Data Valid Delay	0	12	0	10	ns
9	t_{CHLH}	ALE Active Delay		12		10	ns
11	t_{CHLL}	ALE Inactive Delay		12		10	ns
Read Cycle Timing Responses							
25	t_{CLRL}	$\overline{RD}$ Active Delay	0	10	0	10	ns
27	t_{CLRH}	$\overline{RD}$ Inactive Delay	0	12	0	10	ns
68	t_{CHAV}	CLKOUTA High to A Address Valid	0	10	0	10	ns

Internal RAM Show Read Cycle Waveform



Switching Characteristics over Commercial and Industrial Operating Ranges

PSRAM Read Cycle (25 MHz and 33 MHz)

Parameter			Preliminary				Unit
			25 MHz		33 MHz		
No.	Symbol	Description	Min	Max	Min	Max	
General Timing Requirements							
1	t_{DVCL}	Data in Setup	10		8		ns
2	t_{CLDX}	Data in Hold[b]	3		3		ns
General Timing Responses							
5	t_{CLAV}	AD Address Valid Delay	0	20	0	15	ns
7	t_{CLDV}	Data Valid Delay	0	20	0	15	ns
8	t_{CHDX}	Status Hold Time	0		0		ns
9	t_{CHLH}	ALE Active Delay		20		15	ns
10	t_{LHLL}	ALE Width	$t_{CLCL}-10=30$		$t_{CLCL}-10=20$		ns
11	t_{CHLL}	ALE Inactive Delay		20		15	ns
23	t_{LHAV}	ALE High to Address Valid	15		10		ns
80	t_{CLCLX}	$\overline{LCS}$ Inactive Delay	0	20	0	15	ns
81	t_{CLCSL}	$\overline{LCS}$ Active Delay	0	20	0	15	ns
84	t_{LRLL}	$\overline{LCS}$ Precharge Pulse Width	$t_{CLCL} + t_{CLCH} - 3$		$t_{CLCL} + t_{CLCH} - 3$		ns
Read Cycle Timing Responses							
24	t_{AZRL}	AD Address Float to $\overline{RD}$ Active	0		0		ns
25	t_{CLRL}	$\overline{RD}$ Active Delay	0	20	0	15	ns
26	t_{RLRH}	$\overline{RD}$ Pulse Width	$2t_{CLCL}-15=65$		$2t_{CLCL}-15=45$		ns
27	t_{CLRH}	$\overline{RD}$ Inactive Delay	0	20	0	15	ns
28	t_{RHLH}	$\overline{RD}$ Inactive to ALE High[a]	$t_{CLCH}-3$		$t_{CLCH}-3$		ns
59	t_{RHDX}	$\overline{RD}$ High to Data Hold on AD Bus[b]	0		0		ns
66	t_{AVRL}	A Address Valid to $\overline{RD}$ Low	$2t_{CLCL}-15=65$		$2t_{CLCL}-15=45$		ns
68	t_{CHAV}	CLKOUTA High to A Address Valid	0	20	0	15	ns

Notes:

All timing parameters are measured at $V_{CC}/2$ with 50 pF loading on CLKOUTA, unless otherwise noted. All output test conditions are with $C_L=50$ pF. For switching tests, $V_{IL}=0.3$ V and $V_{IH}=V_{CC}-0.3$ V.

a Testing is performed with equal loading on referenced pins.

b If either spec 2 or spec 59 is met with respect to data hold time, the part will function correctly.

Switching Characteristics over Commercial and Industrial Operating Ranges

PSRAM Read Cycle (40 MHz and 50 MHz)

Parameter			Preliminary				Unit
			40 MHz		50 MHz		
No.	Symbol	Description	Min	Max	Min	Max	
General Timing Requirements							
1	t_{DVCL}	Data in Setup	5		5		ns
2	t_{CLDX}	Data in Hold[b]	2		2		ns
General Timing Responses							
5	t_{CLAV}	AD Address Valid Delay	0	12	0	10	ns
7	t_{CLDV}	Data Valid Delay	0	12	0	10	ns
8	t_{CHDX}	Status Hold Time	0		0		ns
9	t_{CHLH}	ALE Active Delay		12		10	ns
10	t_{LHLL}	ALE Width	$t_{CLCL}-5=20$		15		ns
11	t_{CHLL}	ALE Inactive Delay		12		10	ns
23	t_{LHAV}	ALE High to Address Valid	7.5		5		ns
80	t_{CLCLX}	$\overline{LCS}$ Inactive Delay	0	12	0	10	ns
81	t_{CLCSL}	$\overline{LCS}$ Active Delay	0	12	0	10	ns
84	t_{LRLL}	$\overline{LCS}$ Precharge Pulse Width	$t_{CLCL}+t_{CLCH}-1.25$		$t_{CLCL}+t_{CLCH}-1$		ns
Read Cycle Timing Responses							
24	t_{AZRL}	AD Address Float to $\overline{RD}$ Active	0		0		ns
25	t_{CLRL}	$\overline{RD}$ Active Delay	0	10	0	10	ns
26	t_{RLRH}	$\overline{RD}$ Pulse Width	$2t_{CLCL}-10=40$		35		ns
27	t_{CLRH}	$\overline{RD}$ Inactive Delay	0	12	0	10	ns
28	t_{RHLH}	$\overline{RD}$ Inactive to ALE High[a]	$t_{CLCH}-1.25$		$t_{CLCH}-1$		ns
59	t_{RHDX}	$\overline{RD}$ High to Data Hold on AD Bus[b]	0		0		ns
66	t_{AVRL}	A Address Valid to $\overline{RD}$ Low	$2t_{CLCL}-10=40$		$2t_{CLCL}-10=30$		ns
68	t_{CHAV}	CLKOUTA High to A Address Valid	0	10	0	10	ns

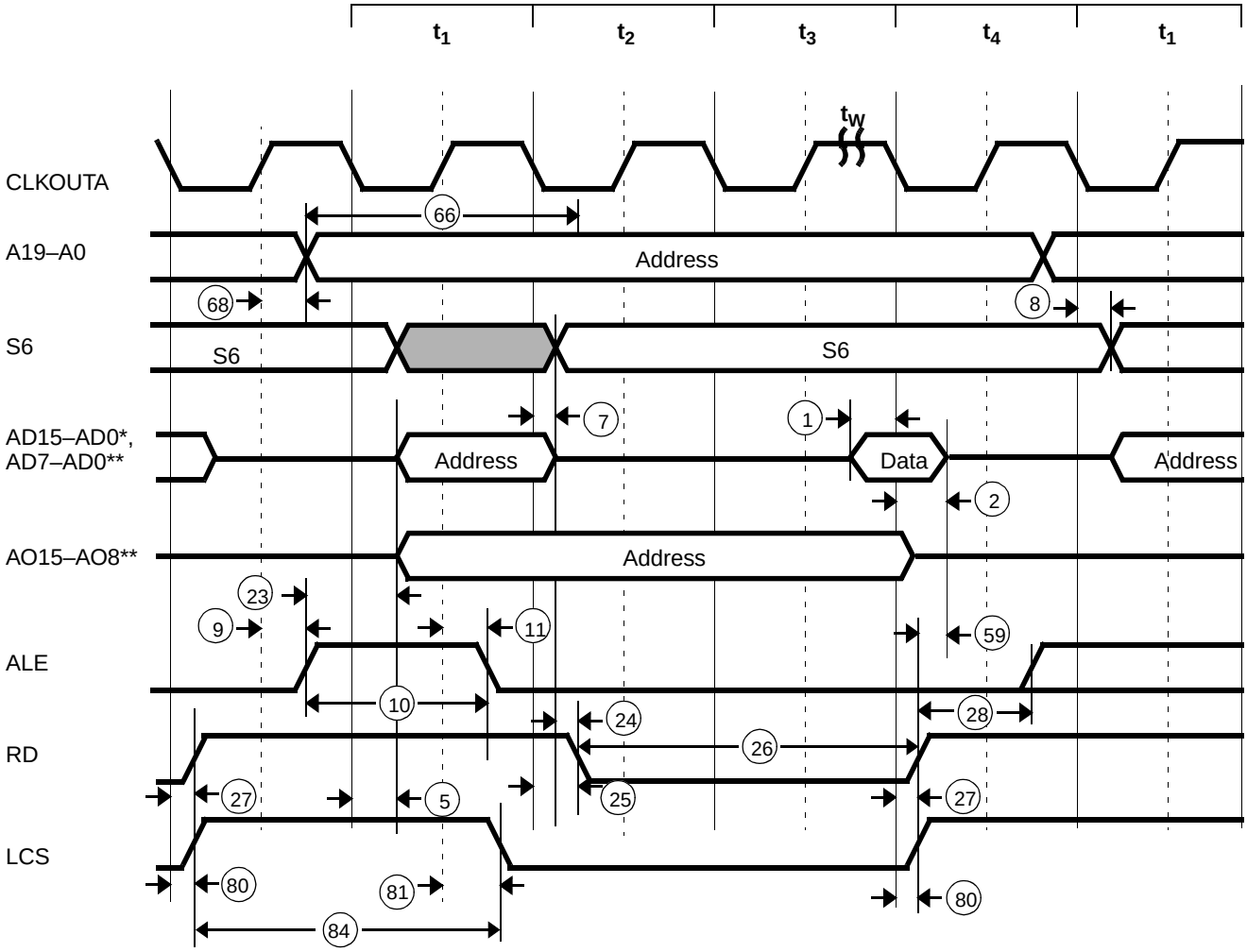
Notes:

All timing parameters are measured at $V_{CC}/2$ with 50 pF loading on CLKOUTA, unless otherwise noted. All output test conditions are with $C_L=50$ pF. For switching tests, $V_{IL}=0.3$ V and $V_{IH}=V_{CC}-0.3$ V.

a Testing is performed with equal loading on referenced pins.

b If either specification 2 or specification 59 is met with respect to data hold time, the part will function correctly.

PSRAM Read Cycle Waveforms



Notes:

* *Am186ER microcontroller only*

** *Am188ER microcontroller only*

Switching Characteristics over Commercial and Industrial Operating Ranges

PSRAM Write Cycle (25 MHz and 33 MHz)

Parameter			Preliminary				Unit
			25 MHz		33 MHz		
No.	Symbol	Description	Min	Max	Min	Max	
General Timing Responses							
5	t_{CLAV}	AD Address Valid Delay	0	20	0	15	ns
7	t_{CLDV}	Data Valid Delay	0	20	0	15	ns
8	t_{CHDX}	Status Hold Time	0		0		ns
9	t_{CHLH}	ALE Active Delay		20		15	ns
10	t_{LHLL}	ALE Width	$t_{CLCL}-10=30$		$t_{CLCL}-10=20$		ns
11	t_{CHLL}	ALE Inactive Delay		20		15	ns
23	t_{LHAV}	ALE High to Address Valid	15		0	15	ns
20	t_{CVCTV}	Control Active Delay 1[b]	0	20	10		ns
80	t_{CLCLX}	$\overline{LCS}$ Inactive Delay	0	20	0	15	ns
81	t_{CLCSL}	$\overline{LCS}$ Active Delay	0	20	0	15	ns
84	t_{LRLL}	$\overline{LCS}$ Precharge Pulse Width	$t_{CLCL} + t_{CLCH} - 3$		$t_{CLCL} + t_{CLCH} - 3$		
Write Cycle Timing Responses							
30	t_{CLDOX}	Data Hold Time	0		0		ns
31	t_{CVCTX}	Control Inactive Delay[b]	0	20	0	15	ns
32	t_{WLWH}	$\overline{WR}$ Pulse Width	$2t_{CLCL}-10=70$		$2t_{CLCL}-10=50$		ns
33	t_{WHLH}	$\overline{WR}$ Inactive to ALE High[a]	$t_{CLCH}-2$		$t_{CLCH}-2$		ns
34	t_{WHDX}	Data Hold after $\overline{WR}$[a]	$t_{CLCL}-10=30$		$t_{CLCL}-10=20$		ns
65	t_{AVWL}	A Address Valid to $\overline{WR}$ Low	$t_{CLCL}+t_{CHCL}-3$		$t_{CLCL}+t_{CHCL}-3$		ns
68	t_{CHAV}	CLKOUTA High to A Address Valid	0	20	0	15	ns
87	t_{AVBL}	A Address Valid to WHB, WLB Low	$t_{CHCL}-3$	20	$t_{CHCL}-3$	15	ns

Notes:

All timing parameters are measured at $V_{CC}/2$ with 50 pF loading on CLKOUTA, unless otherwise noted. All output test conditions are with $C_L=50$ pF. For switching tests, $V_{IL}=0.3$ V and $V_{IH}=V_{CC}-0.3$ V.

a Testing is performed with equal loading on referenced pins.

b This parameter applies to the $\overline{DEN}$, $\overline{WR}$, $\overline{WHB}$ and $\overline{WLB}$ signals.

Switching Characteristics over Commercial and Industrial Operating Ranges

PSRAM Write Cycle (40 MHz and 50 MHz)

Parameter			Preliminary				Unit
			40 MHz		50 MHz		
No.	Symbol	Description	Min	Max	Min	Max	
General Timing Responses							
5	t_{CLAV}	AD Address Valid Delay	0	12	0	10	ns
7	t_{CLDV}	Data Valid Delay	0	12	0	10	ns
8	t_{CHDX}	Status Hold Time	0		0		ns
9	t_{CHLH}	ALE Active Delay		12		10	ns
10	t_{LHLL}	ALE Width	$t_{CLCL}-5=20$		15		ns
11	t_{CHLL}	ALE Inactive Delay		12		10	ns
20	t_{CVCTV}	Control Active Delay 1[b]	0	12	0	10	ns
23	t_{LHAV}	ALE High to Address Valid	7.5		5		ns
80	t_{CLCLX}	$\overline{LCS}$ Inactive Delay	0	12	0	10	ns
81	t_{CLCSL}	$\overline{LCS}$ Active Delay	0	12	0	10	ns
84	t_{LRLL}	$\overline{LCS}$ Precharge Pulse Width	$t_{CLCL}+t_{CLCH}-1.25$		$t_{CLCL}+t_{CLCH}-1$		
Write Cycle Timing Responses							
30	t_{CLDOX}	Data Hold Time	0		0		ns
31	t_{CVCTX}	Control Inactive Delay[b]	0	12	0	10	ns
32	t_{WLWH}	$\overline{WR}$ Pulse Width	$2t_{CLCL}-10=40$		35		ns
33	t_{WHLH}	$\overline{WR}$ Inactive to ALE High[a]	$t_{CLCH}-2$		$t_{CLCH}-2$		ns
34	t_{WHDX}	Data Hold after $\overline{WR}$[a]	$t_{CLCL}-10=15$		12		ns
65	t_{AVWL}	A Address Valid to $\overline{WR}$ Low	$t_{CLCL}+t_{CHCL}-1.25$		$t_{CLCL}+t_{CHCL}-1.25$		ns
68	t_{CHAV}	CLKOUTA High to A Address Valid	0	10	0	10	ns
87	t_{AVBL}	A Address Valid to WHB, WLB Low	$t_{CHCL}-1.25$	18	$t_{CHCL}-1.25$	15	ns

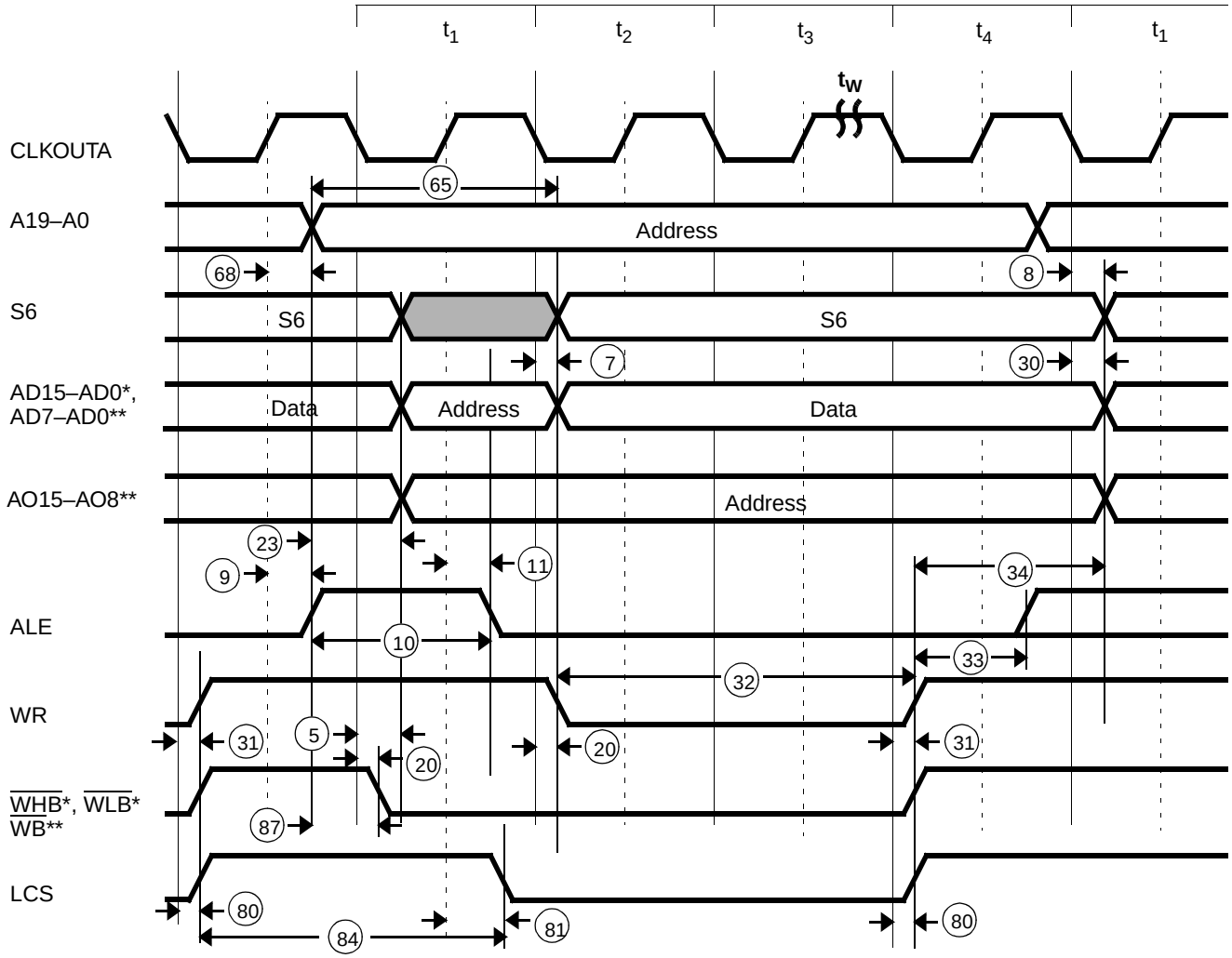
Notes:

All timing parameters are measured at $V_{CC}/2$ with 50 pF loading on CLKOUTA, unless otherwise noted. All output test conditions are with $C_L=50$ pF. For switching tests, $V_{IL}=0.3$ V and $V_{IH}=V_{CC}-0.3$ V.

a Testing is performed with equal loading on referenced pins.

b This parameter applies to the $\overline{DEN}$, $\overline{WR}$, $\overline{WHB}$ and $\overline{WLB}$ signals.

PSRAM Write Cycle Waveforms



Notes:

* *Am186ER microcontroller only*

** *Am188ER microcontroller only*

Switching Characteristics over Commercial and Industrial Operating Ranges

PSRAM Refresh Cycle (25 MHz and 33 MHz)

Parameter			Preliminary				Unit
			25 MHz		33 MHz		
No.	Symbol	Description	Min	Max	Min	Max	
General Timing Responses							
9	t_{CHLH}	ALE Active Delay		20		15	ns
10	t_{LHLL}	ALE Width	$t_{CLCL}-10=30$		$t_{CLCL}-10=20$		ns
11	t_{CHLL}	ALE Inactive Delay		20		15	ns
Read/Write Cycle Timing Responses							
25	t_{CLRL}	$\overline{RD}$ Active Delay	0	20	0	15	ns
26	t_{RLRH}	$\overline{RD}$ Pulse Width	$2t_{CLCL}-15=65$		$2t_{CLCL}-15=45$		ns
27	t_{CLRH}	$\overline{RD}$ Inactive Delay	0	20	0	15	ns
28	t_{RHLH}	$\overline{RD}$ Inactive to ALE High[a]	$t_{CLCH}-3$		$t_{CLCH}-3$		ns
80	t_{CLCLX}	$\overline{LCS}$ Inactive Delay	0	20	0	15	ns
81	t_{CLCSL}	$\overline{LCS}$ Active Delay	0	20	0	15	ns
Refresh Timing Cycle Parameters							
79	t_{CLRFD}	CLKOUTA Low to $\overline{RFSH}$ Valid	0	20	0	15	ns
82	t_{CLRF}	CLKOUTA High to $\overline{RFSH}$ Invalid	0	20	0	15	ns
85	t_{RFCY}	$\overline{RFSH}$ Cycle Time	$6 \times t_{CLCL}$		$6 \times t_{CLCL}$		ns
86	t_{LCRF}	$\overline{LCS}$ Inactive to $\overline{RFSH}$ Active Delay	$2t_{CLCL}-3$		$2t_{CLCL}-3$		ns

Notes:

All timing parameters are measured at $V_{CC}/2$ with 50 pF loading on CLKOUTA unless otherwise noted. All output test conditions are with $C_L=50$ pF. For switching tests, $V_{IL}=0.3$ V and $V_{IH}=V_{CC}-0.3$ V.

a Testing is performed with equal loading on referenced pins.

Switching Characteristics over Commercial and Industrial Operating Ranges

PSRAM Refresh Cycle (40 MHz and 50 MHz)

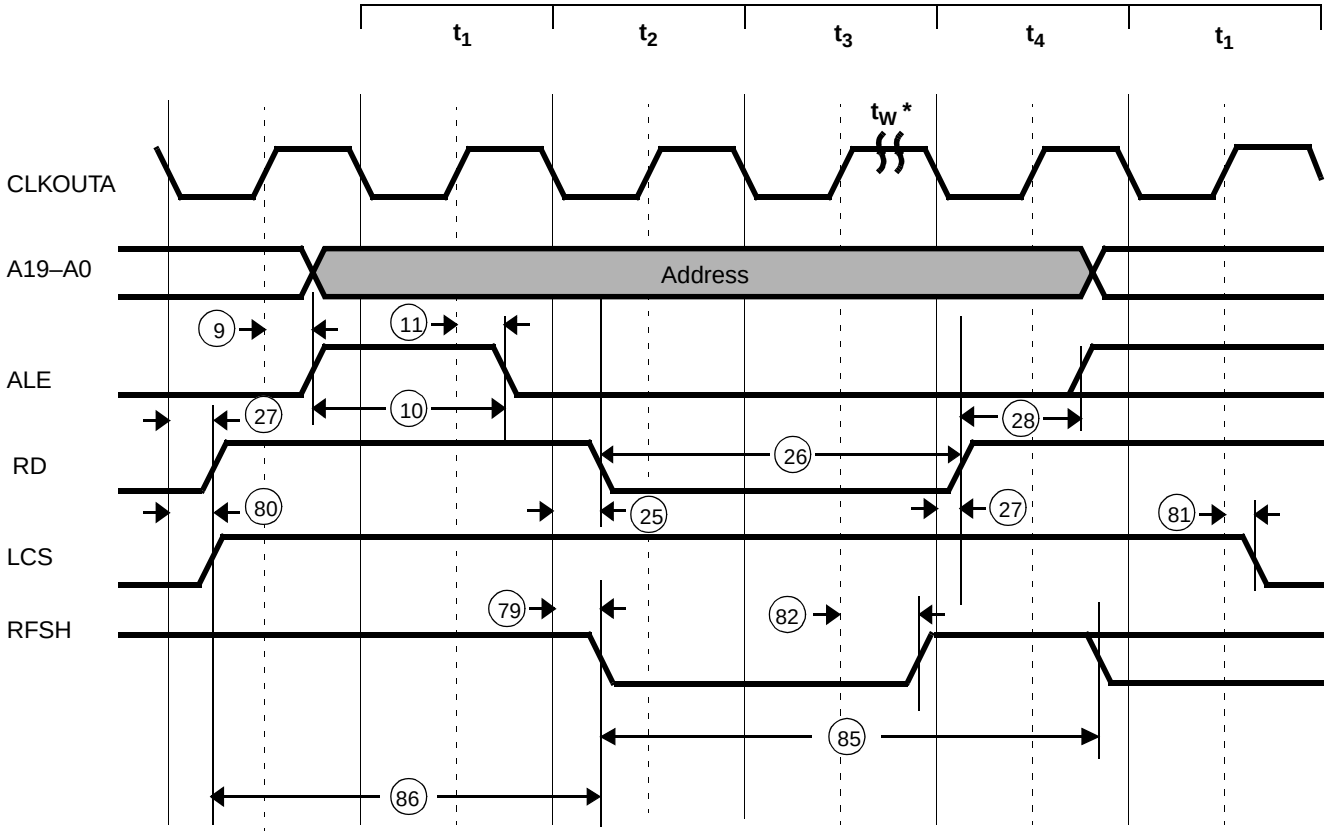
Parameter			Preliminary				Unit
			40 MHz		50 MHz		
No.	Symbol	Description	Min	Max	Min	Max	
General Timing Responses							
9	t_{CHLH}	ALE Active Delay		12		10	ns
10	t_{LHLL}	ALE Width	$t_{CLCL}-5=20$		15		ns
11	t_{CHLL}	ALE Inactive Delay		12		10	ns
Read/Write Cycle Timing Responses							
25	t_{CLRL}	$\overline{RD}$ Active Delay	0	10	0	10	ns
26	t_{RLRH}	$\overline{RD}$ Pulse Width	$2t_{CLCL}-10=40$		35		ns
27	t_{CLRH}	$\overline{RD}$ Inactive Delay	0	12	0	10	ns
28	t_{RHLH}	$\overline{RD}$ Inactive to ALE High[(a)]	$t_{CLCH}-2$		$t_{CLCH}-2$		ns
80	t_{CLCLX}	$\overline{LCS}$ Inactive Delay	0	12	0	10	ns
81	t_{CLCSL}	$\overline{LCS}$ Active Delay	0	12	0	10	ns
Refresh Timing Cycle Parameters							
79	t_{CLRFD}	CLKOUTA Low to $\overline{RFSH}$ Valid	0	12	0	10	ns
82	t_{CLRF}	CLKOUTA High to $\overline{RFSH}$ Invalid	0	12	0	10	ns
85	t_{RFCY}	$\overline{RFSH}$ Cycle Time	$6 \times t_{CLCL}$		$6 \times t_{CLCL}$		ns
86	t_{LCRF}	$\overline{LCS}$ Inactive to $\overline{RFSH}$ Active Delay	$2t_{CLCL}-1.25$		$2t_{CLCL}-1.25$		ns

Notes:

All timing parameters are measured at $V_{CC}/2$ with 50 pF loading on CLKOUTA unless otherwise noted. All output test conditions are with $C_L=50$ pF. For switching tests, $V_{IL}=0.3$ V and $V_{IH}=V_{CC}-0.3$ V.

a Testing is performed with equal loading on referenced pins.

PSRAM Refresh Cycle Waveforms



Note:

***** *The period t_w is fixed at three wait states for PSRAM auto refresh only.*

Switching Characteristics over Commercial and Industrial Operating Ranges

Interrupt Acknowledge Cycle (25 MHz and 33 MHz)

Parameter			Preliminary				Unit
			25 MHz		33 MHz		
No.	Symbol	Description	Min	Max	Min	Max	
General Timing Requirements							
1	t_{DVCL}	Data in Setup	10		8		ns
2	t_{CLDX}	Data in Hold	3		3		ns
General Timing Responses							
3	t_{CHSV}	Status Active Delay	0	20	0	15	ns
4	t_{CLSH}	Status Inactive Delay	0	20	0	15	ns
7	t_{CLDV}	Data Valid Delay	0	20	0	15	ns
8	t_{CHDX}	Status Hold Time	0		0		ns
9	t_{CHLH}	ALE Active Delay		20		15	ns
10	t_{LHLL}	ALE Width	$t_{CLCL}-10=30$		$t_{CLCL}-10=20$		ns
11	t_{CHLL}	ALE Inactive Delay		20		15	ns
12	t_{AVLL}	AD Address Invalid to ALE Low[a]	t_{CLCH}		t_{CLCH}		ns
15	t_{CLAZ}	AD Address Float Delay	$t_{CLAX}=0$	20	$t_{CLAX}=0$	15	ns
19	t_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low[a]	0		0		ns
20	t_{CVCTV}	Control Active Delay 1[b]	0	20	0	15	ns
21	t_{CVDEX}	$\overline{DEN}$ Inactive Delay	0	20	0	15	ns
22	t_{CHCTV}	Control Active Delay 2[c]	0	20	0	15	ns
23	t_{LHAV}	ALE High to Address Valid	15		10		ns
31	t_{CVCTX}	Control Inactive Delay[b]	0	20	0	15	ns
68	t_{CHAV}	CLKOUTA High to A Address Valid	0	20	0	15	ns

Notes:

All timing parameters are measured at $V_{CC}/2$ with 50 pF loading on CLKOUTA, unless otherwise noted. All output test conditions are with $C_L=50$ pF. For switching tests, $V_{IL}=0.3$ V and $V_{IH}=V_{CC}-0.3$ V.

a Testing is performed with equal loading on referenced pins.

b This parameter applies to the $\overline{INTA}1$–$\overline{INTA}0$ signals.

c This parameter applies to the $\overline{DEN}$ and DT/$\overline{R}$ signals.

Switching Characteristics over Commercial Operating Ranges

Interrupt Acknowledge Cycle (40 MHz and 50 MHz)

Parameter			Preliminary				Unit
			40 MHz		50 MHz		
No.	Symbol	Description	Min	Max	Min	Max	
General Timing Requirements							
1	t_{DVCL}	Data in Setup	5		5		ns
2	t_{CLDX}	Data in Hold	2		2		ns
General Timing Responses							
3	t_{CHSV}	Status Active Delay	0	12	0	10	ns
4	t_{CLSH}	Status Inactive Delay	0	12	0	10	ns
7	t_{CLDV}	Data Valid Delay	0	12	0	10	ns
8	t_{CHDX}	Status Hold Time	0		0		ns
9	t_{CHLH}	ALE Active Delay		12		10	ns
10	t_{LHLL}	ALE Width	$t_{CLCL}-5=20$		15		ns
11	t_{CHLL}	ALE Inactive Delay		12		12	ns
12	t_{AVLL}	AD Address Invalid to ALE Low[a]	t_{CLCH}		t_{CLCH}		ns
15	t_{CLAZ}	AD Address Float Delay	$t_{CLAX}=0$	12	0	10	ns
19	t_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low[a]	0		0		ns
20	t_{CVCTV}	Control Active Delay 1[b]	0	12	0	10	ns
21	t_{CVDEX}	$\overline{DEN}$ Inactive Delay	0	14	0	14	ns
22	t_{CHCTV}	Control Active Delay 2[c]	0	12	0	10	ns
23	t_{LHAV}	ALE High to Address Valid	7.5		5		ns
31	t_{CVCTX}	Control Inactive Delay[b]	0	12	0	10	ns
68	t_{CHAV}	CLKOUTA High to A Address Valid	0	10	0	10	ns

Notes:

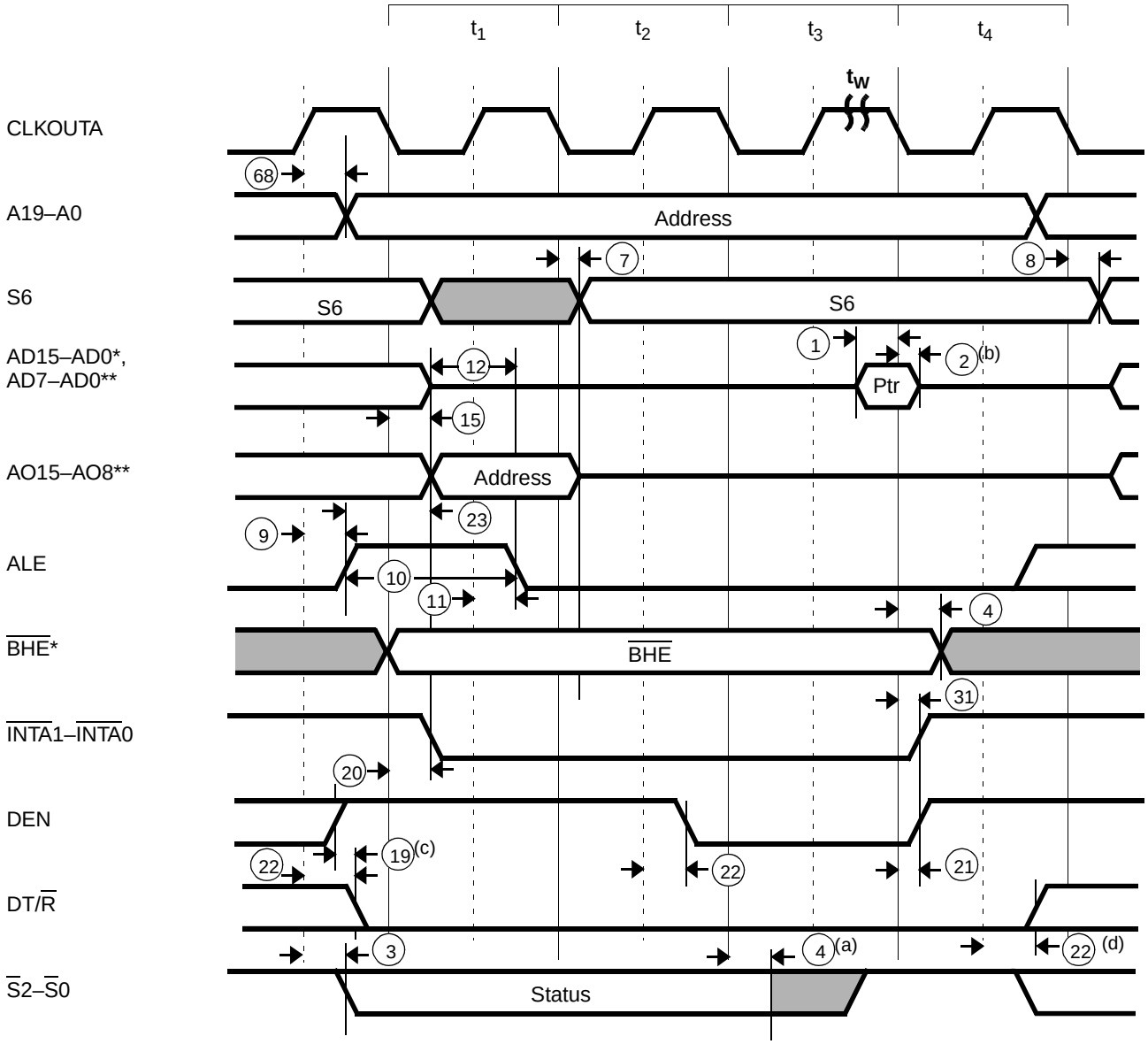
All timing parameters are measured at $V_{CC}/2$ with 50 pF loading on CLKOUTA, unless otherwise noted. All output test conditions are with $C_L=50$ pF. For switching tests, $V_{IL}=0.3$ V and $V_{IH}=V_{CC}-0.3$ V.

a Testing is performed with equal loading on referenced pins.

b This parameter applies to the $\overline{INTA}1$–$\overline{INTA}0$ signals.

c This parameter applies to the $\overline{DEN}$ and DT/$\overline{R}$ signals.

Interrupt Acknowledge Cycle Waveforms



Notes:

* *Am186ER microcontroller only*

** *Am188ER microcontroller only*

a *The status bits become inactive in the state preceding t_4.*

b *The data hold time lasts only until the interrupt acknowledge signal deasserts, even if the interrupt acknowledge transition occurs prior to t_{CLDX} (min).*

c *This parameter applies to an interrupt acknowledge cycle that follows a write cycle.*

d *If followed by a write cycle, this change occurs in the state preceding that write cycle.*

Switching Characteristics over Commercial and Industrial Operating Ranges Software Halt Cycle (25 MHz and 33 MHz)

Parameter			Preliminary				Unit
			25 MHz		33 MHz		
No.	Symbol	Description	Min	Max	Min	Max	
General Timing Responses							
3	t_{CHSV}	Status Active Delay	0	20	0	15	ns
4	t_{CLSH}	Status Inactive Delay	0	20	0	15	ns
5	t_{CLAV}	AD Address Invalid Delay	0	20	0	15	ns
9	t_{CHLH}	ALE Active Delay		20		15	ns
10	t_{LHLL}	ALE Width	$t_{CLCL}-10=30$		$t_{CLCL}-10=20$		ns
11	t_{CHLL}	ALE Inactive Delay		20		15	ns
19	t_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low[a]	0		0		ns
22	t_{CHCTV}	Control Active Delay 2[b]	0	20	0	15	ns
68	t_{CHAV}	CLKOUTA High to A Address Invalid	0	20	0	15	ns

Notes:

All timing parameters are measured at $V_{CC}/2$ with 50 pF loading on CLKOUTA, unless otherwise noted. All output test conditions are with $C_L=50$ pF. For switching tests, $V_{IL}=0.3$ V and $V_{IH}=V_{CC}-0.3$ V.

a Testing is performed with equal loading on referenced pins.

b This parameter applies to the $\overline{DEN}$ signal.

Switching Characteristics over Commercial and Industrial Operating Ranges Software Halt Cycle (40 MHz and 50 MHz)

Parameter			Preliminary				Unit
			40 MHz		50 MHz		
No.	Symbol	Description	Min	Max	Min	Max	
General Timing Responses							
3	t_{CHSV}	Status Active Delay	0	12	0	10	ns
4	t_{CLSH}	Status Inactive Delay	0	12	0	10	ns
5	t_{CLAV}	AD Address Invalid Delay	0	12	0	10	ns
9	t_{CHLH}	ALE Active Delay		12		10	ns
10	t_{LHLL}	ALE Width	$t_{CLCL}-5=20$		15		ns
11	t_{CHLL}	ALE Inactive Delay		12		10	ns
19	t_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low[a]	0		0		ns
22	t_{CHCTV}	Control Active Delay 2[b]	0	12	0	10	ns
68	t_{CHAV}	CLKOUTA High to A Address Invalid	0	10	0	10	ns

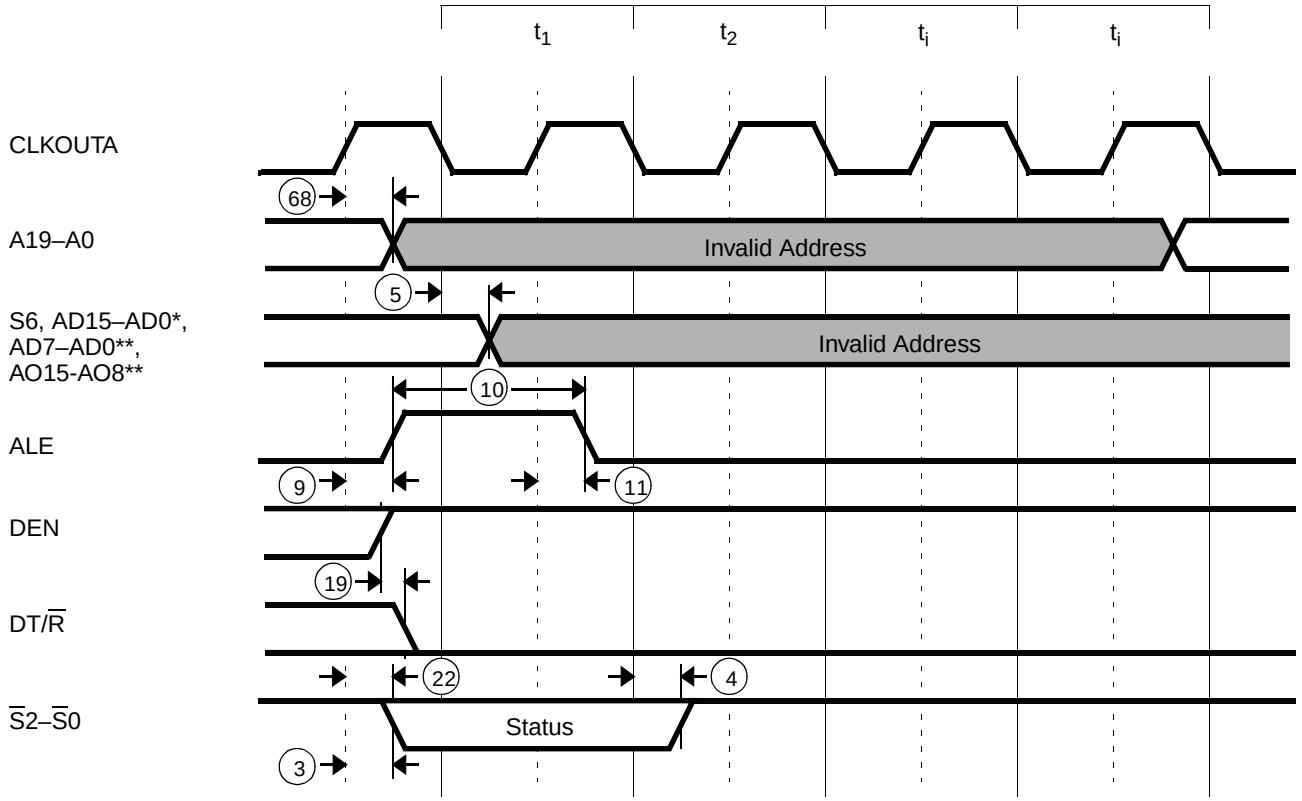
Notes:

All timing parameters are measured at $V_{CC}/2$ with 50 pF loading on CLKOUTA, unless otherwise noted. All output test conditions are with $C_L=50$ pF. For switching tests, $V_{IL}=0.3$ V and $V_{IH}=V_{CC}-0.3$ V.

a Testing is performed with equal loading on referenced pins.

b This parameter applies to the $\overline{DEN}$ signal.

Software Halt Cycle Waveforms



Notes:

* *Am186ER microcontroller only*

** *Am188ER microcontroller only*

Switching Characteristics over Commercial and Industrial Operating Ranges

Clock (25 MHz)

Parameter			Preliminary 25 MHz		Unit
No.	Symbol	Description	Min	Max	
CLKIN Requirements for Times One Mode					
36	t_{CKIN}	X1 Period[a]	40	60	ns
37	t_{CLCK}	X1 Low Time (1.5 V)[a]	15		ns
38	t_{CHCK}	X1 High Time (1.5 V)[a]	15		ns
39	t_{CKHL}	X1 Fall Time (3.5 to 1.0 V)[a]		5	ns
40	t_{CKLH}	X1 Rise Time (1.0 to 3.5 V)[a]		5	ns
CLKIN Requirements for Divide by Two Mode					
36	t_{CKIN}	X1 Period[a]	20	33	ns
37	t_{CLCK}	X1 Low Time (1.5 V)[a]	10		ns
38	t_{CHCK}	X1 High Time (1.5 V)[a]	10		ns
39	t_{CKHL}	X1 Fall Time (3.5 to 1.0 V)[a]		5	ns
40	t_{CKLH}	X1 Rise Time (1.0 to 3.5 V)[a]		5	ns
CLKOUT Timing					
42	t_{CLCL}	CLKOUTA Period	40		ns
43	t_{CLCH}	CLKOUTA Low Time (C_L=50 pF)	$0.5t_{CLCL}-2=18$		ns
44	t_{CHCL}	CLKOUTA High Time (C_L=50 pF)	$0.5t_{CLCL}-2=18$		ns
45	t_{CH1CH2}	CLKOUTA Rise Time (1.0 to 3.5 V)		3	ns
46	t_{CL2CL1}	CLKOUTA Fall Time (3.5 to 1.0 V)		3	ns
61	t_{LOCK}	Maximum PLL Lock Time		1	ms
69	t_{CICOA}	X1 to CLKOUTA Skew		20	ns
70	t_{CICOB}	X1 to CLKOUTB Skew		34	ns

Notes:

All timing parameters are measured at $V_{CC}/2$ with 50 pF loading on CLKOUTA, unless otherwise noted. All output test conditions are with C_L=50 pF. For switching tests, V_{IL}=0.3 V and $V_{IH}=V_{CC}-0.3$ V.

a The specifications for CLKIN are applicable to the Divide by Two and Times One modes.

The Times One mode should be used for operations from 16 MHz to 20 MHz. The Times Four mode should be used for operations above 20 MHz.

Switching Characteristics over Commercial and Industrial Operating Ranges

Clock (33 MHz)

Parameter			Preliminary 33 MHz		Unit
No.	Symbol	Description	Min	Max	
CLKIN Requirements for Times Four Mode					
36	t_{CKIN}	X1 Period[a]	120	125	ns
37	t_{CLCK}	X1 Low Time (1.5 V)[a]	55		ns
38	t_{CHCK}	X1 High Time (1.5 V)[a]	55		ns
39	t_{CKHL}	X1 Fall Time (3.5 to 1.0 V)[a]		5	ns
40	t_{CKLH}	X1 Rise Time (1.0 to 3.5 V)[a]		5	ns
CLKIN Requirements for Times One Mode					
36	t_{CKIN}	X1 Period[a]	30	60	ns
37	t_{CLCK}	X1 Low Time (1.5 V)[a]	10		ns
38	t_{CHCK}	X1 High Time (1.5 V)[a]	10		ns
39	t_{CKHL}	X1 Fall Time (3.5 to 1.0 V)[a]		5	ns
40	t_{CKLH}	X1 Rise Time (1.0 to 3.5 V)[a]		5	ns
CLKIN Requirements for Divide by Two Mode					
36	t_{CKIN}	X1 Period[a]	15	33	ns
37	t_{CLCK}	X1 Low Time (1.5 V)[a]	2.5		ns
38	t_{CHCK}	X1 High Time (1.5 V)[a]	2.5		ns
39	t_{CKHL}	X1 Fall Time (3.5 to 1.0 V)[a]		5	ns
40	t_{CKLH}	X1 Rise Time (1.0 to 3.5 V)[a]		5	ns
CLKOUT Timing					
42	t_{CLCL}	CLKOUTA Period	30		ns
43	t_{CLCH}	CLKOUTA Low Time (C_L=50 pF)	$0.5t_{CLCL}-1.5=13.5$		ns
44	t_{CHCL}	CLKOUTA High Time (C_L=50 pF)	$0.5t_{CLCL}-1.5=13.5$		ns
45	t_{CH1CH2}	CLKOUTA Rise Time (1.0 to 3.5 V)		3	ns
46	t_{CL2CL1}	CLKOUTA Fall Time (3.5 to 1.0 V)		3	ns
61	t_{LOCK}	Maximum PLL Lock Time		1	ms
69	t_{CICOA}	X1 to CLKOUTA Skew		20	ns
70	t_{CICOB}	X1 to CLKOUTB Skew		26	ns

Notes:

All timing parameters are measured at $V_{CC}/2$ with 50 pF loading on CLKOUTA, unless otherwise noted. All output test conditions are with C_L=50 pF. For switching tests, V_{IL}=0.3 V and $V_{IH}=V_{CC}-0.3$ V.

a The Times One mode should be used for operations from 16 MHz to 20 MHz. The Times Four mode should be used for operations above 20 MHz.

Switching Characteristics over Commercial and Industrial Operating Ranges

Clock (40 MHz and 50 MHz)

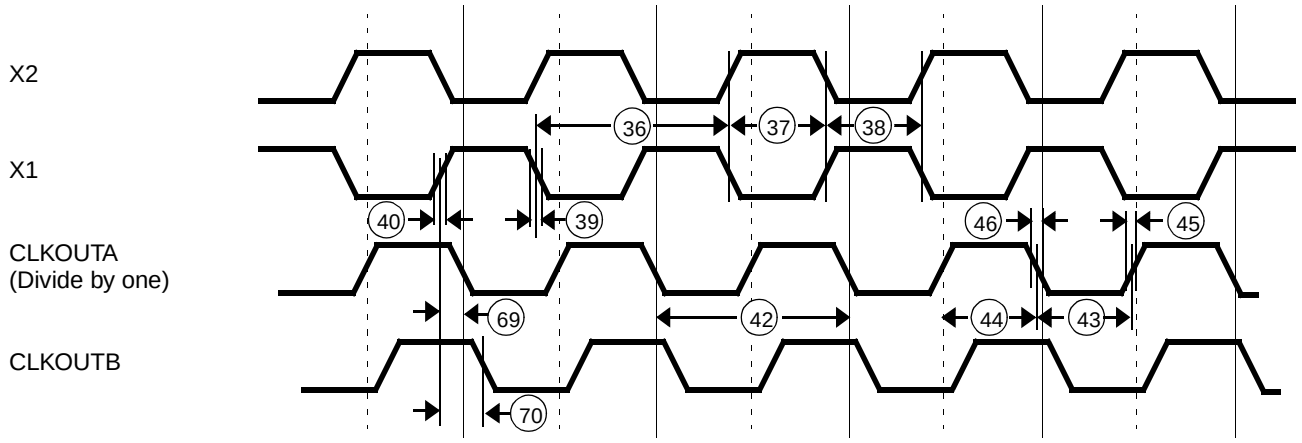
Parameter			Preliminary				Unit
			40 MHz		50 MHz		
No.	Symbol	Description	Min	Max	Min	Max	
CLKIN Requirements for Times Four Mode							
36	t_{CKIN}	X1 Period[a]	100	125	80	125	ns
37	t_{CLCK}	X1 Low Time (1.5 V)[a]	45		35		ns
38	t_{CHCK}	X1 High Time (1.5 V)[a]	45		35		ns
39	t_{CKHL}	X1 Fall Time (3.5 to 1.0 V)[a]		5		5	ns
40	t_{CKLH}	X1 Rise Time (1.0 to 3.5 V)[a]		5		5	ns
CLKIN Requirements for Times One Mode							
36	t_{CKIN}	X1 Period[a]	25	60	Not Supported		ns
37	t_{CLCK}	X1 Low Time (1.5 V)[a]	7.5				ns
38	t_{CHCK}	X1 High Time (1.5 V)[a]	7.5				ns
39	t_{CKHL}	X1 Fall Time (3.5 to 1.0 V)[a]		5			ns
40	t_{CKLH}	X1 Rise Time (1.0 to 3.5 V)[a]		5			ns
CLKIN Requirements for Divide by Two Mode							
36	t_{CKIN}	X1 Period[a]	12.5	33	Not Supported		ns
37	t_{CLCK}	X1 Low Time (1.5 V)[a]	1.25				ns
38	t_{CHCK}	X1 High Time (1.5 V)[a]	1.25				ns
39	t_{CKHL}	X1 Fall Time (3.5 to 1.0 V)[a]		5			ns
40	t_{CKLH}	X1 Rise Time (1.0 to 3.5 V)[a]		5			ns
CLKOUT Timing							
42	t_{CLCL}	CLKOUTA Period	25		20		ns
43	t_{CLCH}	CLKOUTA Low Time (C_L=50 pF)	$0.5t_{CLCL}$–1.25=11.25		$0.5t_{CLCL}$–1=9		ns
44	t_{CHCL}	CLKOUTA High Time (C_L=50 pF)	$0.5t_{CLCL}$–1.25=11.25		$0.5t_{CLCL}$–1=9		ns
45	t_{CH1CH2}	CLKOUTA Rise Time (1.0 to 3.5 V)		3		3	ns
46	t_{CL2CL1}	CLKOUTA Fall Time (3.5 to 1.0 V)		3		3	ns
61	t_{LOCK}	Maximum PLL Lock Time		1		1	ms
69	t_{CICOA}	X1 to CLKOUTA Skew		20		15	ns
70	t_{CICOB}	X1 to CLKOUTB Skew		24		21	ns

Notes:

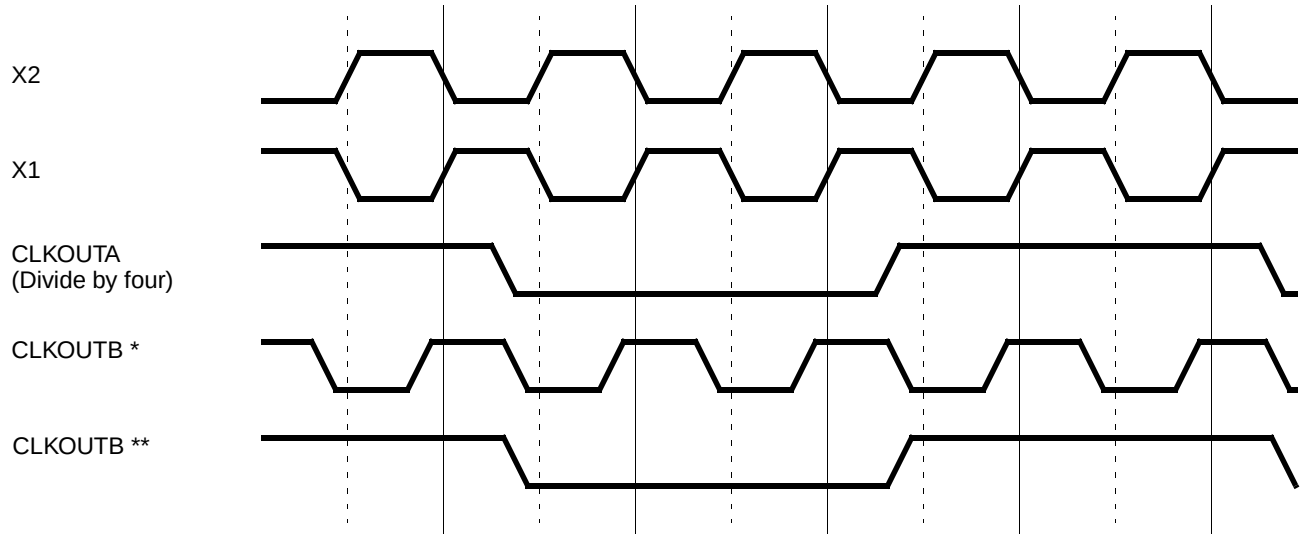
All timing parameters are measured at V_{CC}/2 with 50 pF loading on CLKOUTA, unless otherwise noted. All output test conditions are with C_L=50 pF. For switching tests, V_{IL}=0.3 V and V_{IH}=V_{CC}–0.3 V.

a The Times One mode should be used for operations from 16 MHz to 20 MHz. The Times Four mode should be used for operations above 20 MHz.

Clock Waveforms—Active Mode



Clock Waveforms—Power-Save Mode



Notes:

* *The CLKOUTB Output Frequency (CBF) bit in the Power Save Control Register (PDCON) is set to 1.*

** *The CLKOUTB Output Frequency (CBF) bit in the Power Save Control Register (PDCON) is cleared to 0.*

Switching Characteristics over Commercial and Industrial Operating Ranges
Ready and Peripheral Timing (25 MHz and 33 MHz)

Parameter			Preliminary				Unit
			25 MHz		33 MHz		
No.	Symbol	Description	Min	Max	Min	Max	
Ready and Peripheral Timing Requirements							
47	t_{SRYCL}	SRDY Transition Setup Time[a]	10		8		ns
48	t_{CLSRY}	SRDY Transition Hold Time[a]	3		3		ns
49	t_{ARYCH}	ARDY Resolution Transition Setup Time[b]	10		8		ns
50	t_{CLARX}	ARDY Active Hold Time[a]	4		4		ns
51	t_{ARYCHL}	ARDY Inactive Holding Time	4		4		ns
52	t_{ARYLCL}	ARDY Setup Time[a]	15		10		ns
53	t_{INVCH}	Peripheral Setup Time[b]	10		8		ns
54	t_{INVCL}	DRQ Setup Time[b]	10		8		ns
Peripheral Timing Responses							
55	t_{CLTMV}	Timer Output Delay		20		15	ns

Notes:

All timing parameters are measured at $V_{CC}/2$ with 50 pF loading on CLKOUTA, unless otherwise noted. All output test conditions are with C_L=50 pF. For switching tests, V_{IL}=0.3 V and $V_{IH}=V_{CC}-0.3$ V.

a This timing must be met to guarantee proper operation.

b This timing must be met to guarantee recognition at the clock edge.

Switching Characteristics over Commercial and Industrial Operating Ranges
Ready and Peripheral Timing (40 MHz and 50 MHz)

Parameter			Preliminary				Unit
			40 MHz		50 MHz		
No.	Symbol	Description	Min	Max	Min	Max	
Ready and Peripheral Timing Requirements							
47	t_{SRYCL}	SRDY Transition Setup Time[a]	5		5		ns
48	t_{CLSRY}	SRDY Transition Hold Time[a]	2		2		ns
49	t_{ARYCH}	ARDY Resolution Transition Setup Time[b]	5		5		ns
50	t_{CLARX}	ARDY Active Hold Time[a]	3		3		ns
51	t_{ARYCHL}	ARDY Inactive Holding Time	5		5		ns
52	t_{ARYLCL}	ARDY Setup Time[a]	5		5		ns
53	t_{INVCH}	Peripheral Setup Time[b]	5		5		ns
54	t_{INVCL}	DRQ Setup Time[b]	5		5		ns
Peripheral Timing Responses							
55	t_{CLTMV}	Timer Output Delay		12		10	ns

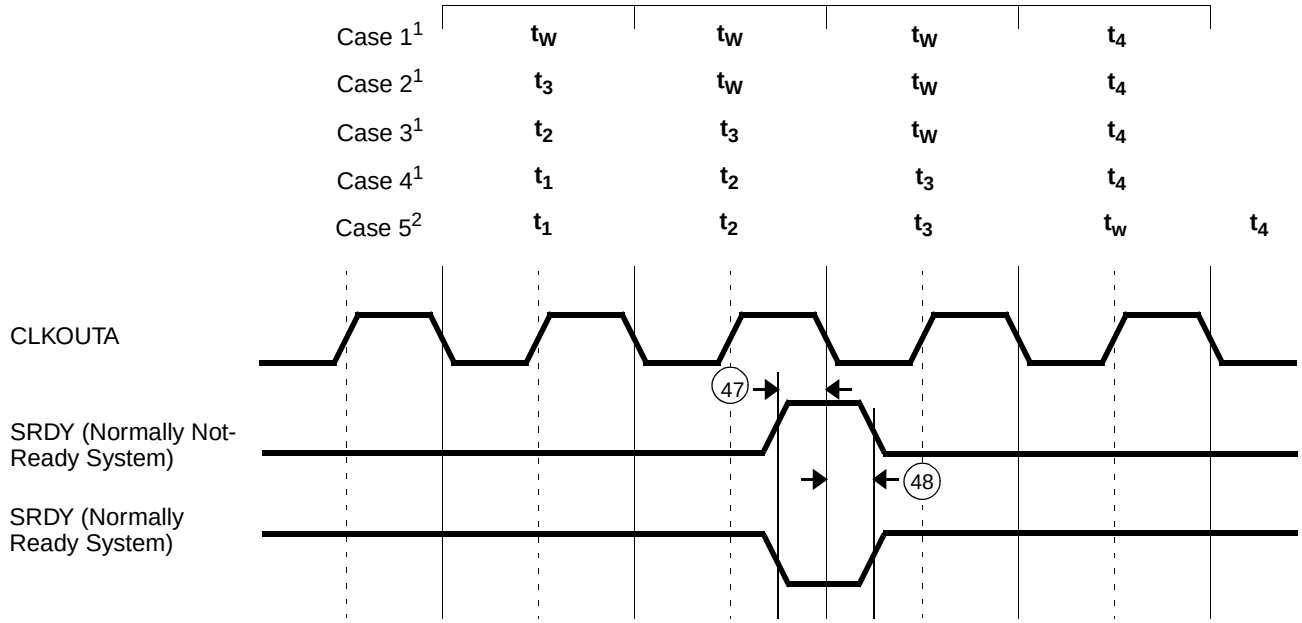
Notes:

All timing parameters are measured at $V_{CC}/2$ with 50 pF loading on CLKOUTA unless otherwise noted. All output test conditions are with C_L=50 pF. For switching tests, V_{IL}=0.3 V and $V_{IH}=V_{CC}-0.3$ V.

a This timing must be met to guarantee proper operation.

b This timing must be met to guarantee recognition at the clock edge.

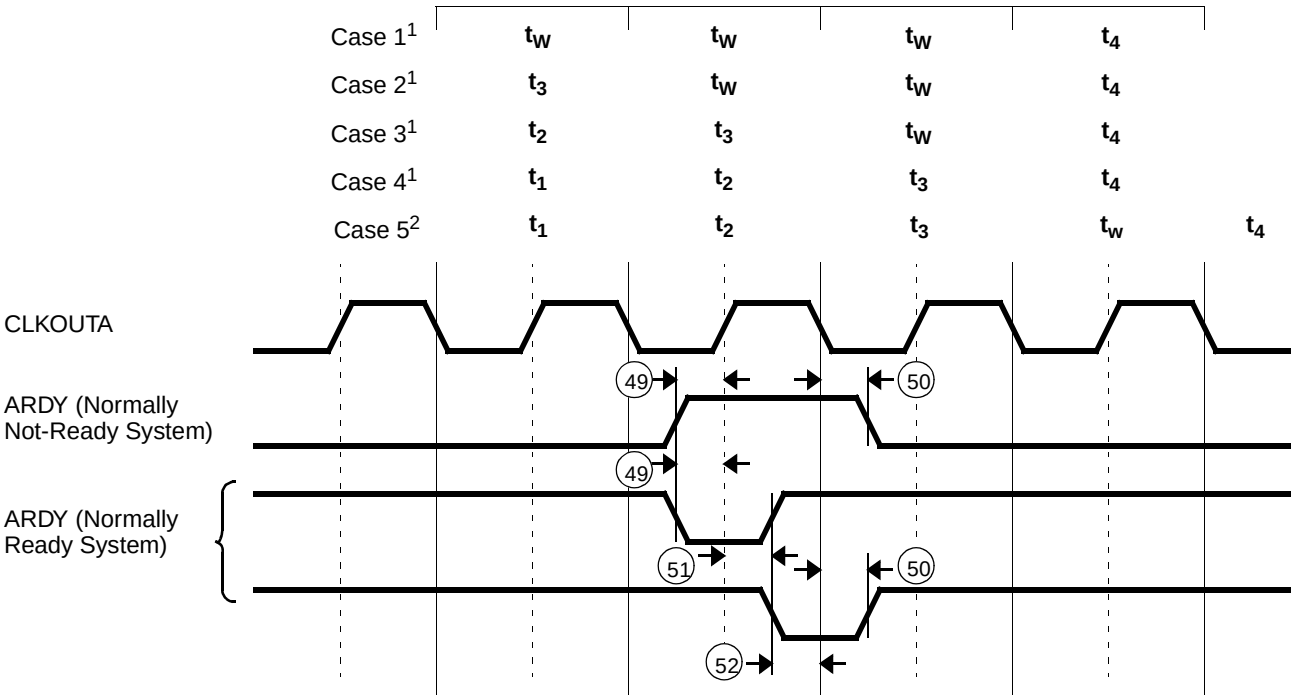
Synchronous Ready Waveforms



Notes:

1. *Normally not-ready system.*
2. *Normally ready system.*

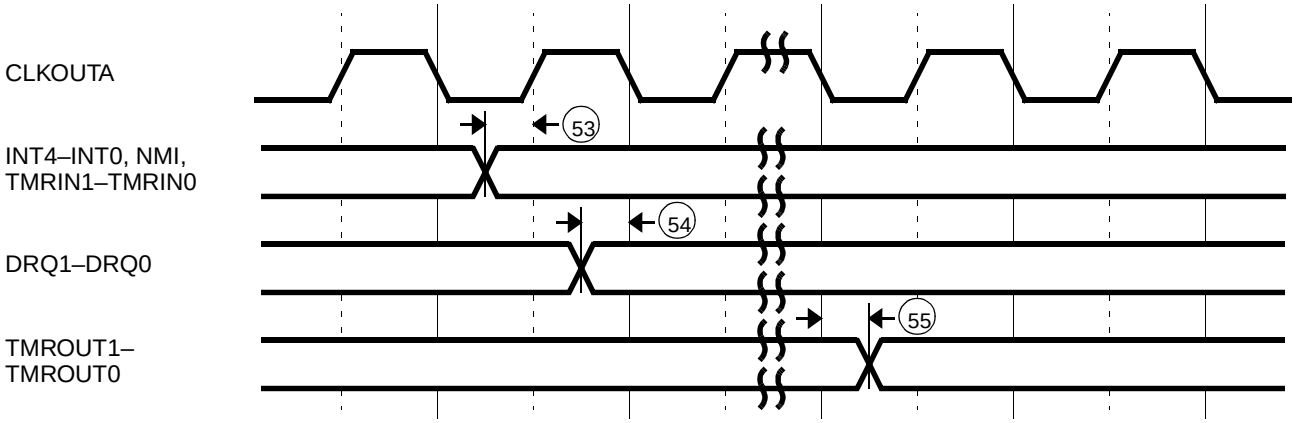
Asynchronous Ready Waveforms



Notes:

1. *Normally not-ready system.*
2. *Normally ready system.*

Peripheral Waveforms



Switching Characteristics over Commercial and Industrial Operating Ranges
Reset and Bus Hold (25 MHz and 33 MHz)

Parameter			Preliminary				Unit
			25 MHz		33 MHz		
No.	Symbol	Description	Min	Max	Min	Max	
Reset and Bus Hold Timing Requirements							
5	t_{CLAV}	AD Address Valid Delay	0	20	0	15	ns
15	t_{CLAZ}	AD Address Float Delay	0	20	0	15	ns
57	t_{RESIN}	$\overline{RES}$ Setup Time	10		8		ns
58	t_{HVCL}	HOLD Setup[a]	10		8		ns
Reset and Bus Hold Timing Responses							
62	t_{CLHAV}	HLDA Valid Delay	0	20	0	15	ns
63	t_{CHCZ}	Command Lines Float Delay		20		15	ns
64	t_{CHCV}	Command Lines Valid Delay (after Float)		20		15	ns

Notes:

All timing parameters are measured at $V_{CC}/2$ with 50 pF loading on CLKOUTA, unless otherwise noted. All output test conditions are with C_L=50 pF. For switching tests, V_{IL}=0.3 V and $V_{IH}=V_{CC}-0.3$ V.

a This timing must be met to guarantee recognition at the next clock.

Switching Characteristics over Commercial and Industrial Operating Ranges
Reset and Bus Hold (40 MHz and 50 MHz)

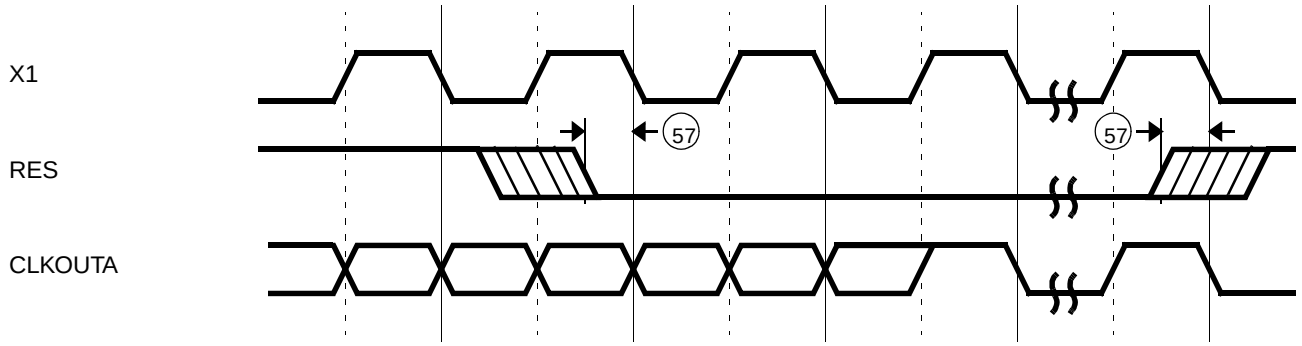
Parameter			Preliminary				Unit
			40 MHz		50 MHz		
No.	Symbol	Description	Min	Max	Min	Max	
Reset and Bus Hold Timing Requirements							
5	t_{CLAV}	AD Address Valid Delay	0	12	0	10	ns
15	t_{CLAZ}	AD Address Float Delay	0	12	0	10	ns
57	t_{RESIN}	$\overline{RES}$ Setup Time	5		5		ns
58	t_{HVCL}	HOLD Setup[a]	5		5		ns
Reset and Bus Hold Timing Responses							
62	t_{CLHAV}	HLDA Valid Delay	0	12	0	10	ns
63	t_{CHCZ}	Command Lines Float Delay		12		10	ns
64	t_{CHCV}	Command Lines Valid Delay (after Float)		12		10	ns

Notes:

All timing parameters are measured at $V_{CC}/2$ with 50 pF loading on CLKOUTA, unless otherwise noted. All output test conditions are with C_L=50 pF. For switching tests, V_{IL}=0.3 V and $V_{IH}=V_{CC}-0.3$ V.

a This timing must be met to guarantee recognition at the next clock.

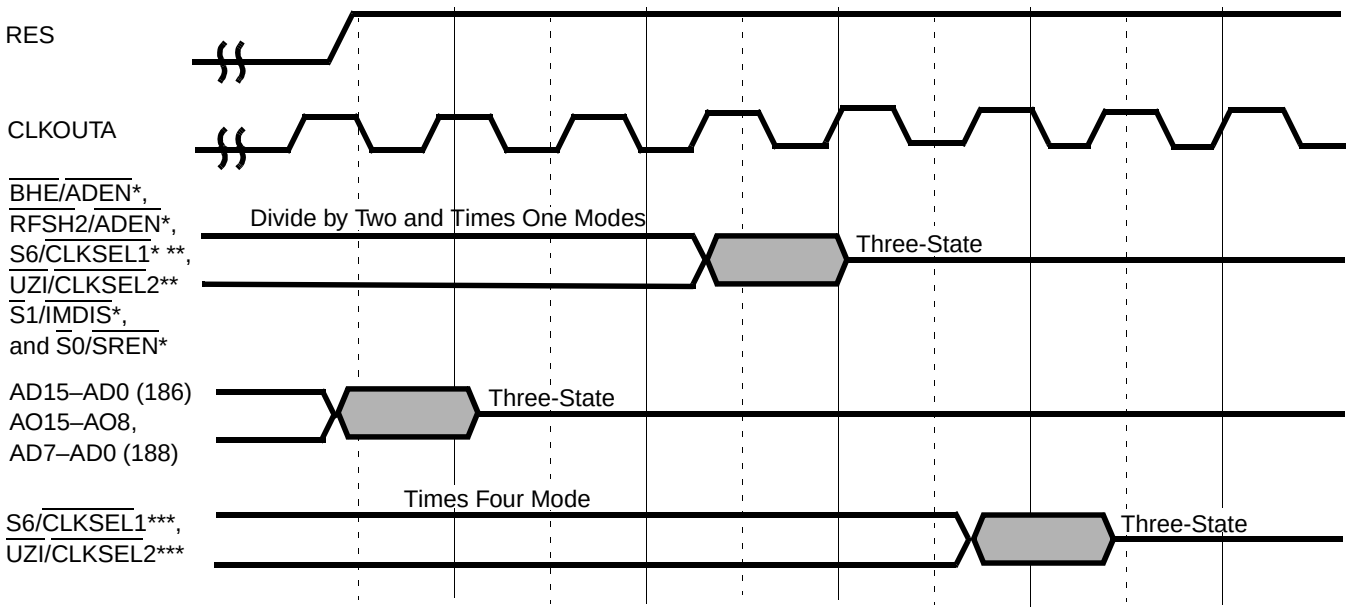
Reset Waveforms



Note:

$\overline{RES}$ must be held Low for 1 ms during power-up to ensure proper device initialization. Activating the PLL will require 1 ms to achieve a stable clock.

Signals Related to Reset Waveforms



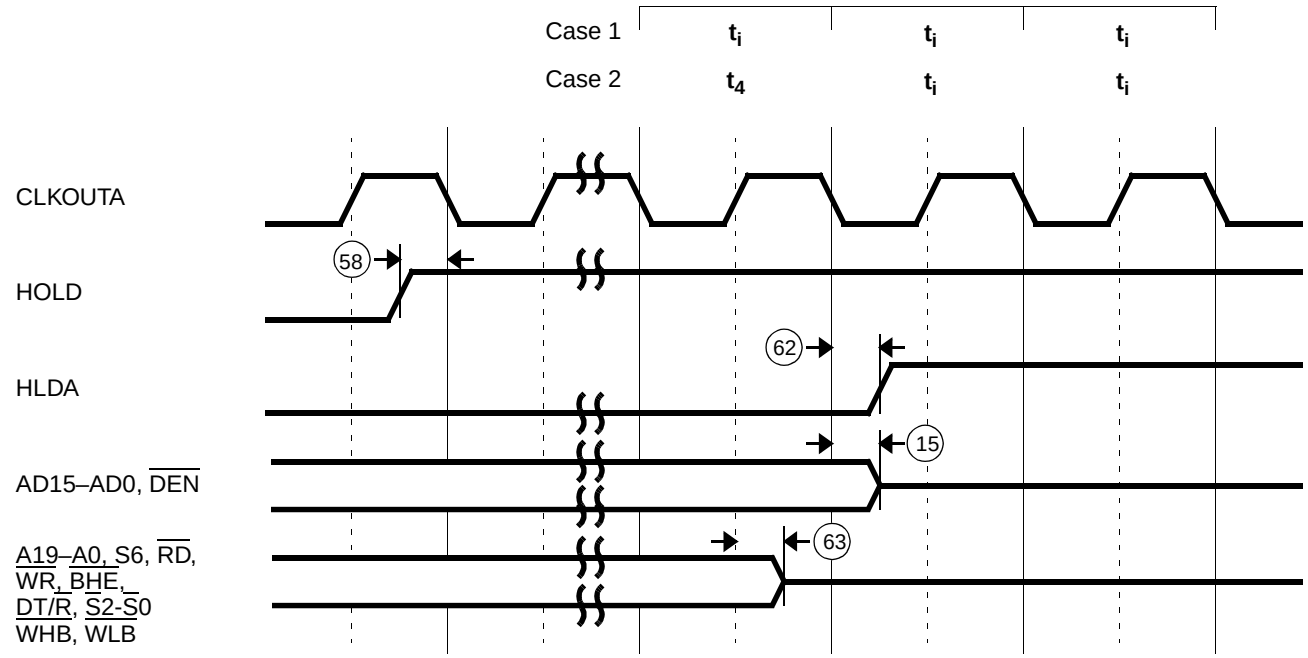
Notes:

* *Because $\overline{BHE}$, $\overline{RFSH2}$, S6, $\overline{UZI}$, $\overline{S1}$, and $\overline{S0}$ are not driven for 6.5 clocks after reset, their alternate functions can be asserted with external pulldown resistors.*

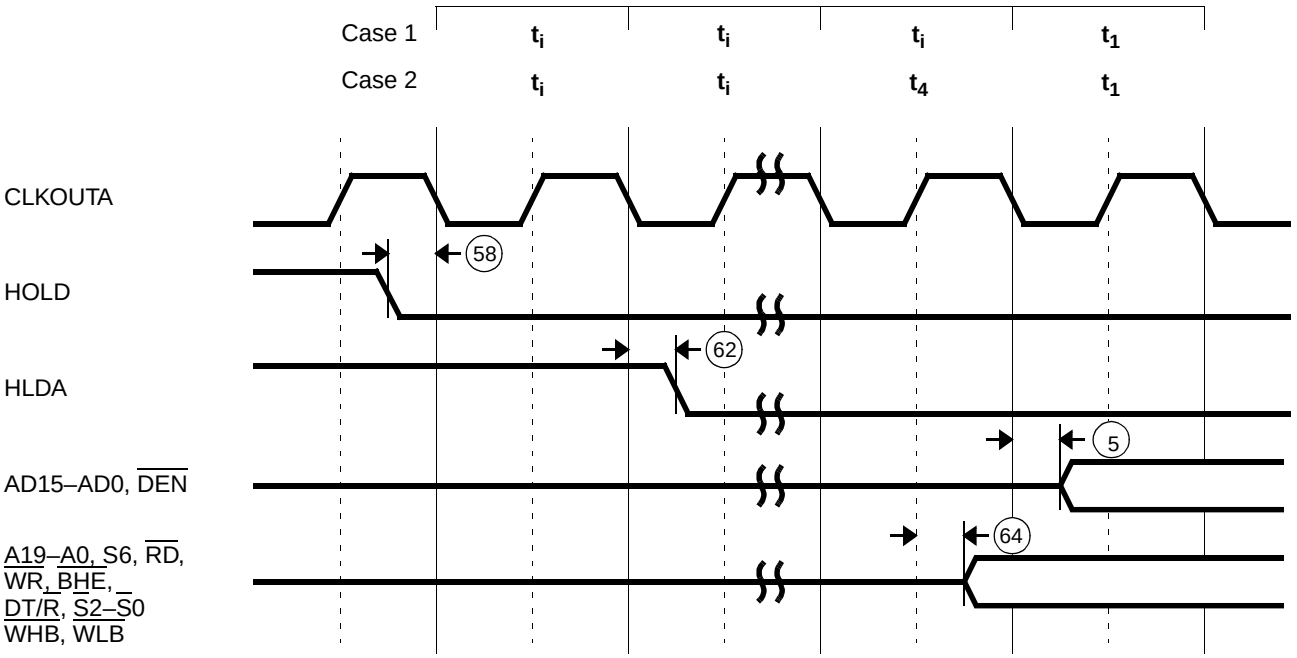
** *In Divide by Two mode and Times One mode, S6/$\overline{CLKSEL1}$ and UZI/$\overline{CLKSEL2}$ must be held for 3 clock cycles after reset negates.*

****In Times Four mode, S6/$\overline{CLKSEL1}$ and UZI/$\overline{CLKSEL2}$ must be held for 5 clock cycles after reset negates.*

Bus Hold Waveforms—Entering



Bus Hold Waveforms—Leaving



Switching Characteristics over Commercial and Industrial Operating Ranges
Synchronous Serial Interface (SSI) (25 MHz and 33 MHz)

Parameter			Preliminary				Unit
			25 MHz		33 MHz		
No.	Symbol	Description	Min	Max	Min	Max	
Synchronous Serial Port Timing Requirements							
75	t_{DVSH}	Data Valid to SCLK High	10		8		ns
77	t_{SHDX}	SCLK High to SPI Data Hold	3		2		ns
Synchronous Serial Port Timing Responses							
71	t_{CLEV}	CLKOUTA Low to SDEN1 or SDEN0 Valid		20	0	15	ns
72	t_{CLSL}	CLKOUTA Low to SCLK Low		20	0	15	ns
78	t_{SLDV}	SCLK Low to Data Valid		20	0	15	ns

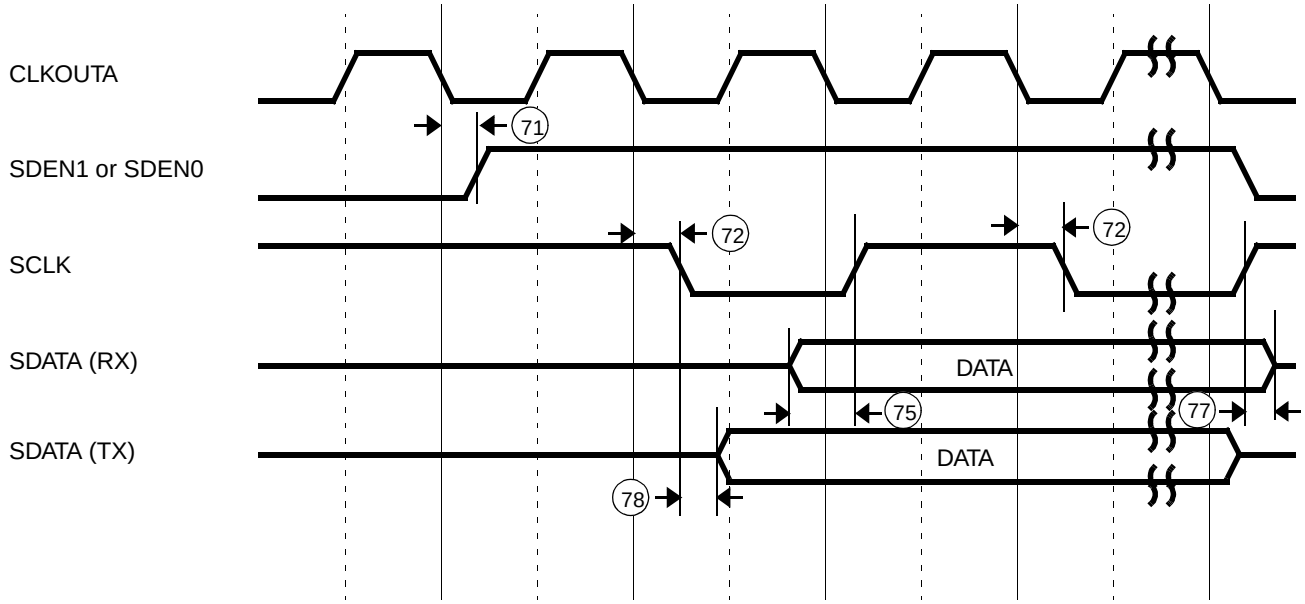
Note:
All timing parameters are measured at $V_{CC}/2$ with 50 pF loading on CLKOUTA, unless otherwise noted. All output test conditions are with C_L=50 pF. For switching tests, V_{IL}=0.3 V and $V_{IH}=V_{CC}-0.3$ V.

Switching Characteristics over Commercial and Industrial Operating Ranges
Synchronous Serial Interface (SSI) (40 MHz and 50 MHz)

Parameter			Preliminary				Unit
			40 MHz		50 MHz		
No.	Symbol	Description	Min	Max	Min	Max	
Synchronous Serial Port Timing Requirements							
75	t_{DVSH}	Data Valid to SCLK High	5		5		ns
77	t_{SHDX}	SCLK High to SPI Data Hold	2		2		ns
Synchronous Serial Port Timing Responses							
71	t_{CLEV}	CLKOUTA Low to SDEN1 or SDEN0 Valid	0	12	0	10	ns
72	t_{CLSL}	CLKOUTA Low to SCLK Low	0	12	0	10	ns
78	t_{SLDV}	SCLK Low to Data Valid	0	12	0	10	ns

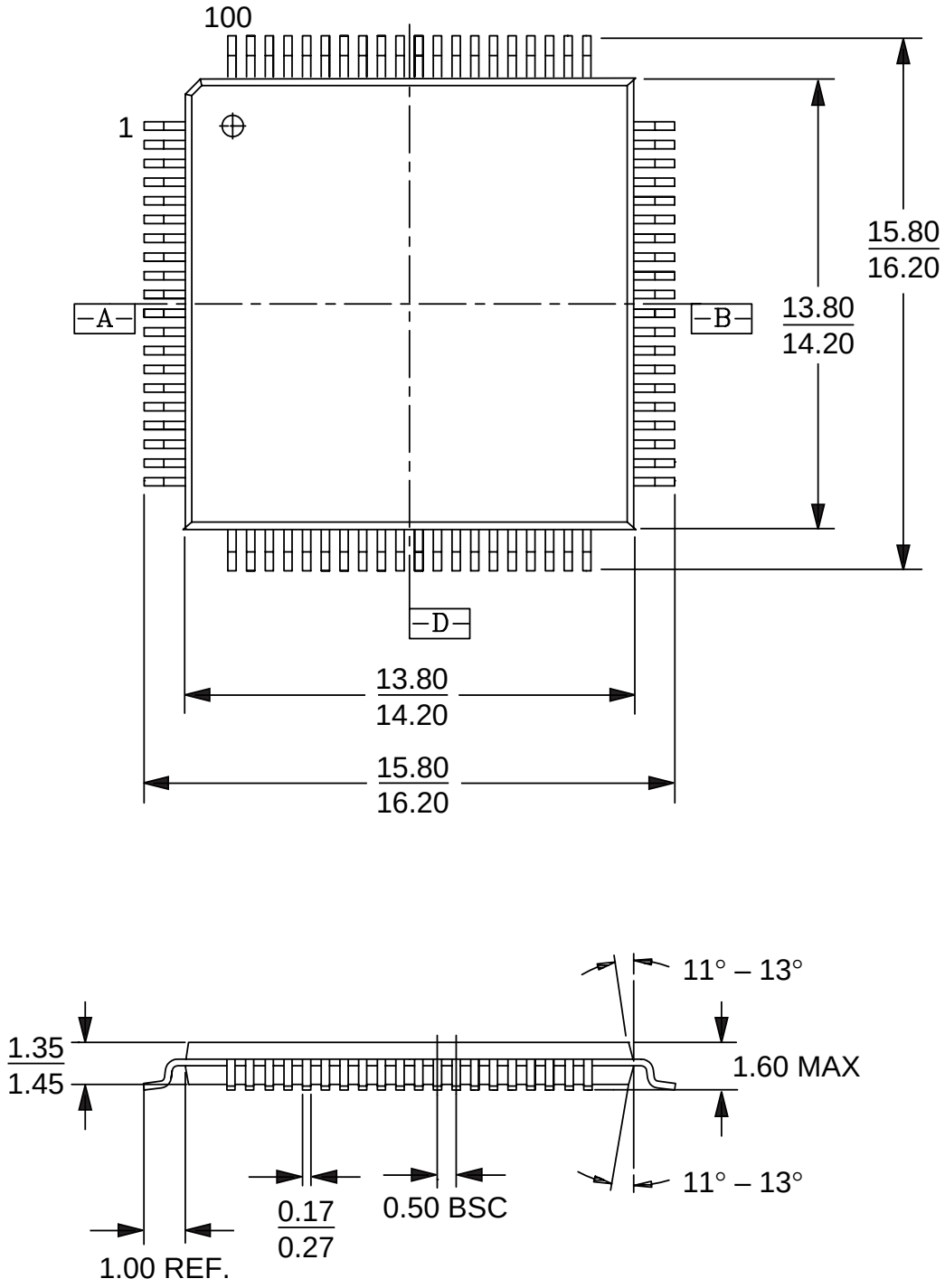
Note:
All timing parameters are measured at $V_{CC}/2$ with 50 pF loading on CLKOUTA, unless otherwise noted. All output test conditions are with C_L=50 pF. For switching tests, V_{IL}=0.3 V and $V_{IH}=V_{CC}-0.3$ V.

Synchronous Serial Interface (SSI) Waveforms



Note:
SDATA is bidirectional and used for either transmit (TX) or receive (RX). Timing is shown separately for each case.

TQFP PHYSICAL DIMENSIONS
PQL 100, Trimmed and Formed
Thin Quad Flat Pack

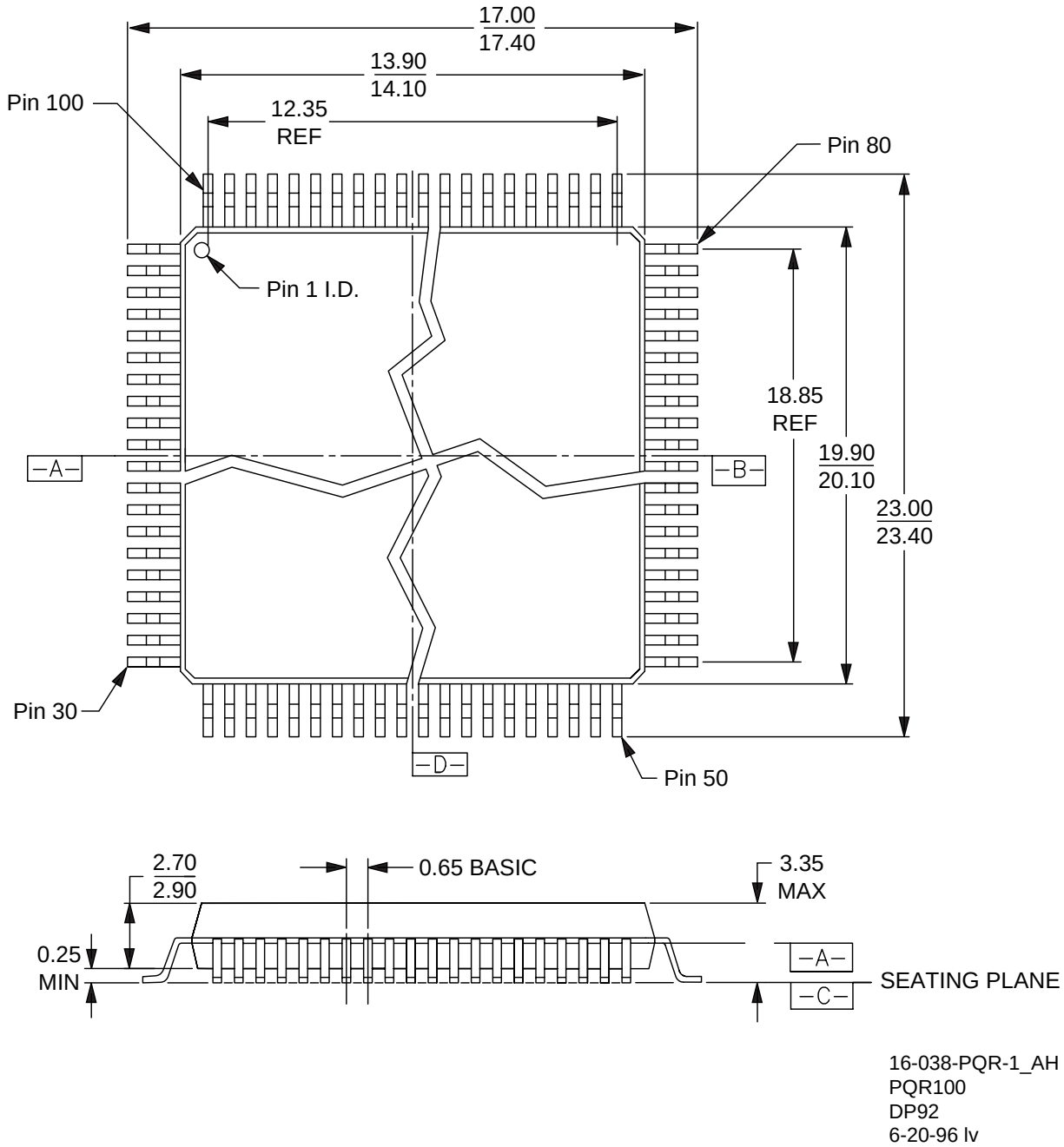


16-038-PQT-2_AI
PQL100
9.3.96 lv

Notes:

1. *All measurements are in millimeters, unless otherwise noted.*
2. *Not to scale; for reference only.*

PQFP PHYSICAL DIMENSIONS
PQR 100, Trimmed and Formed
Plastic Quad Flat Pack



16-038-PQR-1_AH
PQR100
DP92
6-20-96 lv

Notes:

1. *All measurements are in millimeters, unless otherwise noted.*
2. *Not to scale; for reference only.*

INDEX

A

A17/PIO7, 30
A18/PIO8, 30
A19/PIO9, 30
absolute maximum ratings, 60
active mode
  clock waveforms, 95
AD15–AD8, 30
AD7–AD0, 30
address bus
  Am186ER
    disable in effect, 42
    normal operation, 42
  Am188ER
    disable in effect, 43
ALE, 31
alphabetic PIO pin assignments, 36
ambient temperatures
  ambient, 62
  PQFP with four-to-six layer board, 65
  PQFP with two-layer board, 63
  TQFP with four-to-six layer boards, 66
  TQFP with two-layer board, 64
AO15–AO8, 30
application considerations, 14
ARDY, 31
asynchronous ready waveforms, 97
asynchronous serial port, 56

B

$\overline{\text{BHE}}$/$\overline{\text{ADEN}}$, 31
block diagram
  Am186ER, 2
  Am188ER, 3
bus cycle encoding, 37
bus hold waveforms
  entering, 101
  leaving, 101
bus interface unit, 41
bus operation, 41
byte write enables, 41

C

chip-select
  low memory, 51
  overlap, 51
  timing, 49
  unit, 49
  upper memory, 51
chip-selects
  midrange memory, 51
  peripheral, 52
CLKOUTA, 31
CLKOUTB, 31
clock (25 MHz), 92
clock (33 MHz), 93
clock (40 and 50 MHz), 94
clock and power management, 44
clock frequencies
  minimum and maximum, 44
clock generation, 14
clock organization, 48
clock source
  crystal driven, 45
clock waveforms
  active mode, 95
  power-save mode, 95
clocking modes, 39
commercial operating ranges, 60
comparison
  Am186ER and 80C186 microcontrollers, 15
crystal
  selecting, 45
crystal-driven clock source, 45
customer support, 13
  documentation and literature, 13
  hotline and web, 13
  literature ordering, 13
  third-party development support products, 13
  web home page, 13

D

DC characteristics, 60
demonstration board products, 13
$\overline{\text{DEN}}$/PIO5, 31
description, 1
  functional, 40
direct memory access, 54
DMA
  Am186ER maximum transfer rates, 55
  asynchronous serial port transfers, 55
  channel control registers, 55–56
  operation, 55
  priority, 55–56
  transfers through serial port, 56
  unit block diagram, 56
documentation
  See customer support.
DRQ1–DRQ0, 32
DT/$\overline{\text{R}}$/PIO4, 32

E

emulator and debug modes, 52
  internal memory disable, 52
  show read enable, 52
external source clock, 45

F

features
  3.3-V operation with 5-V-tolerant I/O, 14
  available native development tools, applications, and system software, 1
  enhanced bus interface, 1
  enhanced functionality, 1, 14
  enhanced integrated peripherals, 1
  enhanced performance, 14
  faster access to memory and clock input modes, 1
  integrated RAM, 14
  memory integration, 1
  software-compatible, 1
  x86 software compatibility, 14
four-pin interface, 57
functional description, 40

G

GND, 32

H

HLDA, 32
HOLD, 32
hotline and world wide web support, 13

I

I/O circuitry, 59
I/O space, 40
industrial operating ranges, 60
initialization and processor reset, 48
input/output circuitry, 59
INT0, 32
INT1/$\overline{\text{SELECT}}$, 32
INT2/$\overline{\text{INTA}}$0/PIO31, 33
INT3/$\overline{\text{INTA}}$1/IRQ, 33
INT4/PIO30, 33
interaction with external RAM, 52
internal memory, 52
internal memory disable, 52
internal RAM show read cycle waveform, 77
interrupt acknowledge cycle (25 and 33 MHz), 87
interrupt acknowledge cycle (40 and 50 MHz), 88
interrupt acknowledge cycle waveforms, 89
interrupt control unit, 53
  programming, 53

J

junction temperature calculation, 62

L

$\overline{\text{LCS}}$/$\overline{\text{ONCE}}$0, 33
literature
  See customer support.
logic diagram
  ARDY and SRDY synchronization, 49
low memory chip select, 51
low-voltage operation, 57
low-voltage standard, 59

M

MCS2–MCS0, 34
MCS3/RFSH/PIO25, 33
memory interface, 14
  example, 15
memory maps, 50
  diagram, 50
memory organization, 40
midrange memory chip selects, 51
modes
  emulator and debug, 52

N

NMI, 34
nonmultiplexed address bus, 41
numeric PIO pin assignments, 36

O

operating ranges, 60
  commercial and industrial, 60
operation
  low-voltage, 57
ordering information, 4
oscillator configurations, 45
output enable, 41

P

PCB, 44
  reading and writing, 44
PCS0/PIO16, 34
PCS1/PIO17, 34
PCS2/PIO18, 34
PCS3/PIO19, 34
PCS3–PCS0, 34
PCS5/A1/PIO3, 34
PCS6/A2/PIO2, 34
peripheral chip selects, 52
peripheral control block, 44
peripheral waveforms, 98
phase-locked loop, 44
pins
  A19–A0, 30
  AD15–AD8, 30
  AD7–AD0, 30
  ALE, 31
  alphabetic PIO assignments, 36
  AO15–AO8, 30
  ARDY, 31
  BHE/ADEN, 31
  CLKOUTA, 31
  CLKOUTB, 31
  clocking modes, 39
  DEN/PIO5, 31
  descriptions, 30
  DRQ1–DRQ0, 32
  DT/R/PIO4, 32
  GND, 32
  HLDA, 32
  HOLD, 32
  INT0, 32
  INT1/SELECT, 32
  INT2/INTA0/PIO31, 33
  INT3/INTA1/IRQ, 33
  INT4/PIO30, 33
  LCS/ONCE0, 33
  MCS2–MCS0, 34
  MCS3/RFSH/PIO25, 33
  NMI, 34
  numeric PIO assignments, 36
  PCS0/PIO16, 34
  PCS1/PIO17, 34
  PCS3–PCS0, 34
  PCS6/A2/PIO2, 34
  PIO, 57
  PIO31–PIO0, 35
  RD, 35
  RES, 35
  RFSH2/ADEN, 35
  RXD/PIO28, 35
  S0/SREN, 37
  S1/IMDIS, 37
  S2, 35
  S6/CLKSEL1/PIO29, 37
  SCLK/PIO20, 37
  SDATA/PIO21, 37
  SDEN0/PIO22, 37
  SDEN1/PIO23, 37
  SRDY/PIO6, 38
  TMRIN0/PIO11, 38
  TMRIN1/PIO0, 38
  TMROUT0/PIO10, 38
  TMROUT1/PIO1, 38
  TXD/PIO27, 38
  UCS/ONCE1, 38
  used by emulators, 30
  UZI/CLKSEL2/PIO26, 38
  VCC, 39
  WB (Am188ER microcontroller only), 39
  WHB, 39
  WLB (Am186ER microcontroller only), 39
  WR, 39
  X1, 39
  X2, 39
PIO31–PIO0, 35
plastic quad flat pack, 105

PLL, 44
power consumption calculation, 62
power savings, 59
power-save mode
  clock waveforms, 95
power-save operation, 48
PQFP connection diagram and pinouts
  Am186ER, 22
  Am188ER, 25
PQFP physical dimensions, 105
PQFP pin assignments
  Am186ER
    sorted by pin name, 24
    sorted by pin number, 23
  Am188ER
    sorted by pin name, 27
    sorted by pin number, 26
programmable I/O (PIO) pins, 57
programming
  interrupt control unit, 53
  ready and wait-state, 49
pseudo static RAM
  support, 44
PSRAM
  support, 44
PSRAM read cycle (25 and 33 MHz), 78
PSRAM read cycle (40 and 50 MHz), 79
PSRAM read cycle waveforms, 80
PSRAM refresh cycle (25 and 33 MHz), 84
PSRAM refresh cycle (40 and 50 MHz), 85
PSRAM refresh cycle waveforms, 86
PSRAM write cycle
  waveforms, 83
PSRAM write cycle (25 and 33 MHz), 81
PSRAM write cycle (40 and 50 MHz), 82

R

RAM
  interaction with external, 52
$\overline{RD}$, 35
read cycle waveforms, 72
ready and peripheral timing (25 and 33 MHz), 96
ready and peripheral timing (40 and 50 MHz), 96
ready and wait-state programming, 49
refresh control unit, 53
related documents, 13
$\overline{RES}$, 35
reset
  initialization and processor, 48
reset and bus hold (25 and 33 MHz), 99
reset and bus hold (40 and 50 MHz), 99
reset configuration register, 48
reset waveforms, 100
  related signals, 100
revision history, 10
$\overline{RFSH2}$/$\overline{ADEN}$, 35
RXD/PIO28, 35

S

$\overline{S0}$/$\overline{SREN}$, 37
$\overline{S1}$/$\overline{IMDIS}$, 37
$\overline{S2}$, 35
S6/$\overline{CLKSEL1}$/PIO29, 37
SCLK/PIO20, 37
SDATA/PIO21, 37
SDEN0/PIO22, 37
SDEN1/PIO23, 37
serial ports
  DMA transfers, 55
software halt cycle (25 and 33 MHz), 90
software halt cycle (40 and 50 MHz), 90
software halt cycle waveforms, 91
source clock
  external, 45
SRDY/PIO6, 38
SSI, 102
  multiple read, 58
  multiple write, 58
  waveforms, 103
support, 13
switching characteristics
  clock (25 MHz), 92
  clock (33 MHz), 93
  clock (40 and 50 MHz), 94
  commercial, 67
  industrial, 67
  internal RAM show read cycle (25 and 33 MHz), 76
  interrupt acknowledge cycle (25 and 33 MHz), 87
  interrupt acknowledge cycle (40 and 50 MHz), 88
  PSRAM read cycle (25 and 33 MHz), 78
  PSRAM read cycle (40 and 50 MHz), 79
  PSRAM refresh cycle (25 and 33 MHz), 84
  PSRAM refresh cycle (40 and 50 MHz), 85
  PSRAM write cycle (25 and 33 MHz), 81
  PSRAM write cycle (40 and 50 MHz), 82
  read cycle (25 and 33 MHz), 70
  read cycle (40 and 50 MHz), 71
  ready and peripheral timing (25 and 33 MHz), 96
  ready and peripheral timing (40 and 50 MHz), 96
  reset and bus hold (25 and 33 MHz), 99
  reset and bus hold (40 and 50 MHz), 99
  software halt cycle (25 and 33 MHz), 90
  software halt cycle (40 and 50 MHz), 90

synchronous serial interface (25 and 33 MHz), 102
synchronous serial interface (40 and 50 MHz), 102
write cycle (25 and 33 MHz), 72–73
write cycle (40 and 50 MHz), 74, 76
switching parameter symbols
alphabetical key, 68
numerical key, 69
switching waveforms
key, 67
synchronous ready waveforms, 97
synchronous serial interface, 56
multiple read, 58
multiple write, 58
synchronous serial interface (25 and 33 MHz), 102
synchronous serial interface (40 and 50 MHz), 102
synchronous serial interface waveforms, 103

T

thermal characteristics, 61
thermal characteristics equations, 61
thermal resistance, 61
thin quad flat pack, 104
third-party development support products, 13
timer control unit, 53
TMRIN0/PIO11, 38
TMRIN1/PIO0, 38
TMROUT0/PIO10, 38
TMROUT1/PIO1, 38
TQFP connection diagram and pinouts
Am186ER, 16
Am188ER, 19
TQFP package, 61
TQFP physical dimensions, 104
TQFP pin assignments
Am186ER, 19
sorted by pin name, 18
sorted by pin number, 17
Am188ER
sorted by pin name, 21
sorted by pin number, 20
two-component address, 40
TXD/PIO27, 38
typical ambient temperatures, 62

U

$\overline{\text{UCS}}$/$\overline{\text{ONCE}}$1, 38
upper memory chip select, 51
$\overline{\text{UZI}}$/$\overline{\text{CLKSEL}}$2/PIO26, 38

V

VCC, 39

W

watchdog timer, 54
waveform
internal RAM show read, 77
waveforms, 67
asynchronous ready, 97
bus hold
entering, 101
leaving, 101
interrupt acknowledge cycle, 89
peripheral, 98
PSRAM read cycle, 80
PSRAM refresh cycle, 86
PSRAM write cycle, 83
read cycle, 72
reset, 100
signals related to reset, 100
software halt cycle, 91
SSI, 103
synchronous ready, 97
synchronous serial interface, 103
write cycle, 75
$\overline{\text{WB}}$ (Am188ER microcontroller only), 39
$\overline{\text{WHB}}$, 39
$\overline{\text{WLB}}$ (Am186ER microcontroller only), 39
world wide web support, 13
$\overline{\text{WR}}$, 39
write cycle waveforms, 75
www
home page, 13
support, 13

X

X1, 39
X2, 39

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