Data Sheet
April 2001

Quad Differential Receivers
BRF1A, BRF2A, BRS2B, BRR1A, and BRT1A

Features

- Pin equivalent to the general-trade 26LS32 device, with improved speed, reduced power consumption, and significantly lower levels of EMI
- High input impedance approximately 8 kΩ
- Four line receivers per package
- 400 Mbits/s maximum data rate when used with Agere Systems Inc. data transmission drivers
- Meets enhanced small device interface (ESDI) standards
- 4.0 ns maximum propagation delay
- <0.20 V input sensitivity
- −1.2 V to +7.2 V common-mode range
- −40 °C to +125 °C ambient operating temperature range (wider than the 41 Series)
- Single 5.0 V ± 10% supply
- Output defaults to logic 1 when inputs are left open*
- Available in four package types
- Lower power requirement than the 41 Series

Description

These quad differential receivers accept digital data over balanced transmission lines. They translate differential input logic levels to TTL output logic levels. All devices in this family have four receivers with a common enable control. These receivers are pin equivalent to the general-trade 26LS32, but offer increased speed and decreased power consumption. They replace the Agere 41 Series receivers.

* This feature is available on BRF1A and BRF2A.

The BRF1A device is the generic receiver in this family and requires the user to supply external resistors on the circuit board for impedance matching.

The BRF2A is identical to the BRF1A, but has an electrostatic discharge (ESD) protection circuit added to significantly improve the ESD human-body model (HBM) characteristics on the differential input terminals.

The BRS2B is identical to the BRF2A, but has a preferred state feature that places the output in the high state when the inputs are open, shorted to ground, or shorted to the power supply.

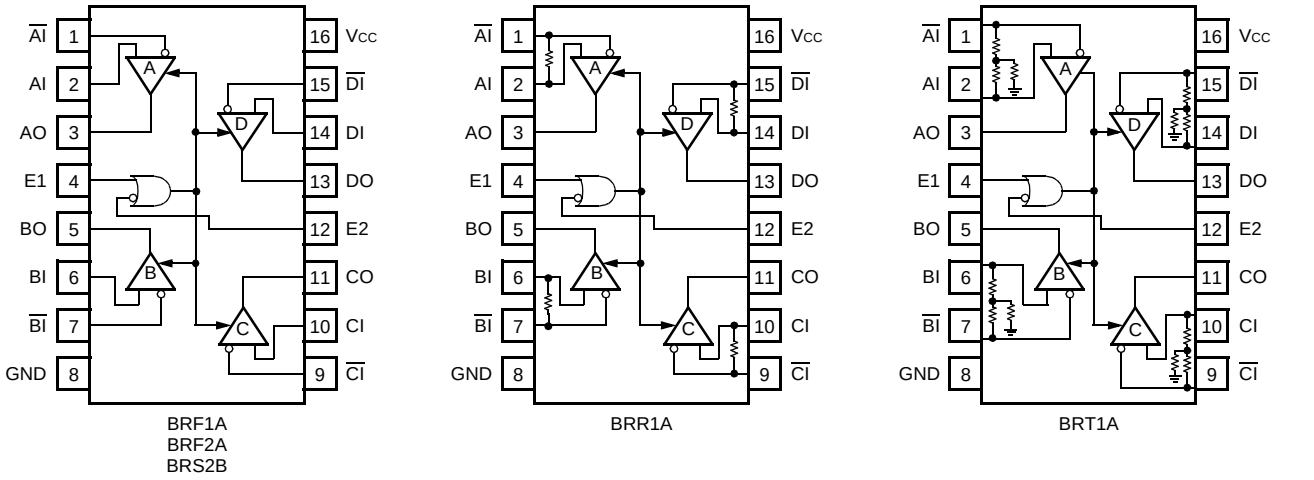
The BRR1A is equivalent to the BRF1A, but has a 110 Ω resistor connected across the differential inputs. This eliminates the need for an external resistor when terminating a 100 Ω impedance line. This device is designed to work with the DP1A or PNPA in point-to-point applications.

The BRT1A is equivalent to the BRF1A; however, it is provided with a Y-type resistor network across the differential inputs and terminated to ground. The Y-type termination provides the best EMI results. This device is not recommended for applications where the differences in ground voltage between the driver and the receiver exceed 1 V. This device is designed to work with the DG1A or PNGA in point-to-point applications.

The powerdown loading characteristics of the receiver input circuit are approximately 8 kΩ relative to the power supplies; hence, they will not load the transmission line when the circuit is powered down. For those circuits with termination resistors, the line will remain impedance matched when the circuit is powered down.

The packaging options that are available for these quad differential line drivers include a 16-pin DIP; a 16-pin, J-lead SOJ; a 16-pin, gull-wing small-outline integrated circuit (SOIC); and a 16-pin, narrow-body, gull-wing SOIC.

Pin Information



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Figure 1. Quad Differential Receiver Logic Diagrams

Table 1. Enable Truth Table

E1	E2	Condition
0	0	Active
1	0	Active
0	1	Disabled
1	1	Active

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Max	Unit
Power Supply Voltage	V_{CC}	—	6.5	V
Ambient Operating Temperature	T_A	–40	125	°C
Storage Temperature	T_{stg}	–40	150	°C

Electrical Characteristics

For electrical characteristics over the temperature range, see Figure 7 through Figure 10.

Table 2. Power Supply Current Characteristics

See Figure 7 for variation in I_{CC} over the temperature range. T_A = –40 °C to +125 °C, V_{CC} = 5 V ± 0.5 V.

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Current (V_{CC} = 5.5 V):					
All Outputs Disabled	I_{CC}	—	30	45	mA
All Outputs Enabled	I_{CC}	—	20	32	mA

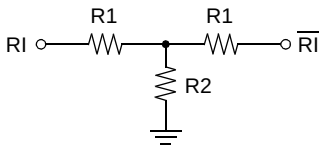
Electrical Characteristics (continued)

Table 3. Voltage and Current Characteristics

For variation in minimum V_{OH} and maximum V_{OL} over the temperature range, see Figure 8. T_A = –40 °C to +125 °C.

Parameter	Sym	Min	Typ	Max	Unit
Output Voltages, V_{CC} = 4.5 V:					
Low, I_{OL} = 8.0 mA	V_{OL}	—	—	0.5	V
High, I_{OH} = –400 µA	V_{OH}	2.4	—	—	V
Enable Input Voltages:					
Low, V_{CC} = 5.5 V	V_{IL}[1]	—	—	0.7	V
High, V_{CC} = 5.5 V	V_{IH}[1]	2.0	—	—	V
Clamp, V_{CC} = 4.5 V, I_I = –5.0 mA	V_{IK}	—	—	–1.0	V
Differential Input Voltages, $V_{IH} - V_{IL}$:[2]					
–0.80 V < V_{IH} < 7.2 V, –1.2 V < V_{IL} < 6.8 V	V_{TH}[1]	—	0.1	0.20	V
Input Offset Voltage	V_{OFF}	—	0.02	0.05	V
Input Offset Voltage BRS2B	V_{OFF}	—	0.1	0.15	V
Output Currents, V_{CC} = 5.5 V:					
Off-state (high Z), V_O = 0.4 V	I_{OZL}	—	—	–20	µA
Off-state (high Z), V_O = 2.4 V	I_{OZH}	—	—	20	µA
Short Circuit	I_{OS}[3]	–25	—	–100	mA
Enable Currents, V_{CC} = 5.5 V:					
Low, V_{IN} = 0.4 V	I_{IL}	—	—	–400	µA
High, V_{IN} = 2.7 V	I_{IH}	—	—	20	µA
Reverse, V_{IN} = 5.5 V	I_{IH}	—	—	100	µA
Differential Input Currents, V_{CC} = 5.5 V:					
Low, V_{IN} = –1.2 V	I_{IL}	—	—	–1.0	mA
High, V_{IN} = 7.2 V	I_{IH}	—	—	1.0	mA
Differential Input Impedance (BRR1A):					
Connected Between RI and $\overline{RI}$	R_O	—	110	—	Ω
Differential Input Impedance (BRT1A)[4]	R_1	—	60	—	Ω
	R_2	—	90	—	Ω

1. The input levels and difference voltage provide zero noise immunity and should be tested only in a static, noise-free environment.
2. Outputs of unused receivers assume a logic 1 level when the inputs are left open. (It is recommended that all unused positive inputs be tied to the positive power supply. No external series resistor is required.)
3. Test must be performed one lead at a time to prevent damage to the device.
4. See Figure 2.



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Figure 2. BRT1A Terminating Resistor Configuration

Timing Characteristics

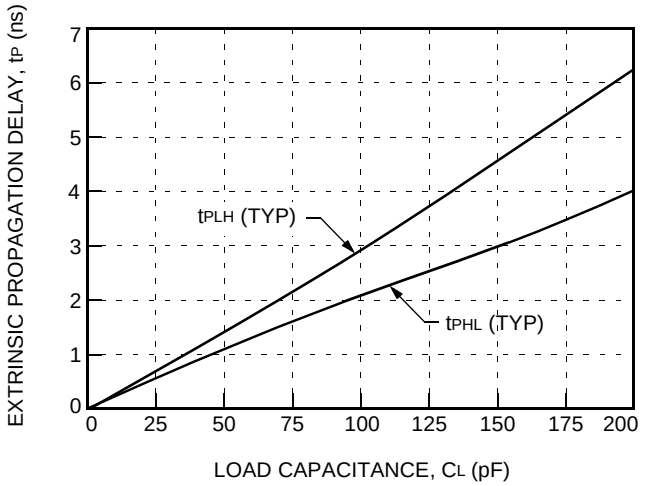
Table 4. Timing Characteristics (See Figure 4 and Figure 5.)

For propagation delays (t_{PLH} and t_{PHL}) over the temperature range, see Figure 9 and Figure 10.

Propagation delay test circuit connected to output is shown in Figure 6.

T_A = –40 °C to +125 °C, V_{CC} = 5 V ± 0.5 V.

Parameter	Symbol	Min	Typ	Max	Unit
Propagation Delay:					
Input to Output High	t_{PLH}	1.5	2.5	4.0	ns
Input to Output Low	t_{PHL}	1.5	2.5	4.0	ns
Disable Time, C_L = 5 pF:					
High-to-high Impedance	t_{PHZ}	—	5	12	ns
Low-to-high Impedance	t_{PLZ}	—	5	12	ns
Pulse Width Distortion, ltpHL – tpLHl:					
Load Capacitance (C_L) = 15 pF	tskew1	—	—	0.7	ns
Load Capacitance (C_L) = 150 pF	tskew1	—	—	4.0	ns
Output Waveform Skews:					
Part-to-Part Skew, T_A = 75 °C	Δtskew1p-p	—	0.8	1.4	ns
Part-to-Part Skew, T_A = –40 °C to +125 °C	Δtskew1p-p	—	—	1.5	ns
Same Part Skew	Δtskew	—	—	0.3	ns
Enable Time:					
High Impedance to High	t_{PZH}	—	8	12	ns
High Impedance to Low	t_{PZL}	—	8	12	ns
Rise Time (20%—80%)	t_{tLH}	—	—	3.0	ns
Fall Time (80%—20%)	t_{tHL}	—	—	3.0	ns



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Note: This graph is included as an aid to the system designers. Total circuit delay varies with load capacitance. The total delay is the sum of the delay due to the external capacitance and the intrinsic delay of the device.

Figure 3. Typical Extrinsic Propagation Delay vs. Load Capacitance at 25 °C

Timing Characteristics (continued)

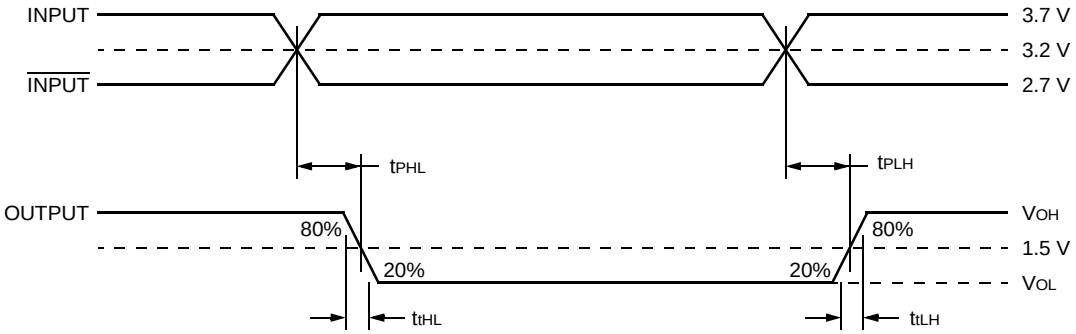
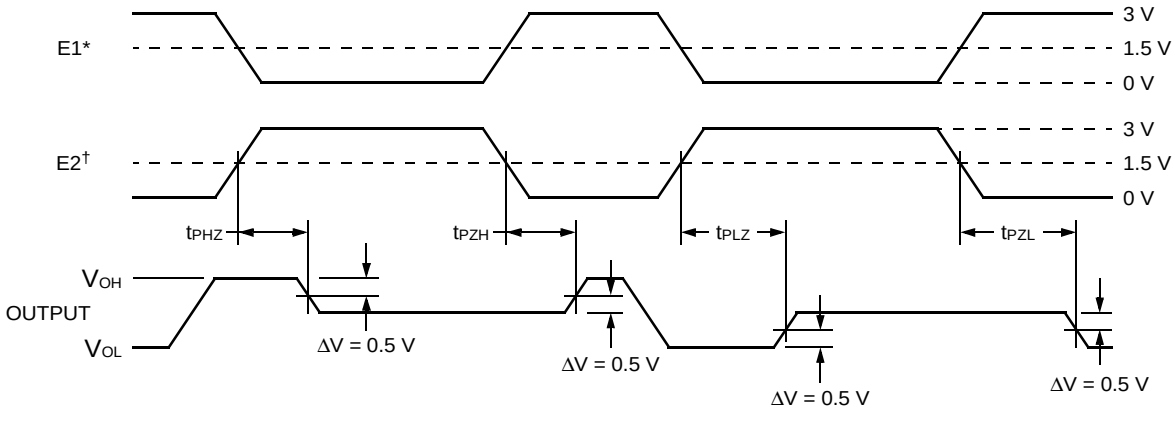


Figure 4. Receiver Propagation Delay Timing

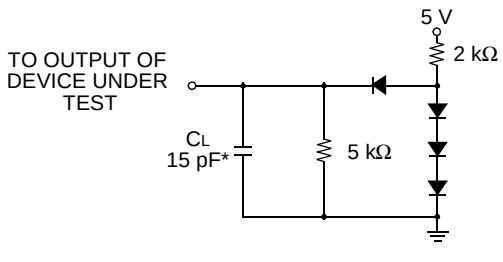


* E2 = 1 while E1 changes state.
† E1 = 0 while E2 changes state.

Figure 5. Receiver Enable and Disable Timing

Test Conditions

Parametric values specified under the Electrical Characteristics and Timing Characteristics sections for the data transmission driver devices are measured with the following output load circuits.



* Includes probe and jig capacitances.

Note: All 458E, IN4148, or equivalent diodes.

Figure 6. Receiver Propagation Delay Test Circuit

Temperature Characteristics

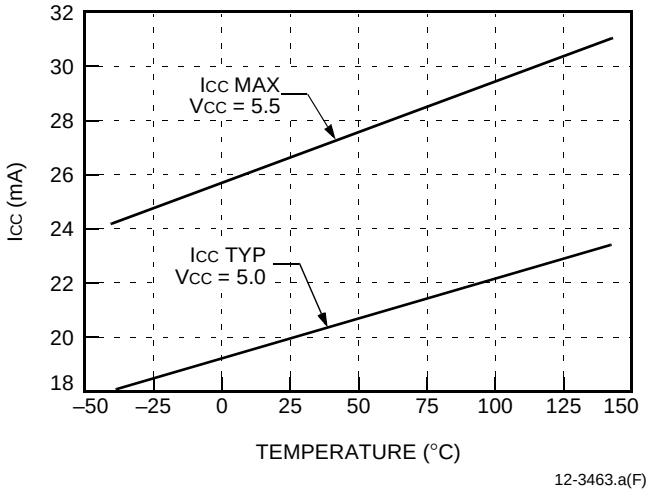


Figure 7. Typical and Maximum I_{CC} vs. Temperature

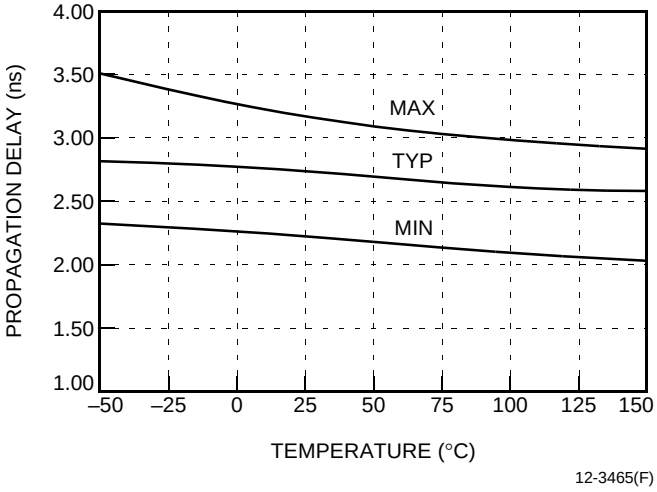


Figure 9. Propagation Delay for a High Output (t_{PLH}) vs. Temperature at V_{CC} = 5.0 V

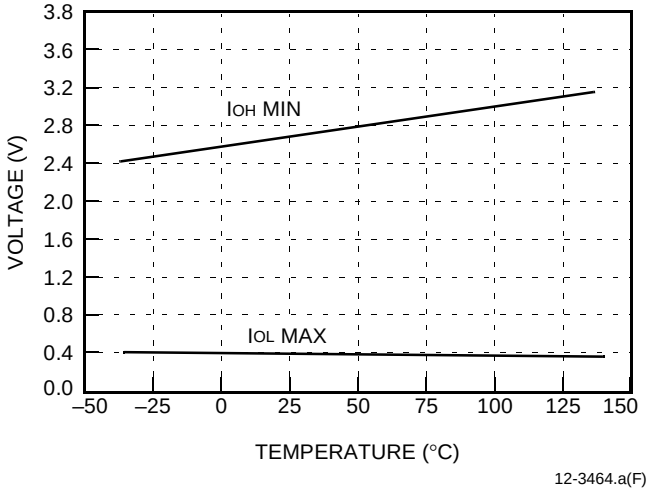


Figure 8. Minimum V_{OH} and Maximum V_{OL} vs. Temperature at V_{CC} = 4.5 V

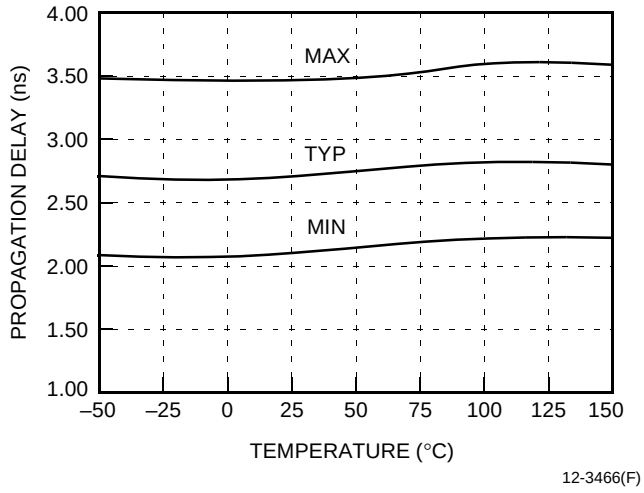


Figure 10. Propagation Delay for a Low Output (t_{PHL}) vs. Temperature at V_{CC} = 5.0 V

Handling Precautions

CAUTION: This device is susceptible to damage as a result of ESD. Take proper precautions during both handling and testing. Follow guidelines such as JEDEC Publication No. 108-A (Dec. 1988).

When handling and mounting line driver products, proper precautions should be taken to avoid exposure to ESD. The user should adhere to the following basic rules for ESD control:

1. Assume that all electronic components are sensitive to ESD damage.
2. Never touch a sensitive component unless properly grounded.
3. Never transport, store, or handle sensitive components except in a static-safe environment.

ESD Failure Models

Agere employs two models for ESD events that can cause device damage or failure:

1. An HBM that is used by most of the industry for ESD-susceptibility testing and protection-design evaluation. ESD voltage thresholds are dependent on the critical parameters used to define the model. A standard HBM (resistance = 1500 Ω, capacitance = 100 pF) is widely used and, therefore, can be used for comparison purposes.
2. A charged-device model (CDM), which many believe is the better simulator of electronics manufacturing exposure.

Table 5 and Table 6 illustrates the role these two models play in the overall prevention of ESD damage. HBM ESD testing is intended to simulate an ESD event from a charged person. The CDM ESD testing simulates charging and discharging events that occur in production equipment and processes, e.g., an integrated circuit sliding down a shipping tube.

The HBM ESD threshold voltage presented here was obtained by using the following circuit parameters:

Table 5. Typical ESD Thresholds for Data Transmission Receivers

Device	HBM Threshold		CDM Threshold
	Differential Inputs	Others	
BRF1A, BRR1A, BRT1A	>800	>2000	>1000
BRF2A, BRS2B	>2000	>2000	>2000

Table 6. ESD Damage Protection

	ESD Threat Controls	
	Personnel	Processes
Control	Wrist straps. ESD shoes. Antistatic flooring.	Static-dissipative materials. Air ionization.
Model	Human body model (HBM).	Charged-device model (CDM).

Latch Up

Latch-up evaluation has been performed on the data transmission receivers. Latch-up testing determines if power-supply current exceeds the specified maximum due to the application of a stress to the device under test. A device is considered susceptible to latch up if the power supply current exceeds the maximum level and remains at that level after the stress is removed.

Agere performs latch up testing per an internal test method that is consistent with JEDEC Standard No. 17 (previously JC-40.2) *CMOS Latch Up Standardized Test Procedure*.

Latch up evaluation involves three separate stresses to evaluate latch up susceptibility levels:

1. dc current stressing of input and output pins.
2. Power supply slew rate.
3. Power supply overvoltage.

Table 7. Latch Up Test Criteria and Test Results

		dc Current Stress of I/O Pins	Power Supply Slew Rate	Power Supply Overvoltage
Data Transmission Receiver ICs	**Minimum Criteria**	≥150 mA	≤1 µs	≥1.75 x Vmax
	Test Results	≥250 mA	≤100 ns	≥2.25 x Vmax

Based on the results in Table 7, the data transmission receivers pass the Agere latch-up esting requirements and are considered not susceptible to latch up.

Power Dissipation

System designers incorporating Agere data transmission drivers in their applications should be aware of package and thermal information associated with these components.

Proper thermal management is essential to the long-term reliability of any plastic encapsulated integrated circuit. Thermal management is especially important for surface-mount devices, given the increasing circuit pack density and resulting higher thermal density. A key aspect of thermal management involves the junction temperature (silicon temperature) of the integrated circuit.

Several factors contribute to the resulting junction temperature of an integrated circuit:

- Ambient use temperature
- Device power dissipation
- Component placement on the board
- Thermal properties of the board
- Thermal impedance of the package

Thermal impedance of the package is referred to as Θ_{ja} and is measured in °C rise in junction temperature per watt of power dissipation. Thermal impedance is also a function of airflow present in system application.

The following equation can be used to estimate the junction temperature of any device:

$T_j = T_A + P_D \Theta_{ja}$

where:

T_j is device junction temperature (°C).

T_A is ambient temperature (°C).

P_D is power dissipation (W).

Θ_{ja} is package thermal impedance (junction to ambient—°C/W).

The power dissipation estimate is derived from two factors:

- Internal device power
- Power associated with output terminations

Multiplying I_{CC} times V_{CC} provides an estimate of internal power dissipation.

The power dissipated in the output is a function of the:

- Termination scheme on the outputs
- Termination resistors
- Duty cycle of the output

Package thermal impedance depends on:

- Airflow
- Package type (e.g., DIP, SOIC, SOIC/NB)

The junction temperature can be calculated using the previous equation, after power dissipation levels and package thermal impedances are known.

Figure 11 illustrates the thermal impedance estimates for the various package types as a function of airflow. This figure shows that package thermal impedance is higher for the narrow-body SOIC package. Particular attention should, therefore, be paid to the thermal management issues when using this package type.

In general, system designers should attempt to maintain junction temperature below 125 °C. The following factors should be used to determine if specific data transmission drivers in particular package types meet the system reliability objectives:

- System ambient temperature
- Power dissipation
- Package type
- Airflow

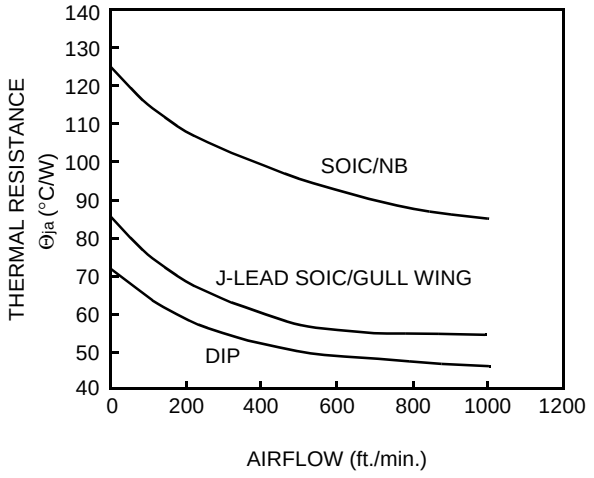
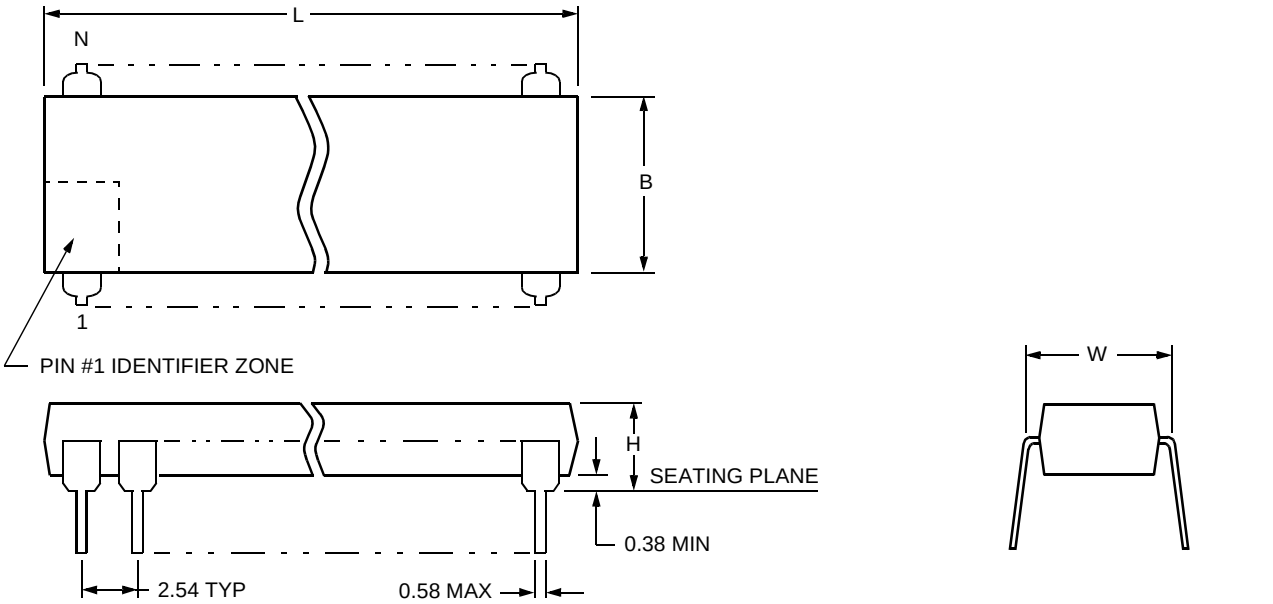


Figure 11. Power Dissipation

Outline Diagrams

16-Pin DIP

Dimensions are in millimeters.



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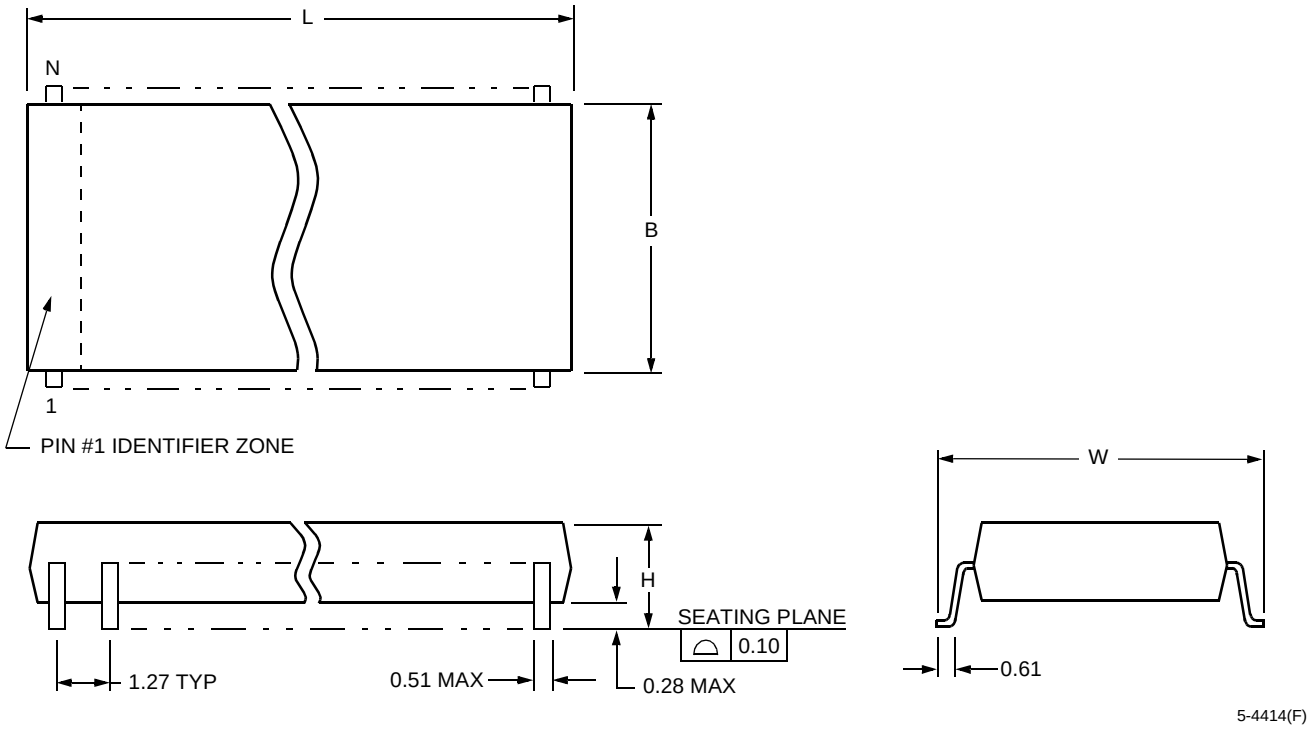
Package Description	Number of Pins (N)	Package Dimensions			
		Maximum Length (L)	Maximum Width Without Leads (B)	Maximum Width Including Leads (W)	Maximum Height Above Board (H)
Plastic Dual In-Line Package (PDIP3)	16	20.57	6.48	7.87	5.08

Note: The dimensions in this outline diagram are intended for informational purposes only. For detailed schematics to assist your design efforts, please contact your Agere Systems sales representative.

Outline Diagrams (continued)

16-Pin SOIC (SONB/SOG)

Dimensions are in millimeters.



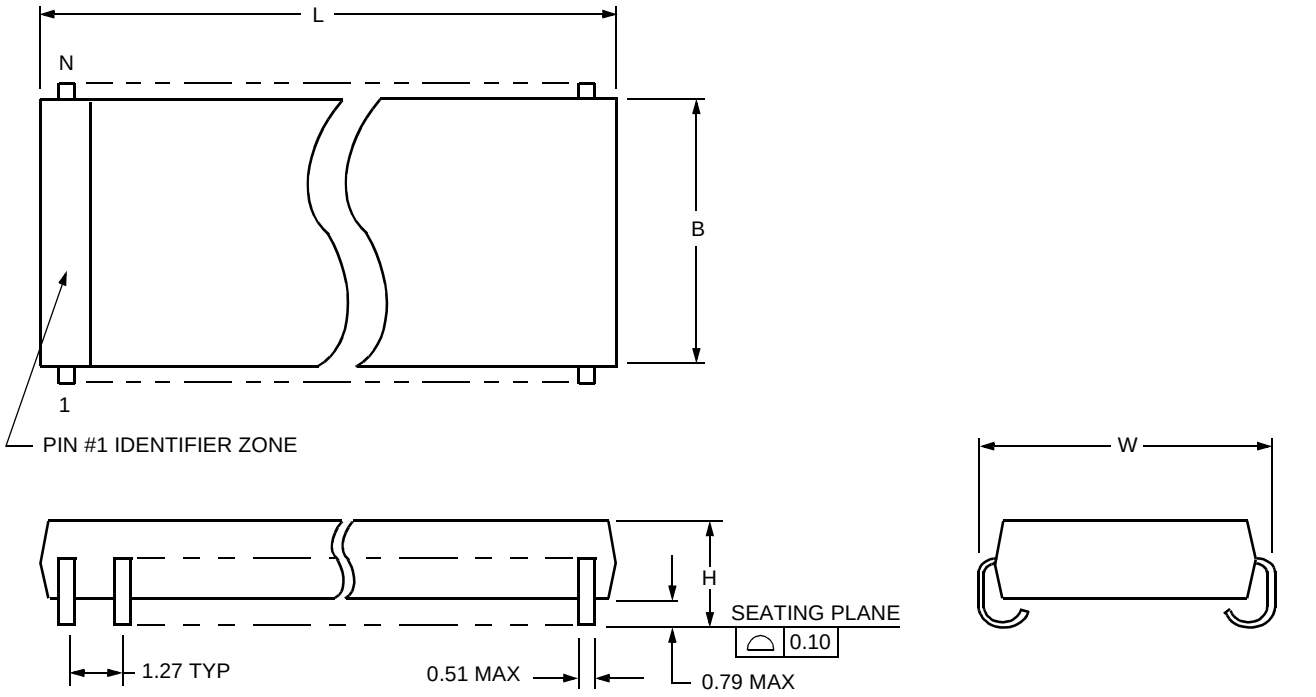
Package Description	Number of Pins (N)	Package Dimensions			
		Maximum Length (L)	Maximum Width Without Leads (B)	Maximum Width Including Leads (W)	Maximum Height Above Board (H)
Small-Outline, Narrow Body (SONB)	16	10.11	4.01	6.17	1.73
Small-Outline, Gull-Wing (SOG)	16	10.49	7.62	10.64	2.67

Note: The dimensions in this outline diagram are intended for informational purposes only. For detailed schematics to assist your design efforts, please contact your Agere Systems sales representative.

Outline Diagrams (continued)

16-Pin SOIC (SOJ)

Dimensions are in millimeters.



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Package Description	Number of Pins (N)	Package Dimensions			
		Maximum Length (L)	Maximum Width Without Leads (B)	Maximum Width Including Leads (W)	Maximum Height Above Board (H)
Small-Outline, J-Lead (SOJ)	16	10.41	7.62	8.81	3.18

Note: The dimensions in this outline diagram are intended for informational purposes only. For detailed schematics to assist your design efforts, please contact your Agere Systems sales representative.

Ordering Information

Part Number	Package Type	Comcode	Former Pkg. Type	Former Part Number
BRF1A16E	16-pin, Plastic SOJ	107949927	1041	LF, MF, LS
BRF1A16E-TR	Tape & Reel SOJ	107949935	1041	LF, MF, LS
BRF1A16G	16-pin, Plastic SOIC	107950297	1141	LF, MF, LS
BRF1A16G-TR	Tape & Reel SOIC	107950305	1141	LF, MF, LS
BRF1A16NB	16-pin, Plastic SOIC/NB	107949968	1241	LF, MF, LS
BRF1A16NB-TR	Tape & Reel SOIC/NB	107949976	1241	LF, MF, LS
BRF1A16P	16-pin, Plastic DIP	107949984	41	LF, MF, LS
BRF2A16E	16-pin, Plastic SOJ	107949992	1041	LF2, MF2
BRF2A16E-TR	Tape & Reel SOJ	107950008	1041	LF2, MF2
BRF2A16G	16-pin, Plastic SOIC	107950016	1141	LF2, MF2
BRF2A16G-TR	Tape & Reel SOIC	107950024	1141	LF2, MF2
BRF2A16NB	16-pin, Plastic SOIC/NB	107950032	1241	LF2, MF2
BRF2A16NB-TR	Tape & Reel SOIC/NB	107950040	1241	LF2, MF2
BRF2A16P	16-pin, Plastic DIP	107950057	41	LF2, MF2
BRR1A16E	16-pin, Plastic SOJ	107950065	1041	LR, MR
BRR1A16E-TR	Tape & Reel SOJ	107950073	1041	LR, MR
BRR1A16G	16-pin, Plastic SOIC	107950081	1141	LR, MR
BRR1A16G-TR	Tape & Reel SOIC	107950099	1141	LR, MR
BRR1A16NB	16-pin, Plastic SOIC/NB	107950107	1241	LR, MR
BRR1A16NB-TR	Tape & Reel SOIC/NB	107950115	1241	LR, MR
BRR1A16P	16-pin, Plastic DIP	107950123	41	LR, MR
BRS2B16E	16-pin, Plastic SOJ	108888470	1041	MF, MF2, LS
BRS2B16E-TR	Tape & Reel SOJ	108888488	1041	MF, MF2, LS
BRS2B16G	16-pin, Plastic SOIC	108699133	1141	MF, MF2, LS
BRS2B16G-TR	Tape & Reel SOIC	108699125	1141	MF, MF2, LS
BRS2B16P	16-pin, Plastic DIP	108888447	41	MF, MF2, LS
BRS2B16NB	16-pin, Plastic SOIC/NB	108888454	1241	MF, MF2, LS
BRS2B16NB-TR	Tape & Reel SOIC/NB	108888462	1241	MF, MF2, LS
BRT1A16E	16-pin, Plastic SOJ	107950131	1041	LT, MT
BRT1A16E-TR	Tape & Reel SOJ	107950149	1041	LT, MT
BRT1A16G	16-pin, Plastic SOIC	107950156	1141	LT, MT
BRT1A16G-TR	Tape & Reel SOIC	107950164	1141	LT, MT
BRT1A16NB	16-pin, Plastic SOIC/NB	107950313	1241	LT, MT
BRT1A16NB-TR	Tape & Reel SOIC/NB	107950321	1241	LT, MT
BRT1A16P	16-pin, Plastic DIP	107950339	41	LT, MT

For additional information, contact your Agere Systems Account Manager or the following:
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