16-Bit, 570 kSPS PulSAR® Unipolar CMOS ADC

AD7664

FEATURES

Throughput:
- 570 kSPS (Warp Mode)
- 500 kSPS (Normal Mode)
- 444 kSPS (Impulse Mode)

INL: ±2.5 LSB Max (±0.0038% of Full Scale)
16-Bit Resolution with No Missing Codes
S/(N+D): 90 dB Typ @ 45 kHz
THD: –100 dB Typ @ 45 kHz
Analog Input Voltage Range: 0 V to 2.5 V
Both AC and DC Specifications
No Pipeline Delay
Parallel and Serial 5 V/3 V Interface
SPI®/QSPI™/MICROWIRE™/DSP Compatible
Single 5 V Supply Operation
Power Dissipation
- 115 mW Maximum,
- 21 µW @ 100 SPS

Power-Down Mode: 7 µW Max
Package: 48-Lead Quad Flat Pack (LQFP)
- 48-Lead Chip Scale Package (LFCSP)

Pin-to-Pin Compatible Upgrade of the AD7660

APPLICATIONS

Data Acquisition
Instrumentation
Digital Signal Processing
Spectrum Analysis
Medical Instruments
Battery-Powered Systems
Process Control

GENERAL DESCRIPTION

The AD7664 is a 16-bit, 570 kSPS, charge redistribution SAR, analog-to-digital converter that operates from a single 5 V power supply. The part contains a high speed 16-bit sampling ADC, an internal conversion clock, error correction circuits, and both serial and parallel system interface ports.

The AD7664 is hardware factory-calibrated and is comprehensively tested to ensure such ac parameters as signal-to-noise ratio (SNR) and total harmonic distortion (THD), in addition to the more traditional dc parameters of gain, offset, and linearity.

It features a very high sampling rate mode (Warp), a fast mode (Normal) for asynchronous conversion rate applications, and for low power applications, a reduced power mode (Impulse) where the power is scaled with the throughput.

FUNCTIONAL BLOCK DIAGRAM

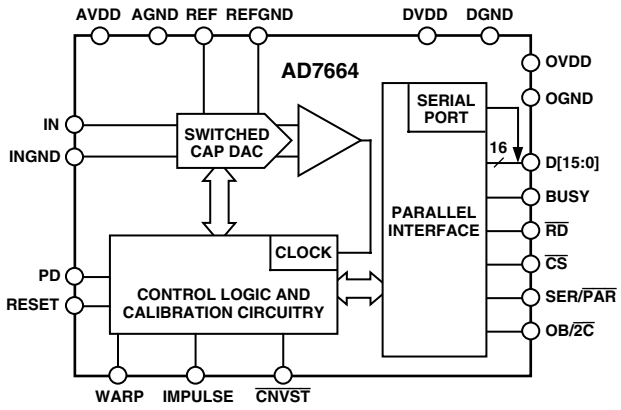


Table I. PulSAR Selection

Type/kSPS	100–250	500–570	800–1000
Pseudo Differential	AD7651 AD7660/AD7661	AD7650/AD7652 AD7664/AD7666	AD7653 AD7667
True Bipolar	AD7663	AD7665	AD7671
True Differential	AD7675	AD7676	AD7677
18-Bit	AD7678	AD7679	AD7674
Simultaneous/ Multichannel		AD7654 AD7655	

It is fabricated using Analog Devices' high performance, 0.6 micron CMOS process, with correspondingly low cost and is available in a 48-lead LQFP and a tiny 48-lead LFCSP with operation specified from –40°C to +85°C.

PRODUCT HIGHLIGHTS

1. Fast Throughput
   The AD7664 is a 570 kSPS, charge redistribution, 16-bit SAR ADC with internal error correction circuitry.
2. Superior INL
   The AD7664 has a maximum integral nonlinearity of 2.5 LSBs with no missing 16-bit code.
3. Single-Supply Operation
   The AD7664 operates from a single 5 V supply and dissipates only a maximum of 115 mW. In Impulse Mode, its power dissipation decreases with the throughput to, for instance, only 21 µW at a 100 SPS throughput. It consumes 7 µW maximum when in power-down.
4. Serial or Parallel Interface
   Versatile parallel or 2-wire serial interface arrangement compatible with both 3 V or 5 V logic.

REV. F

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Tel:781/329-4700 **www.analog.com**
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COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD7664 Evaluation Kit

DOCUMENTATION

Application Notes

- AN-931: Understanding PulSAR ADC Support Circuitry
- AN-932: Power Supply Sequencing

Data Sheet

- AD7664: 16-Bit, 570 kSPS PulSAR® Unipolar CMOS ADC Data Sheet

Product Highlight

- 8- to 18-Bit SAR ADCs ... From the Leader in High Performance Analog

TOOLS AND SIMULATIONS

- AD7664 IBIS Model

REFERENCE MATERIALS

Technical Articles

- MS-2210: Designing Power Supplies for High Speed ADC

DESIGN RESOURCES

- AD7664 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD7664 EngineerZone Discussions.

SAMPLE AND BUY

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AD7664—SPECIFICATIONS (–40°C to +85°C, AVDD = DVDD = 5 V, OVDD = 2.7 V to 5.25 V, unless otherwise noted.)

Parameter	Conditions	Min	Typ	Max	Unit
RESOLUTION		16			Bits
ANALOG INPUT					
Voltage Range	$V_{IN} - V_{INGND}$	0		V_{REF}	V
Operating Input Voltage	V_{IN}	–0.1		+3	V
	V_{INGND}	–0.1		+0.5	V
Analog Input CMRR	f_{IN} = 10 kHz		62		dB
Input Current	570 kSPS Throughput		7		µA
Input Impedance		See Analog Input Section			
THROUGHPUT SPEED					
Complete Cycle	In Warp Mode			1.75	µs
Throughput Rate	In Warp Mode	1		570	kSPS
Time between Conversions	In Warp Mode			1	ms
Complete Cycle	In Normal Mode			2	µs
Throughput Rate	In Normal Mode	0		500	kSPS
Complete Cycle	In Impulse Mode			2.25	µs
Throughput Rate	In Impulse Mode	0		444	kSPS
DC ACCURACY					
Integral Linearity Error		–2.5		+2.5	LSB[1]
Differential Linearity Error		–1		+1.5	LSB
No Missing Codes		16			Bits
Transition Noise			0.7		LSB
Full-Scale Error[2]	REF = 2.5 V			±0.08	% of FSR
Unipolar Zero Error[2]			±5	±15	LSB
Power Supply Sensitivity	AVDD = 5 V ±5%		±3		LSB
AC ACCURACY					
Signal-to-Noise	f_{IN} = 100 kHz		90		dB[3]
Spurious-Free Dynamic Range	f_{IN} = 45 kHz		100		dB
	f_{IN} = 100 kHz		100		dB
Total Harmonic Distortion	f_{IN} = 45 kHz		–100		dB
	f_{IN} = 100 kHz		–100		dB
Signal-to-(Noise+Distortion)	f_{IN} = 45 kHz		90		dB
	f_{IN} = 100 kHz		89		dB
	–60 dB Input, f_{IN} = 100 kHz		30		dB
–3 dB Input Bandwidth			18		MHz
SAMPLING DYNAMICS					
Aperture Delay			2		ns
Aperture Jitter			5		ps rms
Transient Response	Full-Scale Step			250	ns
REFERENCE					
External Reference Voltage Range		2.3	2.5	AVDD – 1.85	V
External Reference Current Drain	570 kSPS Throughput		115		µA
DIGITAL INPUTS					
Logic Levels					
V_{IL}		–0.3		+0.8	V
V_{IH}		2.0		OVDD + 0.3	V
I_{IL}		–1		+1	µA
I_{IH}		–1		+1	µA
DIGITAL OUTPUTS					
Data Format			Parallel or Serial 16-Bits		
Pipeline Delay			Conversion Results Available Immediately after Completed Conversion		
V_{OL}	I_{SINK} = 1.6 mA			0.4	V
V_{OH}	I_{SOURCE} = –500 µA	OVDD – 0.6			V
POWER SUPPLIES					
Specified Performance					
AVDD		4.75	5	5.25	V
DVDD		4.75	5	5.25	V
OVDD		2.7		5.25	V
Operating Current[4]	500 kSPS Throughput				
AVDD			15.5		mA
DVDD[5]			3.8		mA
OVDD[5]			100		µA
Power Dissipation[5]	500 kSPS Throughput[4]			115	mW
	100 SPS Throughput[6]		21		µW
	In Power-Down Mode[7]			7	µW

Parameter	Conditions	Min	Typ	Max	Unit
TEMPERATURE RANGE[8]					
Specified Performance	T_{MIN} to T_{MAX}	–40		+85	°C

NOTES
[1]LSB means least significant bit. With the 0 V to 2.5 V input range, one LSB is 38.15 µV.
[2]See Definition of Specifications section. These specifications do not include the error contribution from the external reference.
[3]All specifications in dB are referred to a full-scale input FS. Tested with an input signal at 0.5 dB below full-scale unless otherwise specified.
[4]In Normal Mode.
[5]Tested in Parallel Reading Mode.
[6]In Impulse Mode.
[7]With all digital inputs forced to OVDD or OGND, respectively.
[8]Contact factory for extended temperature range.

Specifications subject to change without notice.

TIMING SPECIFICATIONS (–40°C to +85°C, AVDD = DVDD = 5 V, OVDD = 2.7 V to 5.25 V, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
REFER TO FIGURES 11 AND 12					
Convert Pulse Width	t_1	5			ns
Time between Conversions	t_2	1.75/2/2.25		Note 1	µs
(Warp Mode/Normal Mode/Impulse Mode)					
$\overline{CNVST}$ LOW to BUSY HIGH Delay	t_3			25	ns
BUSY HIGH All Modes Except in	t_4			1.5/1.75/2	µs
Master Serial Read after Convert Mode					
(Warp Mode/Normal Mode/Impulse Mode)					
Aperture Delay	t_5		2		ns
End of Conversion to BUSY LOW Delay	t_6	10			ns
Conversion Time	t_7			1.5/1.75/2	µs
(Warp Mode/Normal Mode/Impulse Mode)					
Acquisition Time	t_8	250			ns
RESET Pulsewidth	t_9	10			ns
REFER TO FIGURES 13, 14, AND 15 (Parallel Interface Modes)					
$\overline{CNVST}$ LOW to DATA Valid Delay	t_{10}			1.5/1.75/2	µs
(Warp Mode/Normal Mode/Impulse Mode)					
DATA Valid to BUSY LOW Delay	t_{11}	45			ns
Bus Access Request to DATA Valid	t_{12}			40	ns
Bus Relinquish Time	t_{13}	5		15	ns
REFER TO FIGURES 16 AND 17 (Master Serial Interface Modes)[2]					
$\overline{CS}$ LOW to SYNC Valid Delay	t_{14}			10	ns
$\overline{CS}$ LOW to Internal SCLK Valid Delay[2]	t_{15}			10	ns
$\overline{CS}$ LOW to SDOUT Delay	t_{16}			10	ns
$\overline{CNVST}$ LOW to SYNC Delay	t_{17}		25/275/525		ns
(Warp Mode/Normal Mode/Impulse Mode)					
SYNC Asserted to SCLK First Edge Delay	t_{18}	4			ns
Internal SCLK Period	t_{19}	40		75	ns
Internal SCLK HIGH (INVSCLK Low)[3]	t_{20}	30			ns
Internal SCLK LOW (INVSCLK Low)[3]	t_{21}	9.5			ns
SDOUT Valid Setup Time	t_{22}	4.5			ns
SDOUT Valid Hold Time	t_{23}	3			ns
SCLK Last Edge to SYNC Delay	t_{24}	3			
$\overline{CS}$ HIGH to SYNC HI-Z	t_{25}			10	ns
$\overline{CS}$ HIGH to Internal SCLK HI-Z	t_{26}			10	ns
$\overline{CS}$ HIGH to SDOUT HI-Z	t_{27}			10	ns
BUSY HIGH in Master Serial Read after Convert	t_{28}			2.75/3/3.25	µs
(Warp Mode/Normal Mode/Impulse Mode)					
$\overline{CNVST}$ LOW to SYNC Asserted Delay	t_{29}		1/1.25/1.5		µs
(Warp Mode/Normal Mode/Impulse Mode)					
SYNC Deasserted to BUSY LOW Delay	t_{30}		50		ns
REFER TO FIGURES 18 AND 20 (Slave Serial Interface Modes)[2]					
External SCLK Setup Time	t_{31}	5			ns
External SCLK Active Edge to SDOUT Delay	t_{32}	3		16	ns
SDIN Setup Time	t_{33}	5			ns
SDIN Hold Time	t_{34}	5			ns
External SCLK Period	t_{35}	25			ns
External SCLK HIGH	t_{36}	10			ns
External SCLK LOW	t_{37}	10			ns

NOTES
[1]In Warp Mode only, the maximum time between conversions is 1 ms; otherwise, there is no required maximum time.
[2]In Serial Interface Modes, the SYNC, SCLK, and SDOUT timings are defined with a maximum load C_L of 10 pF; otherwise, the load is 60 pF maximum.
[3]If the polarity of SCLK is inverted, the timing references of SCLK are also inverted.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

IN[2], REF, INGND, REFGND to AGND
. . . . . AVDD + 0.3 V to AGND – 0.3 V
Ground Voltage Differences
AGND, DGND, OGND . . . . . ±0.3 V
Supply Voltages
AVDD, DVDD, OVDD . . . . . –0.3 V to +7 V
AVDD to DVDD, AVDD to OVDD . . . . . ±7 V
DVDD to OVDD . . . . . ±7 V
Digital Inputs
Except the Databus D(7:4) . . . . . –0.3 V to DVDD + 3.0 V
Databus D(7:4) . . . . . –0.3 V to OVDD + 3.0 V
Internal Power Dissipation[3] . . . . . 700 mW
Internal Power Dissipation[4] . . . . . 2.5 W
Junction Temperature . . . . . 150°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature Range
(Soldering 10 sec) . . . . . 300°C

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]See Analog Input section.
[3]Specification is for the device in free air:
48-Lead LQFP; θ_{JA} = 91°C/W, θ_{JC} = 30°C/W.
[4]Specification is for device in free air:
48-Lead LFCSP; θ_{JA} = 26°C/W.

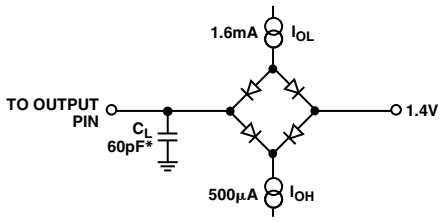


Figure 1. Load Circuit for Digital Interface Timing, SDOUT, SYNC, SCLK Outputs, C_L = 10 pF

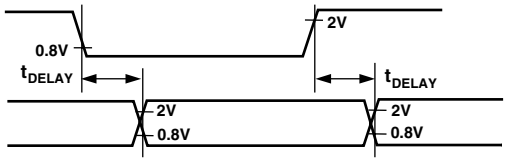


Figure 2. Voltage Reference Levels for Timing

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD7664ASTZ	–40°C to +85°C	48-Lead LQFP	ST-48
AD7664ASTZRL	–40°C to +85°C	48-Lead LQFP	ST-48
AD7664ACPZRL	–40°C to +85°C	48-Lead LFCSP	CP-48-4

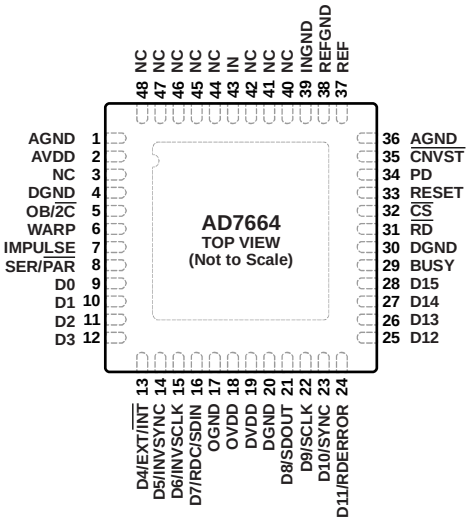
[1]Z = RoHS Compliant Part.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7664 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATION



NOTES
1. NC = NO CONNECT. DO NOT CONNECT TO THIS PIN.
2. THE EPAD IS CONNECTED TO GROUND; HOWEVER, THIS CONNECTION IS NOT REQUIRED TO MEET SPECIFIED PERFORMANCE.

PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Type	Description
1	AGND	P	Analog Power Ground Pin.
2	AVDD	P	Input Analog Power Pins. Nominally 5 V.
3, 40–42, 44–48	NC		No Connect.
4	DGND	DI	Must Be Tied to the Ground Where DVDD Is Referred.
5	OB/$\overline{2C}$	DI	Straight Binary/Binary Twos Complement. When OB/$\overline{2C}$ is HIGH, the digital output is straight binary; when LOW, the MSB is inverted resulting in a twos complement output from its internal shift register.
6	WARP	DI	Mode Selection. When HIGH and IMPULSE LOW, this input selects the fastest mode, the maximum throughput is achievable, and a minimum conversion rate must be applied in order to guarantee full specified accuracy. When LOW, full accuracy is maintained independent of the minimum conversion rate.
7	IMPULSE	DI	Mode Selection. When HIGH and WARP LOW, this input selects a reduced power mode. In this mode, the power dissipation is approximately proportional to the sampling rate.
8	SER/$\overline{PAR}$	DI	Serial/Parallel Selection Input. When LOW, the Parallel Port is selected; when HIGH, the Serial Interface Mode is selected and some bits of the DATA bus are used as a Serial Port.
9–12	D[0:3]	DO	Bit 0 to Bit 3 of the Parallel Port Data Output Bus. These pins are always outputs, regardless of the state of SER/$\overline{PAR}$.
13	D4 or EXT/$\overline{INT}$	DI/O	When SER/$\overline{PAR}$ is LOW, this output is used as Bit 4 of the Parallel Port Data Output Bus. When SER/$\overline{PAR}$ is HIGH, this input, part of the Serial Port, is used as a digital select input for choosing the internal or an external data clock. With EXT/$\overline{INT}$ tied LOW, the internal clock is selected on the SCLK output. With EXT/$\overline{INT}$ set to a logic HIGH, output data is synchronized to an external clock signal connected to the SCLK input.
14	D5 or INVSYNC	DI/O	When SER/$\overline{PAR}$ is LOW, this output is used as Bit 5 of the Parallel Port Data Output Bus. When SER/$\overline{PAR}$ is HIGH, this input, part of the Serial Port, is used to select the active state of the SYNC signal. It is active in both Master and Slave Mode. When LOW, SYNC is active HIGH. When HIGH, SYNC is active LOW.
15	D6 or INVSCLK	DI/O	When SER/$\overline{PAR}$ is LOW, this output is used as Bit 6 of the Parallel Port Data Output Bus. When SER/$\overline{PAR}$ is HIGH, this input, part of the Serial Port, is used to invert the SCLK signal. It is active in both Master and Slave Mode.

Pin No.	Mnemonic	Type	Description
16	D7 or RDC/SDIN	DI/O	When SER/$\overline{PAR}$ is LOW, this output is used as Bit 7 of the Parallel Port Data Output Bus. When SER/$\overline{PAR}$ is HIGH, this input, part of the Serial Port, is used as either an external data input or a Read Mode selection input depending on the state of EXT/$\overline{INT}$. When EXT/$\overline{INT}$ is HIGH, RDC/SDIN could be used as a data input to daisy-chain the conversion results from two or more ADCs onto a single SDOUT line. The digital data level on SDIN is output on DATA with a delay of 16 SCLK periods after the initiation of the read sequence. When EXT/$\overline{INT}$ is LOW, RDC/SDIN is used to select the Read Mode. When RDC/SDIN is HIGH, the data is output on SDOUT during conversion. When RDC/SDIN is LOW, the data can be output on SDOUT only when the conversion is complete.
17	OGND	P	Input/Output Interface Digital Power Ground.
18	OVDD	P	Input/Output Interface Digital Power. Nominally at the same supply as the supply of the host interface (5 V or 3 V).
19	DVDD	P	Digital Power. Nominally at 5 V.
20	DGND	P	Digital Power Ground.
21	D8 or SDOUT	DO	When SER/$\overline{PAR}$ is LOW, this output is used as Bit 8 of the Parallel Port Data Output Bus. When SER/$\overline{PAR}$ is HIGH, this output, part of the Serial Port, is used as a serial data output synchronized to SCLK. Conversion results are stored in an on-chip register. The AD7664 provides the conversion result, MSB first, from its internal shift register. The DATA format is determined by the logic level of OB/$\overline{2C}$. In Serial Mode, when EXT/$\overline{INT}$ is LOW, SDOUT is valid on both edges of SCLK. In Serial Mode, when EXT/$\overline{INT}$ is HIGH: If INVSCLK is LOW, SDOUT is updated on the SCLK rising edge and valid on the next falling edge. If INVSCLK is HIGH, SDOUT is updated on the SCLK falling edge and valid on the next rising edge.
22	D9 or SCLK	DI/O	When SER/$\overline{PAR}$ is LOW, this output is used as Bit 9 of the Parallel Port Data Output Bus. When SER/$\overline{PAR}$ is HIGH, this pin, part of the Serial Port, is used as a serial data clock input or output, dependent upon the logic state of the EXT/$\overline{INT}$ pin. The active edge where the data SDOUT is updated depends upon the logic state of the INVSCLK pin.
23	D10 or SYNC	DO	When SER/$\overline{PAR}$ is LOW, this output is used as the Bit 10 of the Parallel Port Data Output Bus. When SER/$\overline{PAR}$ is HIGH, this output, part of the Serial Port, is used as a digital output frame synchronization for use with the internal data clock (EXT/$\overline{INT}$ = Logic LOW). When a read sequence is initiated and INVSYNC is LOW, SYNC is driven HIGH and remains HIGH while the SDOUT output is valid. When a read sequence is initiated and INVSYNC is HIGH, SYNC is driven LOW and remains LOW while the SDOUT output is valid.
24	D11 or RDERROR	DO	When SER/$\overline{PAR}$ is LOW, this output is used as Bit 11 of the Parallel Port Data Output Bus. When SER/$\overline{PAR}$ is HIGH and EXT/$\overline{INT}$ is HIGH, this output, part of the Serial Port, is used as an incomplete read error flag. In Slave Mode, when a data read is started and not complete when the following conversion is complete, the current data is lost and RDERROR is pulsed HIGH.
25–28	D[12:15]	DO	Bit 12 to Bit 15 of the Parallel Port Data Output Bus. These pins are always outputs regardless of the state of SER/$\overline{PAR}$.
29	BUSY	DO	Busy Output. Transitions HIGH when a conversion is started and remains HIGH until the conversion is complete and the data is latched into the on-chip shift register. The falling edge of BUSY could be used as a data-ready clock signal.
30	DGND	P	Must Be Tied to Digital Ground.
31	$\overline{RD}$	DI	Read Data. When $\overline{CS}$ and $\overline{RD}$ are both LOW, the interface parallel or serial output bus is enabled.
32	$\overline{CS}$	DI	Chip Select. When $\overline{CS}$ and $\overline{RD}$ are both LOW, the interface parallel or serial output bus is enabled. $\overline{CS}$ is also used to gate the external clock.
33	RESET	DI	Reset Input. When set to a logic HIGH, reset the AD7664. Current conversion if any is aborted. If not used, this pin could be tied to DGND.
34	PD	DI	Power-Down Input. When set to a logic HIGH, power consumption is reduced and conversions are inhibited after the current one is completed.

Pin No.	Mnemonic	Type	Description
35	$\overline{\text{CNVST}}$	DI	Start Conversion. A falling edge on $\overline{\text{CNVST}}$ puts the internal sample-and-hold into the hold state and initiates a conversion. In Impulse Mode (IMPULSE HIGH and WARP LOW), if $\overline{\text{CNVST}}$ is held LOW when the acquisition phase (t_8) is complete, the internal sample-and-hold is put into the hold state and a conversion is immediately started.
36	AGND	P	Must Be Tied to Analog Ground.
37	REF	AI	Reference Input Voltage.
38	REFGND	AI	Reference Input Analog Ground.
39	INGND	AI	Analog Input Ground.
43	IN	AI	Primary Analog Input with a Range of 0 V to V_{REF}.
	EPAD		Exposed Pad. The EPAD is connected to ground; however, this connection is not required to meet specified performance.

NOTES
AI = Analog Input
DI = Digital Input
DI/O = Bidirectional Digital
DO = Digital Output
P = Power

DEFINITION OF SPECIFICATIONS

Integral Nonlinearity Error (INL)
Linearity error refers to the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs 1/2 LSB before the first code transition. Positive full scale is defined as a level 1 1/2 LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line.

Differential Nonlinearity Error (DNL)
In an ideal ADC, code transitions are 1 LSB apart. Differential nonlinearity is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

Full-Scale Error
The last transition (from 011 . . . 10 to 011 . . . 11 in twos complement coding) should occur for an analog voltage 1 1/2 LSB below the nominal full scale (2.49994278 V for the 0 V–2.5 V range). The full-scale error is the deviation of the actual level of the last transition from the ideal level.

Unipolar Zero Error
The first transition should occur at a level 1/2 LSB above analog ground (19.073 µV for the 0 V–2.5 V range). Unipolar zero error is the deviation of the actual transition from that point.

Spurious-Free Dynamic Range (SFDR)
The difference, in decibels (dB), between the rms amplitude of the input signal and the peak spurious signal.

Effective Number of Bits (ENOB)
ENOB is a measurement of the resolution with a sine wave input. It is related to S/(N+D) by the following formula:

$$ENOB = \left(S/\left[N + D\right]_{dB} - 1.76\right)/6.02$$

and is expressed in bits.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in decibels.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

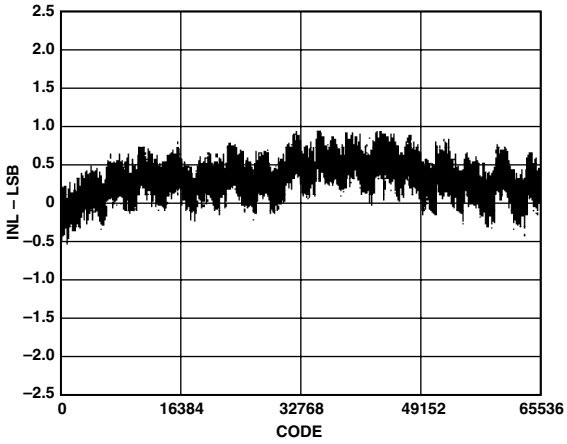
Signal to (Noise + Distortion) Ratio (S/[N+D])
S/(N+D) is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/(N+D) is expressed in decibels.

Aperture Delay
Aperture delay is a measure of the acquisition performance and is measured from the falling edge of the $\overline{\text{CNVST}}$ input to when the input signal is held for a conversion.

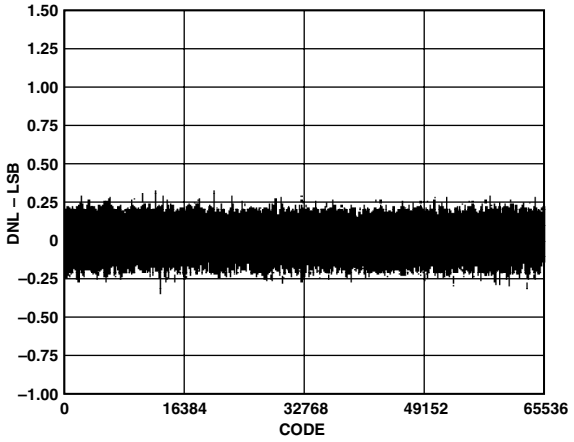
Transient Response
The time required for the AD7664 to achieve its rated accuracy after a full-scale step function is applied to its input.

Overvoltage Recovery
The time required for the ADC to recover to full accuracy after an analog input signal 150% of full-scale is reduced to 50% of the full-scale value.

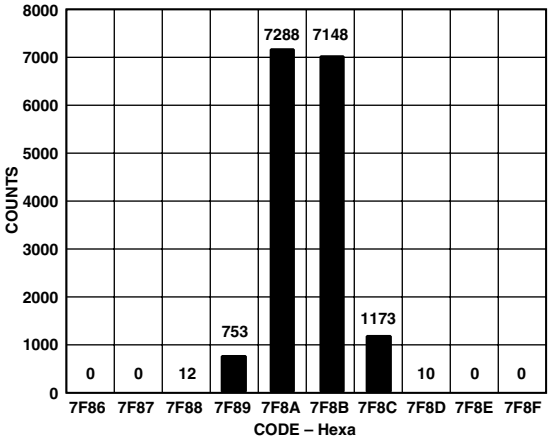
AD7664–Typical Performance Characteristics



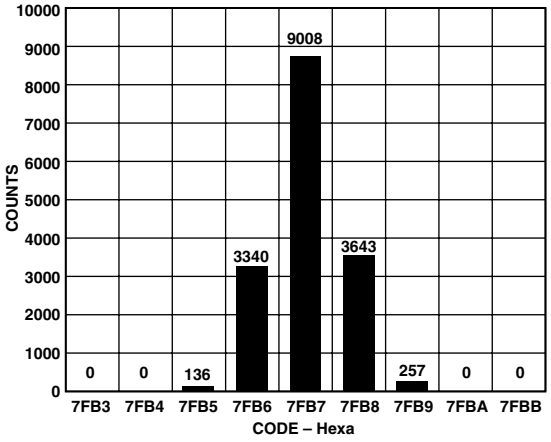
TPC 1. Integral Nonlinearity vs. Code



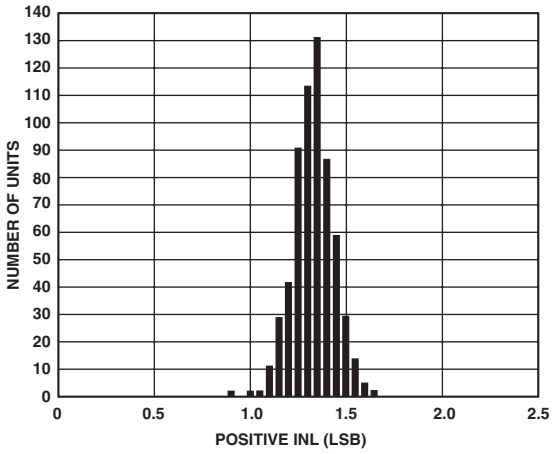
TPC 4. Differential Nonlinearity vs. Code



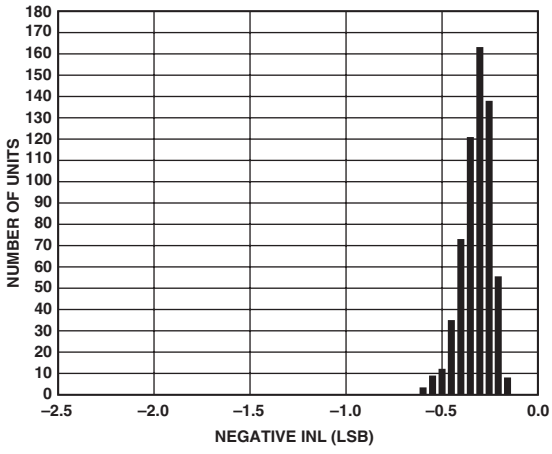
TPC 2. Histogram of 16,384 Conversions of a DC Input at the Code Transition



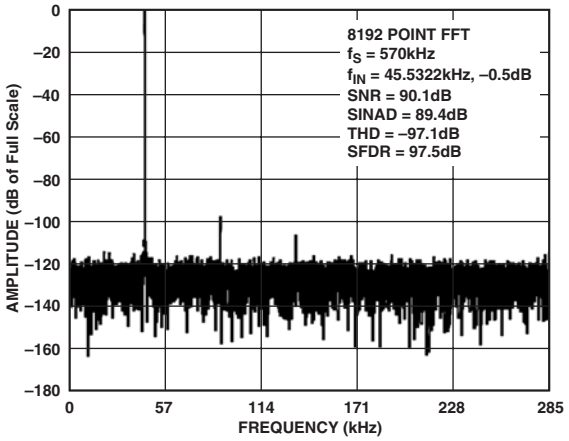
TPC 5. Histogram of 16,384 Conversions of a DC Input at the Code Center



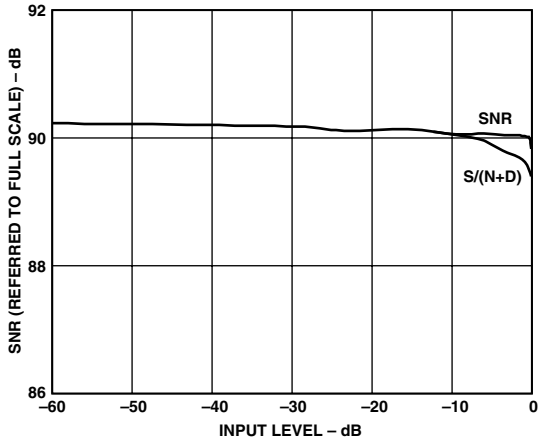
TPC 3. Typical Positive INL Distribution (600 Units)



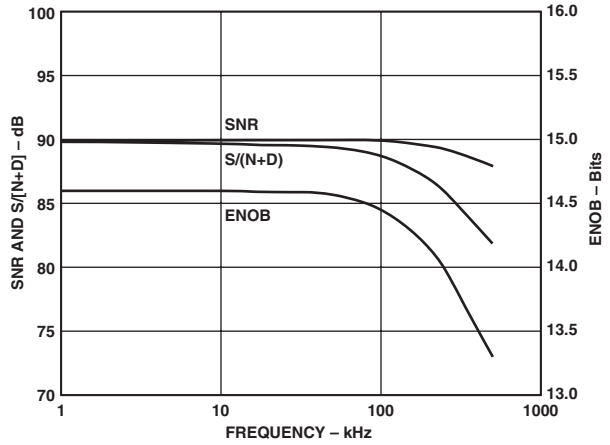
TPC 6. Typical Negative INL Distribution (600 Units)



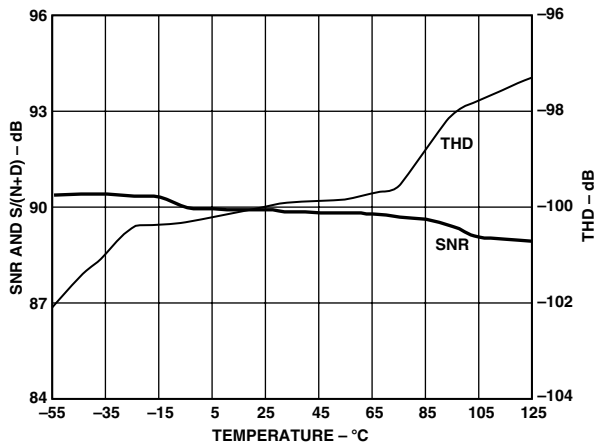
TPC 7. FFT Plot



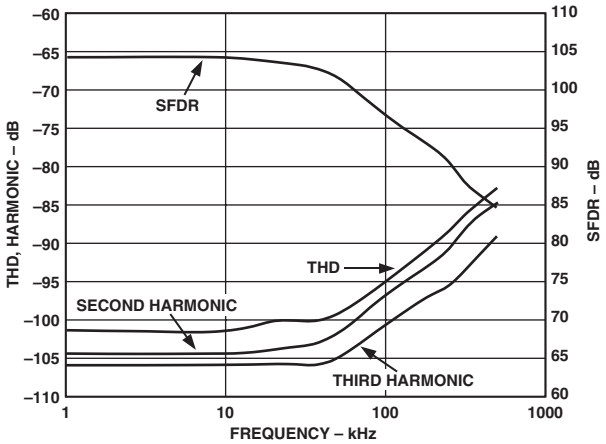
TPC 10. SNR and S/(N+D) vs. Input Level (Referred to Full Scale)



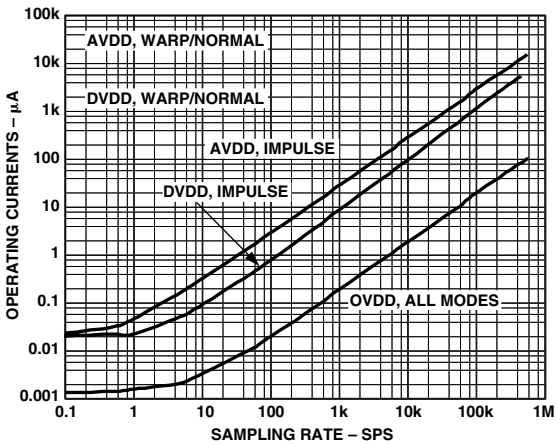
TPC 8. SNR, S/(N+D), and ENOB vs. Frequency



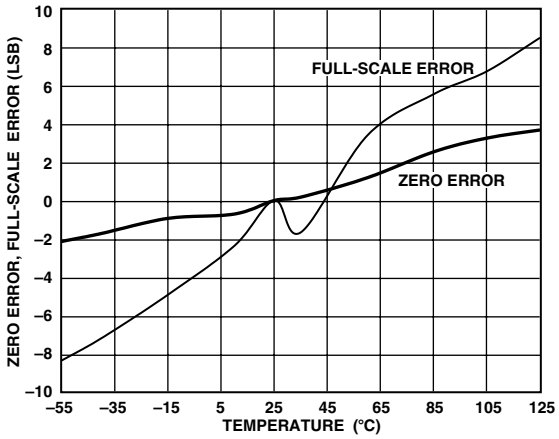
TPC 11. SNR, S/(N+D), THD vs. Temperature



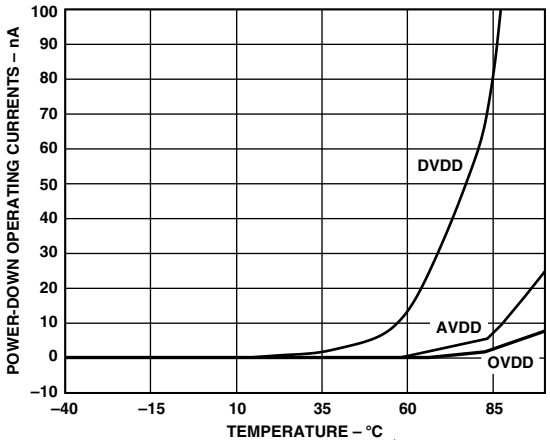
TPC 9. THD, Harmonics, and SFDR vs. Frequency



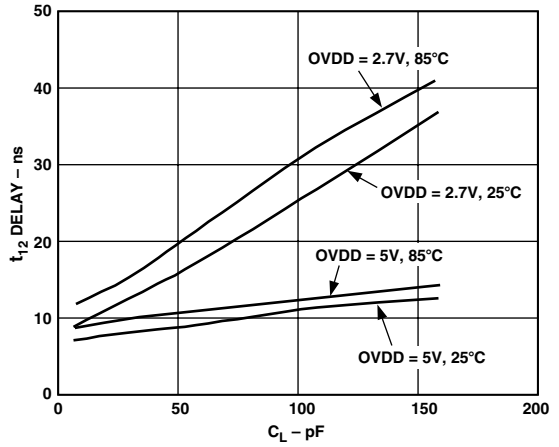
TPC 12. Operating Currents vs. Sample Rate



TPC 13. Zero Error, Full-Scale Error vs. Temperature



TPC 15. Power-Down Operating Currents vs. Temperature



TPC 14. Typical Delay vs. Load Capacitance C_L

CIRCUIT INFORMATION

The AD7664 is a very fast, low power, single-supply, precise 16-bit analog-to-digital converter (ADC). The AD7664 features different modes to optimize performances according to the applications.

In Warp Mode, the AD7664 is capable of converting 570,000 samples per second (570 kSPS).

The AD7664 provides the user with an on-chip track-and-hold, successive-approximation ADC that does not exhibit any pipeline or latency, making it ideal for multiple multiplexed channel applications.

The AD7664 can be operated from a single 5 V supply and interfaced to either 5 V or 3 V digital logic. It is housed in a 48-lead LQFP package or a 48-lead LFCSP package that saves space and allows flexible configurations as either a serial or parallel interface. The AD7664 is a pin-to-pin compatible upgrade of the AD7660.

CONVERTER OPERATION

The AD7664 is a successive-approximation analog-to-digital converter based on a charge redistribution DAC. Figure 3 shows the simplified schematic of the ADC. The capacitive DAC consists of an array of 16 binary weighted capacitors and an additional LSB capacitor. The comparator's negative input is connected to a dummy capacitor of the same value as the capacitive DAC array.

During the acquisition phase, the common terminal of the array tied to the comparator's positive input is connected to AGND via SW_A. All independent switches are connected to the analog input IN. Thus, the capacitor array is used as a sampling capacitor and acquires the analog signal on the IN input. Similarly, the dummy capacitor acquires the analog signal on the INGND input.

When the $\overline{\text{CNVST}}$ input goes LOW, a conversion phase is initiated. When the conversion phase begins, SW_A and SW_B are opened first. The capacitor array and the dummy capacitor are then disconnected from the inputs and connected to the REFGND input. Therefore, the differential voltage between IN and INGND captured at the end of the acquisition phase is applied to the comparator inputs, causing the comparator to become unbalanced. By switching each element of the capacitor array between REFGND or REF, the comparator input varies by binary-weighted voltage steps ($V_{REF}/2$, $V_{REF}/4$, . . . $V_{REF}/65536$). The control logic toggles these switches, starting with the MSB first, to bring the comparator back into a balanced condition. After the completion of this process, the control logic generates the ADC output code and brings BUSY output LOW.

Modes of Operation

The AD7664 features three modes of operation: Warp, Normal, and Impulse. Each of these modes is suitable for specific applications.

The Warp Mode allows the fastest conversion rate up to 570 kSPS. However, in this mode and this mode only, the full specified accuracy is guaranteed only when the time between conversions does not exceed 1 ms. If the time between two consecutive conversions is longer than 1 ms, for instance, after power-up, the first conversion result should be ignored. This mode makes the AD7664 ideal for applications where both high accuracy and fast sample rate are required.

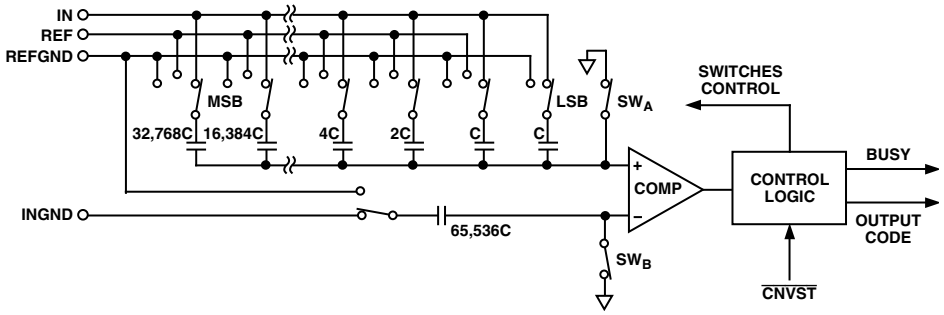


Figure 3. ADC Simplified Schematic

The Normal Mode is the fastest mode (500 kSPS) without any limitation on the time between conversions. This mode makes the AD7664 ideal for asynchronous applications such as data acquisition systems, where both high accuracy and fast sample rate are required.

The Impulse Mode, the lowest power dissipation mode, allows power saving between conversions. When operating at 100 SPS, for example, it typically consumes only 21 µW. This feature makes the AD7664 ideal for battery-powered applications.

Transfer Functions

Using the OB/$\overline{2C}$ digital input, the AD7664 offers two output codings: straight binary and twos complement. The LSB size is $V_{REF}/65536$, which is about 38.15 µV. The ideal transfer characteristics for the AD7664 are shown in Figure 4 and Table II.

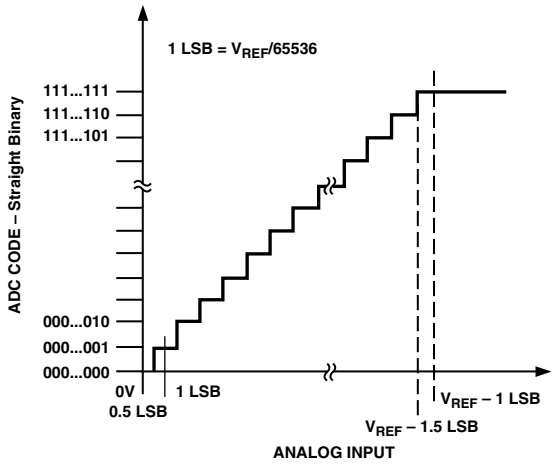


Figure 4. ADC Ideal Transfer Function

Table II. Output Codes and Ideal Input Voltages

Description	Analog Input	Digital Output Code Hexa Straight Binary	Digital Output Code Hexa Twos Complement
FSR – 1 LSB	2.499962 V	FFFF[1]	7FFF[1]
FSR – 2 LSB	2.499923 V	FFFE	7FFE
Midscale + 1 LSB	1.250038 V	8001	0001
Midscale	1.25 V	8000	0000
Midscale – 1 LSB	1.249962 V	7FFF	FFFF
–FSR + 1 LSB	38 µV	0001	8001
–FSR	0 V	0000[2]	8000[2]

NOTES
[1]This is also the code for overrange analog input ($V_{IN} – V_{INGND}$ above $V_{REF} – V_{REFGND}$).
[2]This is also the code for underrange analog input (V_{IN} below V_{INGND}).

TYPICAL CONNECTION DIAGRAM

Figure 5 shows a typical connection diagram for the AD7664.

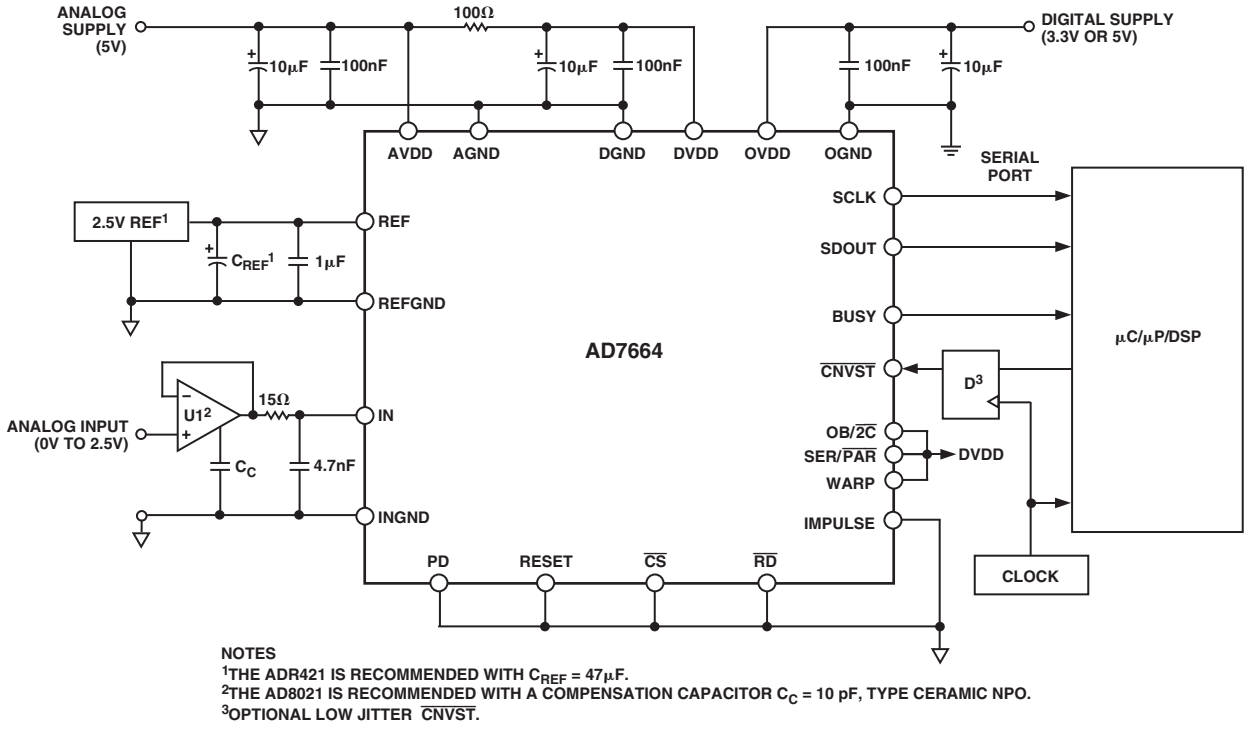


Figure 5. Typical Connection Diagram

Analog Input

Figure 6 shows an equivalent circuit of the input structure of the AD7664.

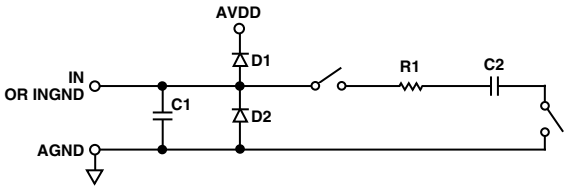


Figure 6. Equivalent Analog Input Circuit

The two diodes D1 and D2 provide ESD protection for the analog inputs IN and INGND. Care must be taken to ensure that the analog input signal never exceeds the supply rails by more than 0.3 V. This will cause these diodes to become forward-biased and start conducting current. These diodes can handle a forward-biased current of 100 mA maximum. For instance, these conditions could eventually occur when the input buffer's (U1) supplies are different from AVDD. In such cases, an input buffer with a short circuit current limitation can be used to protect the part.

This analog input structure allows the sampling of the differential signal between IN and INGND. Unlike other converters, the INGND input is sampled at the same time as the IN input. By using this differential input, small signals common to both inputs are rejected, as shown in Figure 7, which represents the typical CMRR over frequency. For instance, by using INGND to sense a remote signal ground, difference of ground potentials between the sensor and the local ADC ground are eliminated.

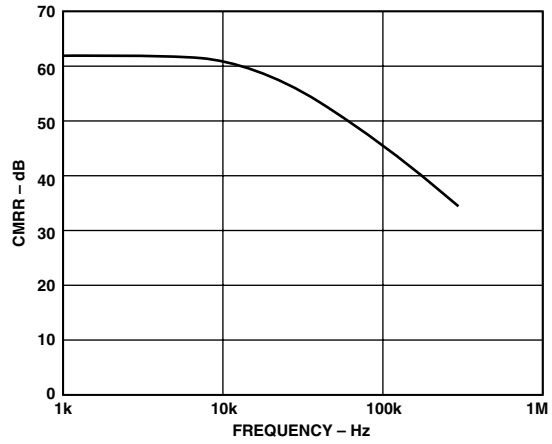


Figure 7. Analog Input CMRR vs. Frequency

During the acquisition phase, the impedance of the analog input IN can be modeled as a parallel combination of capacitor C1 and the network formed by the series connection of R1 and C2. Capacitor C1 is primarily the pin capacitance. The resistor R1 is typically 140 Ω and is a lumped component made up of some serial resistors and the on resistance of the switches. The capacitor C2 is typically 60 pF and is mainly the ADC sampling capacitor. During the conversion phase, where the switches are opened, the input impedance is limited to C1. The R1, C2 makes a one-pole low-pass filter that reduces the undesirable aliasing effect and limits the noise.

When the source impedance of the driving circuit is low, the AD7664 can be driven directly. Large source impedances will significantly affect the ac performances, especially the total harmonic distortion (THD). The maximum source impedance depends on the amount of THD that can be tolerated. The THD degrades in function of the source impedance and the maximum input frequency as shown in Figure 8.

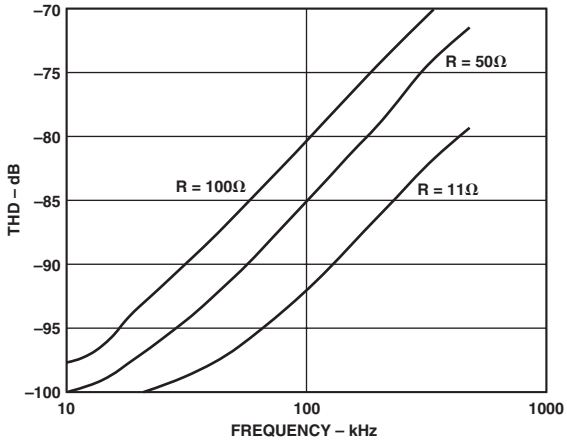


Figure 8. THD vs. Analog Input Frequency and Source Resistance

Driver Amplifier Choice

Although the AD7664 is easy to drive, the driver amplifier needs to meet at least the following requirements:

- The driver amplifier and the AD7664 analog input circuit must be able, together, to settle for a full-scale step of the capacitor array at a 16-bit level (0.0015%). In the amplifier's data sheet, the settling at 0.1% to 0.01% is more commonly specified. It could significantly differ from the settling time at 16-bit level and it should, therefore, be verified prior to the driver selection. The tiny op amp AD8021, which combines ultralow noise and a high gain bandwidth, meets this settling time requirement even when used with high gain up to 13.
- The noise generated by the driver amplifier needs to be kept as low as possible in order to preserve the SNR and transition noise performance of the AD7664. The noise coming from the driver is filtered by the AD7664 analog input circuit one-pole low-pass filter made by R1 and C2 or the external filter, if any is used. The SNR degradation due to the amplifier is:

$$SNR_{LOSS} = 20 \log \left[\frac{28}{\sqrt{784 + \frac{\pi}{2} f_{-3dB} \left(N e_N \right)^2}} \right]$$

where:

$f_{-3\,dB}$ is the –3 dB input bandwidth in MHz of the AD7664 (18 MHz) or the cutoff frequency of the input filter, if any used.

N is the noise gain of the amplifier (1, if in buffer configuration).

e_N is the equivalent input noise voltage of the op amp in nV/√Hz.

For instance, in a driver like the AD8021, with an equivalent input noise of 2 nV/√Hz and configured as a buffer, thus with a noise gain of 1, the SNR degrades by 0.58 dB.

- The driver needs to have a THD performance suitable to that of the AD7664. TPC 12 gives the THD versus frequency that the driver should preferably exceed.

The AD8021 meets these requirements and is usually appropriate for almost all applications. The AD8021 needs an external compensation capacitor of 10 pF. This capacitor should have good linearity as an NPO ceramic or mica type.

The AD8022 could also be used where a dual version is needed and a gain of 1 is used.

The AD829 is another alternative where high frequency (above 100 kHz) performance is not required. In a gain of 1, it requires an 82 pF compensation capacitor.

The AD8610 is another option where low bias current is needed in low frequency applications.

Voltage Reference Input

The AD7664 uses an external 2.5 V voltage reference.

The voltage reference input REF of the AD7664 has a dynamic input impedance; it should, therefore, be driven by a low impedance source with an efficient decoupling between REF and REFGND inputs. This decoupling depends on the choice of the voltage reference, but usually consists of a 1 µF ceramic capacitor and a low ESR tantalum capacitor connected to the REF and REFGND inputs with minimum parasitic inductance. 47 µF is an appropriate value for the tantalum capacitor when used with one of the recommended reference voltages:

- The low noise, low temperature drift ADR421 and AD780 voltage references
- The low power ADR291 voltage reference
- The low cost AD1582 voltage reference

For applications using multiple AD7664s, it is more effective to buffer the reference voltage with a low noise, very stable op amp like the AD8031.

Care should also be taken with the reference temperature coefficient of the voltage reference that directly affects the full-scale accuracy, if this parameter matters. For instance, a ±15 ppm/°C tempco of the reference changes the full scale by ±1 LSB/°C.

V_{REF}, as mentioned in the specification table, could be increased to AVDD – 1.85 V. The benefit here is the increased SNR obtained as a result of this increase. Since the input range is defined in terms of V_{REF}, this would essentially increase the range to make it a 0 V to 3 V input range with an AVDD above 4.85 V. The theoretical improvement as a result of this increase in reference is 1.58 dB (20 log [3/2.5]). Due to the theoretical quantization noise, however, the observed improvement is approximately 1 dB. The AD780 can be selected with a 3 V reference voltage.

Power Supply

The AD7664 uses three sets of power supply pins: an analog 5 V supply AVDD, a digital 5 V core supply DVDD, and a digital input/output interface supply OVDD. The OVDD supply allows direct interface with any logic working between 2.7 V and 5.25 V. To reduce the number of supplies needed, the digital core (DVDD) can be supplied through a simple RC filter from the analog supply as shown in Figure 5. The AD7664 is independent of power supply sequencing and thus free from supply voltage induced latch-up. Additionally, it is very insensitive to power supply variations over a wide frequency range, as shown in Figure 9.

POWER DISSIPATION VERSUS THROUGHPUT

Operating currents are very low during the acquisition phase, which allows significant power savings when the conversion rate is reduced, as shown in Figure 10. This power saving depends on the mode used. In Impulse Mode, the AD7664 automatically reduces its power consumption at the end of each conversion phase. This feature makes the AD7664 ideal for very low power battery-operated applications. It should be noted that the digital interface remains active even during the acquisition phase. To reduce the operating digital supply currents even further, the digital inputs need to be driven close to the power supply rails (i.e., DVDD or DGND for all inputs except EXT/$\overline{INT}$, INVSYNC, INVSCLK, RDC/SDIN, and OVDD or OGND for these last four inputs).

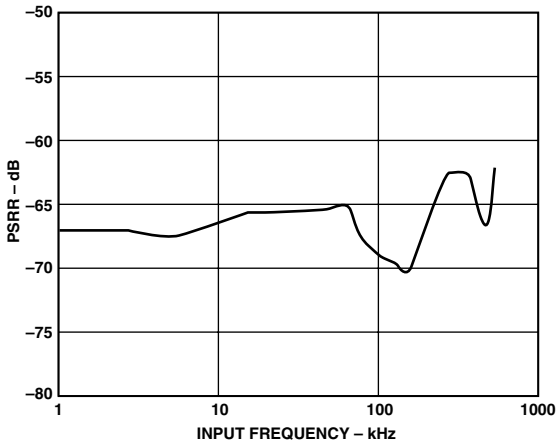


Figure 9. PSRR vs. Frequency

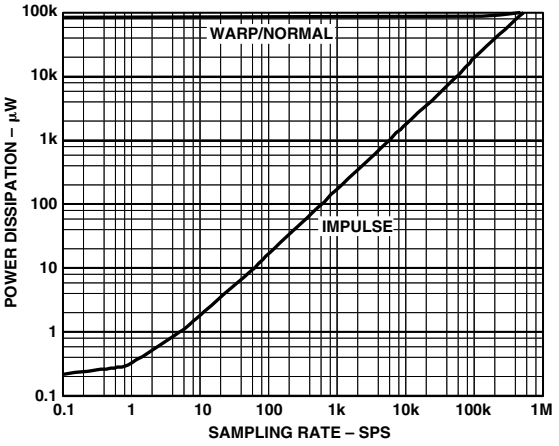


Figure 10. Power Dissipation vs. Sample Rate

CONVERSION CONTROL

Figure 11 shows the detailed timing diagrams of the conversion process. The AD7664 is controlled by the signal $\overline{\text{CNVST}}$, which initiates conversion. Once initiated, it cannot be restarted or aborted, even by the power-down input PD, until the conversion is complete. The $\overline{\text{CNVST}}$ signal operates independently of $\overline{\text{CS}}$ and $\overline{\text{RD}}$ signals.

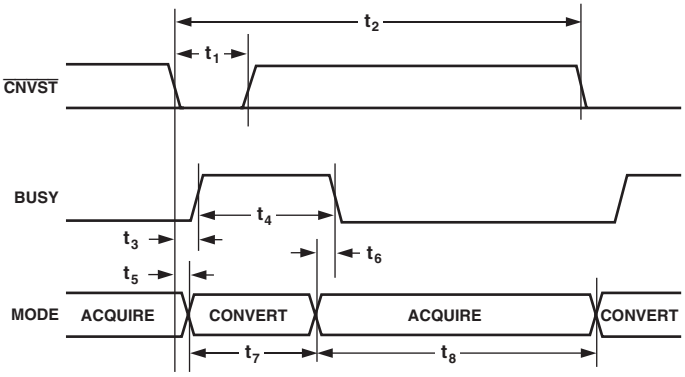


Figure 11. Basic Conversion Timing

In Impulse Mode, conversions can be automatically initiated. If $\overline{\text{CNVST}}$ is held LOW when BUSY is LOW, the AD7664 controls the acquisition phase and then automatically initiates a new conversion. By keeping $\overline{\text{CNVST}}$ LOW, the AD7664 keeps the conversion process running by itself. It should be noted that the analog input has to be settled when BUSY goes LOW. Also, at power-up, $\overline{\text{CNVST}}$ should be brought LOW once to initiate the conversion process. In this mode, the AD7664 could sometimes run slightly faster then the guaranteed limits in the Impulse Mode of 444 kSPS. This feature does not exist in Warp or Normal Modes.

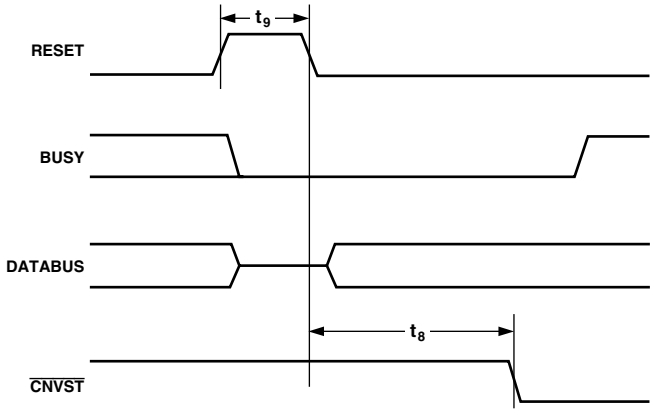


Figure 12. RESET Timing

Although $\overline{\text{CNVST}}$ is a digital signal, it should be designed with special care with fast, clean edges, and levels with minimum overshoot and undershoot or ringing.

It is a good thing to shield the $\overline{\text{CNVST}}$ trace with ground and also to add a low value serial resistor (i.e., 50 Ω) termination close to the output of the component that drives this line.

For applications where the SNR is critical, the $\overline{\text{CNVST}}$ signal should have a very low jitter. This may be achieved by using a dedicated oscillator for $\overline{\text{CNVST}}$ generation or, at least, to clock it with a high frequency, low jitter clock as shown in Figure 5.

DIGITAL INTERFACE

The AD7664 has a versatile digital interface; it can be interfaced with the host system by using either a serial or parallel interface. The serial interface is multiplexed on the parallel databus. The AD7664 digital interface also accommodates both 3 V or 5 V logic by simply connecting the OVDD supply pin of the AD7664 to the host system interface digital supply. Finally, by using the OB/$\overline{\text{2C}}$ input pin, either twos complement or straight binary coding can be used.

The two signals $\overline{\text{CS}}$ and $\overline{\text{RD}}$ control the interface. $\overline{\text{CS}}$ and $\overline{\text{RD}}$ have a similar effect, because they are OR'd together internally. When at least one of these signals is HIGH, the interface outputs are in high impedance. Usually, $\overline{\text{CS}}$ allows the selection of each AD7664 in multicircuit applications and is held LOW in a single AD7664 design. $\overline{\text{RD}}$ is generally used to enable the conversion result on the databus.

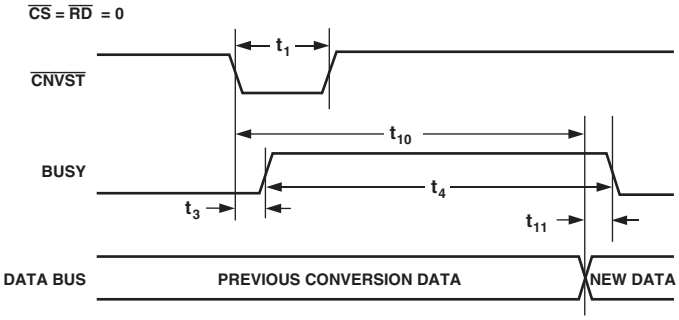


Figure 13. Master Parallel Data Timing for Reading (Continuous Read)

PARALLEL INTERFACE

The AD7664 is configured to use the parallel interface when the SER/$\overline{\text{PAR}}$ is held LOW. The data can be read either after each conversion, which is during the next acquisition phase, or during the following conversion as shown, respectively, in Figures 14 and 15. When the data is read during the conversion, however, it is recommended that it be read-only during the first half of the conversion phase. This avoids any potential feedthrough between voltage transients on the digital interface and the most critical analog conversion circuitry.

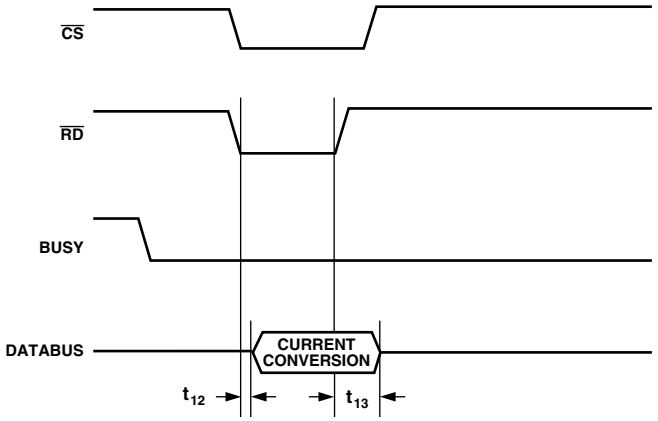


Figure 14. Slave Parallel Data Timing for Reading (Read after Convert)

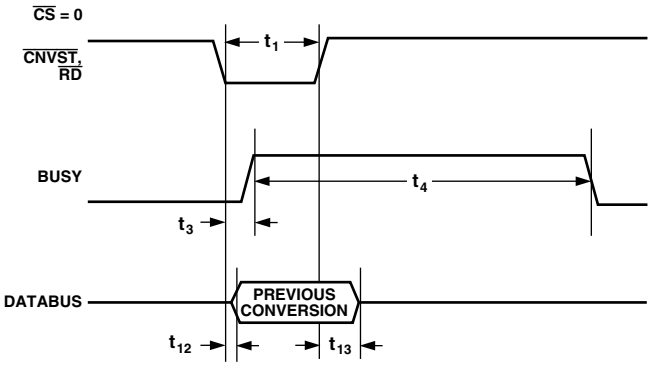


Figure 15. Slave Parallel Data Timing for Reading (Read during Convert)

SERIAL INTERFACE

The AD7664 is configured to use the serial interface when the SER/$\overline{\text{PAR}}$ is held HIGH. The AD7664 outputs 16 bits of data, MSB first, on the SDOUT pin. This data is synchronized with the 16 clock pulses provided on the SCLK pin. The output data is valid on both the rising and falling edge of the data clock.

MASTER SERIAL INTERFACE

Internal Clock

The AD7664 is configured to generate and provide the serial data clock SCLK when the EXT/$\overline{\text{INT}}$ pin is held LOW. The AD7664 also generates a SYNC signal to indicate to the host when the serial data is valid. The serial clock SCLK and the SYNC signal can be inverted, if desired. Depending on RDC/SDIN input, the data can be read after each conversion or during the following conversion. Figures 16 and 17 show the detailed timing diagrams of these two modes.

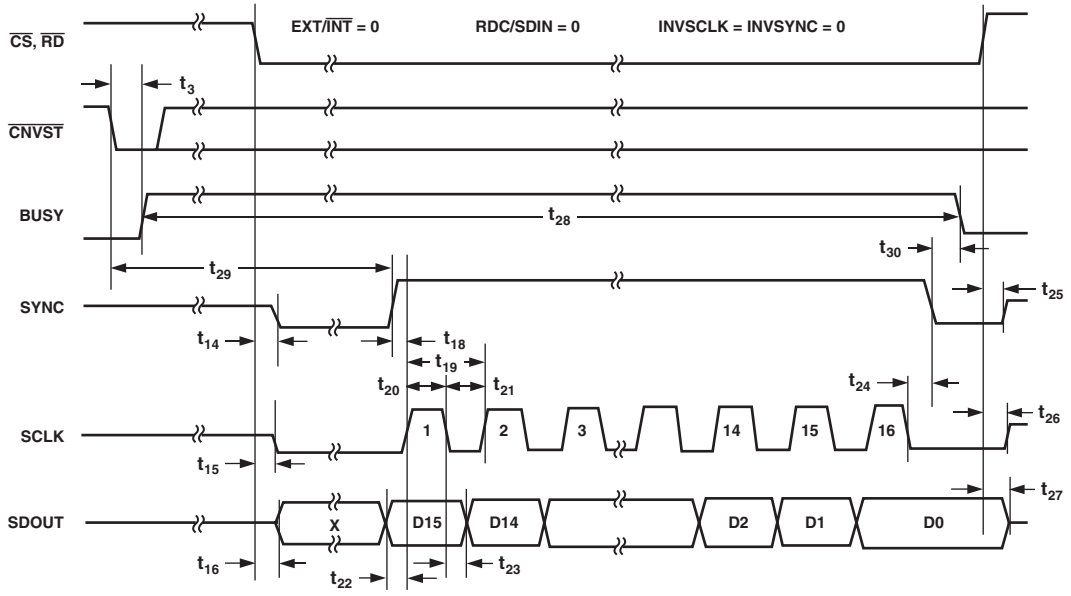


Figure 16. Master Serial Data Timing for Reading (Read after Convert)

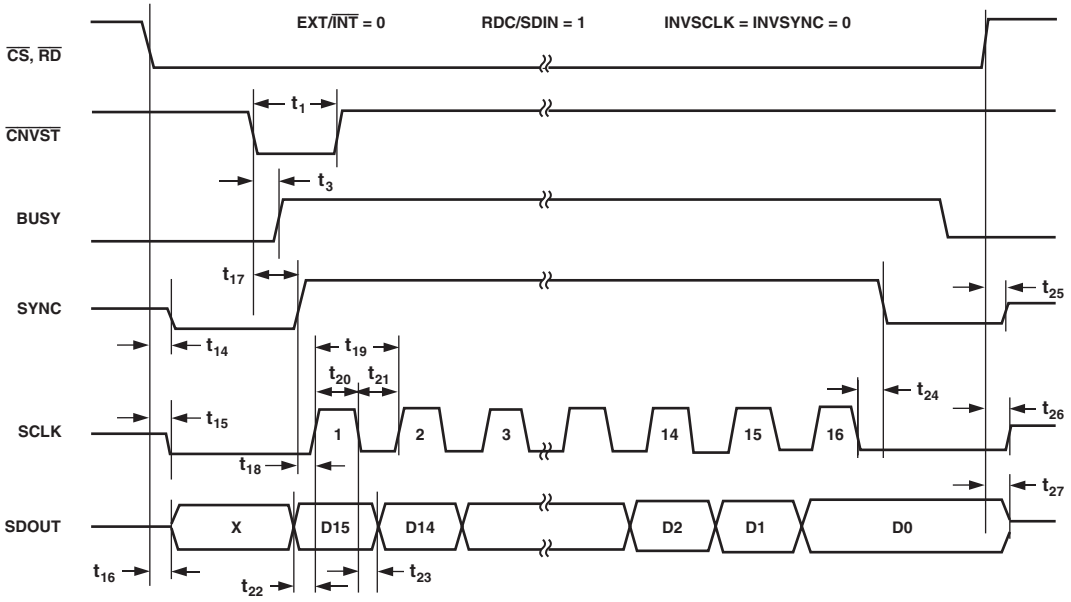


Figure 17. Master Serial Data Timing for Reading (Read Previous Conversion during Convert)

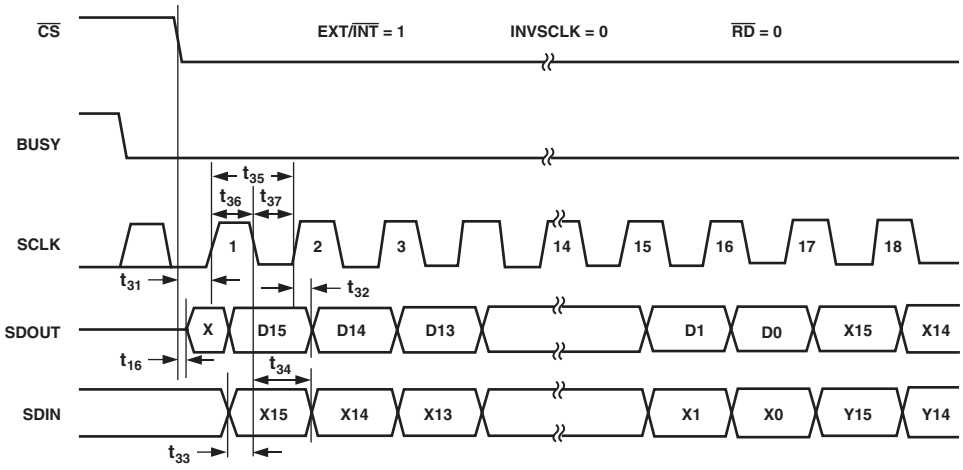


Figure 18. Slave Serial Data Timing for Reading (Read after Convert)

Because the AD7664 is used with a fast throughput, the Master Read During Conversion Mode is the most often recommended Serial Mode, when it can be used. In this mode, the serial clock and data toggle at appropriate instants that minimize potential feedthrough between digital activity and the critical conversion decisions.

In Read-after-Conversion Mode, it should be noted that, unlike in other modes, the signal BUSY returns LOW after the 16 data bits are pulsed out and not at the end of the conversion phase, which results in a longer BUSY width.

SLAVE SERIAL INTERFACE

External Clock

The AD7664 is configured to accept an externally supplied serial data clock on the SCLK pin when the EXT/$\overline{INT}$ pin is held HIGH. In this mode, several methods can be used to read the data. The external serial clock is gated by $\overline{CS}$. When $\overline{CS}$ and $\overline{RD}$ are both LOW, the data can be read after each conversion or during the following conversion. The external clock can be either a continuous or discontinuous clock. A discontinuous clock can be either normally HIGH or normally LOW, when inactive. Figures 18 and 20 show the detailed timing diagrams of these methods.

While the AD7664 is performing a bit decision, it is important that voltage transients not occur on digital input/output pins or degradation of the conversion result could occur. This is particularly important during the second half of the conversion phase, because the AD7664 provides error correction circuitry that can correct for an improper bit decision made during the first half of the conversion phase. For this reason, it is recommended that when an external clock is being provided, it is a discontinuous clock that is toggling only when BUSY is LOW or, more importantly, that it does not transition during the latter half of BUSY HIGH.

External Discontinuous Clock Data Read after Conversion

Though the maximum throughput cannot be achieved using this mode, it is the most often recommended of the serial Slave Modes. Figure 18 shows the detailed timing diagrams of this method. After a conversion is complete, indicated by BUSY returning LOW, the result of this conversion can be read while both $\overline{CS}$ and $\overline{RD}$ are LOW. The data is shifted out, MSB first, with 16 clock pulses and is valid on both the rising and falling edge of the clock.

Among the advantages of this method, the conversion performance is not degraded, because there are no voltage transients on the digital interface during the conversion process.

Another advantage is the ability to read the data at any speed up to 40 MHz, which accommodates both slow digital host interface and the fastest serial reading.

Finally, in this mode only, the AD7664 provides a daisy-chain feature using the RDC/SDIN input pin for cascading multiple converters together. This feature is useful for reducing component count and wiring connections when desired as, for instance, in isolated multiconverter applications.

An example of the concatenation of two devices is shown in Figure 19. Simultaneous sampling is possible by using a common $\overline{CNVST}$ signal. It should be noted that the RDC/SDIN input is latched on the edge of SCLK opposite to the one used to shift out the data on SDOUT. Therefore, the MSB of the upstream converter just follows the LSB of the downstream converter on the next SCLK cycle.

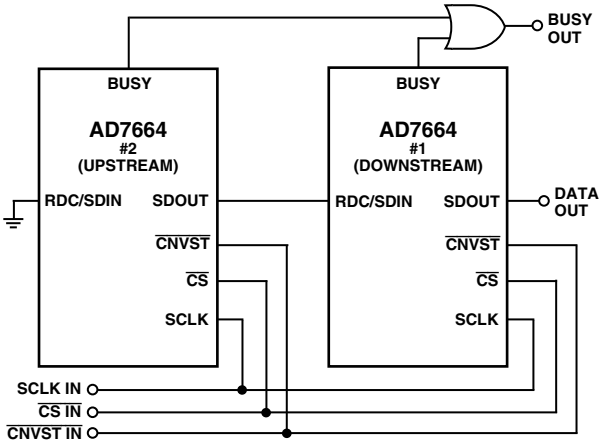


Figure 19. Two AD7664s in a Daisy-Chain Configuration

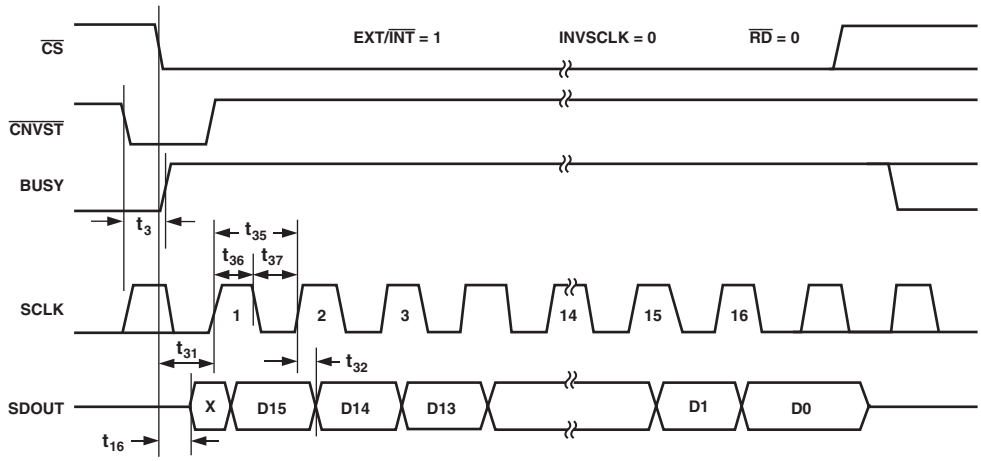


Figure 20. Slave Serial Data Timing for Reading (Read Previous Conversion during Convert)

External Clock Data Read during Conversion

Figure 20 shows the detailed timing diagram of this method. During a conversion, while both $\overline{CS}$ and $\overline{RD}$ are LOW, the result of the previous conversion can be read. The data is shifted out MSB first with 16 clock pulses, and is valid on both the rising and falling edge of the clock. The 16 bits have to be read before the current conversion is complete; otherwise, RDERROR is pulsed HIGH and can be used to interrupt the host interface to prevent incomplete data reading. There is no daisy-chain feature in this mode and RDC/SDIN input should always be tied either HIGH or LOW.

To reduce performance degradation due to digital activity, a fast discontinuous clock of at least 18 MHz when in Impulse Mode, 25 MHz when in Normal Mode, or 40 MHz when in Warp Mode is recommended to ensure that all the bits are read during the first half of the conversion phase. It is also possible to begin to read the data after conversion and continue to read the last bits even after a new conversion has been initiated. That allows the use of a slower clock speed such as 14 MHz in Impulse Mode, 18 MHz in Normal Mode, and 25 MHz in Warp Mode.

MICROPROCESSOR INTERFACING

The AD7664 is ideally suited for traditional dc measurement applications supporting a microprocessor and ac signal processing applications interfacing to a digital signal processor. The AD7664 is designed to interface either with a parallel 8-bit or 16-bit wide interface, or with a general-purpose serial port or I/O ports on a microcontroller. A variety of external buffers can be used with the AD7664 to prevent digital noise from coupling into the ADC. The following section discusses the use of an AD7664 with an ADSP-219x SPI equipped DSP.

SPI Interface (ADSP-219x)

Figure 21 shows an interface diagram between the AD7664 and an SPI-equipped ADSP-219x. To accommodate the slower speed of the DSP, the AD7664 acts as a slave device and data must be read after conversion. This mode also allows the daisy-chain feature. The convert command can be initiated in response to an internal timer interrupt. The reading process can be initiated in response to the end-of-conversion signal (BUSY going LOW) using an interrupt line of the DSP. The serial interface (SPI) on the ADSP-219x is configured for master mode— (MSTR) = 1, Clock Polarity bit (CPOL) = 0, Clock Phase bit (CPHA) = 1, and SPI Interrupt Enable (TIMOD) = 00— by writing to the SPI control register (SPICLTx). To meet all timing requirements, the SPI clock should be limited to 17 Mbps, which allows it to read an ADC result in less than 1 µs. When a higher sampling rate is desired, use of one of the parallel interface modes is recommended.

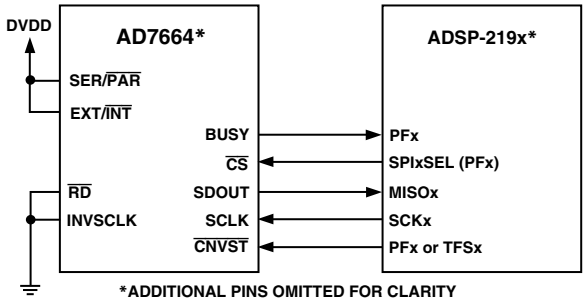


Figure 21. Interfacing the AD7664 to an SPI Interface

APPLICATION HINTS

Bipolar and Wider Input Ranges

In some applications, it is desired to use a bipolar or wider analog input range like, for instance, ±10 V, ±5 V, or 0 V to 5 V. Although the AD7664 has only one unipolar range, by simple modifications of the input driver circuitry, bipolar and wider input ranges can be used without any performance degradation.

Figure 22 shows a connection diagram that allows this. Component values required and resulting full-scale ranges are shown in Table III.

For applications where accurate gain and offset are desired, they can be calibrated by acquiring a ground and a voltage reference using an analog multiplexer, U2, as shown for bipolar input ranges in Figure 22.

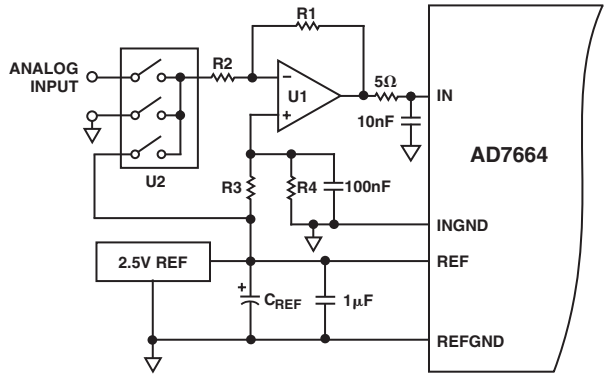


Figure 22. Using the AD7664 in 16-Bit Bipolar and/or Wider Input Ranges

Table III. Component Values and Input Ranges

Input Range	R1 (kΩ)	R2 (kΩ)	R3 (kΩ)	R4 (kΩ)
±10 V	1	8	10	8
±5 V	1	4	10	6.67
0 V to –5 V	1	2	None	0

Layout

The AD7664 has very good immunity to noise on the power supplies, as can be seen in Figure 9. However, care should still be taken with regard to grounding layout.

The printed circuit board that houses the AD7664 should be designed so that the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes that can be easily separated. Digital and analog ground planes should be joined in only one place, preferably underneath the AD7664, or, at least, as close as possible to the AD7664. If the AD7664 is in a system where multiple devices require analog-to-digital ground connections, the connection should still be made at one point only, a star ground point that should be established as close as possible to the AD7664.

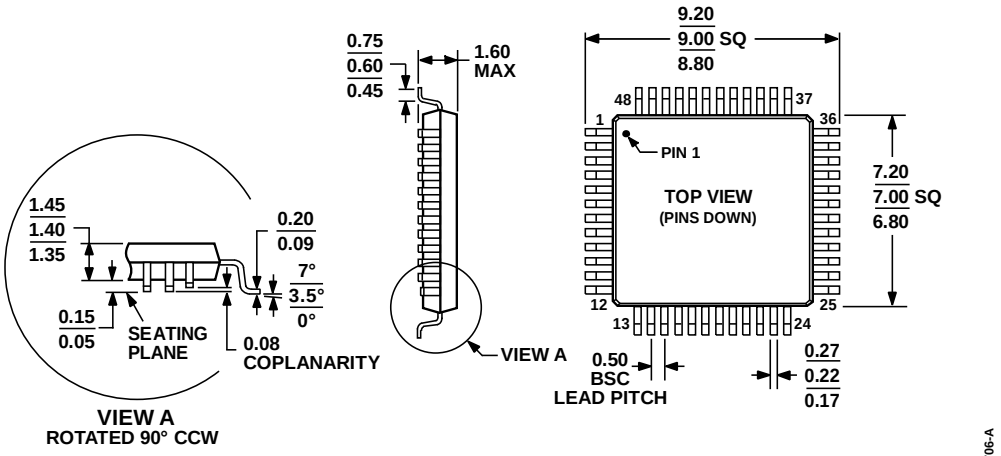
It is recommended to avoid running digital lines under the device, because these couple noise onto the die. The analog ground plane should be allowed to run under the AD7664 to avoid noise coupling. Fast switching signals like $\overline{\text{CNVST}}$ or clocks should be shielded with digital ground to avoid radiating noise to other sections of the board and should never run near analog signal paths. Crossover of digital and analog signals should be avoided. Traces on different but close layers of the board should run at right angles to each other. This reduces the effect of feedthrough through the board.

The power supplies' lines to the AD7664 should use as large a trace as possible to provide low impedance paths and reduce the effect of glitches on the power supplies' lines. Good decoupling is also important to lower the supplies' impedance presented to the AD7664 and to reduce the magnitude of the supply spikes. Decoupling ceramic capacitors, typically 100 nF, should be placed on each power supply's pins AVDD, DVDD, and OVDD close to, and ideally right up against, these pins and their corresponding ground pins. Additionally, low ESR 10 µF capacitors should be located in the vicinity of the ADC to further reduce low frequency ripple.

The DVDD supply of the AD7664 can be either a separate supply or come from the analog supply AVDD or the digital interface supply OVDD. When the system digital supply is noisy, or fast switching digital signals are present, it is recommended that, if no separate supply is available, to connect the DVDD digital supply to the analog supply, AVDD, through an RC filter, as shown in Figure 5, and to connect the system supply to the interface digital supply, OVDD, and the remaining digital circuitry. When DVDD is powered from the system supply, it is useful to insert a bead to further reduce high frequency spikes.

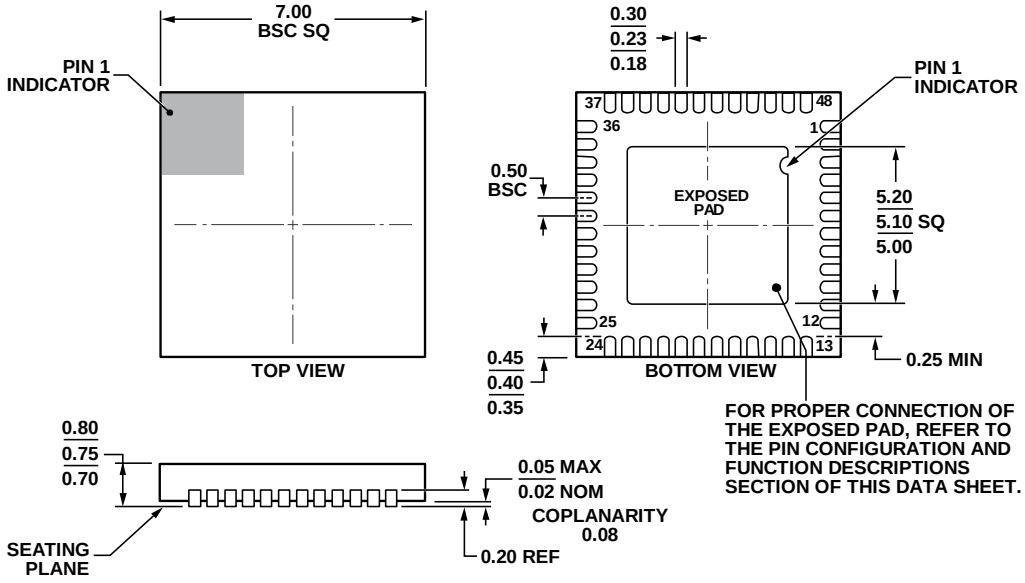
The AD7664 has five different ground pins: INGND, REFGND, AGND, DGND, and OGND. INGND is used to sense the analog input signal. REFGND senses the reference, voltage and should be a low impedance return to the reference because it carries pulsed currents. AGND is the ground to which most internal ADC analog signals are referenced. This ground must be connected with the least resistance to the analog ground plane. DGND must be tied to the analog or digital ground plane, depending on the configuration. OGND is connected to the digital system ground.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-026-BBC

Figure 40. 48-Lead Plastic Quad Flat Package [LQFP]
(ST-48)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-WKKD.

Figure 41. 48-Lead Lead Frame Chip Scale Package [LFCSP]
7 x 7 mm Body and 0.75 mm Package Height
(CP-48-4)
Dimensions shown in millimeters

Revision History

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Changes to PIN CONFIGURATION	5
Changes to PIN FUNCTION DESCRIPTIONS	7
Deleted Evaluating the AD7664 Performance Section	19
Updated OUTLINE DIMENSIONS	20
1/04—Data Sheet changed from REV. D to REV. E.	
Changes to title	1
Changes to FEATURES	1
10/03—Data Sheet changed from REV. C to REV. D.	
Changes to title	1
Added PulSAR Selection table	1
Changes to FEATURES	1
Changes to GENERAL DESCRIPTION	1
Changes to ABSOLUTE MAXIMUM RATINGS	4
Changes to ORDERING GUIDE	4
Added new TPC 2, 3, and 13 and renumbered successive TPCs	8
Changes to Circuit Information section	10
Changes to Driver Amplifier Choice section	12
Replaced MICROPROCESSOR INTERFACING section	17
Deleted Figure 22 and renumbered successive figures	18
Changes to Table III	18
Added CP-48	19
Updated OUTLINE DIMENSIONS	19
11/01—Data Sheet changed from REV. B to REV. C.	
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Edits to SPECIFICATIONS	3
Edits to ORDERING GUIDE	4
TPC 12 replaced with new data	9
Edits to Voltage Reference Input	13
Edits to OUTLINE DIMENSIONS	19

8/01 Revision History continued on next page

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