DS2745
Low-Cost I²C Battery Monitor

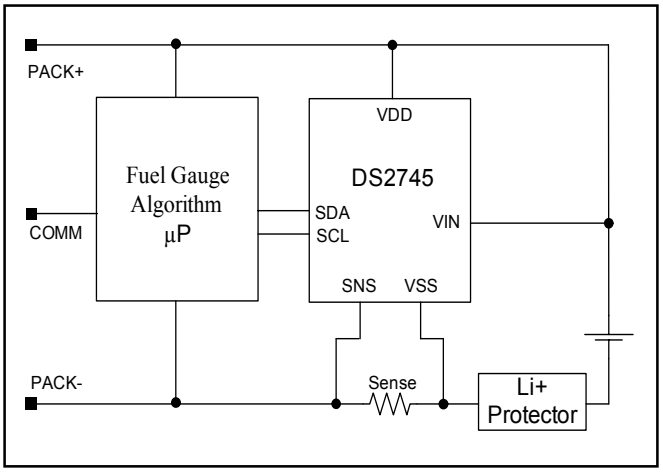
FEATURES

16-Bit Bidirectional Current Measurement
- 1.56µV LSB, ±51.2mV Dynamic Range
- 104µA LSB, ±3.4A Dynamic Range (RSNS = 15mΩ)

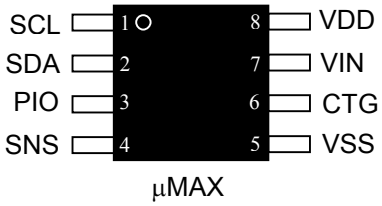
Current Accumulation Register Resolution
- 6.25µVhr LSB, ±204.8mVh Range
- 0.417mAhr LSB, ±13.65Ah Range (R_{SNS} = 15mΩ)

11-Bit Voltage Measurement
4.88mV LSB, 0V to 5V Input Range
11-Bit Temperature Measurement
0.125ºC Resolution, -20ºC to +70ºC
Industry Standard I²C* Interface
Low Power Consumption:
- Active Current:
- 70µA typical, 100µA max
- Sleep Current:
- 1µA typical, 3µA max

BLOCK DIAGRAM



PIN CONFIGURATION



µMAX

See Table 1 for Ordering Information.

DESCRIPTION

The DS2745 provides current-flow, voltage, and temperature measurement data to support battery-capacity monitoring in cost-sensitive applications. The DS2745 can be mounted on either the host side or pack side of the application. Current measurement and coulomb counting is accomplished by monitoring the voltage drop across an external sense resistor, voltage measurement is accomplished through a separate voltage-sense input, and temperature measurement takes place on-chip. A standard I²C interface with software programmable address gives the controlling microprocessor access to all data and status registers inside the DS2745. A low-power sleep mode state conserves energy when the cell pack is in storage.

APPLICATIONS

Cellular
GPS
PDAs
Handheld Products

Table 1. ORDERING INFORMATION

PART	MARKING	PIN-PACKAGE
DS2745U+	2745	µMAX package
DS2745U+/T&R	2745	DS2745U+ in Tape-and-Reel

+Denotes lead-free package.
**I²C is a trademark of Philips Corp. Purchase of I²C components from Maxim Integrated Products, Inc., or one of its sublicensed Associated Companies, conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.*

ABSOLUTE MAXIMUM RATINGS*

Voltage on All Pins Relative to V_{SS}	-0.3V to +6V
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-55°C to +125°C
Soldering Temperature	See IPC/JEDECJ-STD-020A

** This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.*

RECOMMENDED DC OPERATING CONDITIONS

(2.5V ≤ V_{DD} ≤ 5.5V; T_A = 0°C to +70°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}	(Note 1)	2.5		5.5	V
Serial Data I/O Pin	SDA	(Note 1)	-0.3		+5.5	V
Serial Clock Pin	SCL	(Note 1)	-0.3		+5.5	V
Programmable I/O Pin	PIO	(Note 1)	-0.3		+5.5	V
VIN Pin	V_{IN}	(Note 1)	-0.3		V_{DD} +0.3	V

DC ELECTRICAL CHARACTERISTICS

(2.5V ≤ V_{DD} ≤ 4.5V; T_A = 0°C to +70°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Active Current	I_{ACTIVE}			70	100	µA
		V_{DD} = 5.5V			105	
Sleep-Mode Current	I_{SLEEP}	SCL = SDA = V_{SS}, PIO = V_{SS}		1	3	µA
Current Resolution	I_{LSB}			1.56		µV/R
Current Full-Scale Magnitude	I_{FS}	(Note 1)		□51.2		mV/R
Current Offset	I_{OERR}	(Note 2)	- 7.82		+ 12.5	µV/R
Current Gain Error	I_{GERR}		- 1.0		+1.0	% of reading
Accumulated Current Resolution	q_{CA}			6.25		µVh/R
Accumulated Current Offset	q_{OERR}	V_{SNS} = V_{SS}, (Notes 4, 5)	- 188		+ 0	µVh/R per day
Voltage Resolution	V_{LSB}			4.88		mV
Voltage Full-Scale	V_{FS}		0		4.992	V
Voltage Error	V_{GERR}	(Note 12)	- 25		+ 25	mV
Temperature Resolution	T_{LSB}			0.125		°C
Temperature Error	T_{ERR}		- 3		+ 3	ºC
Current Sample Clock Frequency	f_{SAMP}			18.6		kHz
Timebase Accuracy	t_{ERR}	V_{DD} = 3.8V, T_A = +25°C			±1	%

				±2	
		-20°C ≤ T_A ≤ +70°C, 2.5V ≤ V_{DD} ≤ 5.5V		±3	
Input Resistance, VIN	R_{IN}		15		MΩ
Input Logic High: SCL, SDA	V_{IH}	(Note 1)	1.5		V
Input Logic Low: SCL, SDA	V_{IL}	(Note 1)		0.6	V
Output Logic Low: SDA, PIO	V_{OL}	I_{OL} = 4mA (Note 1)		0.4	V
Pulldown Current: SCL, SDA	I_{PD}		0.25		µA
Input Capacitance: SCL, SDA	C_{BUS}			50	pF
SLEEP Timeout	t_{SLEEP}	(Note 3)		2.2	S
Input Logic High: PIO	V_{IH}	(Note 1)	V_{DD} x 0.7		V
Input Logic Low: PIO	V_{IL}	(Note 1)		V_{DD} x 0.3	V

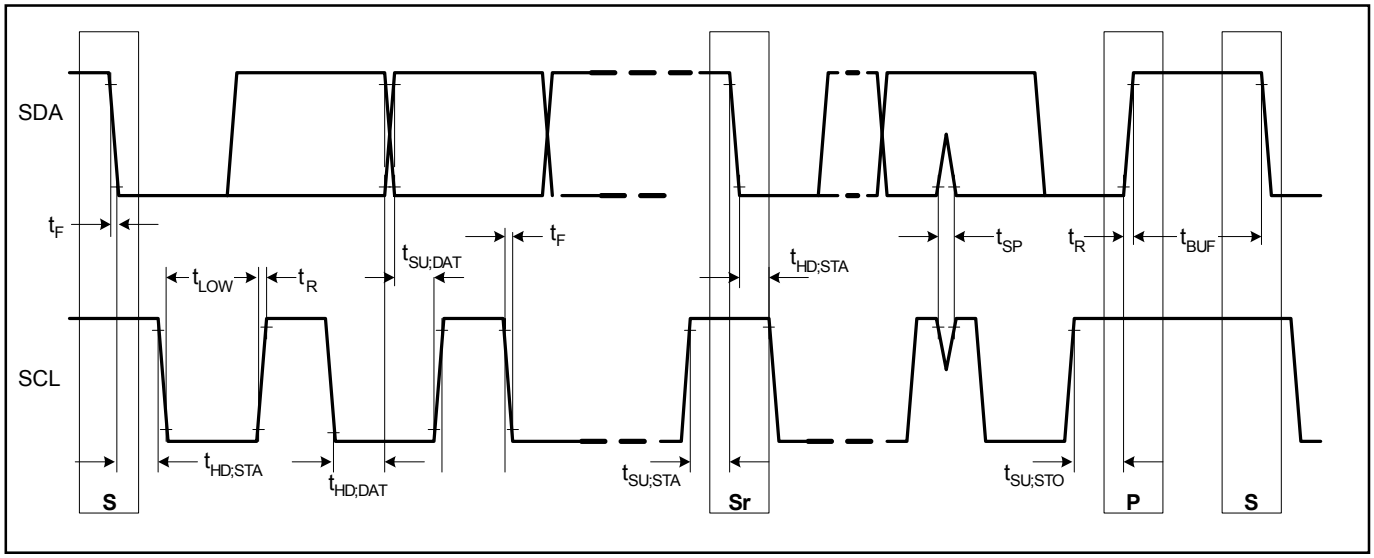
2-WIRE INTERFACE TIMING SPECIFICATIONS

(V_{DD} = 2.5V to 5.5V, T_A = -20°C to +70°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	(Note 6)	0		400	KHz
Bus Free Time Between a STOP and START Condition	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD:STA}$	(Note 7)	0.6			µs
Low Period of SCL Clock	t_{LOW}		1.3			µs
High Period of SCL Clock	t_{HIGH}		0.6			µs
Setup Time for a Repeated START Condition	$t_{SU:STA}$		0.6			µs
Data Hold Time	$t_{HD:DAT}$	(Note 8, 9)	0		0.9	µs
Data Setup Time	$t_{SU:DAT}$	(Note 8)	100			ns
Rise Time of Both SDA and SCL Signals	t_R		20 + 0.1C_B		300	ns
Fall Time of Both SDA and SCL Signals	t_F		20 + 0.1C_B		300	ns
Setup Time for STOP Condition	$t_{SU:STO}$		0.6			µs
Spike Pulse Widths Suppressed by Input Filter	t_{SP}	(Note 10)	0		50	ns
Capacitive Load for Each Bus Line	C_B	(Note 11)			400	pF
SCL, SDA Input Capacitance	C_{BIN}				60	pF

Note 1: All voltages are referenced to V_{SS}.
Note 2: Offset specified after auto-calibration cycle and Current Offset Bias register (COBR) set to 00h.
Note 3: To properly enter sleep mode, SMOD=1, and the application should hold SDA and SCL low for longer than the maximum t_{SLEEP}.
Note 4: NBEN = 0, Current Offset Bias Register (COBR) set to 00h, and Accumulation Bias Register (ABR) set to 00h.
Note 5: Parameters guaranteed by design.
Note 6: Timing must be fast enough to prevent the DS2745 from entering sleep mode due to SDA,SCL low for period > t_{SLEEP}.
Note 7: f_{SCL} must meet the minimum clock low time plus the rise/fall times.
Note 8: The maximum $t_{HD:DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
Note 9: This device internally provides a hold time of at least 300 ns for the SDA signal (referred to the VIHmin of the SCL signal) to bridge the undefined region of the falling edge of SCL.
Note 10: Filters on SDA and SCL suppress noise spikes at the input buffers and delay the sampling instant.
Note 11: C_B—total capacitance of one bus line in pF.
Note 12: The first voltage measurement after writing the ACR or after device POR is not valid.

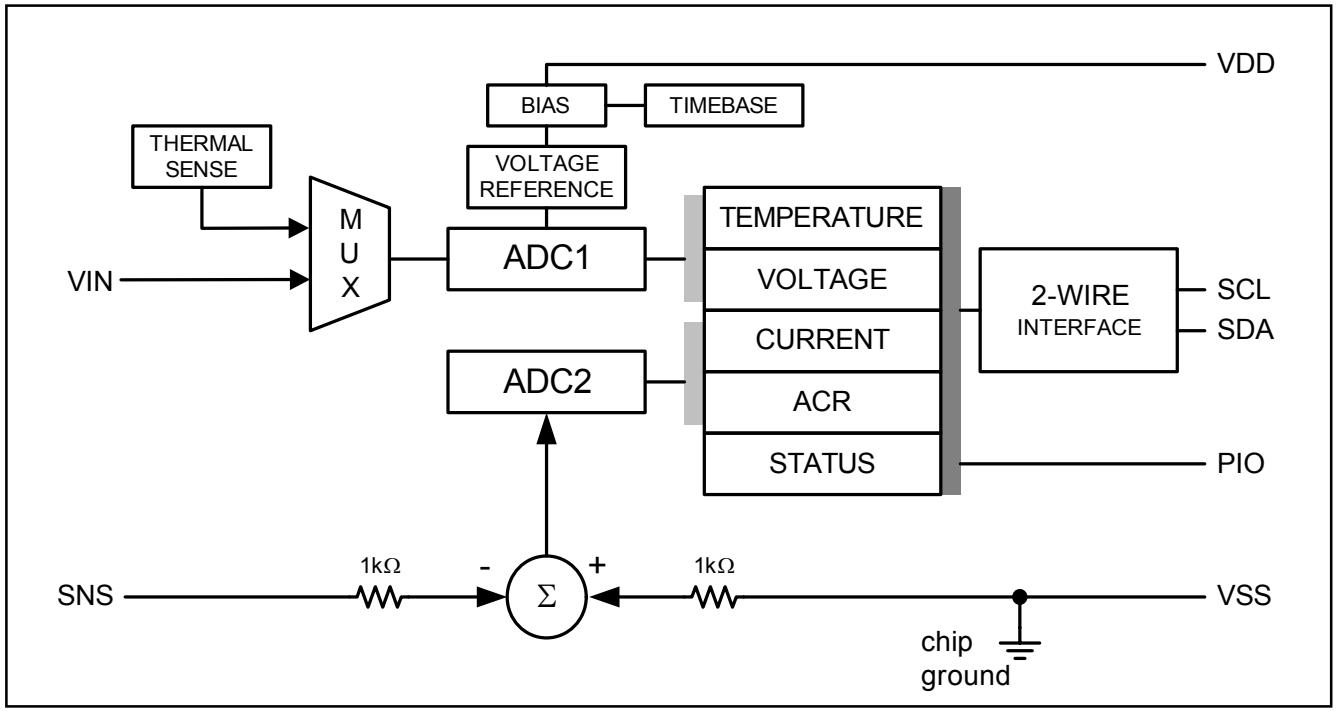
Figure 1. I²C Bus Timing Diagram



PIN DESCRIPTION

PIN	SYMBOL	FUNCTION
1	SCL	**Serial Clock Input.** 2-Wire clock line. Input only. Connect this pin to the CLOCK terminal of the battery pack. Pin has an internal pulldown (I_{PD}) for sensing disconnection.
2	SDA	**Serial Data Input/Output.** 2-Wire data line. Open-drain output driver. Connect this pin to the DATA terminal of the battery pack. Pin has an internal pulldown (I_{PD}) for sensing disconnection.
3	PIO	**General Purpose Input/Output.** Open-drain output driver with input sense. Connect to a pull up resistor for bidirectional operation.
4	SNS	**Sense Resistor Connection.** Connect to the negative terminal of the battery pack. Connect the sense resistor between V_{SS} and SNS.
5	V_{SS}	**Device Ground.** Connect to the negative terminal of the Li+ cell outside the cell protection FETs. Connect the sense resistor between V_{SS} and SNS.
6	CTG	**Connect to Ground.** Connect to the negative terminal of the Li+ cell outside the cell protection FETs.
7	VIN	**Voltage Sense Input.** The voltage of the Li+ cell is monitored through this input pin.
8	V_{DD}	**Power-Supply Input.** Connect to the positive terminal of the Li+ cell through a decoupling network.

Figure 2. BLOCK DIAGRAM



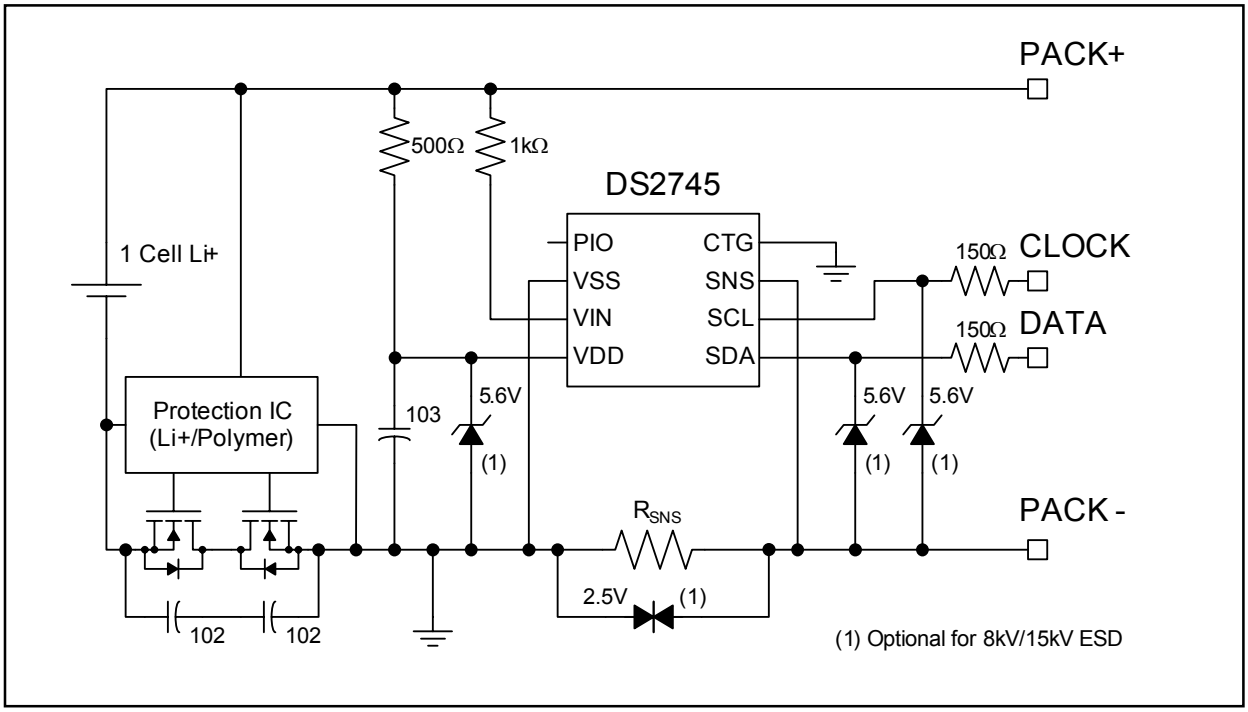
DETAILED DESCRIPTION

Current is measured bidirectionally over a dynamic range of ±51.2mV with a resolution of 1.56μV. Assuming a 15mΩ sense resistor, the current sense range is ±3.4A, with a 1 LSB resolution of 104μA. Current measurements are performed at regular intervals and accumulated with each measurement to support accurate "coulomb counting". Each current measurement is reported with sign and magnitude in the two-byte Current register. The Accumulated Current register (ACR) reports the coulomb count and supports a wide range of battery sizes. Battery voltage measurements are reported in the two-byte Voltage register with 11-bit (4.88mV) resolution, and Temperature is reported in the two-byte Temperature register with 0.125C resolution.

The DS2745 measurements can be used directly to provide accurate fuel gauging in typical use conditions, or along with FuelPack™ algorithms to form a complete and accurate solution for estimating remaining capacity over wide temperature and operating conditions.

Through its two wire I²C interface, the DS2745 allows a host system read/write access to the Status, Configuration and Measurement registers. Additionally, the I²C slave address can be changed from the default after power up.

Figure 3. APPLICATION EXAMPLE



FuelPack is a trademark of Dallas Semiconductor.

POWER MODES

The DS2745 operates in one of two power modes: active and sleep. While in active mode, the DS2745 operates as a high-precision battery monitor with voltage, temperature, current and accumulated current measurements acquired continuously and the resulting values updated in the measurement registers. Read and write access is allowed to all registers.

In sleep mode, the DS2745 operates in a low-power mode with no measurement activity. Serial access to current, accumulated current, and status/control registers is allowed in sleep mode if V_{DD} > 2V.

The DS2745 operating mode transitions from SLEEP to ACTIVE when:

SDA > V_{IH} OR SCL > V_{IH}

The DS2745 operating mode transitions from ACTIVE to SLEEP when:

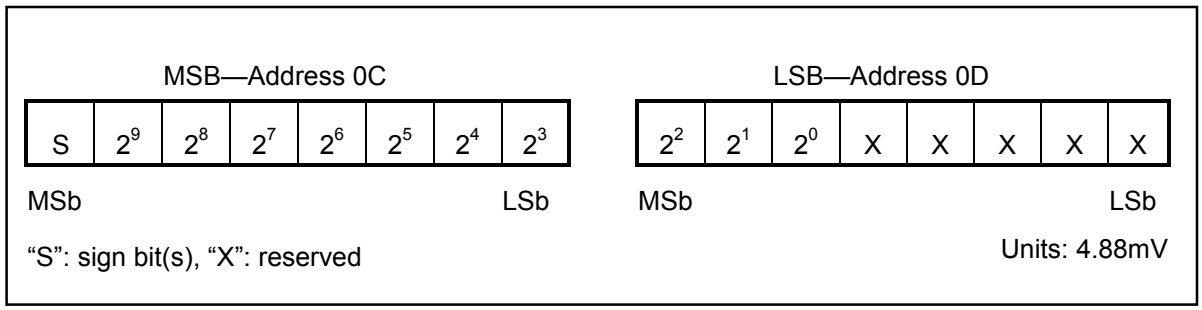
SMOD = 1 AND (SDA < VIL AND SCL < VIL) for t_{SLEEP}.

***CAUTION**: If SMOD = 1, pull-up resistors are required on SCL and/or SDA in order to ensure that the DS2745 transitions from SLEEP to ACTIVE mode when the battery is charged. If the bus is not pulled up, the DS2745 remains in SLEEP and cannot accumulate the charge current. This caution statement applies particularly to on a battery that is charged on a standalone charger.*

VOLTAGE MEASUREMENT

Battery voltage is measured at the VIN input with respect to VSS over a range of 0V to 4.992V and with a resolution of 4.88mV. The result is updated every 440ms and placed in the VOLTAGE register in two's compliment form. Voltages above the maximum register value are reported as 7FFFh.

Figure 4. VOLTAGE REGISTER FORMAT

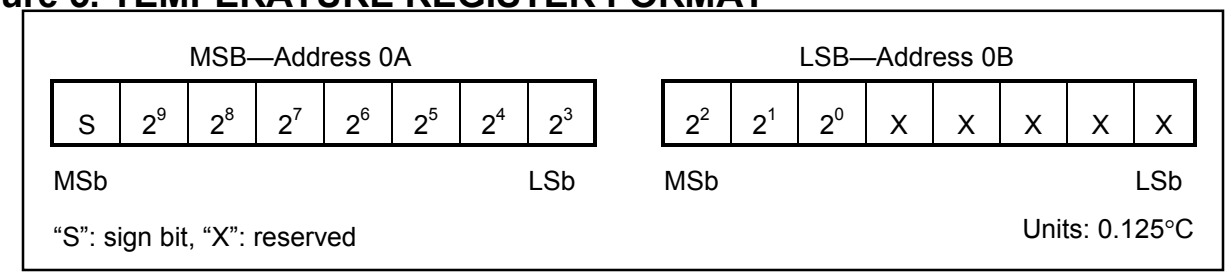


The input impedance of VIN is sufficiently large (>15MΩ) to be connected to a high impedance voltage divider in order to support multiple cell applications. The pack voltage should be divided by the number of series cells to present a single cell average voltage to the VIN input. Note that the first voltage measurement made after the DS2745 is powered or after the ACR register is written will not be valid. The host should wait one measurement cycle after either of these two conditions occur before reading voltage.

TEMPERATURE MEASUREMENT

The DS2745 uses an integrated temperature sensor to measure battery temperature with a resolution of 0.125°C. Temperature measurements are updated every 440ms and placed in the Temperature Register in two's complement form.

Figure 5. TEMPERATURE REGISTER FORMAT



CURRENT MEASUREMENT

In the active mode of operation, the DS2745 continually measures the current flow into and out of the battery by measuring the voltage drop across a low-value current-sense resistor, R_{SNS}, connected between the SNS and VSS pins. The voltage sense range between SNS and VSS is ±51.2mV. Note that positive current values occur when V_{SNS} is less than V_{SS}, and negative current values occur when V_{SNS} is greater than V_{SS}. Peak signal amplitudes up to 102mV are allowed at the input as long as the continuous or average signal level does not exceed ±51.2mV over the conversion cycle period. The ADC samples the input differentially at with an 18.6kHz sample clock and updates the current register at the completion of each conversion cycle. Figure 6 describes the current measurement register format and resolution. Charge currents above the maximum register value are reported at the maximum value (7FFFh = +51.2mV). Discharge currents below the minimum register value are reported at the minimum value (8000h = -51.2mV).

Figure 6. CURRENT REGISTER FORMATS

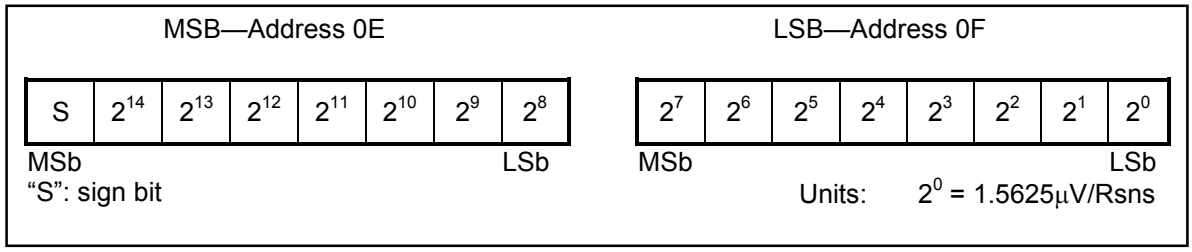


Table 2. CURRENT RESOLUTION FOR VARIOUS RSNS VALUES

CONVERSION TIME	CURRENT RESOLUTION (1 LSB)				
	$\lvert V_{SS} - V_{SNS} \rvert$	R_{SNS}			
		20mΩ	15mΩ	10mΩ	5mΩ
3.5s	1.5625µV	78.13µA	104.2µA	156.3µA	312.5µA

Table 3. CURRENT RANGE FOR VARIOUS RSNS VALUES

CURRENT INPUT RANGE				
$V_{SS} - V_{SNS}$	R_{SNS}			
	20mΩ	15mΩ	10mΩ	5mΩ
±51.2mV	±2.56A	±3.41A	±5.12A	±10.24A

Every 1024th conversion, the ADC measures its input offset to facilitate offset correction. Offset correction occurs approximately once per hour. The resulting correction factor is applied to the subsequent 1023 measurements. During the offset correction conversion, the ADC does not measure the SNS to VSS signal. A maximum error of 1/1024 in the accumulated current register (ACR) is possible, however, to reduce the error, the current measurement just prior to the offset conversion is displayed in the current register and is substituted for the dropped current measurement in the current accumulation process. The error due to offset correction is typically much less than 1/1024.

CURRENT ACCUMULATION

The Accumulated Current register (ACR) serves as an up/down counter holding a running count of charge stored in the battery. Current measurement results, plus a programmable bias value are internally summed, or accumulated, at the completion of each current measurement conversion period with the results displayed in the ACR. The ACR has a range of 0mVh to +409.6mVh with an LSb of 6.25µVh. Additional registers hold fractional results of each accumulation, however, these bits are not user accessible. The ACR count clamps at FFFFh when accumulating charge values and at 0000h when accumulating discharge values.

Read and write access is allowed to the ACR. Whenever the ACR is written, fractional accumulation results are cleared. A write to the ACR also forces the ADC to measure its offset and update the offset correction factor. Current measurement and accumulation resume (using the new offset correction) with the second conversion following the write to the ACR. Figure 7 describes the ACR address, format, and resolution.

Figure 7. ACCUMULATED CURRENT REGISTER FORMAT

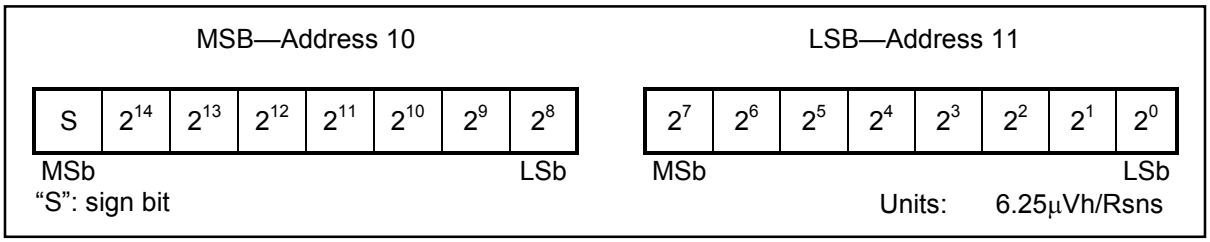


Table 4. ACCUMULATED CURRENT RANGE FOR VARIOUS RSNS VALUES

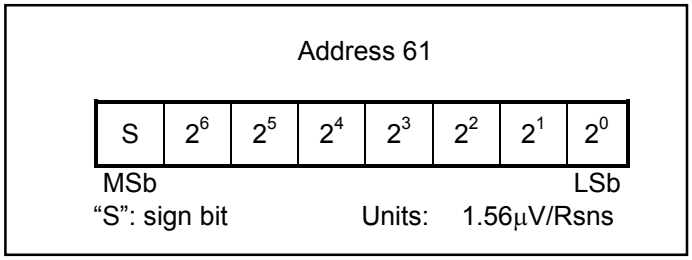
ACR RANGE				
V_{SS} - V_{SNS}	R_{SNS}			
	20mµ	15mµ	10mΩ	5mΩ
409.6mVh	20.48Ah	27.31Ah	40.96Ah	81.92Ah

CURRENT OFFSET BIAS

The Current Offset Bias register (COBR) allows a programmable offset value to be added to raw current measurements. The result of the raw current measurement plus the COBR value is displayed as the current measurement result in the CURRENT register, and is used for current accumulation. The COBR value can be used to correct for a static offset error, or can be used to intentionally skew the current results and therefore the current accumulation.

Read and write access is allowed to COBR. Whenever the COBR is written, the new value is applied to all subsequent current measurements. COBR can be programmed in 1.56µV steps to any value between +198.1µV and -199.7µV. The COBR value is stored as a two's complement value in volatile memory, and must be initialized via the interface on power-up. Figure 8 describes the COBR address, format, and resolution.

Figure 8. CURRENT OFFSET BIAS REGISTER FORMAT



CURRENT BLANKING

The Current Blanking feature modifies current measurement result prior to being accumulated in the ACR. Current Blanking occurs conditionally when a current measurement (raw current + COBR) falls in one of two defined ranges. The first range prevents charge currents less than 100μV from being accumulated. The second range prevents discharge currents less than 25μV in magnitude from being accumulated. Charge current blanking is always performed, however, discharge current blanking must be enabled by setting the NBEN bit in the Status/Config register. See the register description for additional information.

ACCUMULATION BIAS

The Accumulation Bias register (ABR) allows a programmable offset value to be added to the current accumulation process. The new ACR value results from the addition of the Current register value plus ABR plus the previous ACR value. ABR can be used to intentionally skew the current accumulation to estimate system stand-by currents that are too small to measure. ABR value is not subject to the Current Blanking thresholds.

Read and write access is allowed to the ABR. Whenever the ABR is written, the new value is applied to all subsequent current measurements. ABR can be set to any value between +198.1μV and -199.7μV in 1.56μV steps. The ABR value is stored as a two's complement value in volatile memory, and must be initialized via the interface on power-up. Figure 9 describes the ABR address, format, and resolution.

Figure 9. ACCUMULATION BIAS REGISTER FORMAT

Address 62

S	2^6	2^5	2^4	2^3	2^2	2^1	2^0

MSb LSb

"S": sign bit Units: 1.56μV/Rsns

MEMORY

The DS2745 has memory space with registers for instrumentation, status, and control. When the MSB of a two-byte register is read, both the MSB and LSB are latched and held for the duration of the read data command to prevent updates during the read and ensure synchronization between the two register bytes. For consistent results, always read the MSB and the LSB of a two-byte register during the same read data command sequence.

Table 5. MEMORY MAP

ADDRESS (HEX)	DESCRIPTION	READ/WRITE	POR DEFAULT
00	Reserved	—	
01	Status/Config Register	R/W	11000000b
02 to 08	Reserved	—	
09 to 0D	Reserved	—	
0A	Temperature Register MSB	R	
0B	Temperature Register LSB	R	
0C	Voltage Register MSB	R	
0D	Voltage Register LSB	R	
0E	Current Register MSB	R	
0F	Current Register LSB	R	
10	Accumulated Current Register MSB	R/W	No Change
11	Accumulated Current Register LSB	R/W	No Change
12 to 61	Reserved	—	
61	Offset Bias Register	R/W	00h
62	Accumulation Bias Register	R/W	00h
63 to FF	Reserved	—	

STATUS/CONFIG REGISTER

The Status/Config register is read/write with individual bits designated as read only. Bit values indicate status as well as program or select device functionality.

Figure 10. STATUS/CONFIG REGISTER FORMAT

ADDRESS 01

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
X	PORF	SMOD	NBEN	PIO	A2	A1	A0

X — Reserved.

PORF — The Power-On-Reset Flag is set to indicate initial power-up. PORF is not cleared internally. The user must write this flag value to a 0 in order to use it to indicate subsequent power-up events. If PORF indicates a power-on-reset, the ACR could be misaligned with the actual battery state of charge. The system can request a charge to full in order to synchronize the ACR with the battery charge state. PORF is read/write-to-zero.

SMOD — SLEEP Mode Enable. A value of 1 allows the DS2745 to enter sleep mode when both SDA and SCL pins is low for 2s. A value of 0 disables the transition to sleep mode. The power-up default of SMOD = 0.

NBEN — Negative Blanking Enable. A value of 1 enables blanking of negative current values up to 25μV. A value of 0 disables blanking of negative currents. The power-up default of NBEN = 0.

PIO — Programmable Input/Output. PIO provides both control of the PIO open-drain output driver and readback of the PIO pin logic level. Writing a 0 to PIO drives PIO pin low. Writing a 1 deactivates the PIO output and allows readback of an external signal. Reading PIO returns the logic state on the pin. PIO is RESET on POR.

A2:A0 — I²C Slave Address bits. A2:A0 set the lower 3 bits of the I²C slave address. When modified from the power-up default slave address of **1001000b**, accessing the DS2745 requires the modified slave address following a start or repeated start.

2-WIRE BUS SYSTEM

The 2-Wire bus system supports operation as a slave only device in a single or multi-slave, and single or multi-master system. Up to 128 slave devices may share the bus by uniquely setting the 7-bit slave address. The 2-wire interface consists of a serial data line (SDA) and serial clock line (SCL). SDA and SCL provide bidirectional communication between the DS2745 slave device and a master device at speeds up to 400kHz. The DS2745's SDA pin operates bidirectionally, that is, when the DS2745 receives data, SDA operates as an input, and when the DS2745 returns data, SDA operates as an open-drain output, with the host system providing a resistive pull-up. The DS2745 always operates as a slave device, receiving and transmitting data under the control of a master device. The master initiates all transactions on the bus and generates the SCL signal as well as the START and STOP bits which begin and end each transaction.

Bit Transfer

One data bit is transferred during each SCL clock cycle, with the cycle defined by SCL transitioning low-to-high and then high-to-low. The SDA logic level must remain stable during the high period of the SCL clock pulse. Any change in SDA when SCL is high is interpreted as a START or STOP control signal.

Bus Idle

The bus is defined to be idle, or not busy, when no master device has control. Both SDA and SCL remain high when the bus is idle. The STOP condition is the proper method to return the bus to the idle state.

START and STOP Conditions

The master initiates transactions with a START condition (S), by forcing a high-to-low transition on SDA while SCL is high. The master terminates a transaction with a STOP condition (P), a low-to-high transition on SDA while SCL is high. A Repeated START condition (Sr) can be used in place of a STOP then START sequence to terminate one transaction and begin another without returning the bus to the idle state. In multimaster systems, a Repeated START allows the master to retain control of the bus. The START and STOP conditions are the only bus activities in which the SDA transitions when SCL is high.

Acknowledge Bits

Each byte of a data transfer is acknowledged with an Acknowledge bit (A) or a No Acknowledge bit (N). Both the master and the DS2745 slave generate acknowledge bits. To generate an Acknowledge, the receiving device must pull SDA low before the rising edge of the acknowledge-related clock pulse (ninth pulse) and keep it low until SCL returns low. To generate a No Acknowledge (also called NAK), the receiver releases SDA before the rising edge of the acknowledge-related clock pulse and leaves SDA high until SCL returns low. Monitoring the acknowledge bits allows for detection of unsuccessful data transfers. An unsuccessful data transfer can occur if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master should re-attempt communication.

Data Order

A byte of data consists of 8 bits ordered most significant bit (msb) first. The least significant bit (lsb) of each byte is followed by the Acknowledge bit. DS2745 registers composed of multi-byte values are ordered most significant byte (MSB) first. The MSB of multi-byte registers is stored on even data memory addresses.

Slave Address

A bus master initiates communication with a slave device by issuing a START condition followed by a Slave Address (SAddr) and the read/write (R/W) bit. When the bus is idle, the DS2745 continuously monitors for a START condition followed by its slave address. When the DS2745 receives a slave address that matches the value in its Status/Config register, it responds with an Acknowledge bit during the clock period following the R/W bit. The default Slave Address at power-up is 1001000. The lower three bits of the slave address can be re-programmed, refer to the Status/Config register description for details.

Read/Write Bit

The R/W bit following the slave address determines the data direction of subsequent bytes in the transfer. R/W = 0 selects a write transaction, with the following bytes being written by the master to the slave. R/W = 1 selects a read transaction, with the following bytes being read from the stave by the master.

Bus Timing

The DS2745 is compatible with any bus timing up to 400kHz. No special configuration is required to operate at any speed.

2-Wire Command Protocols

The command protocols involve several transaction formats. The simplest format consists of the master writing the START bit, slave address, R/W bit, and then monitoring the acknowledge bit for presence of the DS2745. More complex formats such as the Write Data, Read Data and Function command protocols write data, read data and execute device specific operations. All bytes in each command format require the slave or host to return an Acknowledge bit before continuing with the next byte. Each function command definition outlines the required transaction format. The following key applies to the transaction formats.

Table 3. 2-Wire Protocol Key

KEY	DESCRIPTION	KEY	DESCRIPTION
S	START bit	Sr	Repeated START
SAddr	Slave Address (7-bit)	W	R/W bit = 0
FCmd	Function Command byte	R	R/W bit = 1
MAddr	Memory Address byte	P	STOP bit
Data	Data byte written by master	Data	Data byte returned by slave
A	Acknowledge bit - Master	A	Acknowledge bit—Slave
N	No Acknowledge - Master	N	No Acknowledge—Slave

Basic Transaction Formats

Write: S SAddr W A MAddr A Data0 A P

A write transaction transfers one or more data bytes *to* the DS2745. The data transfer begins at the memory address supplied in the MAddr byte. Control of the SDA signal is retained by the master throughout the transaction, except for the Acknowledge cycles.

Read: S SAddr W A MAddr A Sr SAddr R A Data0 N P



Write Portion Read Portion

A read transaction transfers one or more bytes *from* the DS2745. Read transactions are composed of two parts, a write portion followed by a read portion, and is therefore inherently longer than a write transaction. The write portion communicates the starting point for the read operation. The read portion follows immediately, beginning with a Repeated START, Slave Address with R/W set to a 1. Control of SDA is assumed by the DS2745 beginning with the Slave Address Acknowledge cycle. Control of the SDA signal is retained by the DS2745 throughout the transaction, except for the Acknowledge cycles. The master indicates the end of a read transaction by responding to the last byte it requires with a No Acknowledge. This signals the DS2745 that control of SDA is to remain with the master following the Acknowledge clock.

Write Data Protocol

The write data protocol is used to write to register and shadow RAM data to the DS2745 starting at memory address MAddr. Data0 represents the data written to MAddr, Data1 represents the data written to MAddr + 1 and DataN represents the last data byte, written to MAddr + N. The master indicates the end of a write transaction by sending a STOP or Repeated START after receiving the last acknowledge bit.

S SAddr W A MAddr A Data0 A Data1 A … DataN A P

The msb of the data to be stored at address MAddr can be written immediately after the MAddr byte is acknowledged. Because the address is automatically incremented after the least significant bit (lsb) of each byte is received by the DS2745, the msb of the data at address MAddr + 1 is can be written immediately after the acknowledgement of the data at address MAddr. If the bus master continues an auto-incremented write transaction beyond address FFh, the DS2745 ignores the data. Data is also ignored on writes to read-only addresses and reserved addresses. Incomplete bytes and bytes that are Not Acknowledged by the DS2745 are not written to memory.

Read Data Protocol

The Read Data protocol is used to read register and shadow RAM data from the DS2745 starting at memory address specified by MAddr. Data0 represents the data byte in memory location MAddr, Data1 represents the data from MAddr + 1 and DataN represents the last byte read by the master.

S SAddr W A MAddr A Sr SAddr R A Data0 A Data1 A … DataN N P

Data is returned beginning with the most significant bit (msb) of the data in MAddr. Because the address is automatically incremented after the least significant bit (lsb) of each byte is returned, the msb of the data at address MAddr + 1 is available to the host immediately after the acknowledgement of the data at address MAddr. If the bus master continues to read beyond address FFh, the DS2745 outputs data values of FFh. Addresses labeled “Reserved” in the memory map return undefined data. The bus master terminates the read transaction at any byte boundary by issuing a No Acknowledge followed by a STOP or Repeated START.

Package Information

For the latest package outline information, go to **www.maxim-ic.com/DallasPackInfo**.