

# PESD5V0F1BRLD

## Femtofarad bidirectional ESD protection diode

Rev. 1 — 30 January 2014 Product data sheet

## 1. Product profile

### 1.1 General description

Femtofarad bidirectional ElectroStatic Discharge (ESD) protection diode designed to protect one signal line from the damage caused by ESD and other transients. The device is encapsulated in a leadless ultra small DFN1006D-2 (SOD882D) Surface-Mounted Device (SMD) plastic package with visible and solderable side pads.

The combination of extremely low capacitance, high ESD maximum rating and ultra small package makes the device ideal for high-speed data line protection and antenna protection applications.

### 1.2 Features and benefits

- Bidirectional ESD protection of one line
- Femtofarad capacitance: $C_d$ = 400 fF
- Low ESD clamping voltage: 30 V at 30 ns and ±8 kV
- Very low leakage current: $I_{RM}$ < 1 nA
- ESD protection up to 10 kV (contact) and 15 kV (air)
- IEC 61000-4-2; level 4 (ESD)
- Package height typ. 0.37 mm
- AEC-Q101 qualified

### 1.3 Applications

- 10/100/1000 Mbit/s Ethernet
- FireWire
- High-speed data lines
- SIM card protection
- Cellular handsets and accessories
- Portable electronics
- Communication systems
- Computers and peripherals
- Audio and video equipment
- Antenna protection

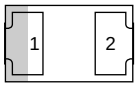
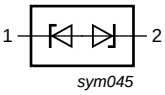
### 1.4 Quick reference data

Table 1. Quick reference data

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Per device** | | | | | | |
| $V_{RWM}$ | reverse standoff voltage | | - | - | 5.5 | V |
| $C_d$ | diode capacitance | f = 1 MHz; $V_R$ = 0 V | - | 0.4 | 0.55 | pF |

## 2. Pinning information

**Table 2. Pinning**

| Pin | Description | Simplified outline | Graphic symbol |
|---|---|---|---|
| 1 | cathode (diode 1) |   Transparent top view |   |
| 2 | cathode (diode 2) | | |

## 3. Ordering information

**Table 3. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| PESD5V0F1BRLD | DFN1006D-2 | leadless ultra small plastic package; 2 terminals; body 1 × 0.6 × 0.4 mm | SOD882D |

## 4. Marking

**Table 4. Marking codes**

| Type number | Marking code |
|---|---|
| PESD5V0F1BRLD | H |

## 5. Limiting values

**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| **Per device** | | | | | | |
| $I_{PPM}$ | rated peak pulse current | $t_p$ = 8/20 μs | [1] | - | 2.5 | A |
| $T_j$ | junction temperature | | | - | +125 | °C |
| $T_{amb}$ | ambient temperature | | | −40 | +125 | °C |
| $T_{stg}$ | storage temperature | | | −55 | +125 | °C |

[1] Device stressed with ten non-repetitive current pulses (8/20 μs exponential decay waveform according to IEC 61000-4-5 and IEC 61643-321).


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**Table 6. ESD maximum ratings**

*$T_{amb}$ = 25 °C unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| **Per device** | | | | | | |
| $V_{ESD}$ | electrostatic discharge voltage | IEC 61000-4-2 (contact discharge) | [1] | - | 10 | kV |
| | | IEC 61000-4-2 (air discharge) | [1] | - | 15 | kV |
| | | MIL-STD-883 (human body model) | | - | 10 | kV |

[1] Device stressed with ten non-repetitive ESD pulses.

**Table 7. ESD standards compliance**

| Standard | Conditions |
|---|---|
| **Per device** | |
| IEC 61000-4-2; level 4 (ESD) | > 15 kV (air); > 8 kV (contact) |
| MIL-STD-883; class 3B (human body model) | > 8 kV |

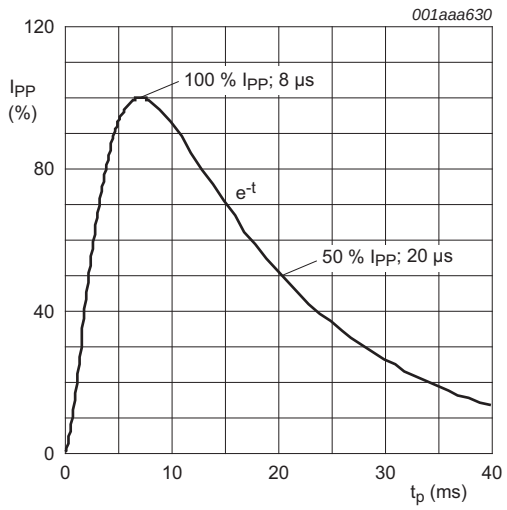



**Fig 1. 8/20 µs pulse waveform according to IEC 61000-4-5 and IEC 61643-321**

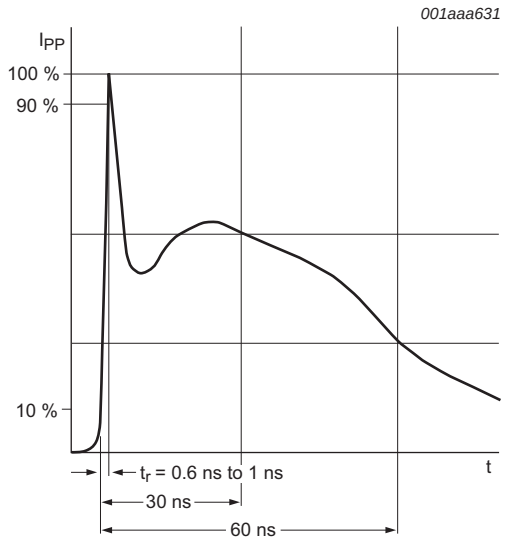



**Fig 2. ESD pulse waveform according to IEC 61000-4-2**


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# 6. Characteristics

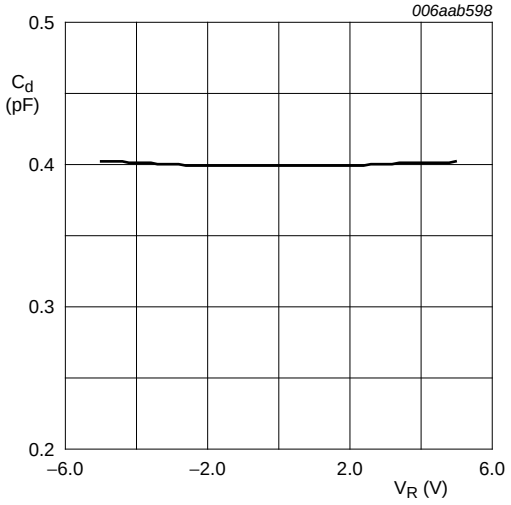
**Table 8. Characteristics**

*$T_{amb}$ = 25 °C unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Per device** | | | | | | | |
| $V_{RWM}$ | reverse standoff voltage | | | - | - | 5.5 | V |
| $I_{RM}$ | reverse leakage current | $V_{RWM}$ = 5 V | | - | 1 | 100 | nA |
| $V_{BR}$ | breakdown voltage | $I_R$ = 1 mA | | 6 | 8 | 10 | V |
| $C_d$ | diode capacitance | f = 1 MHz; $V_R$ = 0 V | | - | 0.4 | 0.55 | pF |
| $V_{CL}$ | clamping voltage | $I_{PP}$ = 1 A | [1] | - | - | 11 | V |
| | | $I_{PPM}$ = 2.5 A | [1] | - | - | 15 | V |
| $r_{dyn}$ | dynamic resistance | $I_R$ = 10 A | [2] | - | 1.5 | - | Ω |

[1] Device stressed with 8/20 μs exponential decay waveform according to IEC 61000-4-5 and IEC 61643-321.

[2] Non-repetitive current pulse, Transmission Line Pulse (TLP) $t_p$ = 100 ns; square pulse; ANSI/ESD STM5.5.1-2008.




f = 1 MHz; $T_{amb}$ = 25 °C

**Fig 3. Diode capacitance as a function of reverse voltage; typical values**

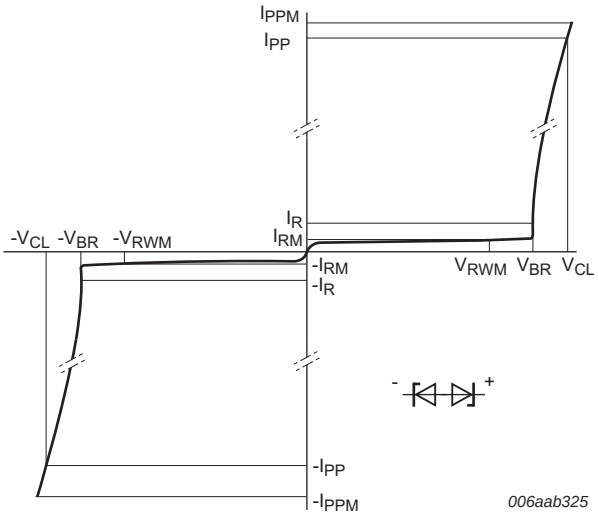



**Fig 4. V-I characteristics for a bidirectional ESD protection diode**


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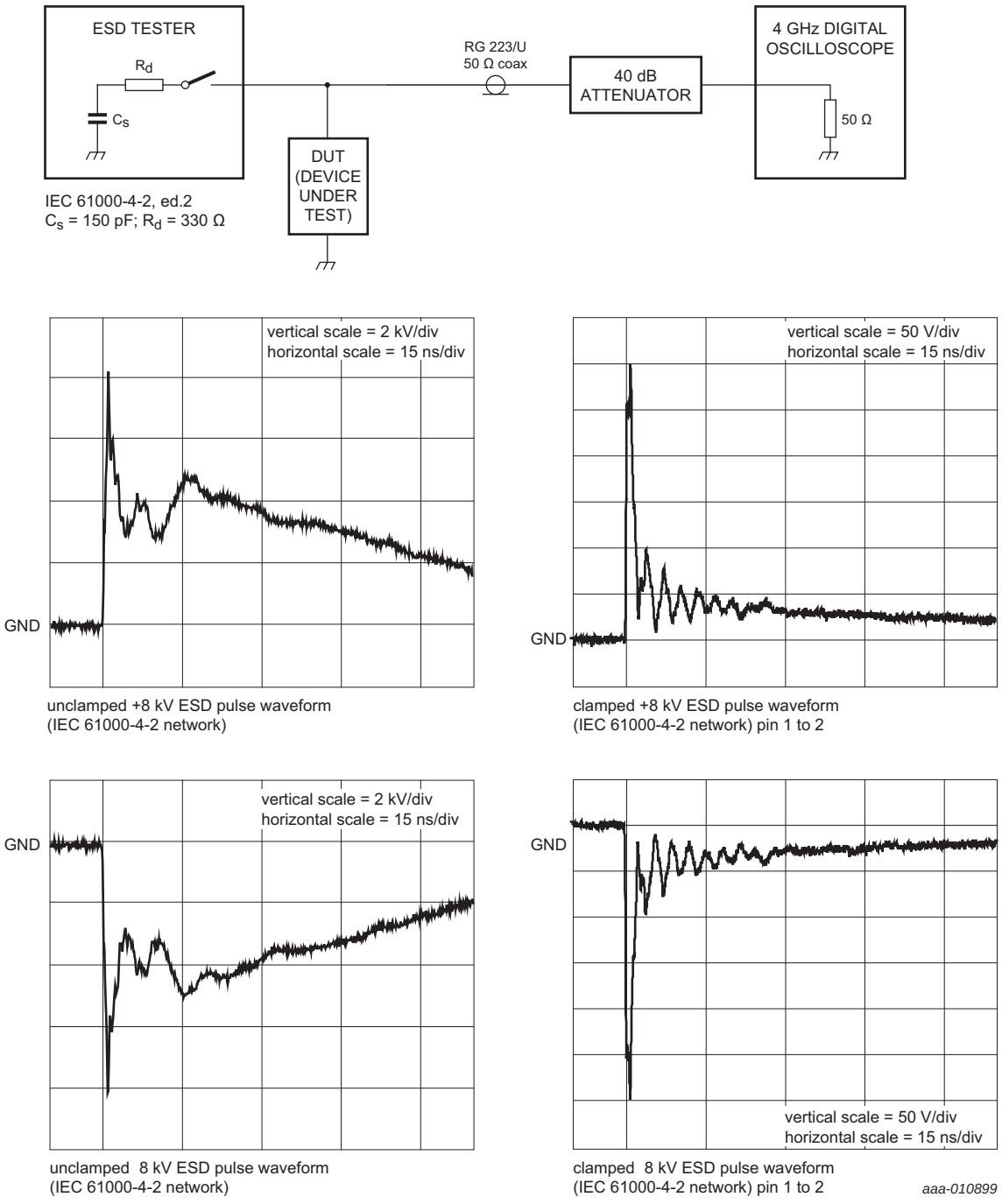



**Fig 5. ESD clamping test setup and waveforms**


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# 7. Application information

The device is designed for the protection of one bidirectional data or signal line from surge pulses and ESD damage. The device is suitable on lines where the signal polarities are both, positive and negative with respect to ground.

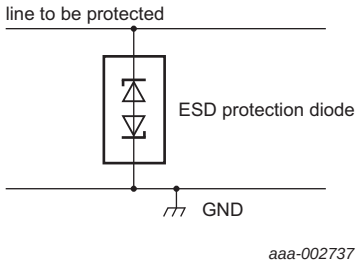



**Fig 6. Application diagram**

**Circuit board layout and protection device placement**

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the device as close to the input terminal or connector as possible.
2. Minimize the path length between the device and the protected line.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

# 8. Test information

## 8.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q101 - Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.


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## 9. Package outline

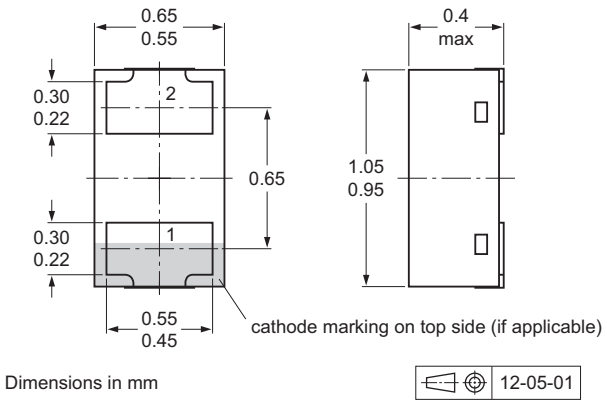



**Fig 7. Package outline DFN1006D-2 (SOD882D)**

## 10. Soldering

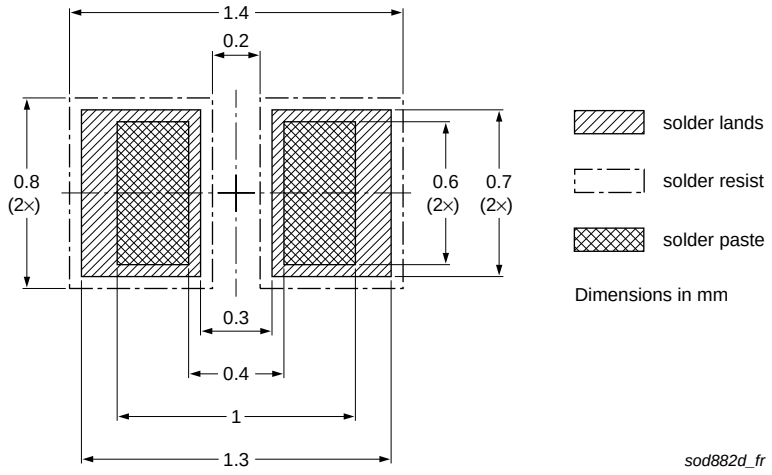



**Fig 8. Reflow soldering footprint DFN1006D-2 (SOD882D)**


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## 11. Revision history

**Table 9. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| PESD5V0F1BRLD v.1 | 20140130 | Product data sheet | - | - |


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| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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