BUK9E2R4-40C

N-channel TrenchMOS logic level FET

Rev. 01 — 11 April 2008 **Product data sheet**

1. Product profile

1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

1.2 Features and benefits

- Low conduction losses due to low on-state resistance
- Suitable for logic level gate drive sources
- Q101 compliant
- Suitable for thermally demanding environments due to 175 °C rating

1.3 Applications

- 12 V loads
- General purpose power switching
- Automotive systems
- Motors, lamps and solenoids

1.4 Quick reference data

Table 1. Quick reference

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C		-	-	40	V
I_D	drain current	V_{GS} = 5 V; T_j = 25 °C; see Figure 1 and 4	[1][2]	-	-	100	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; see Figure 2		-	-	333	W
Avalanche ruggedness							
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 100 A; $V_{sup} \leq 40$ V; R_{GS} = 50 Ω; V_{GS} = 5 V; $T_{j(init)}$ = 25 °C; unclamped		-	-	1.2	J
Dynamic characteristics							
Q_{GD}	gate-drain charge	V_{GS} = 5 V; I_D = 25 A; V_{DS} = 32 V; see Figure 14		-	73	-	nC
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 5 V; I_D = 25 A; T_j = 25 °C; see Figure 12, 11 and 13		-	2.1	2.4	mΩ

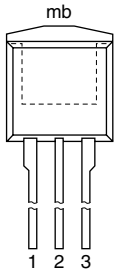
[1] Continuous current is limited by package.

[2] Refer to document 9397 750 12572 for further information.

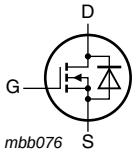
2. Pinning information

Table 2. Pinning

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		



SOT226 (I2-PAK)



3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK9E2R4-40C	I2PAK	plastic single-ended package (I2PAK); low-profile 3-lead TO-220AB	SOT226

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C		-	40	V
V_{DGR}	drain-gate voltage	R_{GS} = 20 kΩ		-	40	V
V_{GS}	gate-source voltage			-15	15	V
I_D	drain current	T_{mb} = 25 °C; V_{GS} = 5 V; see Figure 1	[1]	-	270	A
		V_{GS} = 5 V; T_j = 100 °C; see Figure 1	[2][3]	-	100	A
		V_{GS} = 5 V; T_j = 25 °C; see Figure 1 and 4	[2][3]	-	100	A
I_{DM}	peak drain current	T_{mb} = 25 °C; $t_p \leq 10$ µs; pulsed; see Figure 4		-	1080	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; see Figure 2		-	333	W
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 100 A; $V_{sup} \leq 40$ V; R_{GS} = 50 Ω; V_{GS} = 5 V; $T_{j(init)}$ = 25 °C; unclamped		-	1.2	J
$E_{DS(AL)R}$	repetitive drain-source avalanche energy	see Figure 3	[4][5][6]	-	-	J
Source-drain diode						
I_S	source current	T_{mb} = 25 °C	[2][3]	-	100	A
I_{SM}	peak source current	$t_p \leq 10$ µs; pulsed; T_{mb} = 25 °C		-	1080	A

[1] Current is limited by chip power dissipation rating.

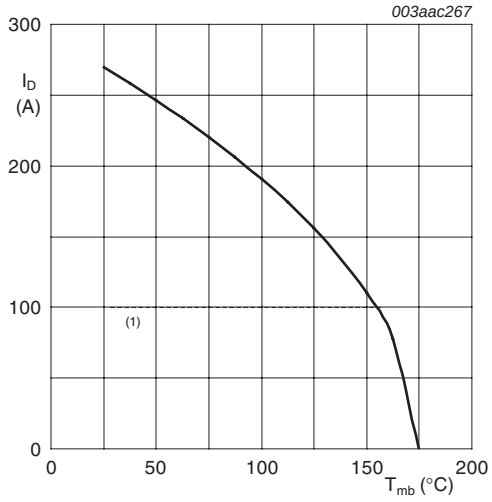
[2] Continuous current is limited by package.

[3] Refer to document 9397 750 12572 for further information.

[4] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.

[5] Repetitive avalanche rating limited by an average junction temperature of 170 °C.

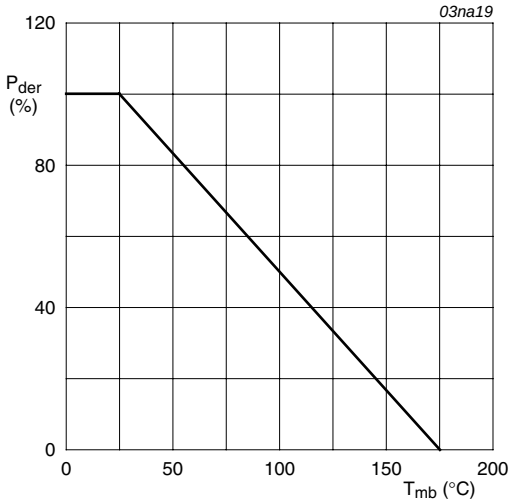
[6] Refer to application note AN10273 for further information.



$V_{GS} \geq 5V$

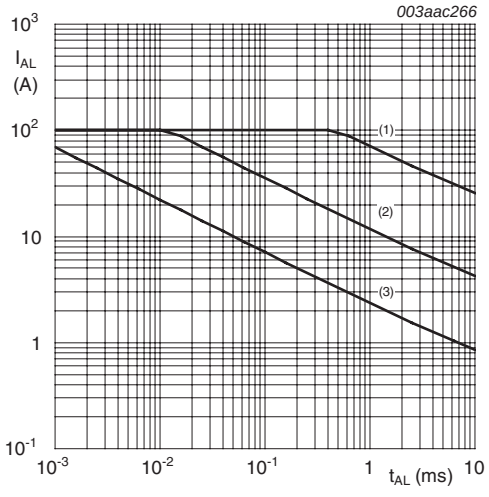
(1) Capped at 100 A due to package.

Fig 1. Continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\ \%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature

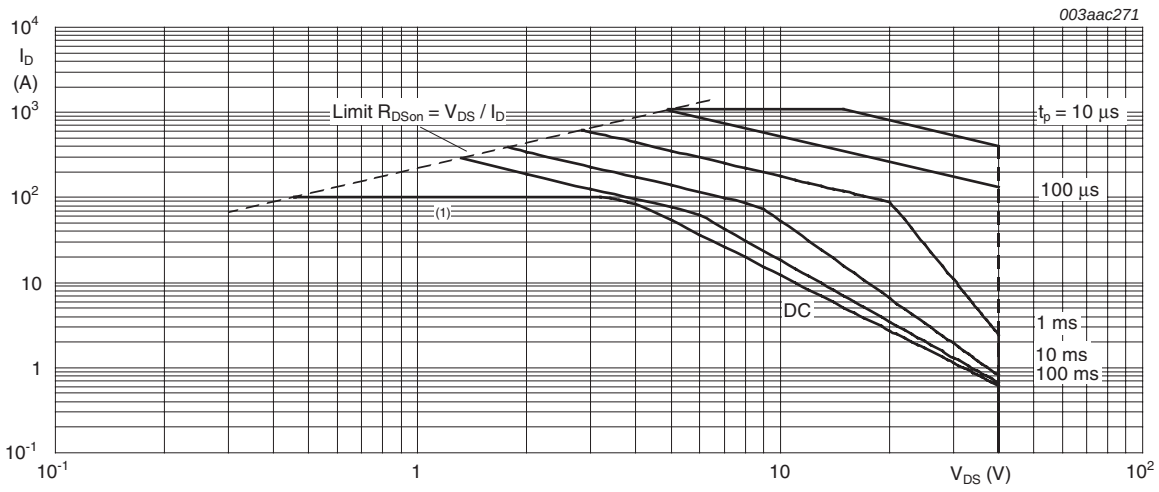


(1) Single−pulse; T_j = 25 °C.

(2) Single−pulse; T_j = 150 °C.

(3) Repetitive.

Fig 3. Single-pulse and repetitive avalanche rating; avalanche current as a function of avalanche time



T_{mb} = 25 °C; I_{DM} is single pulse

(1) Capped at 100 A due to package.

Fig 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	vertical in free air	-	60	-	K/W
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 5	-	-	0.45	K/W

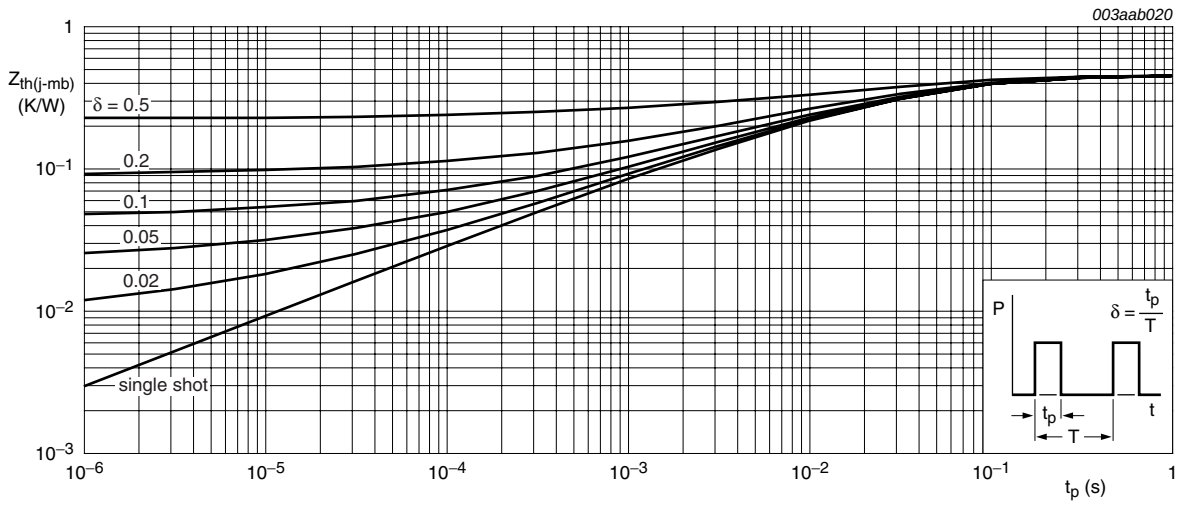


Fig 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

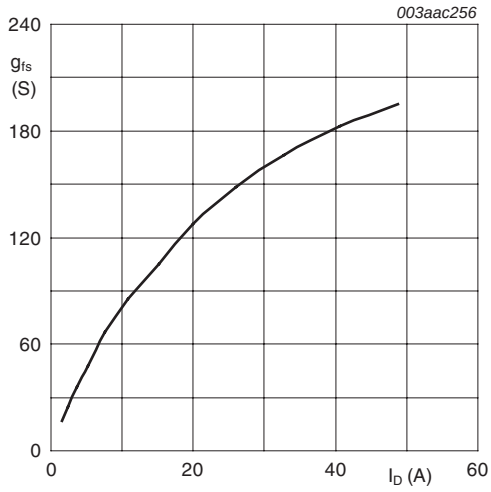
6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 μA; V_{GS} = 0 V; T_j = 25 °C	40	-	-	V
		I_D = 250 μA; V_{GS} = 0 V; T_j = -55 °C	36	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 °C; see Figure 9 and 10	1	1.5	2	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = -55 °C; see Figure 9	-	-	2.3	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = 175 °C; see Figure 9	0.5	-	-	V
I_{DSS}	drain leakage current	V_{DS} = 40 V; V_{GS} = 0 V; T_j = 175 °C	-	-	500	μA
		V_{DS} = 40 V; V_{GS} = 0 V; T_j = 25 °C	-	0.02	1	μA

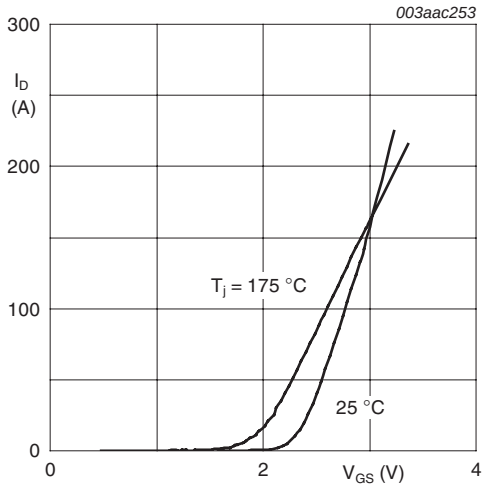
Table 6. Characteristics *…continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{GSS}	gate leakage current	V_{DS} = 0 V; V_{GS} = 15 V; T_j = 25 °C	-	2	100	nA
		V_{DS} = 0 V; V_{GS} = -15 V; T_j = 25 °C	-	2	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 25 A; T_j = 25 °C	-	-	2.7	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C	-	1.8	2.1	mΩ
		V_{GS} = 5 V; I_D = 25 A; T_j = 175 °C; see Figure 11	-	-	4.6	mΩ
		V_{GS} = 5 V; I_D = 25 A; T_j = 25 °C; see Figure 12, 11 and 13	-	2.1	2.4	mΩ
Source-drain diode						
V_{SD}	source-drain voltage	I_S = 25 A; V_{GS} = 0 V; T_j = 25 °C; see Figure 16	-	0.85	1.2	V
t_{rr}	reverse recovery time	I_S = 25 A; dI_S/dt = 100 A/μs; V_{GS} = 0 V; V_{DS} = 30 V	-	70	-	ns
Q_r	recovered charge		-	60	-	nC
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	I_D = 25 A; V_{DS} = 32 V; V_{GS} = 5 V; see Figure 14	-	120	-	nC
Q_{GS}	gate-source charge		-	30	-	nC
Q_{GD}	gate-drain charge		-	73	-	nC
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz; T_j = 25 °C; see Figure 15	-	12487	16700	pF
C_{oss}	output capacitance		-	1323	1600	pF
C_{rss}	reverse transfer capacitance		-	938	1290	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 30 V; R_L = 1.2 Ω; V_{GS} = 5 V; $R_{G(ext)}$ = 10 Ω	-	130	-	ns
t_r	rise time		-	310	-	ns
$t_{d(off)}$	turn-off delay time		-	380	-	ns
t_f	fall time		-	250	-	ns
L_D	internal drain inductance	from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_S	internal source inductance	from source lead to source bond pad	-	7.5	-	nH



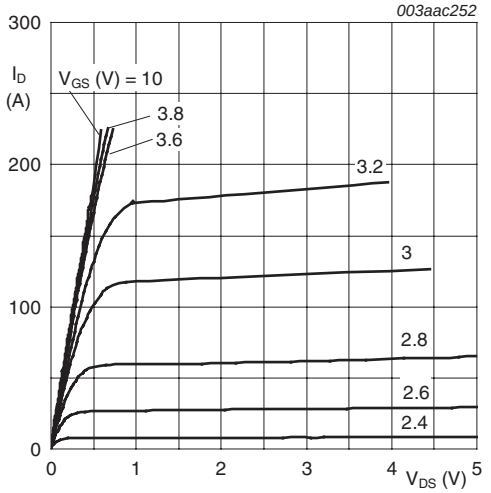
$T_j = 25\,°C; V_{DS} = 25\,V$

Fig 6. Forward transconductance as a function of drain current; typical values



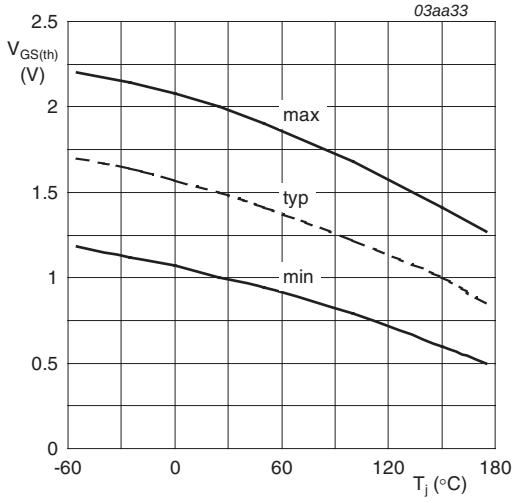
$V_{DS} = 25\,V$

Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values



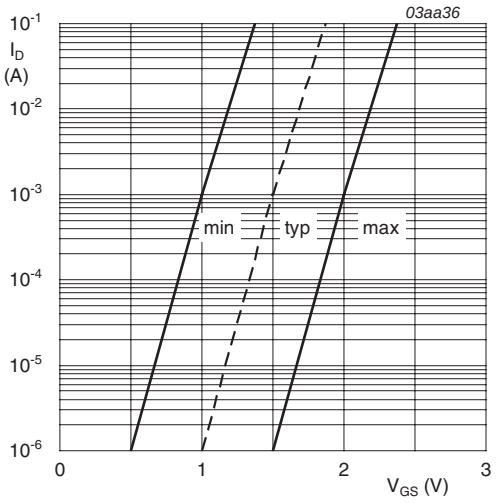
$T_j = 25\,°C$

Fig 8. Output characteristics: drain current as a function of drain-source voltage; typical values



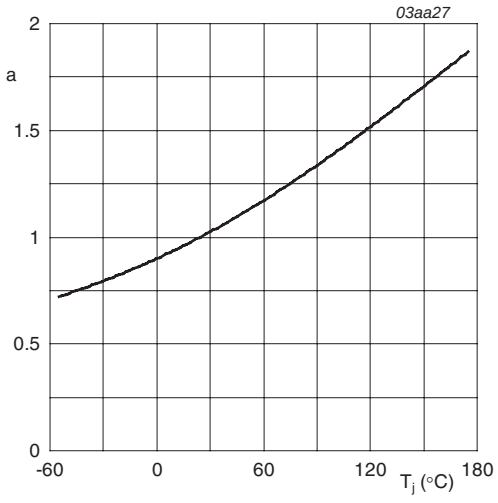
$I_D = 1\,mA; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature



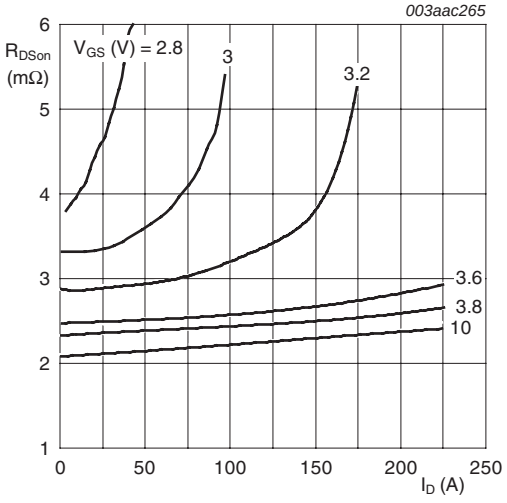
$T_j = 25\ °C; V_{DS} = V_{GS}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage



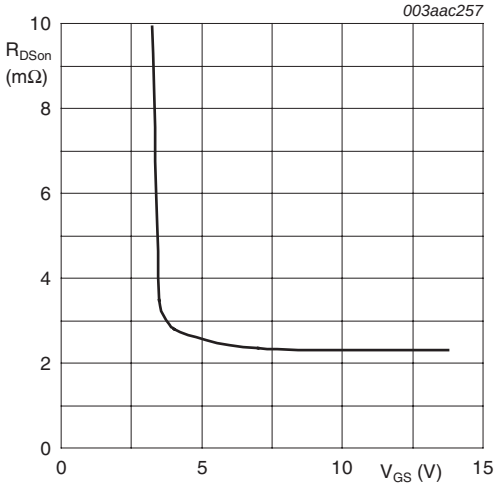
$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig 11. Normalized drain-source on-state resistance factor as a function of junction temperature



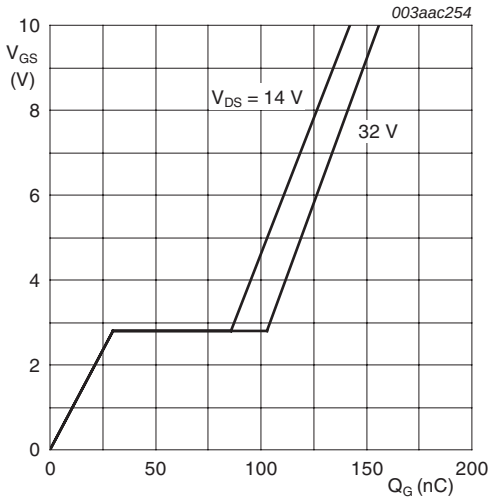
$T_j = 25\ °C$

Fig 12. Drain-source on-state resistance as a function of drain current; typical values



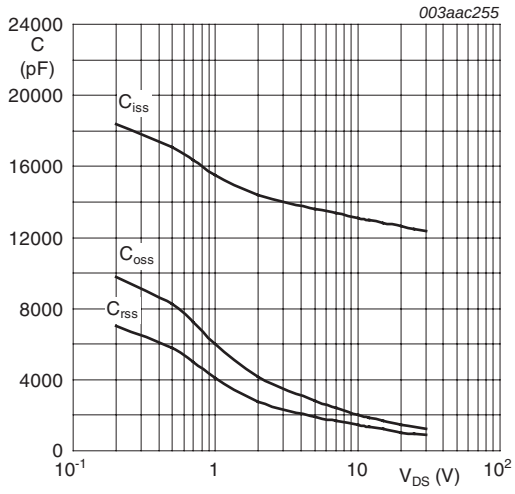
$T_j = 25\ °C; I_D = 25\ A$

Fig 13. Drain-source on-state resistance as a function of gate-source voltage; typical values



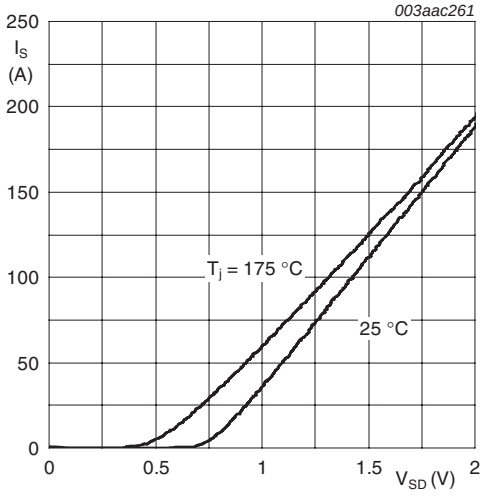
$T_j = 25\,°C; I_D = 25\,A$

Fig 14. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0\,V; f = 1\,MHz$

Fig 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

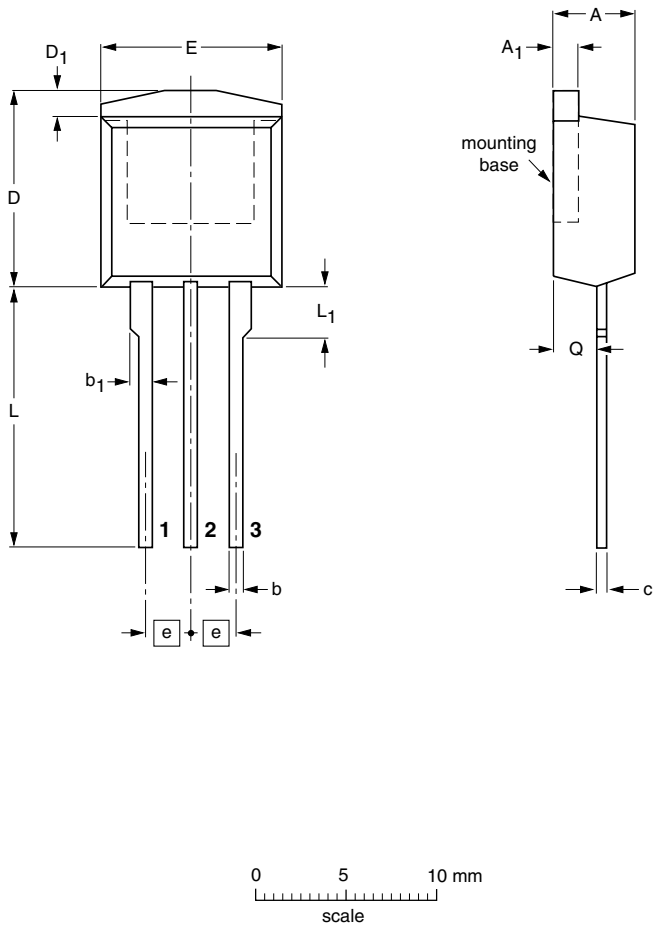


$V_{GS} = 0\,V$

Fig 16. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

7. Package outline

Plastic single-ended package (I2PAK); low-profile 3-lead TO-220AB **SOT226**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	b_1	c	D max	D_1	E	e	L	L_1	Q
mm	4.5 4.1	1.40 1.27	0.85 0.60	1.3 1.0	0.7 0.4	11	1.6 1.2	10.3 9.7	2.54	15.0 13.5	3.30 2.79	2.6 2.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT226		low-profile 3-lead TO-220AB				~~05-06-23~~ 06-02-14

Fig 17. Package outline SOT226 (I2PAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK9E2R4-40C_1	20080411	Product data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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11. Contents

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