Differential Input, Quad,14-Bit, Simultaneous Sampling, SAR ADC

Data Sheet

AD7381-4

FEATURES

- 14-bit ADC family
- Quad simultaneous sampling
- Fully differential analog inputs
- Wide common-mode range
- High throughput rate: 4 MSPS
- Buffered 2.5 V internal voltage reference (10 ppm/°C maximum)
- On-chip oversampling function
- INL (maximum): 1.5 LSB
- SNR (typical)
  - 85.3 dB at V_{REF} = 3.3 V
  - 90.6 dB at OSR = 8× rolling average oversampling, RES = 1
- 2-bit resolution boost
- Out of range indicator ($\overline{ALERT}$)
- High-speed serial interface
- −40°C to +125°C operation
- 4 mm × 4 mm, 24-lead LFCSP

APPLICATIONS

- Motor control position feedback
- Motor control current sense
- Data acquisition systems
- Erbium doped fiber amplifier (EDFA) applications
- In phase and quadrature demodulation

FUNCTIONAL BLOCK DIAGRAM

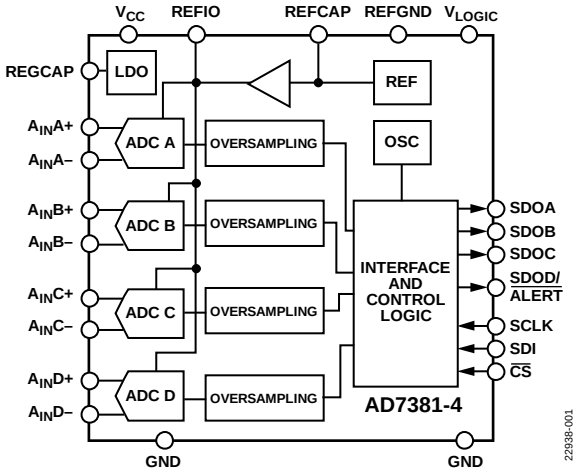


Figure 1.

GENERAL DESCRIPTION

The AD7381-4 a 16-bit, quad, simultaneous sampling, high speed, successive approximation register (SAR), analog-to-digital converter (ADC) that operates from a 3.0 V to 3.6 V power supply and features throughput rates up to 4 MSPS. The analog input type is differential, accepts a wide common-mode input voltage, and the analog inputs are sampled and converted on the falling edge of $\overline{CS}$.

The AD7381-4 has on-chip oversampling blocks to improve dynamic range and reduce noise at lower bandwidths. The oversampling can boost up to two bits of added resolution. A buffered internal 2.5 V reference (10 ppm/°C) is included. Alternatively, an external reference up to 3.3 V can be used.

The conversion process and data acquisition use standard control inputs allowing for easy interfacing to microprocessors or digital signal processors (DSPs). The conversion result can clock out simultaneously via 4-wire mode for faster throughput or via 1-wire serial mode when slower throughput is allowed. The device is compatible with 1.8 V, 2.5 V, and 3.3 V interfaces, using the separate logic supply.

The AD7381-4 is available in a 24-lead lead frame chip scale package (LFCSP) with operation specified from −40°C to +125°C.

Table 1. Related Devices

No. of Channels	Input Type	16 Bits	14 Bits
4	Differential	AD7380-4 AD7389-4	AD7381-4
2	Differential	AD7380 AD4680 AD4681	AD7381
	Single-ended	AD7386	AD7387

PRODUCT HIGHLIGHTS

1. Quad simultaneous sampling and conversion.
2. Pin-compatible product family.
3. High throughput rate, 4 MSPS at 14-bit.
4. Space-saving, 4 mm × 4 mm LFCSP.
5. Integrated oversampling block to increase dynamic range, reduce noise and reduce SCLK speed requirements.
6. Differential analog inputs with wide common-mode range.
7. Small sampling capacitor reduces amplifier drive burden.

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REVISION HISTORY

1/2022—Revision 0: Initial Version

SPECIFICATIONS

V_{CC} = 3.0 V to3.6 V, V_{LOGIC} = 1.65 V to 3.6 V, reference voltage (V_{REF}) = 2.5 V, f_{SAMPLE} = 4 MSPS, T_A = −40°C to +125°C, no oversampling enabled, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RESOLUTION		14			Bits
THROUGHPUT					
Conversion Rate (f_{SAMPLE})				4	MSPS
ANALOG INPUT					
Voltage Range	$A_{IN}x+ - A_{IN}x-$	$-V_{REF}$		$+V_{REF}$	V
Absolute Input Voltage	$A_{IN}x+$, $A_{IN}x-$	−0.1		V_{REF} + 0.1	V
Common-Mode Input Range	$A_{IN}x+$, $A_{IN}x-$	0.2	$V_{REF} \times 0.5$	V_{REF} − 0.2	V
Analog Input Common-Mode Rejection Ratio (CMRR)	f_{IN} = 500 kHz		−76		dB
DC Leakage Current			0.1	1	µA
Input Capacitance	Track mode		18		pF
	Hold mode		5		pF
DC ACCURACY					
No Missing Codes		14			Bits
Differential Nonlinearity (DNL) Error		−1	±0.7	+1	LSB
Integral Nonlinearity (INL) Error		−1	±0.4	+1	LSB
	V_{REF} = 2.5 V (internal), 2 MSPS	−1.5	±0.4	+1.5	LSB
Gain Error		−0.025	±0.006	+0.025	% FS
Gain Error Temperature Drift		−1	±0.2	+1	ppm/°C
Gain Error Match		−0.025	±0.005	+0.025	% FS
Zero Error		−3	±0.25	+3	LSB
Zero Error Temperature Drift		−3	±0.5	+3	µV/°C
Zero Error Match		−1. 5	±0.25	+1.5	mV
AC ACCURACY	f_{IN} = 1 kHz				
Dynamic Range			85.4		dB
Oversampled Dynamic Range	OSR = 4×, RES = 1 (decimal)		91.3		dB
Signal-to-Noise Ratio (SNR)	V_{REF} = 3.3 V, 4 MSPS	84.5	85.3		dB
	V_{REF} = 2.5 V (internal), 2 MSPS	83.5	85		dB
	Rolling average OSR = 8×, RES = 1 (decimal)		90.6		dB
	f_{IN} = 100 kHz		84.4		dB
Spurious-Free Dynamic Range (SFDR)			−109		dB
Total Harmonic Distortion (THD)			−110		dB
	f_{IN} = 100 kHz		−103.2		dB
Signal-to-Noise-and-Distortion (SINAD) Ratio	V_{REF} = 3.3 V	84	84.8		dB
		83.5	84.5		dB
Channel to Channel Isolation			−126		dB

V_{CC} = 3.0 V to3.6 V, V_{LOGIC} = 1.65 V to 3.6 V, V_{REF} = 2.5 V, T_A = −40°C to +125°C, no oversampling enabled, unless otherwise noted.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SAMPLING DYNAMICS					
Input Bandwidth	At −0.1 dB		6.6		MHz
	At −3 dB		26.8		MHz
Aperture Delay			2		ns
Aperture Delay Match			46.8	145	ps
Aperture Jitter			20		ps
REFERENCE INPUT/OUTPUT					
V_{REF} Input Voltage Range	External reference	2.49		3.4	V
V_{REF} Input Current			0.9	1.2	mA
V_{REF} Output Voltage	−40°C to +125°C	2.495	2.5	2.505	V
V_{REF} Temperature Coefficient			1	10	ppm/°C
V_{REF} Noise			7		µV rms
DIGITAL INPUTS (SCLK, SDI, $\overline{CS}$)					
Logic Levels					
Input Low Voltage (V_{IL})				0.2 × V_{LOGIC}	V
Input High Voltage (V_{IH})		0.8 × V_{LOGIC}			V
Input Low Current (I_{IL})		−1		+1	µA
Input High Current (I_{IH})		−1		+1	µA
DIGITAL OUTPUTS (SDOA, SDOB, SDOC, SDOD/$\overline{ALERT}$)					
Output Coding			Twos complement		Bits
Output Low Voltage (V_{OL})	Current sink (I_{SINK}) = 300 µA			0.4	V
Output High Voltage (V_{OH})	Current source (I_{SOURCE}) = −300 µA	V_{LOGIC} − 0.3			V
Floating State Leakage Current				±1	µA
Floating State Output Capacitance			10		pF
POWER SUPPLIES					
V_{CC}		3.0	3.3	3.6	V
	External reference = 3.3 V	3.15	3.3	3.6	V
V_{LOGIC}		1.65		3.6	V
V_{CC} Supply Current (I_{VCC})					
Normal Mode (Operational)			38	42	mA
Normal Mode (Static)			1.7	2	mA
Shutdown Mode			101	200	µA
V_{LOGIC} Current (I_{VLOGIC})	Analog inputs at positive full scale				
Normal Mode (Static)			10	200	nA
Normal Mode (Operational)			7.3	8	mA
Shutdown Mode			10	200	nA
Power Dissipation					
Total (P_{TOTAL})			163.1	180	mW
V_{CC} Power (P_{VCC})					
Normal Mode (Operational)			136.8	151.2	mW
Normal Mode (Static)			6.1	7.2	mW
Shutdown Mode			363.6	720	µW
V_{LOGIC} Power (P_{VLOGIC})	Analog inputs at positive full scale				
Normal Mode (Static)			36	720	nW
Normal Mode (Operational)			26.3	29	mW
Shutdown Mode			36	720	nW

TIMING SPECIFICATIONS

V_{CC} = 3.0 V to3.6 V, V_{LOGIC} = 1.65 V to 3.6 V, V_{REF} = 2.5 V, T_A = −40°C to +125°C, unless otherwise noted. For SCLK frequencies ≥ 70 MHz, load capacitance (C_{LOAD}) = 10 pF. For SCLK frequencies < 70 MHz, C_{LOAD} = 20 pF.

When referencing a single function of a multifunction pin in the parameters, only the portion of the pin name that is relevant to the specification is listed, such as $\overline{\text{ALERT}}$. For full pin names of multifunction pins, refer to the Pin Configuration and Function Descriptions section.

Table 4.

Parameter	Min	Typ	Max	Unit	Description
t_{CYC}	250			ns	Time between conversions
t_{SCLKED}	5			ns	$\overline{CS}$ falling edge to first SCLK falling edge
t_{SCLK}	12.5			ns	SCLK period
t_{SCLKH}	5.5			ns	SCLK high time
t_{SCLKL}	5.5			ns	SCLK low time
t_{CSH}	20			ns	$\overline{CS}$ pulse width
t_{QUIET}	20			ns	Interface quiet time prior to conversion
t_{SDOEN}					$\overline{CS}$ low to SDOA and SDOB enabled
			5.5	ns	V_{LOGIC} ≥ 2.25V
			8	ns	1.65V ≤ V_{LOGIC} < 2.25 V
t_{SDOH}	2				SCLK rising edge to SDOA and SDOB hold time
t_{SDOS}					SCLK rising edge to SDOA and SDOB setup time
			5	ns	V_{LOGIC} ≥ 2.25 V
			8	ns	1.65V ≤ V_{LOGIC} < 2.25V
t_{SDOT}			8	ns	$\overline{CS}$ rising edge to SDOA and SDOB high impedance
t_{SDIS}	4			ns	SDI setup time prior to SCLK falling edge
t_{SDIH}	4			ns	SDI hold time after SCLK falling edge
t_{SCLKCS}	0			ns	SCLK rising edge to $\overline{CS}$ rising edge
$t_{CONVERT}$			190	ns	Conversion time
$t_{ACQUIRE}$	110			ns	Acquire time
t_{RESET}					Valid time to start conversion after software reset (see Figure 35)
		250		ns	Valid time to start conversion after soft reset
		800		ns	Valid time to start conversion after hard reset
$t_{POWERUP}$					Supply active to conversion
			5	ms	First conversion allowed
			11	ms	Settled to within 1% with internal reference
			5	ms	Settled to within 1% with external reference
$t_{REGWRITE}$			5	ms	Supply active to register read write access allowed
$t_{STARTUP}$					Exiting shutdown mode to conversion
			11	ms	Settled to within 1% with internal reference
			10	µs	Settled to within 1% with external reference
$t_{CONVERT0}$	6	8	10	ns	Conversion time for first sample in oversampling (OS) normal mode
$t_{CONVERTx}$	$t_{CONVERT0} + (250 \times (x - 1))$			ns	Conversion time for x^{th} sample in OS normal mode
t_{ALERTS}			220	ns	Time from $\overline{CS}$ to $\overline{ALERT}$ indication
t_{ALERTC}			10	ns	Time from $\overline{CS}$ to $\overline{ALERT}$ clear
t_{ALERTS_NOS}			20	ns	Time from internal conversion with exceeded threshold to $\overline{ALERT}$ indication

Timing Diagrams

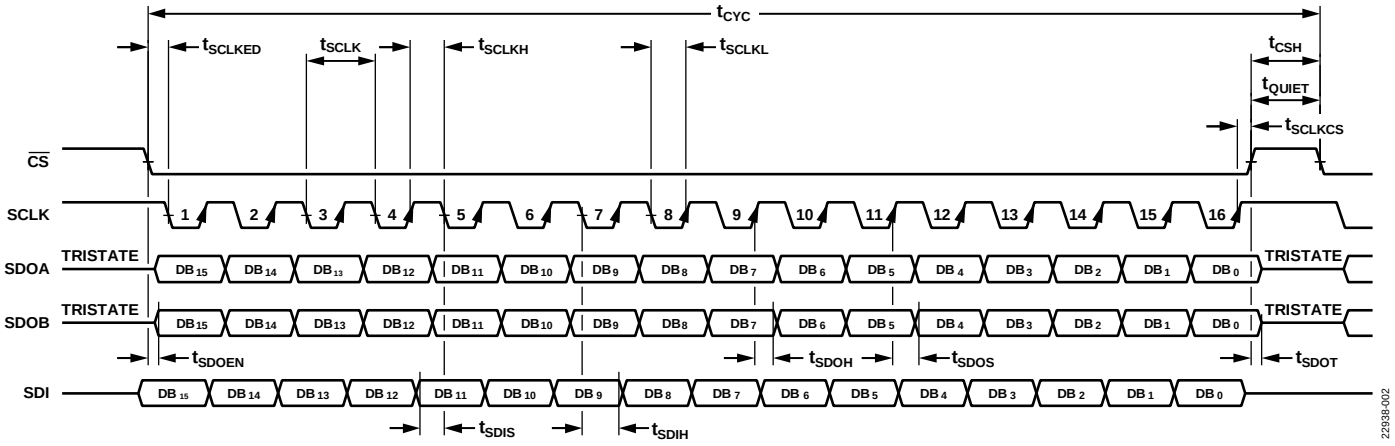


Figure 2. Serial Interface Timing Diagram

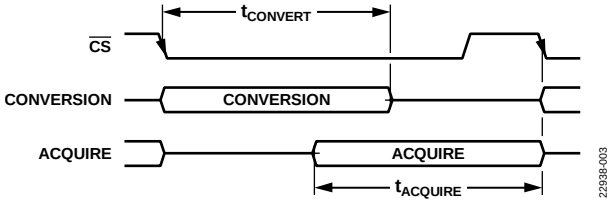


Figure 3. Internal Conversion Acquire Timing

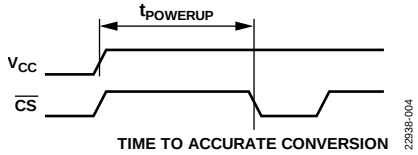


Figure 4. Power-Up Time to Conversion

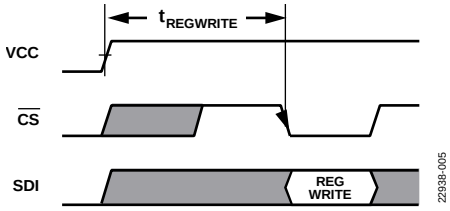


Figure 5. Power-Up Time to Register Read Write Access

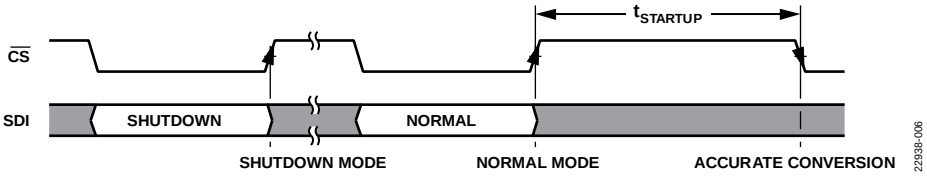


Figure 6. Shutdown Mode to Normal Mode Timing

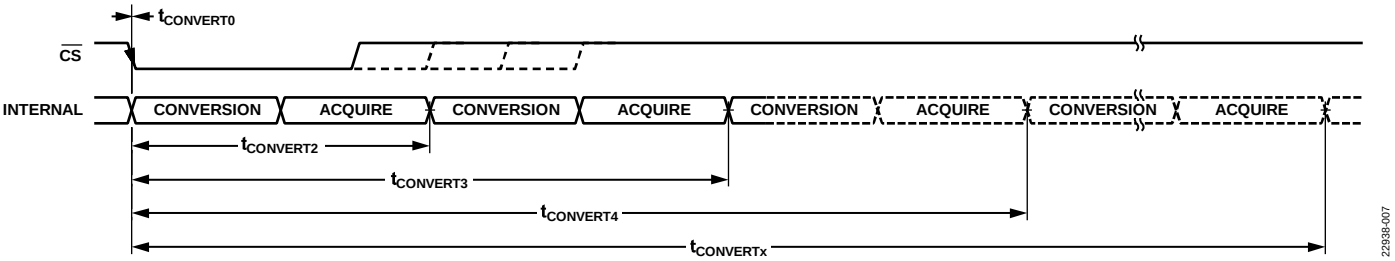


Figure 7. Conversion Timing During OS Normal Mode

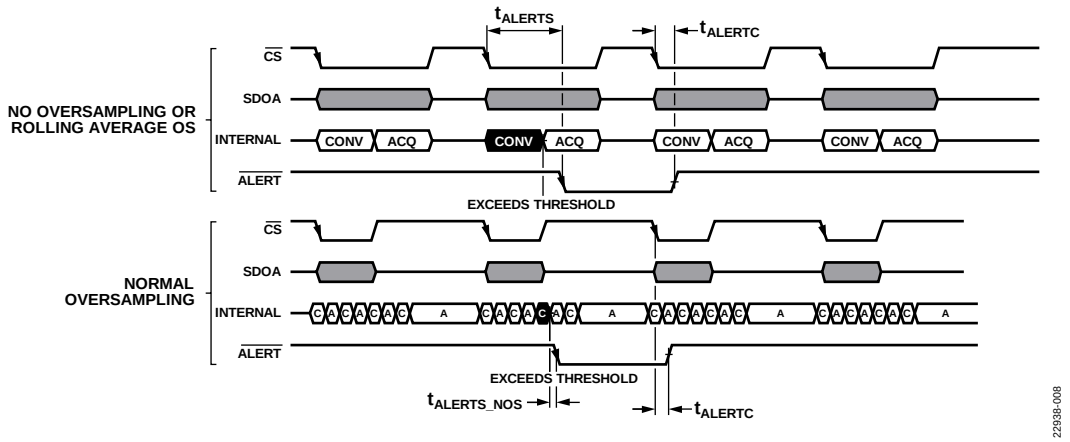


Figure 8. $\overline{ALERT}$ Timing

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
V_{CC} to GND	−0.3 V to +4 V
V_{LOGIC} to GND	−0.3 V to +4 V
Analog Input Voltage to GND	−0.3 V to V_{REF} +0.3 V, or V_{CC} + 0.3 V
Digital Input Voltage to GND	−0.3 V to V_{LOGIC} + 0.3 V
Digital Output Voltage to GND	−0.3 V to V_{LOGIC} + 0.3 V
REFIO Input to GND	−0.3 V to V_{CC} +0.3 V
Input Current to Any Pin Except Supplies	±10 mA
Temperature Range	
Operating	−40°C to +125°C
Storage	−65°C to +150°C
Maximum Junction Temperature	150°C
Pb-Free Soldering Reflow Temperature	260°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case thermal resistance.

Table 6. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
CP-24-25[1]	48.4	0.43[2]	°C/W

1 Test Condition 1: thermal impedance simulated values are based on JEDEC 2S2P thermal test board with four thermal vias. See JEDEC JESDS1.
2 Test Condition 2: a cold plate attached to the package surface and measured at the exposed pad.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Field induced charge device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for AD7381-4

Table 7. AD7381-4, 24-Lead LFCSP

ESD Model	Withstand Threshold (V)	Class
HBM	±4000	3A
FICDM	±1250	C3

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

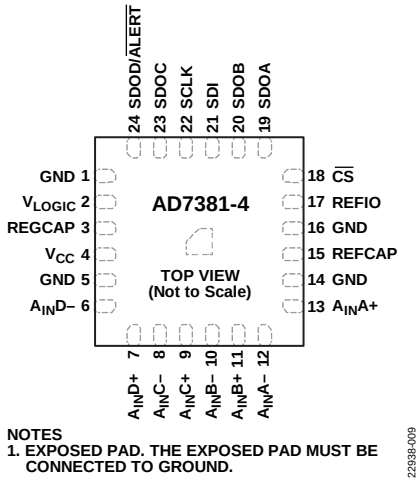


Figure 9. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 5, 14, 16	GND	Ground Reference Point. These pins are the ground reference points for all circuitry on the device.
2	V_{LOGIC}	Logic Interface Supply Voltage, 1.65 V to 3.6 V. Decouple this pin to GND with a 1 µF capacitor.
3	REGCAP	Decoupling Capacitor Pin for Voltage Output from Internal Regulator. Decouple this pin to GND with a 1 µF capacitor. The voltage at this pin is 1.9 V typical.
4	V_{CC}	Power Supply Input Voltage. 3.0 V to 3.6 V. Decouple this pin to GND using a 1 µF capacitor.
6, 7	$A_{IN}D–$, $A_{IN}D+$	Analog Inputs of ADC D. These analog inputs form a fully differential pair.
8, 9	$A_{IN}C–$, $A_{IN}C+$	Analog Inputs of ADC C. These analog inputs form a fully differential pair.
10, 11	$A_{IN}B–$, $A_{IN}B+$	Analog Inputs of ADC B. These analog inputs form a fully differential pair.
12, 13	$A_{IN}A–$, $A_{IN}A+$	Analog Inputs of ADC A. These analog inputs form a fully differential pair.
15	REFCAP	Decoupling Capacitor Pin for Bandgap Reference. Decouple this pin to GND with a 0.1 µF capacitor. The voltage at this pin is 2.5 V typical. If the device is configured for external reference operation the 0.1µF capacitor is not required.
17	REFIO	Reference Input. An external reference of 2.5 V to 3.3 V can be input to this pin. Decoupling is required on this pin. Apply a 1 µF capacitor from this pin to GND.
18	$\overline{CS}$	Chip Select Input. Active low, logic input. This input provides the dual function of initiating conversions on the AD7381-4 and framing the serial data transfer.
19	SDOA	Serial Data Output A. This pin functions as a serial data output pin to access the conversion results and register contents.
20	SDOB	Serial Data Output B. This pin functions as a serial data output pin to access the conversion results.
21	SDI	Serial Data Input. This input provides the data written to the on-chip control registers.
22	SCLK	Serial Clock Input. This serial clock input is for data transfers to and from the ADC.
23	SDOC	Serial Data Output C. This pin functions as a serial data output pin to access the conversion results and register contents.
24	SDOD/$\overline{ALERT}$	Serial Data Output D (SDOD). This pin functions as a serial data output to access the conversion results. Alert Indication Output ($\overline{ALERT}$). This pin operates as an alert going low to indicate that a conversion result has exceeded a configured threshold. This pin can operate as a serial data output pin or alert indication output.
Not applicable	EPAD	Exposed Pad. The exposed pad must be connected to ground.

TYPICAL PERFORMANCE CHARACTERISTICS

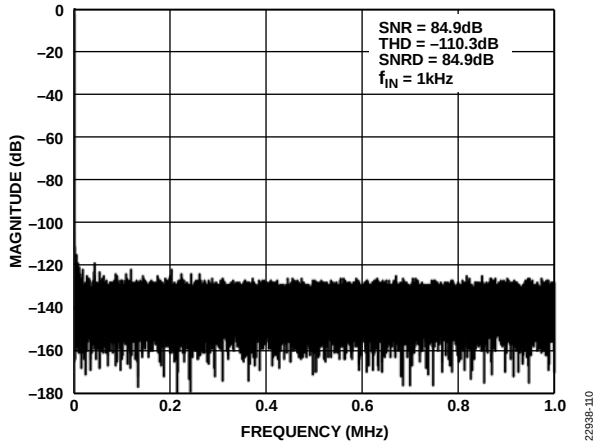


Figure 10. Fast Fourier Transform (FFT), 1 kHz Input Tone, −0.5 dBFS, Internal Reference = 2.5 V

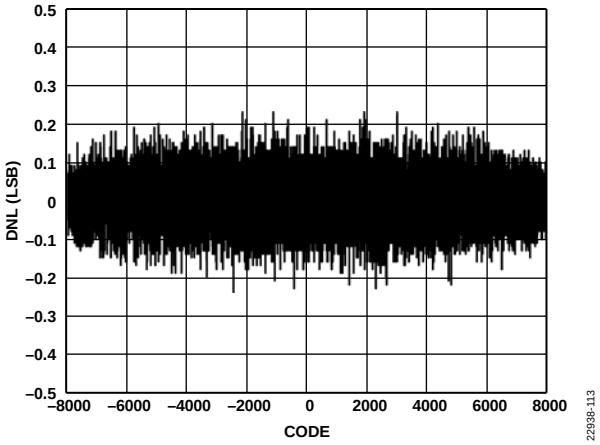


Figure 13. DNL vs. Code

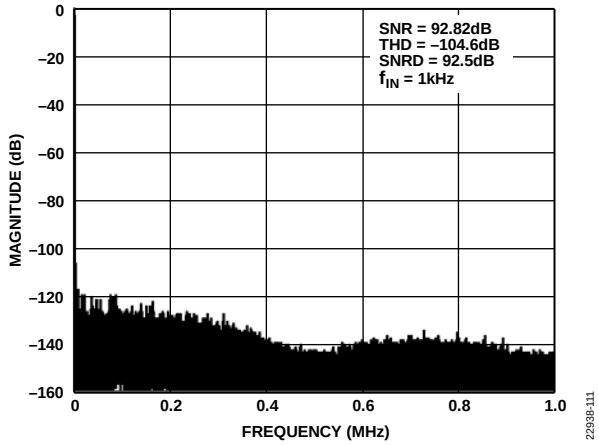


Figure 11. FFT, 1 kHz Input Tone, −0.5 dBFS, External Reference = 3.3 V

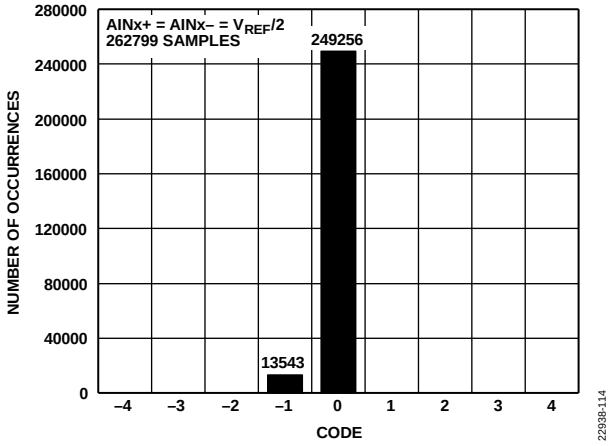


Figure 14. Code Histogram

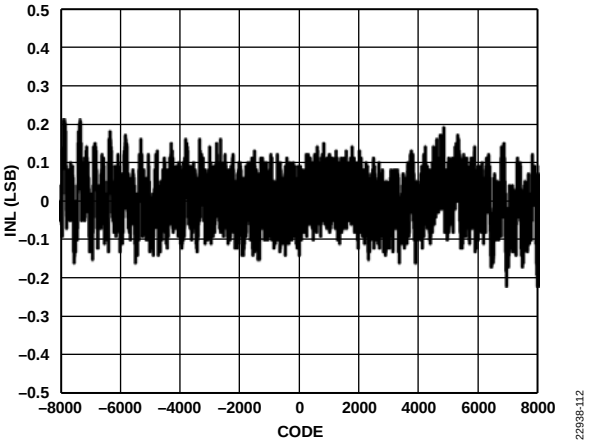


Figure 12. INL vs. Code

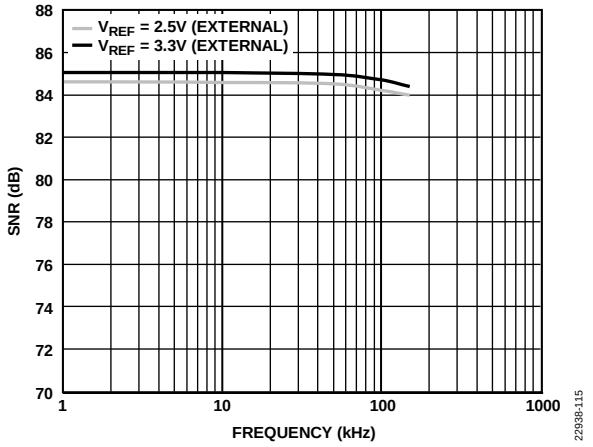


Figure 15. SNR vs. Frequency

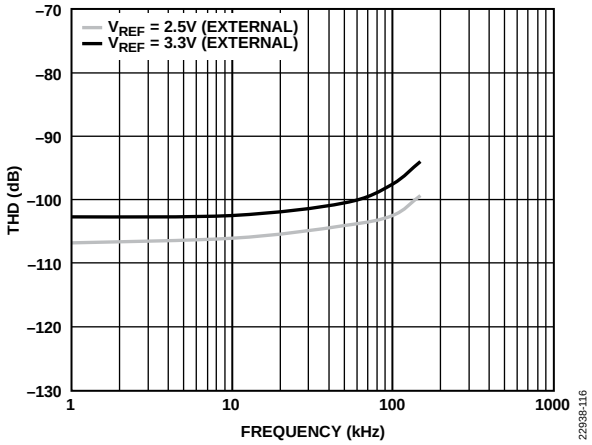


Figure 16. THD vs. Frequency

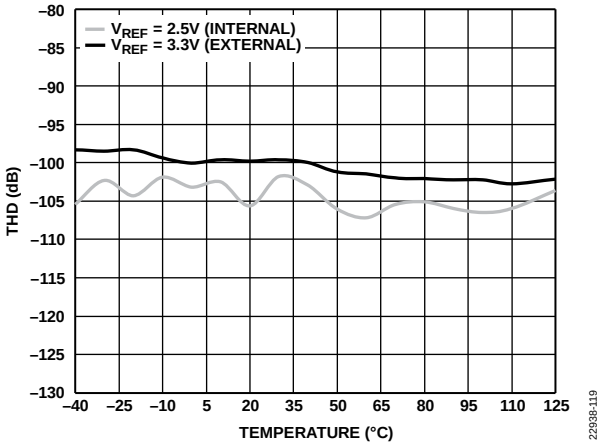


Figure 19. THD vs. Temperature

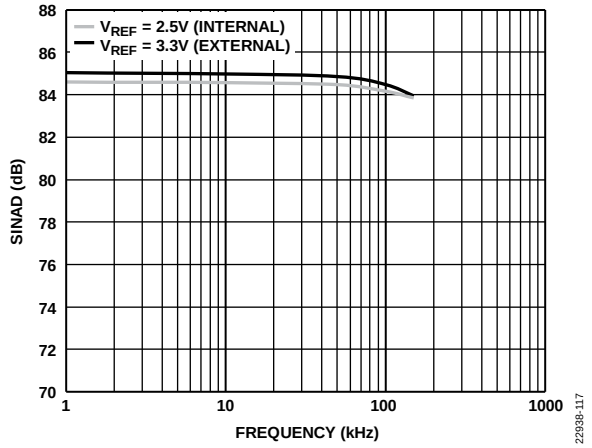


Figure 17. SINAD vs. Frequency

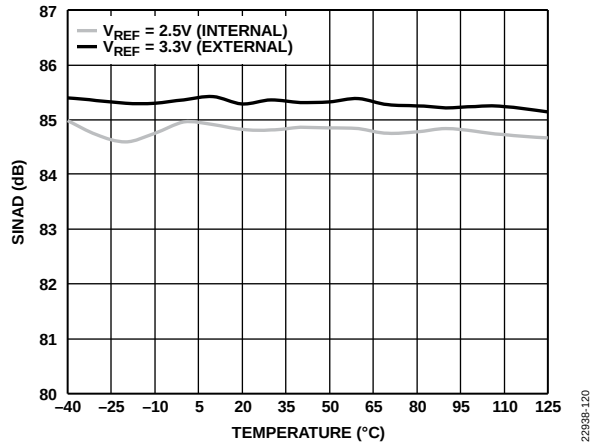


Figure 20. SINAD vs. Temperature

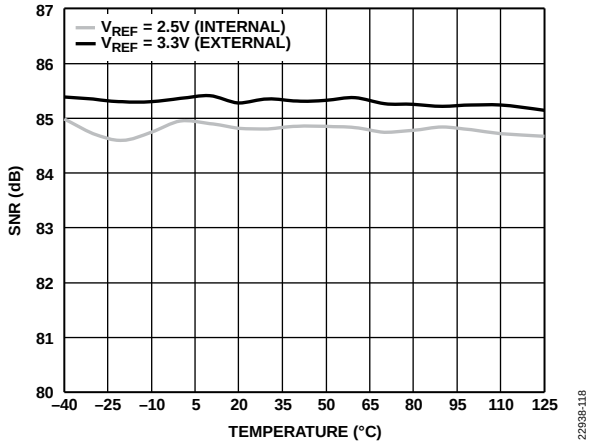


Figure 18. SNR vs. Temperature

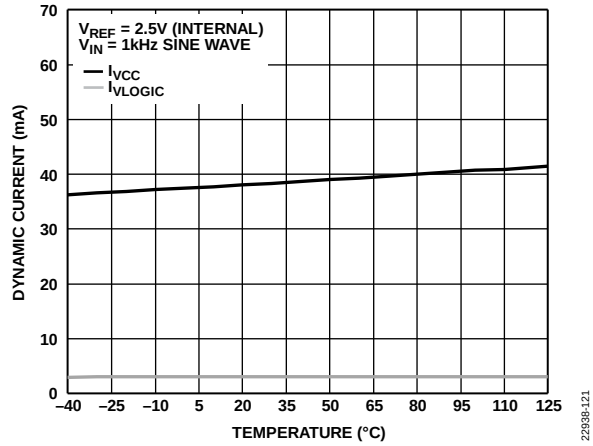


Figure 21. Dynamic Current vs. Temperature

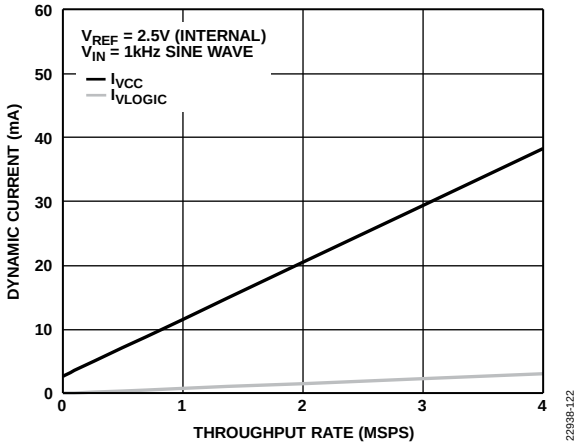


Figure 22. Dynamic Current vs. Throughput Rate

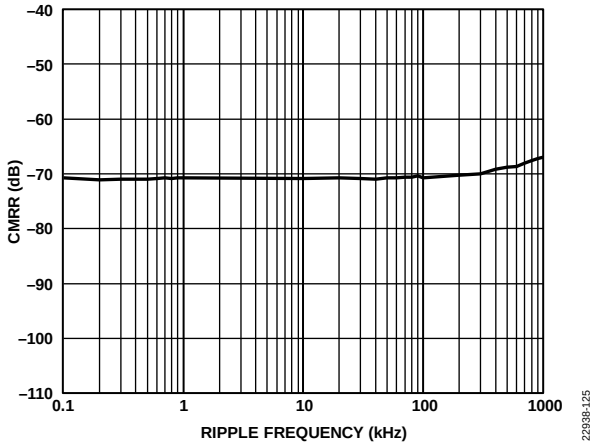


Figure 25. CMRR vs. Ripple Frequency

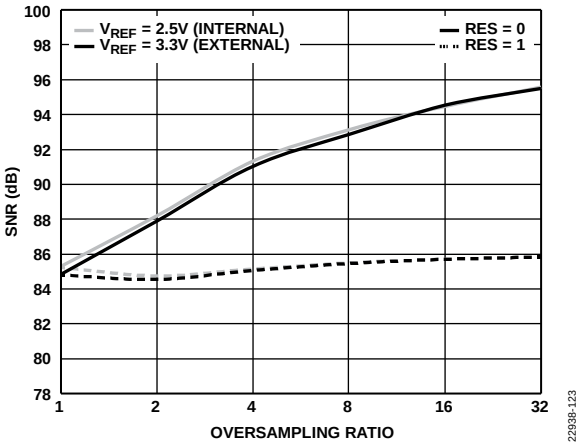


Figure 23. SNR vs. Oversampling Ratio, Normal Averaging

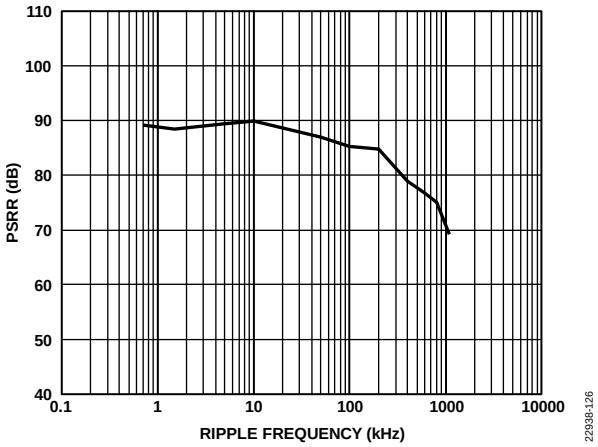


Figure 26. PSRR vs. Ripple Frequency

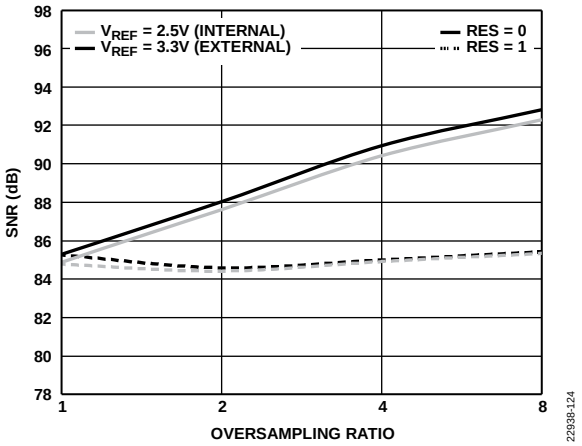


Figure 24. SNR vs. Oversampling Ratio, Rolling Average

TERMINOLOGY

Differential Nonlinearity (DNL)
In an ideal ADC, code transitions are 1 LSB apart. DNL is the maximum deviation from this ideal value. DNL is often specified in terms of resolution for which no missing codes are guaranteed.

Integral Nonlinearity (INL)
INL is the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line.

Gain Error
The first transition (from 100 … 000 to 100 …001) occurs at a level ½ LSB above nominal negative full scale. The last transition (from 011 … 110 to 011 … 111) occurs for an analog voltage 1½ LSB below the nominal full scale. The gain error is the deviation of the difference between the actual level of the last transition and the actual level of the first transition from the difference between the ideal levels.

Gain Error Drift
The gain error change due to a temperature change of 1°C.

Gain Error Matching
Gain error matching is the difference in negative full-scale error between the input channels and the difference in positive full-scale error between the input channels.

Zero Error
Zero error is the difference between the ideal midscale voltage, 0 V, and the actual voltage producing the midscale output code, 0 LSB.

Zero Error Temperature Drift
Zero error temperature drift is the zero error change due to a temperature change of 1°C.

Zero Error Match
Zero error match is the difference in zero error between the input channels.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

Spurious-Free Dynamic Range (SFDR)

SFDR is the difference, in decibels (dB), between the rms amplitude of the input signal and the peak spurious signal.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in decibels.

Signal-to-Noise-and-Distortion (SINAD) Ratio
SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components that are less than the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in decibels.

Common-Mode Rejection Ratio (CMRR)
CMRR is the ratio of the power in the ADC output at the frequency, f, to the power of a 200 mV p-p sine wave applied to the common-mode voltage of $A_{INx}+$ and $A_{INx}-$ of frequency, f. CMRR is expressed in decibels.

$$CMRR = 10\log(P_{ADC_IN}/P_{ADC_OUT})$$

where:
P_{ADC_IN} is the common-mode power at the frequency, f, applied to the $A_{INx}+$ and A_{INx} inputs.
P_{ADC_OUT} is the power at the frequency, f, in the ADC output.

Aperture Delay
Aperture delay is the measure of the acquisition performance and is the time between the falling edge of the $\overline{CS}$ input and when the input signal is held for a conversion.

Aperture Delay Match
Aperture delay match is the difference of the aperture delay between each ADC channel.

Aperture Jitter
Aperture jitter is the variation in aperture delay.

THEORY OF OPERATION

CIRCUIT INFORMATION

The AD7381-4 is a high speed, quad, fully differential, 14-bit, SAR ADC. The device operates from a 3.0 V to 3.6 V power supply and features throughput rates up to 4 MSPS.

The AD7381-4 contains four successive approximation ADCs, and a serial interface with four separate data output pins. The device is housed in a 24-lead LFCSP, offering the user considerable space-saving advantages over alternative solutions.

Data is accessed from the device via the serial interface. The interface can be operated with two, four, or one serial output. The AD7381-4 has an on-chip 2.5 V internal reference (10 ppm/°C). If an external reference is desired, the internal reference can be disabled, and an external reference voltage ranging from 2.5 V to 3.3 V can be supplied. If the internal reference is used elsewhere in the system, the reference output must be buffered. The differential analog input range for the AD7381-4 is $V_{CM} \pm V_{REF}/2$.

The AD7381-4 features on-chip oversampling blocks to improve performance. Normal averaging and rolling average oversampling modes are available. Power-down options to allow power saving between conversions are available. Configuration of the device is implemented via the standard serial interface, as described in the Interface section.

CONVERTER OPERATION

The AD7381-4 has four successive approximation ADCs, each based around two capacitive DACs. Figure 27 and Figure 28 show simplified schematics of one of these ADCs in acquisition and conversion phases, respectively. The ADC comprises control logic, a SAR, and two capacitive DACs. In Figure 27 (the acquisition phase), SW3 is closed, SW1 and SW2 are in Position A, the comparator is held in a balanced condition, and the sampling capacitor (C_S) arrays can acquire the differential signal on the input.

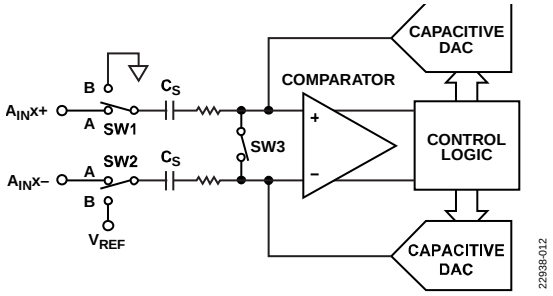


Figure 27. ADC Acquisition Phase

When the ADC starts a conversion (see Figure 28), SW3 opens and SW1 and SW2 move to Position B, causing the comparator to become unbalanced. Both inputs are disconnected when the conversion begins. The control logic and charge redistribution DACs are used to add and subtract fixed amounts of charge from the sampling capacitor arrays to bring the comparator back into a balanced condition. When the comparator is rebalanced, the conversion is complete. The control logic generates the ADC output code. The output impedances of the sources driving the $A_{IN}x+$ and $A_{IN}x-$ pins must be matched. Otherwise, the two inputs have different settling times, resulting in errors.

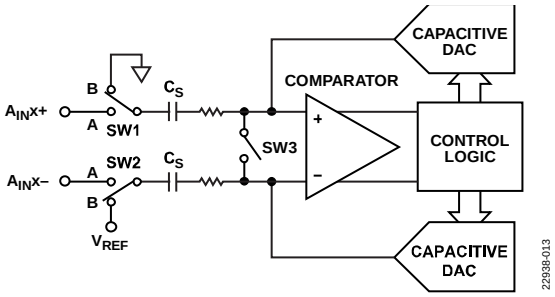


Figure 28. ADC Conversion Phase

ANALOG INPUT STRUCTURE

Figure 29 shows the equivalent circuit of the analog input structure of the AD7381-4. The four diodes provide ESD protection for the analog inputs. Ensure that the analog input signals never exceed the supply rails by more than 300 mV. Exceeding the limit causes these diodes to become forward-biased and start conducting into the substrate. These diodes can conduct up to 10 mA without causing irreversible damage to the device.

The C1 capacitors in Figure 29 are typically 3 pF and can primarily be attributed to pin capacitance. The R1 resistors are lumped components made up of the on resistance of the switches. The value of these resistors is typically about 200 Ω. The C2 capacitors are the ADC sampling capacitors with a typical capacitance of 15 pF.

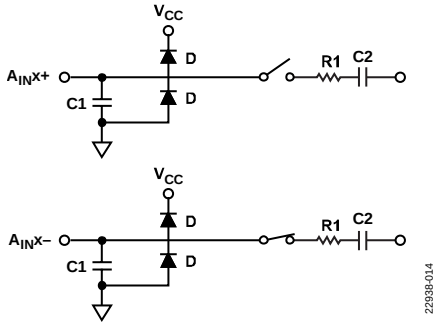


Figure 29. Equivalent Analog Input Circuit, Conversion Phase—Switches Open, Track Phase—Switches Closed

ADC TRANSFER FUNCTION

The AD7381-4 uses a 2.5 V to 3.3 V reference. The AD7381-4 converts the differential voltage of the analog inputs ($A_{IN}x+$ and $A_{IN}x-$) into a digital output.

The conversion result is MSB first, twos complement. The LSB size is $(2 \times V_{REF})/2^N$, where N is the ADC resolution. The ADC resolution is determined by the resolution of the device chosen and if resolution boost mode is enabled. Table 9 outlines the LSB size expressed in microvolts for different resolutions and reference voltage options.

The ideal transfer characteristic of the AD7381-4 is shown in Figure 30.

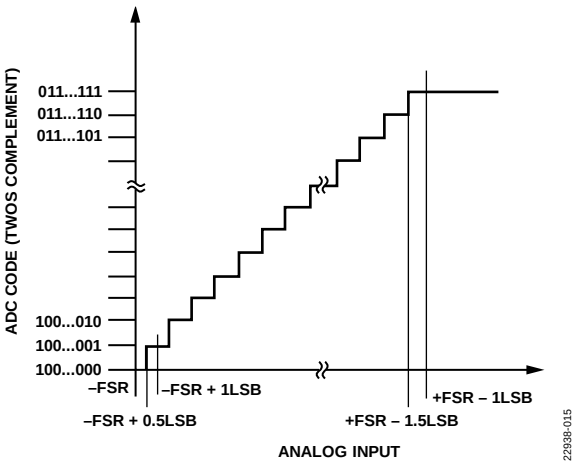


Figure 30. ADC Ideal Transfer Function (FSR = Full-Scale Range)

Table 9. LSB Size

Resolution (Bits)	2.5 V Reference (µV)	3.3 V Reference (µV)
14	305.2	402.8
16	76.3	100.7

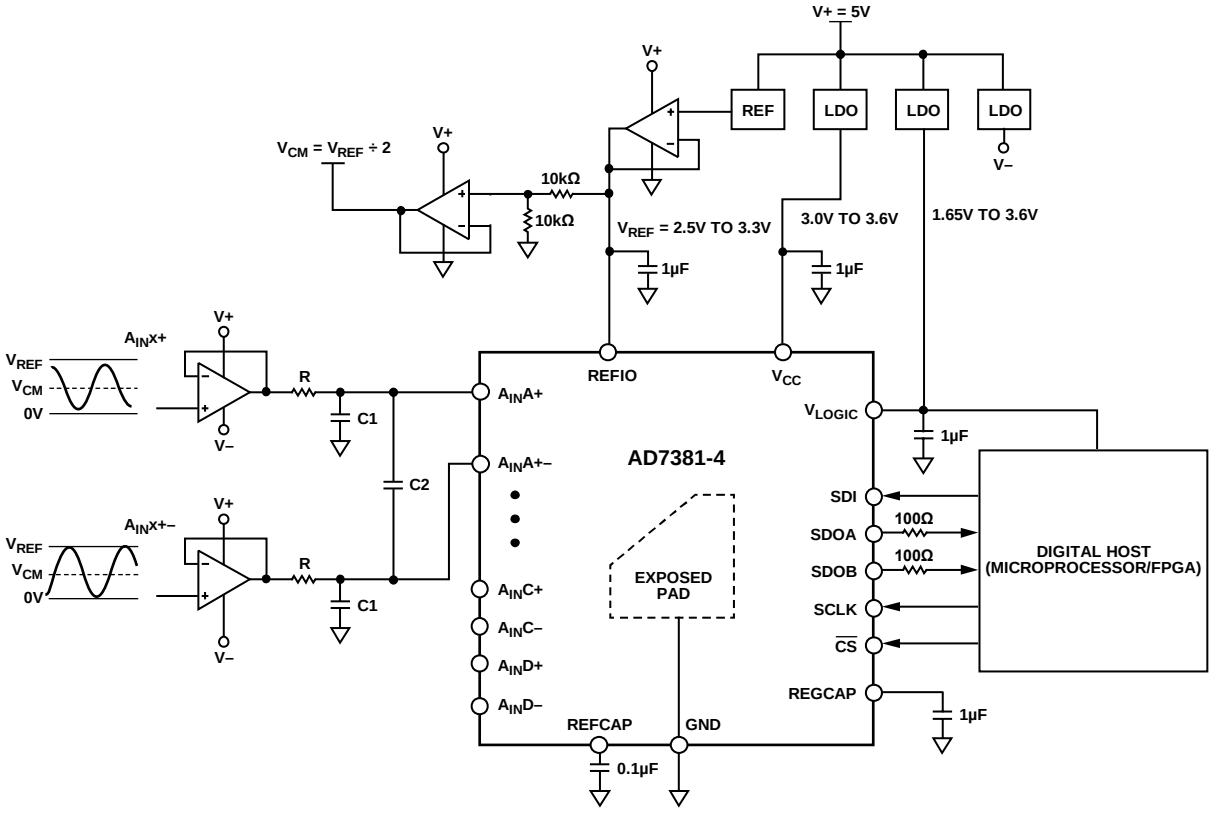


Figure 31. Typical Application Circuit

APPLICATIONS INFORMATION

Figure 31 shows an example of a typical application circuit for the AD7381-4. Decouple the V_{CC}, V_{LOGIC}, REGCAP, and REFIO pins with suitable decoupling capacitors as shown. The exposed pad is a ground reference point for circuitry on the device and must be connected to the board ground.

A differential RC filter must be placed on the analog inputs to ensure optimal performance is achieved. In a typical application, R = 33 Ω, C1 = 68 pF, and C2 = 68 pF are recommended. These RC combinations must be the same for all channels of the AD7381-4.

The four differential channels of the AD7381-4 can accept an input voltage range from 0 V to V_{REF} and have a wide common-mode range to convert a variety of signals. These analog input pins ($A_{IN}x\pm$) can easily be driven with an amplifier. Table 10 lists the recommended driver amplifiers that can best fit and add value to the application.

The performance of the AD7381-4 device can be impacted by noise on the digital interface. This impact is dependent on-board layout and design. Keep a minimal distance of the digital line to the digital interface or place a 100 Ω resistor in series and close to the SDOA, SDOB, SDOC, and SDOD/$\overline{\text{ALERT}}$ pins to reduce noise from the digital interface coupling of the AD7381-4.

The AD7381-4 can use an ultralow noise, high accuracy voltage reference ranging from 2.5 V to 3.3 V, such as the ADR4533 or ADR4525, as the external voltage source. A 1 µF reservoir capacitor is recommended to be connected between the REFIO pin and the ground. When using this external reference voltage in another circuit within the application, for example, as a common-mode voltage for the driver amplifier, it is recommended to use a buffer amplifier like the ADA4807-2 for a stable reference.

POWER SUPPLY

For a typical application, the AD7381-4 circuitry shown in Figure 31 can be driven from a 5 V (V+) supply to power the system. The 5 V (V+) can be supplied from the ADP7104. The ADC driver can be supplied by a 5 V (V+) and a −2.5 V (V−) derived from the inverting charge pump, the ADP5600, that converts 5 V to −5 V, then to the ADP7182 for the low noise voltage regulator to output −2.5 V. Two independent power supply sources are derived from a low dropout (LDO) regulator to power the V_{CC} supply for the analog circuitry and the V_{LOGIC} supply for the digital interface of the AD7381-4. A very low quiescent current LDO regulator like the ADP166 is a suitable supply with a fixed output voltage range from 1.2 V to 3.3 V for typical V_{CC} and V_{LOGIC} levels. The V_{CC} supply and the V_{LOGIC} supply must be decoupled separately with a 1 µF capacitor. Additionally, an LDO regulator supplies the AD7381-4. The on-chip regulator provides a 1.9 V supply only for internal use on the device. Decouple the REGCAP pin with a 1 µF capacitor to GND.

Power-Up

The AD7381-4 is not easily damaged by power supply sequencing. V_{CC} and V_{LOGIC} can be applied in any sequence. The external reference must be applied after V_{CC} and V_{LOGIC} are applied. Analog and digital signals must be applied after the external reference is applied.

The AD7381-4 requires $t_{POWERUP}$ from applying V_{CC} and V_{LOGIC} until the ADC conversion results are stable. Interfacing with the AD7381-4 prior to the setup time elapsing does not have a negative impact on ADC operation. See Figure 4 for the recommended signal condition during power-up. It is highly recommended to issue a software reset after power-up (see the Software Reset section for details).Conversion results are not guaranteed to meet data sheet specifications during this time, however.

Table 10. Signal Chain Components

Companion Devices	Part Name	Description	Typical Application
ADC Driver	ADA4896-2	1 nV/√Hz, rail-to-rail output amplifier	Precision, low noise, high frequency
	ADA4940-2	Ultra low power, full differential, low distortion amplifier	Precision, low density, low power
	ADA4807-2	1 mA, rail-to-rail output amplifier	Precision, low power, high frequency
External Reference	ADR4525	Ultralow noise, high accuracy voltage reference	2.5 V reference voltage
	ADR4533	Ultralow noise, high accuracy voltage reference	3.3 V reference voltage
Reference Buffer	ADA4807-2	1 mA, rail-to-rail output amplifier	Precision, low power, high frequency
LDO Regulator	ADP166	Very low quiescent, 150 mA, LDO regulator	3.0 V to 3.6 V supply for V_{CC} and V_{LOGIC}
	ADP7104	Low noise, CMOS, LDO regulator	5 V supply for driver amplifier
	ADP7182	Low noise line regulator	−2.5 V supply for ADC driver amplifier
	ADP5600	Interleaved inverting charge pump with negative LDO	Voltage inverter for negative supply

MODES OF OPERATION

The AD7381-4 has several on-chip configuration registers for controlling the operational mode of the device.

OVERSAMPLING

Oversampling is a common method used in analog electronics to improve the accuracy of the ADC result. Multiple samples of the analog input are captured and averaged to reduce the noise component from quantization noise and thermal noise (kTC noise) of the ADC. The AD7381-4 offers an oversampling function on-chip. The AD7381-4 has two user configurable oversampling modes: normal averaging and rolling average.

The oversampling functionality is configured by programming the OS_MODE bit and OSR bits in the Configuration 1 register.

Normal Averaging Oversampling

Normal averaging oversampling mode can be used in applications where slower output data rates are allowed and where higher SNR or dynamic range is desirable. Normal averaging involves taking a number of samples, adding them together and dividing the result by the number of samples taken. This result is then output from the device. The sample data is cleared when the process completes.

Normal averaging oversampling mode is configured by setting the OS_MODE bit to Logic 0 and having a valid nonzero value in the OSR bits. Writing to the OSR bits has a two-cycle latency before the register updates. That is, after writing to the OSR bits, two conversion cycles take place before the conversion results clock out with the updated OSR bits. The oversampling ratio of the digital filter is controlled using the oversampling bits, OSR (see Table 11). Table 11 provides the oversampling bit decoding to select the different oversample rates. The output result is decimated to 14-bit resolution. If required, additional resolution can be achieved by configuring the resolution boost bit (RES) in the Configuration 1 register. See the Resolution Boost section for further details.

The number of samples (n), defined by the OSR bits, are taken and added together, and the result is divided by n. The initial ADC conversion is initiated by the falling edge of $\overline{CS}$ and the AD7381-4 controls all subsequent samples in the oversampling sequence internally. The sampling rate of the additional n samples at the device maximum sampling rate is 4 MSPS. The data is ready for readback on the next serial interface access. After the averaging technique is applied, the sample data used in the calculation is discarded. This process is repeated every time the application needs a new conversion result and is initiated by the next falling edge of $\overline{CS}$.

As the output data rate is reduced by the oversampling ratio, the serial peripheral interface (SPI) SCLK frequency required to transmit the data is reduced accordingly.

Table 11. Normal Averaging Oversampling Overview

		SNR (dB Typical)				
		2.5 V Internal Reference		3.3 V External Reference		
OSR, Bits[2:0]	OS Ratio	RES = 0	RES = 1	RES = 0	RES = 1	Data Output Rate (kSPS Maximum)
000	No OS	85	85	85	85.2	4000
001	2	85	88	85	88.2	1500
010	4	85	91.1	85	91.3	750
011	8	85	93	85.5	93.1	375
100	16	85.7	94.6	85.7	94.4	187.5
101	32	85.9	95.6	85.8	95.5	93.75
110	Invalid	Not applicable	Not applicable	Not applicable	Not applicable	Not applicable
111	Invalid	Not applicable	Not applicable	Not applicable	Not applicable	Not applicable

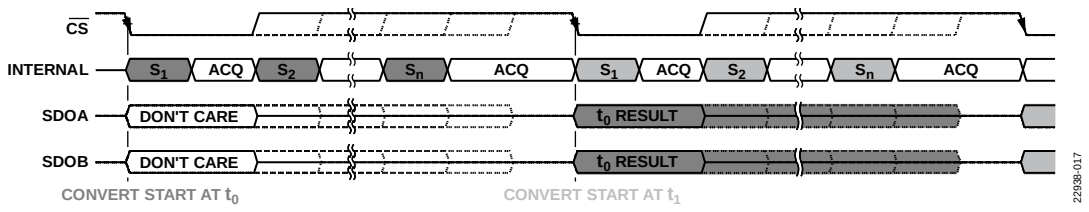


Figure 32. Normal Averaging Oversampling Operation

Rolling Average Oversampling

Rolling average oversampling mode can be used in applications where higher output data rates are required and where a higher SNR or dynamic range is desirable. Rolling averaging involves taking a number of samples, adding them together, and dividing the result by the number of samples taken. This result is then output from the device. The sample data is not cleared when the process completes. The rolling oversampling mode uses a first in, first out (FIFO) buffer of the most recent samples in the averaging calculation, allowing the ADC throughput rate and output data rate to stay the same.

Rolling average oversampling mode is configured by setting the OS_MODE bit to Logic 1 and having a valid nonzero value in the OSR bits. The oversampling ratio of the digital filter is controlled using the oversampling bits, OSR (see Table 12). Table 12 provides the oversampling bit decoding to select the different oversample rates. The output result is decimated to 16-bit resolution for the AD7381-4. If required, additional resolution can be achieved by configuring the resolution boost bit in the Configuration 1 register. See the Resolution Boost section for further details.

In rolling average oversampling mode, all ADC conversions are controlled and initiated by the falling edge of $\overline{CS}$. When a conversion is complete, the result is loaded into the FIFO. The FIFO length is 8, regardless of the oversampling ratio set. The FIFO is filled on the first conversion after a power-on reset (POR), on the first conversion after a software controlled hard or soft reset, or on the first conversion after the REFSEL bit is toggled. A new conversion result is shifted into the FIFO on completion of every ADC conversion regardless of the status of the OSR bits and the OS_MODE bit. This conversion allows a seamless transition from no oversampling to rolling average oversampling, or different rolling average oversampling ratios without waiting for the FIFO to fill.

The number of samples, n, defined by the OSR bits are taken from the FIFO, added together and the result is divided by n.

Table 12. Rolling Average Oversampling Overview

		SNR (dB Typical)				
		2.5 V External Reference		3.3 V External Reference		Data Output Rate
OSR, Bits[2:0][1]	OS Ratio	RES = 0	RES = 1	RES = 0	RES = 1	(kSPS Maximum)
000	No OS	84.4	84.8	84.2	85.2	4000
001	2	84.4	87.6	84.5	88.0	4000
010	4	84.9	90.4	85.0	90.9	4000
011	8	85.3	92.3	85.4	92.8	4000
1XX	Invalid	Not applicable	Not applicable	Not applicable	Not applicable	Not applicable

[1] X means don't care.

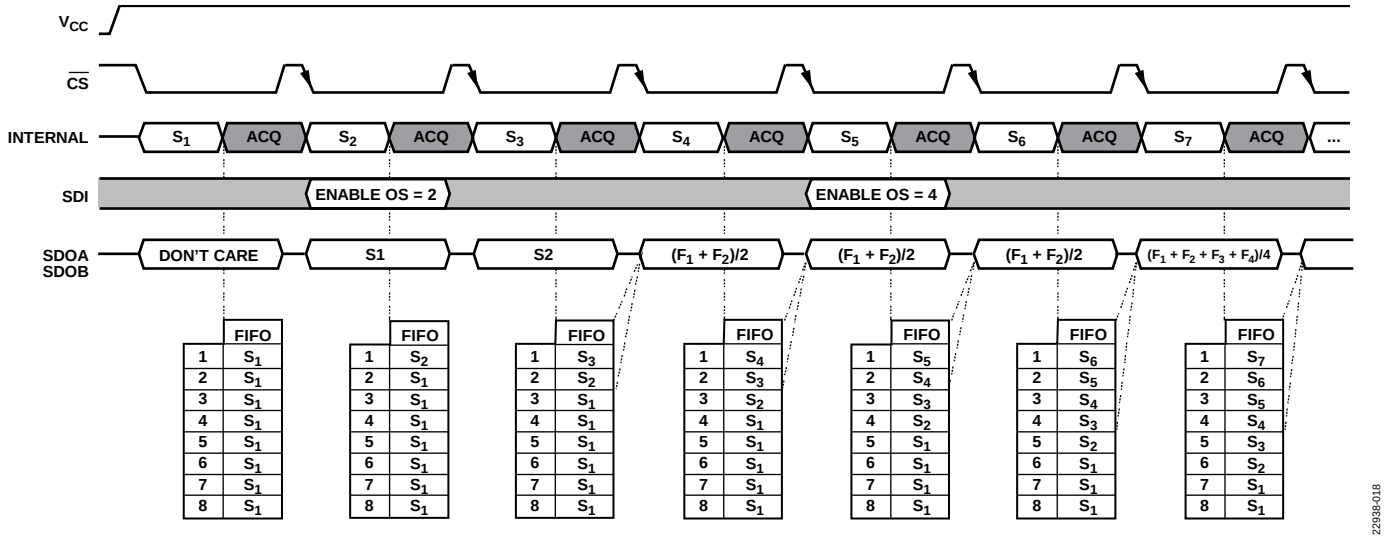


Figure 33. Rolling Average Oversampling Mode Configuration

RESOLUTION BOOST

The default resolution and output data size for the AD7381-4 is 14 bits. When the on-chip oversampling function is enabled the performance of the ADC can exceed the default resolution. To accommodate the performance boost achievable, it is possible to enable an additional two bits of resolution. If the RES bit in the Configuration 1 register is set to Logic 1 and the AD7381-4 is in a valid oversampling mode, the conversion result size for the AD7381-4 is 16-bit. In this mode, 16 SCLK cycles are required to propagate the data for the AD7381-4.

ALERT

The alert functionality is an out of range indicator and can be used as an early indicator of an out of bounds conversion result. An alert event triggers when the value in the conversion result register exceeds the alert high limit value in the alert high threshold register or falls below the alert low limit value in the alert low threshold register. The alert high threshold register and the alert low threshold register are common to all ADCs. When setting the threshold limits, the alert high threshold must always be greater than the alert low threshold. Detailed alert information is accessible in the alert indication register.

The register contains two status bits per ADC, one corresponding to the high limit, and the other to the low limit. A logical OR of alert signals for all ADCs creates a common alert value. This value can be configured to drive out on the $\overline{\text{ALERT}}$ function of the SDOD/$\overline{\text{ALERT}}$ pin. The SDOD/$\overline{\text{ALERT}}$ pin is configured as $\overline{\text{ALERT}}$ by configuring the following bits in the Configuration 1 register and Configuration 2 register:

- Set the SDO bits to any value other than 0b00.
- Set the ALERT_EN bit to 1.
- Set a valid value in the alert high threshold register and the alert low threshold register.

The alert indication function is available in oversampling (rolling average, normal averaging, and in nonoversampling modes).

The alert function of the SDOD/$\overline{\text{ALERT}}$ pin updates at the end of conversion. The alert indication status bits in the $\overline{\text{ALERT}}$ register are updated as well and must be read before the end of the next conversion.

Bits[7:0] in the alert indication register are cleared by reading the alert indication register contents. The alert function of the SDOD/$\overline{\text{ALERT}}$ pin is cleared with a falling edge of $\overline{\text{CS}}$. Issuing a software reset also clears the alert status in the alert indication register.

See Figure 8 for the $\overline{\text{ALERT}}$ timing diagram.

POWER MODES

The AD7381-4 has two power modes that can be set in the Configuration 1 register: normal mode and shutdown mode. These modes of operation provide flexible power management options, allowing optimization of the power dissipation and throughput rate ratio for different application requirements.

Program the PMODE bit in the Configuration 1 register to configure the power modes in the AD7381-4. Set PMODE to Logic 0 for normal mode and Logic 1 for shutdown mode.

Normal Mode

Keep the AD7381-4 in normal mode to achieve the fastest throughput rate. All blocks within the AD7381-4 always remain fully powered and an ADC conversion can be initiated by a falling edge of $\overline{\text{CS}}$ when required. When the AD7381-4 is not converting, it is in static mode and power consumption is automatically reduced. Additional current is required to perform a conversion. Therefore, power consumption of the AD7381-4 scales with throughput.

Shutdown Mode

When slower throughput rates and lower power consumption are required, use shutdown mode by either powering down the ADC between each conversion or by performing a series of conversions at a high throughput rate and then powering down the ADC for a relatively long duration between these burst conversions. When the AD7381-4 is in shutdown mode, all analog circuitry powers down. The serial interface remains active during shutdown mode to allow the AD7381-4 to exit shutdown mode.

To enter shutdown mode, write to the power mode configuration bit, PMODE, in the Configuration 1 register.

The AD7381-4 shuts down, and current consumption reduces. To exit shutdown mode and return to normal mode, set the PMODE bit in the Configuration 1 register to Logic 0. All register configuration settings remain unchanged entering or leaving shutdown mode. After exiting shutdown mode, allow sufficient time for the circuitry to turn on before starting a conversion.

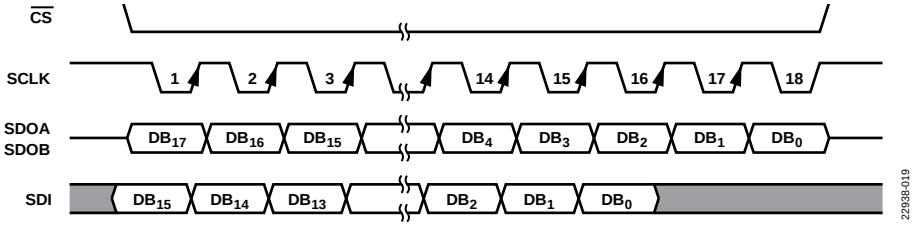


Figure 34. Resolution Boost

INTERNAL/EXTERNAL REFERENCE

The AD7381-4 has a 2.5 V internal reference with a buffer. Alternatively, if a more accurate reference or dynamic range is required, an external can be supplied. An externally supplied reference can be in the range of 2.5 V to 3.3 V.

Reference selection, internal or external, is configured by the REFSEL bit in the Configuration 1 register. If REFSEL is set to 0, the internal reference buffer is enabled. If an external reference is preferred, the REFSEL bit must be set to 1, and an external reference must be supplied to the REFIO pin.

SOFTWARE RESET

The AD7381-4 has two reset modes: a soft reset and a hard reset. A reset is initiated by writing to the reset bits in the Configuration 2 register.

A soft reset maintains the contents of the configurable registers but refreshes the interface and the ADC blocks. Any internal state machines are reinitialized, and the oversampling block and FIFO are flushed. The alert indication register is cleared. The reference and LDO regulator remain powered.

A hard reset, in addition to the blocks reset by a soft reset, resets all user registers to the default status, resets the reference buffer, and resets the internal oscillator block.

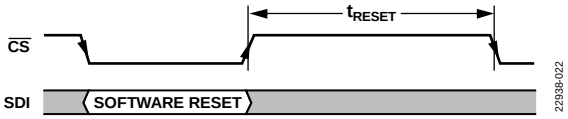


Figure 35. Software Reset Operation

DIAGNOSTIC SELF TEST

The AD7381-4 runs a diagnostic self test after a POR or after a software hard reset to ensure the correct configuration is loaded into the device.

The result of the self test is displayed in the SETUP_F bit in the alert indication register. If the SETUP_F bit is set to Logic 1, the diagnostic self test has failed. If the test fails, perform a software hard reset to reset the AD7381-4 registers to the default status.

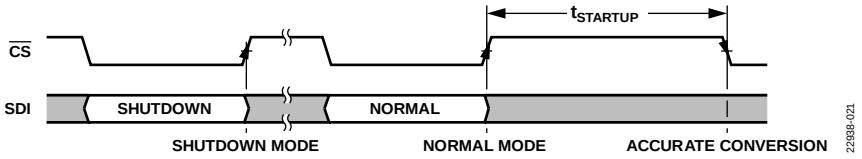


Figure 36. Shutdown Mode Operation

INTERFACE

The interface to the AD7381-4 is via a serial interface. The interface consists of $\overline{CS}$, SCLK, SDOA, SDOB, SDOC, and SDOD, and SDI. When referencing a single function of a multifunction pin, only the portion of the pin name that is relevant to the specification is listed, such as SDOD. For full pin names of multifunction pins, refer to the Pin Configuration and Function Descriptions section.

The $\overline{CS}$ signal frames a serial data transfer and initiates an ADC conversion process. The falling edge of $\overline{CS}$ puts the track-and-hold into hold mode, at which point the analog input is sampled and the bus is taken out of three-state. The ADC conversion operation is driven internally by an on-board oscillator and is independent of the SCLK signal.

The SCLK signal synchronizes data in and out of the device via the SDOA, SDOB, SDOC, SDOD, and SDI signals. A minimum of 14 SCLK cycles are required for a write to or read from a register. The minimum numbers of SCLKs for a conversion read is dependent on the resolution of the device and the configuration settings (see Table 13).

The ADC conversion operation is driven internally by an on-board oscillator and is independent of the SCLK signal.

The AD7381-4 has four serial output signals: SDOA, SDOB, SDOC, and SDOD. Programming the SDO bits in the Configuration 2 register configures 2-wire, 1-wire, or 4-wire mode. To achieve the highest throughput of the device, it is required to use either the 2-wire or 4-wire mode to read the conversion results. If a reduced throughput is required or oversampling is used, it is possible to use 1-wire mode, SDOA signal only, for reading conversion results.

Configuring cyclic redundancy check (CRC) operation for SPI reads, SPI writes, and oversampling mode with resolution boost mode enabled can alter the operation of the interface. Refer to the CRC section to ensure correct operation.

READING CONVERSION RESULTS

The $\overline{CS}$ signal initiates the conversion process. A high to low transition on the $\overline{CS}$ signal initiates a simultaneous conversion of the four ADCs, ADC A, ADC B, ADC C, and ADC D. The AD7381-4 has a one-cycle readback latency. Therefore, the conversion results are available on the next SPI access. Then, take the $\overline{CS}$ signal low, and the conversion result clocks out on the serial data output pins. The next conversion is also initiated at this point.

The conversion result is shifted out of the device as a 14-bit result for the AD7381-4. The MSB of the conversion result is shifted out on the $\overline{CS}$ falling edge. The remaining data is shifted out of the device under the control of the serial clock (SCLK) input. The data is shifted out on the rising edge of SCLK, and the data bits are valid on both the falling edge and the rising edge. After the final SCLK falling edge, take $\overline{CS}$ high again to return the serial data output pins to a high impedance state.

The number of SCLK cycles to propagate the conversion results on the serial data output pins is dependent on the serial mode of operation configured and if resolution boost mode is enabled (see Figure 37 and Table 13 for details). If CRC reading is enabled, additional SCLK pulses are required to propagate the CRC information. See the CRC section for more details.

Because the $\overline{CS}$ signal initiates a conversion as well as framing the data, any data access must be completed within a single frame.

Table 13. Number of SCLK Cycles (n) Required for Reading Conversion Results

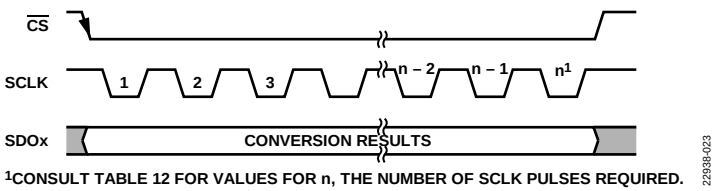
Interface Configuration	Resolution Boost Mode	CRC Read	No. of SCLK Cycles
4-Wire	Disabled	Disabled	14
		Enabled	22
	Enabled	Disabled	16
		Enabled	24
2-Wire	Disabled	Disabled	28
		Enabled	36
	Enabled	Disabled	32
		Enabled	40
1-Wire	Disabled	Disabled	56
		Enabled	64
	Enabled	Disabled	64
		Enabled	72

Serial 4-Wire Mode

Configure 4-wire mode by setting the SDO bits to 0b10 in the Configuration 2 register. In 4-wire mode, the conversion results for ADC A is output on SDOA, ADC B on SDOB, ADC C on SDOC, and ADC D on SDOD.

Serial 2-Wire Mode

Configure 2-wire mode by setting the SDO bits to 0b00 in the Configuration 2 register. In 2-wire mode, the conversion results for ADC A and ADC C are output on SDOA. The conversion result for ADC B and ADC D are output on SDOB.



[1]CONSULT TABLE 12 FOR VALUES FOR n, THE NUMBER OF SCLK PULSES REQUIRED.

Figure 37. Reading Conversion Results

Serial 1-Wire Mode

In applications where slower throughput rates are allowed or normal averaging oversampling is used, the serial interface can be configured to operate in 1-wire mode. In 1-wire mode, the conversion results from ADC A, ADC B, ADC C, and ADC D are output on SDOA. Additional SCLK cycles are required to propagate all data. ADC A data is output first followed by the ADC B, ADC C, and ADC D conversion results.

LOW LATENCY READBACK

The interface on the AD7381-4 has a one-cycle latency as shown in Figure 38. For applications that operate at lower throughput rates the latency of reading the conversion result can be reduced. After the conversion time ($t_{CONVERT}$) elapses, a second $\overline{CS}$ pulse after the initial $\overline{CS}$ pulse that initiated the conversion can be used to read back the conversion result. This operation is shown in Figure 41.

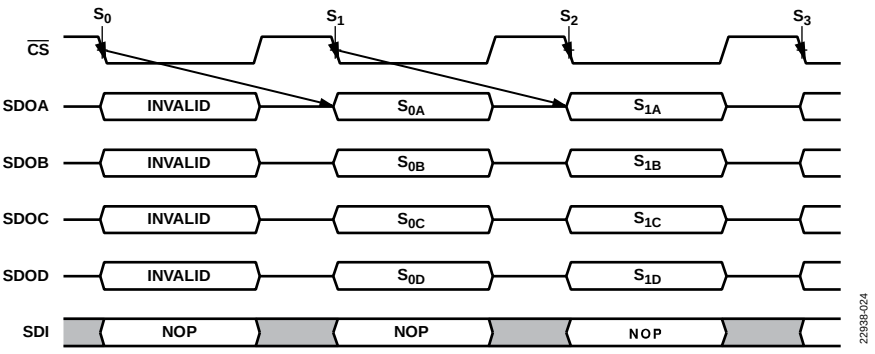


Figure 38. Read Conversion Results, 4-Wire Mode

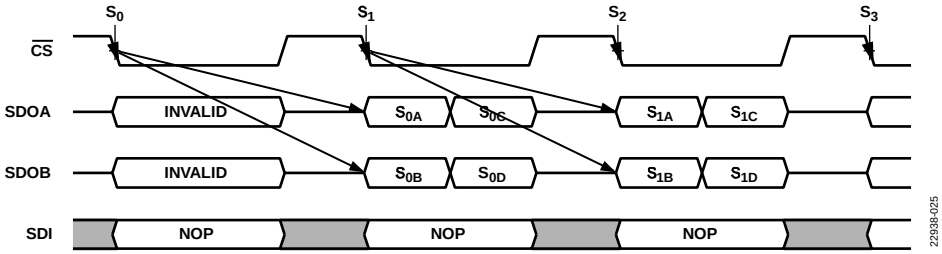


Figure 39. Reading Conversion Results, 2-Wire Mode

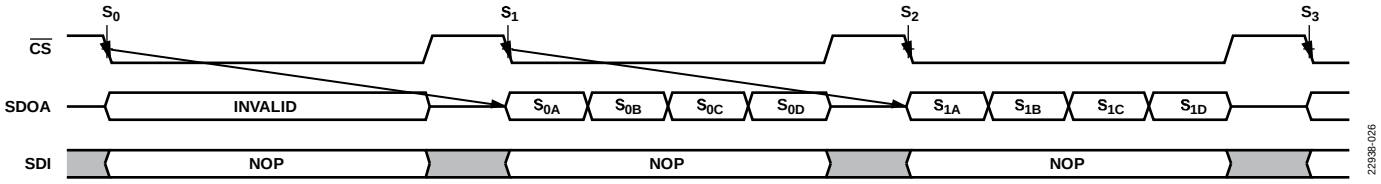


Figure 40. Read Conversion Results, 1-Wire Mode

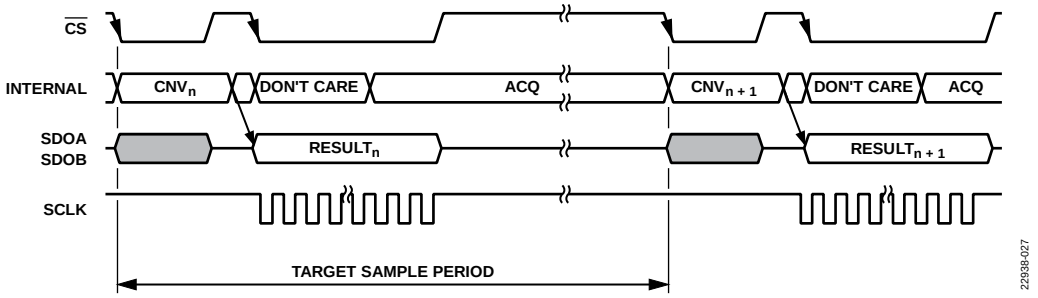


Figure 41. Low Throughput Low Latency

READING FROM DEVICE REGISTERS

All the registers in the device can be read over the serial interface. A register read is performed by issuing a register read command followed by an additional SPI command that can be either a valid command or no operation command (NOP). The format for a read command is shown in Table 16. Bit D15 must be set to 0 to select a read command. Bits[D14:D12] contain the register address. The subsequent 12 bits, Bits[D11:D0], are ignored.

WRITING TO DEVICE REGISTERS

All the read/write registers in the AD7381-4 can be written to over the serial interface. The length of a SPI write access is determined by the CRC write function. An SPI access is 16-bit if CRC write is disabled and 24-bit when CRC write is enabled. The format for a write command is shown in Table 16. Bit D15 must be set to 1 to select a write command. Bits[D14:D12] contain the register address. The subsequent 12 bits, Bits[D11:D0], contain the data to be written to the selected register.

CRC

The AD7381-4 has CRC checksum modes that can be used to improve interface robustness by detecting errors in data transmissions. The CRC feature is independently selectable for SPI interface reads and writes. For example, enable the CRC function for SPI writes to prevent unexpected changes to the device configuration but do not enable it on SPI reads to maintain a higher throughput rate. The CRC feature is controlled by programming of the CRC_W bit and CRC_R bit in the Configuration 1 register.

CRC Read

If enabled, a CRC consisting of an 8-bit word is appended to the conversion result or register reads. The CRC is calculated on the conversion result for ADC A, ADC B, ADC C, and ADC D, and is output on SDOA. A CRC is also calculated and appended to register read outputs.

The CRC read function can be used in 2-wire SPI mode, 1-wire SPI mode, 4-wire SPI mode, and resolution boost mode.

CRC Write

To enable the CRC write function the CRC_W bit in the Configuration 1 register must be set to 1. To set the CRC_W bit to 1 to enable the CRC feature, a valid CRC must be appended to the request frame.

After the CRC feature is enabled, all register write requests are ignored unless they are accompanied by a valid CRC command. A valid CRC is required to both enable and disable the CRC write feature.

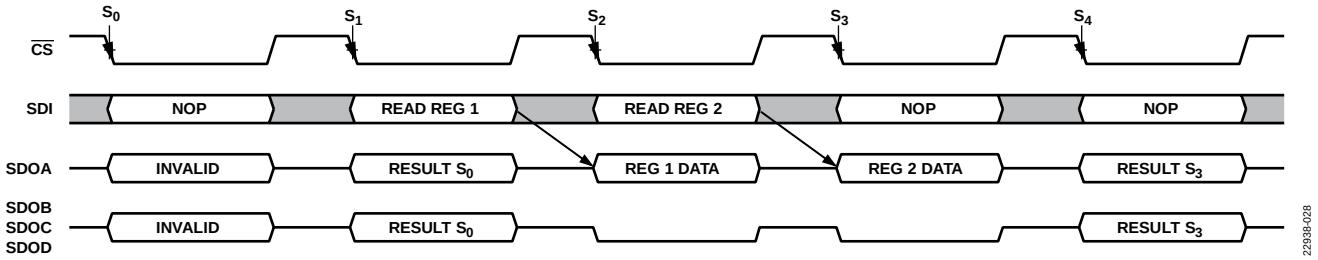


Figure 42. Register Read

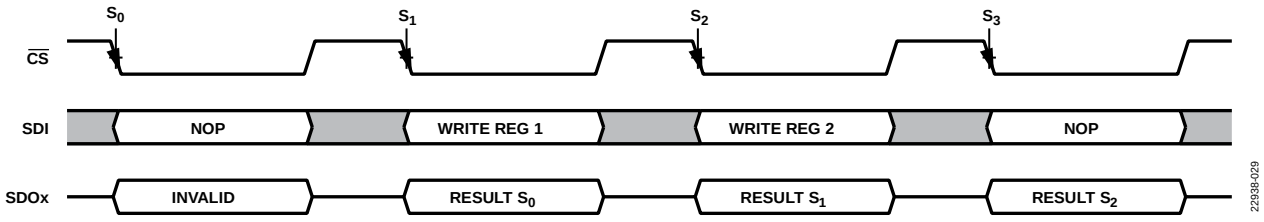


Figure 43. Register Write

CRC Polynomial

For CRC checksum calculations, the following polynomial is always used: $x^8 + x^2 + x + 1$.

To generate the checksum, the 14-bit data conversion result of the four channels are combined to produce a 56-bit data stream. The 8 MSBs of the 56-bit data are inverted and then the data is appended by eight bits to create a number ending in eight Logic 0s. The polynomial is aligned such that its MSB is adjacent to the leftmost Logic 1 of the data. An exclusive OR (XOR) function is applied to the data to produce a new, shorter number. The polynomial is again aligned such that its MSB is adjacent to the leftmost Logic 1 of the new result, and the procedure is repeated. This process repeats until the original data is reduced to a value less than the polynomial, which is the 8-bit checksum.

For example, the AD7381-4 polynomial is 100000111. Let the original data of four channels be 0xAAAA, 0x5555, 0xAAAA, and 0x5555. The eight MSBs of the data are inverted. The data is then appended to include eight 0s on right. In the final XOR operation, the reduced data is less than the polynomial. Therefore, the remainder is the CRC for the assumed data.

Table 14. Example CRC Calculation for 4-Channel, 16-Bit Data

Data	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**X**[1]	**X**[1]	**X**[1]	**X**[1]	**X**[1]	**X**[1]	**X**[1]	**X**[1]
Process Data	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
		1	0	0	0	0	0	1	1	1																														
				1	0	1	0	0	0	1	1	0																												
				1	0	0	0	0	0	1	1	1																												
						1	0	0	0	0	0	1	1	0																										
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																														1	0	0	1	0	0	0	0	0		
																														1	0	0	0	0	0	1	1	1		
CRC																																	1	0	0	1	1	1	0	0

[1] X means don't care.

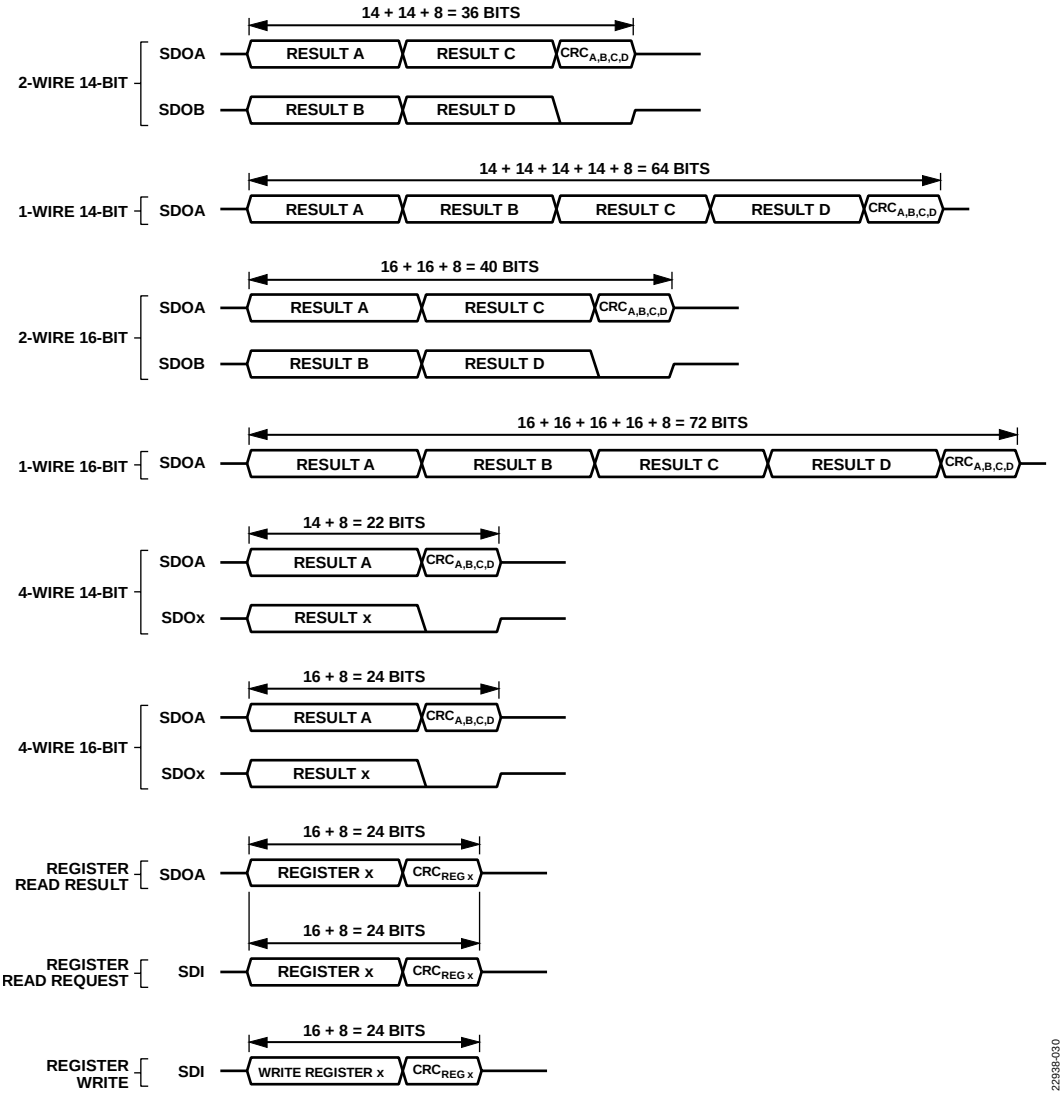


Figure 44. CRC Operation

REGISTERS

The AD7381-4 has user-programmable, on-chip registers for configuring the device. Table 15 shows a complete overview of the registers available on the AD7381-4.

The registers are either read/write (R/W) or read only (R). Any read request to a write only register is ignored. Any write to a read only register is ignored. Writes to the NOP registers and the reserved register are ignored. Any read request to the NOP registers or reserved registers are considered a no operation and the data transmitted in the next SPI frame are the conversion results.

Table 15. Register Description

Reg	Name	Bits	Bit 15 / Bit 7	Bit 14 / Bit 6	Bit 13 / Bit 5	Bit 12 / Bit 4	Bit 11 / Bit 3	Bit 10 / Bit 2	Bit 9 / Bit 1	Bit 8 / Bit 0	Reset	RW
0x1	Configuration 1	[15:8]	ADDRESSING				RESERVED		OS_MODE	OSR, Bit 2	0x0000	R/W
		[7:0]	OSR, Bits[1:0]		CRC_W	CRC_R	ALERT_EN	RES	REFSEL	PMODE		
0x2	Configuration 2	[15:8]	ADDRESSING				RESERVED		SDO		0x0000	R/W
		[7:0]	RESET									
0x3	Alert indication	[15:8]	ADDRESSING				RESERVED		CRCW_F	SETUP_F	0x0000	R
		[7:0]	AL_D_HIGH	AL_D_LOW	AL_C_HIGH	AL_C_LOW	AL_B_HIGH	AL_B_LOW	AL_A_HIGH	AL_A_LOW		
0x4	Alert low threshold	[15:8]	ADDRESSING				ALERT_LOW, Bits[11:8]				0x0800	R/W
		[7:0]	ALERT_LOW, Bits[7:0]									
0x5	Alert high threshold	[15:8]	ADDRESSING				ALERT_HIGH, Bits[11:8]				0x07FF	R/W
		[7:0]	ALERT_HIGH, Bits[7:0]									

ADDRESSING REGISTERS

A serial register transfer on the AD7381-4 consists of 16 SCLK cycles. The four MSBs written to the device are decoded to determine which register is addressed. The four MSBs consist of the register address (REGADDR), Bits[2:0], and the read/write bit (WR). The register address bits determine which on-chip register is selected. If the addressed register is a valid write register, the read/write bit determines whether the remaining 12 bits of data on the SDI input are loaded into the addressed register. If the WR bit is 1, the bits load into the register addressed by the register select bits. If the WR bit is 0, the command is seen as a read request. The addressed register data is available to be read during the next read operation.

Table 16. Addressing Register Format

MSB **LSB**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
WR	REGADDR, Bits[2:0]			Data, Bits[11:0]											

Table 17. Bit Descriptions for Addressing Registers

Bit	Mnemonic	Description
D15	WR	When a 1 is written to this bit, Bits[11:0] of this register are written to the register specified by REGADDR if it is a valid address. Alternatively, when a 0 is written, the next data sent out on the SDOA pin is a read from the designated register if it is a valid address.
D14 to D12	REGADDR	When WR = 1, the contents of REGADDR determine the register for selection as outlined in Table 15. When WR = 0 and the REGADDR bits contain a valid register address, the contents on the requested register are output on the SDOA pin during the next interface access. When WR = 0 and the REGADDR bits contain 0x0, 0x6, or 0x7, the contents on the SDI line are ignored. The next interface access results in the conversion results being read back.
D11 to D0	Data	These bits are written into the corresponding register specified by the REGADDR bits when the WR bit = 1 and the REGADDR bits contain a valid address.

CONFIGURATION 1 REGISTER

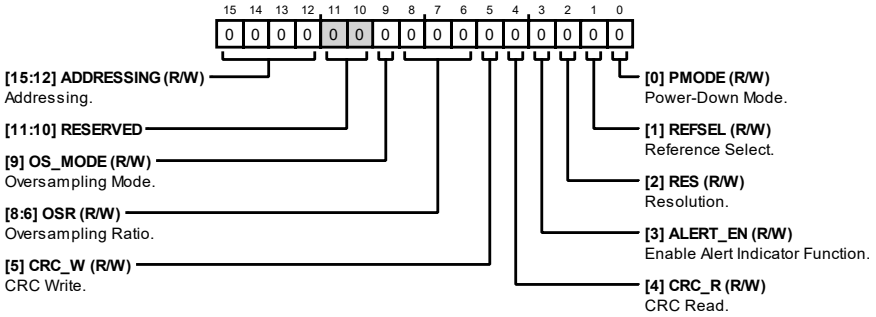


Table 18. Bit Descriptions for Configuration 1 Register

Bits	Bit Name	Description	Reset	Access
[15:12]	ADDRESSING	Addressing. Bits[15:12] define the address of the relevant register. See the Addressing Registers section for further details.	0x0	R/W
[11:10]	RESERVED	Reserved.	0x0	R
9	OS_MODE	Oversampling Mode. Sets the oversampling mode of the ADC. 0: normal averaging. 1: rolling average.	0x0	R/W
[8:6]	OSR	Oversampling Ratio. Sets the oversampling ratio for all the ADCs in the relevant mode. Normal averaging mode supports oversampling ratios of 2×, 4×, 8×, 16×, and 32×. Rolling average mode supports oversampling ratios of 2×, 4×, and 8×. 000: disabled. 001: 2×. 010: 4×. 011: 8×. 100: 16×. 101: 32×. 110: disabled. 111: disabled.	0x0	R/W
5	CRC_W	CRC Write. Controls the CRC functionality for the SDI interface When setting this bit from a 0 to a 1, the command must be followed by a valid CRC to set this configuration bit. If a valid CRC is not received, the entire frame is ignored. If the bit is set to 1, it requires a CRC to clear it to 0. 0: no CRC function. 1: CRC function.	0x0	R/W
4	CRC_R	CRC Read. Controls the CRC functionality for the SDOx interface 0: no CRC function. 1: CRC function.	0x0	R/W
3	ALERT_EN	Enable Alert Indicator Function. This bit functions when the SDO bits = 01. Otherwise, the ALERT_EN bit is ignored. 0: SDOB. 1: $\overline{\text{ALERT}}$.	0x0	R/W
2	RES	Resolution. Sets the size of the conversion result data. If OSR = 0 these bits are ignored and the resolution is set to default resolution. 0: normal resolution. 1: 2-bit higher resolution.	0x0	R/W
1	REFSEL	Reference Select. Selects the ADC reference source. 0: selects internal reference. 1: selects external reference.	0x0	R/W
0	PMODE	Power-Down Mode. Sets the power modes. 0: normal mode. 1: shutdown mode.	0x0	R/W

CONFIGURATION 2 REGISTER

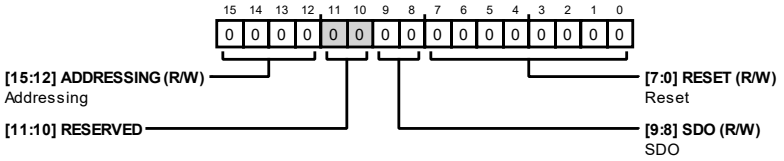


Table 19. Bit Descriptions for Configuration 2 Register

Bits	Bit Name	Description	Reset	Access
[15:12]	ADDRESSING	Addressing. Bits[15:12] define the address of the relevant register. See the Addressing Registers section for further details.	0x0	R/W
[11:10]	RESERVED	Reserved.	0x0	R
[9:8]	SDO	SDO. Conversion Results Serial Data Output 00: 2-wire. Conversion data are output on both SDOA and SDOB. 01: 1-wire. Conversion data are output on SDOA only. 10: 4-wire. Conversion data are output on SDOA, SDOB, SDOC, and SDOD/$\overline{\text{ALERT}}$. 11: 1-wire. Conversion data are output on SDOA only.	0x0	R/W
[7:0]	RESET	Reset. 0x3C: performs a soft reset. Refreshes some blocks. Register contents remain unchanged. Clears alert indication register and flushes any oversampling stored variables or active state machine. 0xFF: performs a hard reset. Resets all possible blocks in the device. Registers contents are set to defaults. All other values are ignored.	0x0	R/W

ALERT INDICATION REGISTER

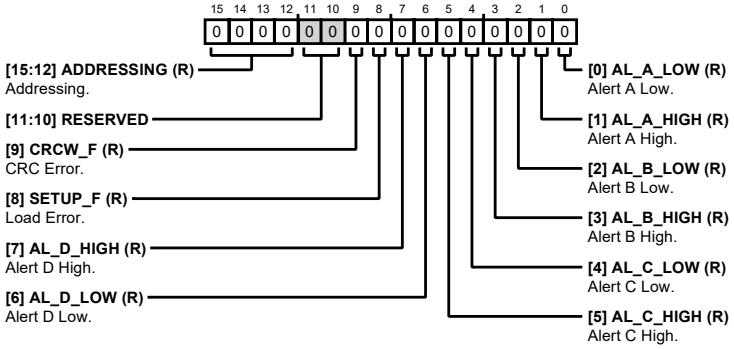


Table 20. Bit Descriptions for Alert Indication Register

Bits	Bit Name	Description	Reset	Access
[15:12]	ADDRESSING	Addressing. Bits[15:12] define the address of the relevant register. See the Addressing Registers section for further details.	0x0	R
[11:10]	RESERVED	Reserved.	0x0	R
9	CRCW_F	CRC Error. Indicates that a register write command failed due to a CRC error. This fault bit is sticky and remains set until the register is read 0: no CRC error. 1: CRC error.	0x0	R
8	SETUP_F	Load Error. The SETUP_F indicates that the device configuration data did not load correctly on startup. This bit does not clear on an alert indication register read. A hard reset via the Configuration 2 register is required to clear this bit and restart the device setup again. 0: no setup error. 1: setup error.	0x0	R
7	AL_D_HIGH	Alert D High. The alert indication high bit indicates if a conversion result for the respective input channel exceeds the value set in the alert high threshold register. This fault bit is sticky and remains set until the register is read. 1: alert indication. 0: no alert indication.	0x0	R

Bits	Bit Name	Description	Reset	Access
6	AL_D_LOW	Alert D Low. The alert indication low bit indicates if a conversion result for the respective input channel exceeds the value set in the alert low threshold register. This fault bit is sticky and remains set until the register is read. 0: no alert indication. 1: alert indication.	0x0	R
5	AL_C_HIGH	Alert C High. The alert indication high bit indicates if a conversion result for the respective input channel exceeds the value set in the alert high threshold register. This fault bit is sticky and remains set until the register is read. 1: alert indication. 0: no alert indication.	0x0	R
4	AL_C_LOW	Alert C Low. The alert indication low bit indicates if a conversion result for the respective input channel exceeds the value set in the alert low threshold register. This fault bit is sticky and remains set until the register is read. 1: alert indication. 0: no alert indication.	0x0	R
3	AL_B_HIGH	Alert B High. The alert indication high bit indicates if a conversion result for the respective input channel exceeds the value set in the alert high threshold register. This fault bit is sticky and remains set until the register is read. 1: alert indication. 0: no alert indication.	0x0	R
2	AL_B_LOW	Alert B Low. The alert indication low bit indicates if a conversion result for the respective input channel exceeds the value set in the alert low threshold register. This fault bit is sticky and remains set until the register is read. 1: alert indication. 0: no alert indication.	0x0	R
1	AL_A_HIGH	Alert A High. The alert indication high bit indicates if a conversion result for the respective input channel exceeds the value set in the alert high threshold register. This fault bit is sticky and remains set until the register is read. 0: no alert indication. 1: alert indication.	0x0	R
0	AL_A_LOW	Alert A Low. The alert indication low bit indicates if a conversion result for the respective input channel exceeds the value set in the alert low threshold register. This fault bit is sticky and remains set until the register is read. 1: alert indication. 0: no alert indication.	0x0	R

ALERT LOW THRESHOLD REGISTER

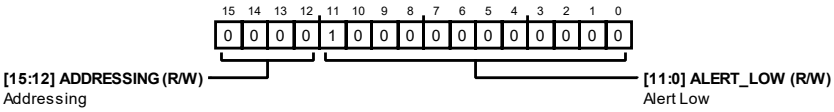


Table 21. Bit Descriptions for Alert Low Threshold Register

Bits	Bit Name	Description	Reset	Access
[15:12]	ADDRESSING	Addressing. Bits[15:12] define the address of the relevant register. See the Addressing Registers section for further details.	0x0	R/W
[11:0]	ALERT_LOW	Alert Low. Bits[11:0] from ALERT_LOW move to the MSBs of the internal alert low register, D[15:4]. The remaining bits, D[3:0] of the internal register are fixed at 0x0. Sets an alert when the converter result is below the value in the alert low threshold register, and the alert is disabled when it is above the value in the alert low threshold register.	0x800	R/W

ALERT HIGH THRESHOLD REGISTER

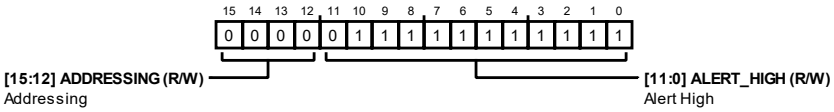
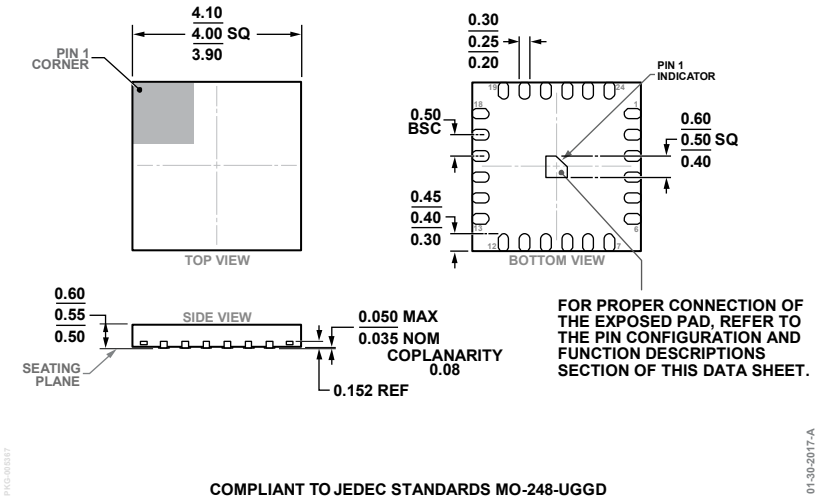


Table 22. Bit Descriptions for Alert High Threshold Register

Bits	Bit Name	Description	Reset	Access
[15:12]	ADDRESSING	Addressing. Bits[15:12] define the address of the relevant register. See the Addressing Registers section for further details.	0x0	R/W
[11:0]	ALERT_HIGH	Alert High. Bits D[11:0] from ALERT_HIGH move to the MSBs of the internal alert high register, D[15:4]. The remaining bits, D[3:0] of the internal are fixed at 0xF. Sets an alert when the converter result is above the value in the alert high threshold register, and the alert is disabled when it is below the value in the alert high threshold register.	0x7FF	R/W

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-248-UGGD

Figure 45. 24-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.55 mm Package Height
(CP-24-25)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2, 3]	Resolution	Temperature Range	Package Description	Package Option
AD7381-4BCPZ	14-Bit	−40°C to +125°C	24-Lead Lead Frame Chip Scale Package [LFCSP]	CP-24-25
AD7381-4BCPZ-RL	14-Bit	−40°C to +125°C	24-Lead Lead Frame Chip Scale Package [LFCSP]	CP-24-25
AD7381-4BCPZ-RL7	14-Bit	−40°C to +125°C	24-Lead Lead Frame Chip Scale Package [LFCSP]	CP-24-25
EVAL-AD7380-4FMCZ			AD7380-4 Evaluation Board	
EVAL-SDP-CH1Z			Evaluation Board Controller	

[1] Z = RoHS Compliant Part.
[2] The EVAL-AD7380-4FMCZ is configurable to use with the AD7381-4.
[3] The EVAL-AD7380-4FMCZ is compatible with the EVAL-SDP-CH1Z high speed controller board.

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