

MITSUBISHI MICROCOMPUTERS 3850 Group (Spec. H)

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The 3850 group (spec. H) is the 8-bit microcomputer based on the 740 family core technology.

The 3850 group (spec. H) is designed for the household products and office automation equipment and includes serial I/O functions, 8-bit timer, and A-D converter.

FEATURES

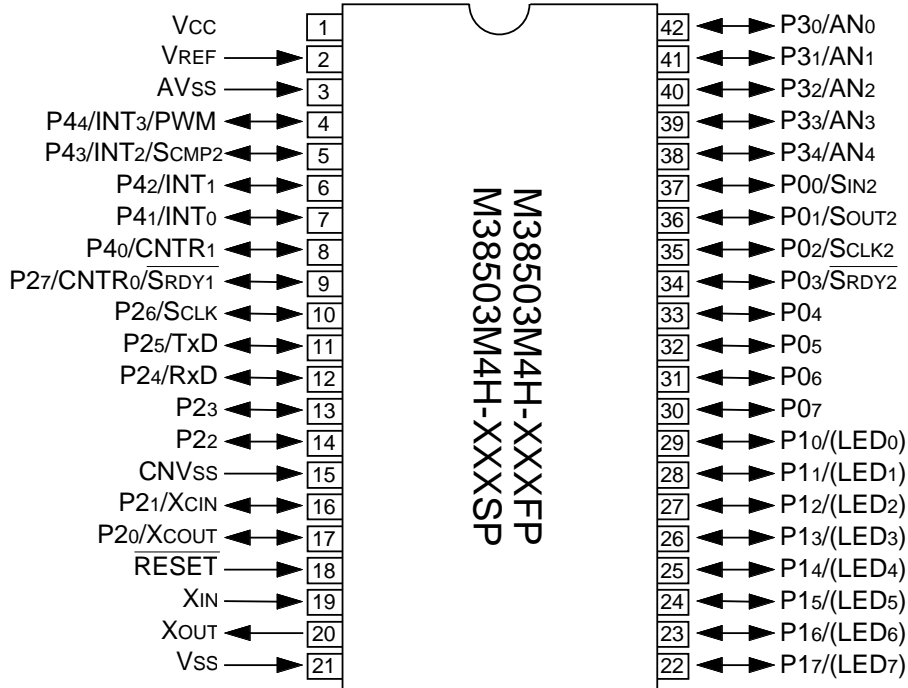
- Basic machine-language instructions 71
- Minimum instruction execution time 0.5 μ s
(at 8 MHz oscillation frequency)
- Memory size
 - ROM 8K to 32K bytes
 - RAM 512 to 1024 bytes
- Programmable input/output ports 34
- Interrupts 14 sources, 14 vectors
- Timers 8-bit X 4
- Serial I/O1 8-bit X 1 (UART or Clock-synchronized)
- Serial I/O2 8-bit X 1 (Clock-synchronized)
- PWM 8-bit X 1
- A-D converter 10-bit X 5 channels
- Watchdog timer 16-bit X 1
- Clock generating circuit Built-in 2 circuits
(connect to external ceramic resonator or quartz-crystal oscillator)

- Power source voltage
 - In high-speed mode 4.0 to 5.5 V
(at 8 MHz oscillation frequency)
 - In middle-speed mode 2.7 to 5.5 V
(at 8 MHz oscillation frequency)
 - In low-speed mode 2.7 to 5.5 V
(at 32 kHz oscillation frequency)
- Power dissipation
 - In high-speed mode 34 mW
(at 8 MHz oscillation frequency, at 5 V power source voltage)
 - In low-speed mode 60 μ W
(at 32 kHz oscillation frequency, at 3 V power source voltage)
- Operating temperature range -20 to 85°C

APPLICATION

Office automation equipment, FA equipment, Household products, Consumer electronics, etc.

PIN CONFIGURATION (TOP VIEW)

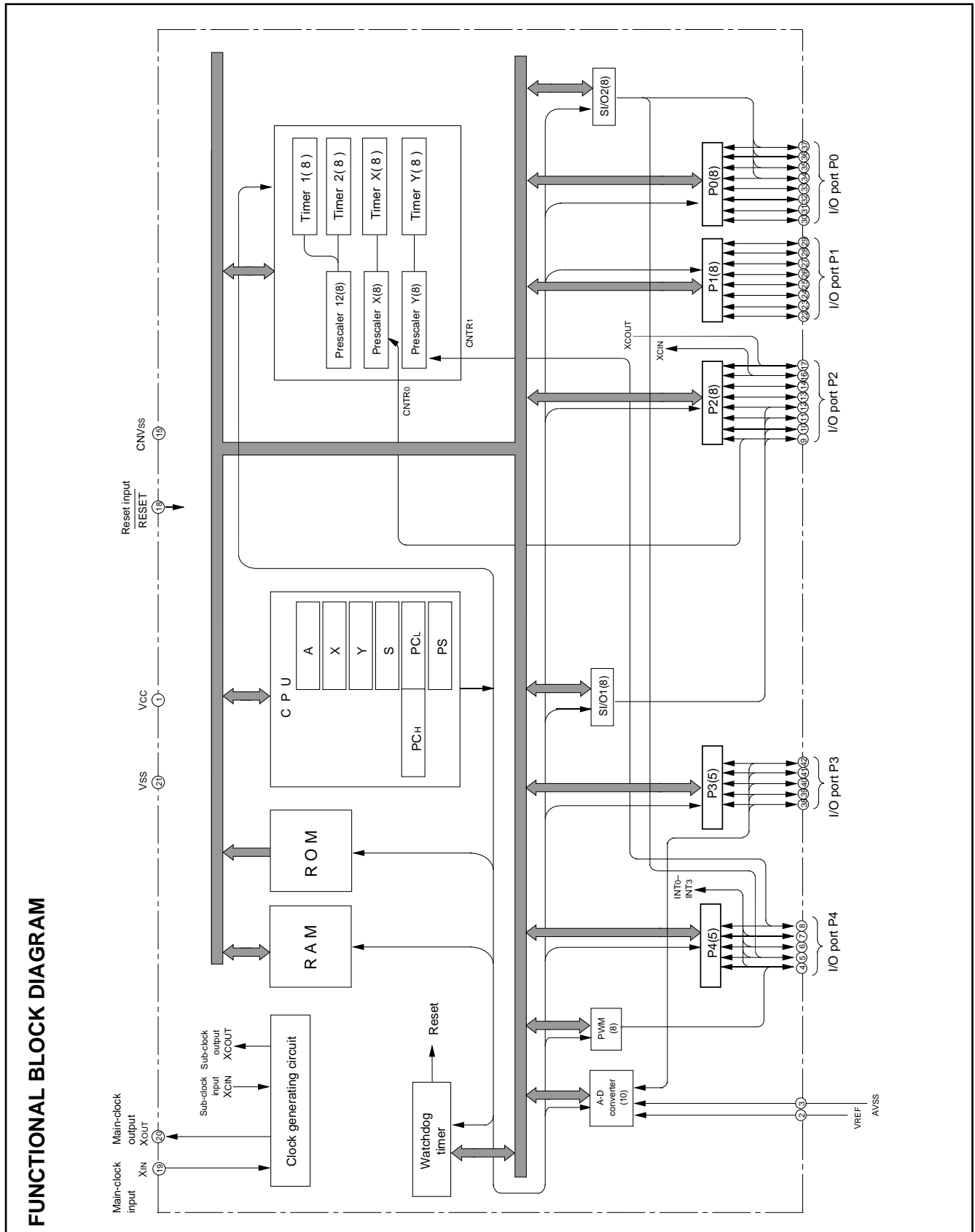


Package type : FP 42P2R-A/E (42-pin plastic-molded SSOP)

Package type : SP 42P4B (42-pin plastic-molded SDIP)

Fig. 1 M38503M4H-XXXXFP/SP pin configuration

FUNCTIONAL BLOCK



FUNCTIONAL BLOCK DIAGRAM

Fig. 2 Functional block diagram

PIN DESCRIPTION

Table 1 Pin description

Pin	Name	Functions	Function except a port function
VCC, VSS	Power source	<ul style="list-style-type: none"> Apply voltage of 2.7 V – 5.5 V to Vcc, and 0 V to Vss. 	
CNVSS	CNVSS input	<ul style="list-style-type: none"> This pin controls the operation mode of the chip. Normally connected to VSS. 	
RESET	Reset input	<ul style="list-style-type: none"> Reset input pin for active “L.” 	
XIN	Clock input	<ul style="list-style-type: none"> Input and output pins for the clock generating circuit. Connect a ceramic resonator or quartz-crystal oscillator between the XIN and XOUT pins to set the oscillation frequency. 	
XOUT	Clock output	<ul style="list-style-type: none"> When an external clock is used, connect the clock source to the XIN pin and leave the XOUT pin open. 	
P00/SIN2 P01/SOUT2 P02/SCLK2 P03/SRDY2 P04–P07	I/O port P0	<ul style="list-style-type: none"> 8-bit CMOS I/O port. I/O direction register allows each pin to be individually programmed as either input or output. CMOS compatible input level. CMOS 3-state output structure. 	<ul style="list-style-type: none"> Serial I/O2 function pin
P10–P17	I/O port P1	<ul style="list-style-type: none"> P10 to P17 (8 bits) are enabled to output large current for LED drive. 	
P20/XCOUT P21/XCIN P22 P23 P24/RxD P25/TxD P26/SCLK P27/CNTR0/ SRDY1	I/O port P2	<ul style="list-style-type: none"> 8-bit CMOS I/O port. I/O direction register allows each pin to be individually programmed as either input or output. CMOS compatible input level. P20, P21, P24 to P27: CMOS3-state output structure. P22, P23: N-channel open-drain structure. 	<ul style="list-style-type: none"> Sub-clock generating circuit I/O pins (connect a resonator) Serial I/O1 function pin Serial I/O1 function pin/ Timer X function pin
P30/AN0– P34/AN4	I/O port P3	<ul style="list-style-type: none"> 8-bit CMOS I/O port with the same function as port P0. CMOS compatible input level. CMOS 3-state output structure. 	<ul style="list-style-type: none"> A-D converter input pin
P40/CNTR1 P41/INT0 P42/INT1 P43/INT2/SCMP2 P44/INT3/PWM	I/O port P4	<ul style="list-style-type: none"> 8-bit CMOS I/O port with the same function as port P0. CMOS compatible input level. CMOS 3-state output structure. 	<ul style="list-style-type: none"> Timer Y function pin Interrupt input pins Interrupt input pin SCMP2 output pin Interrupt input pin PWM output pin

PART NUMBERING

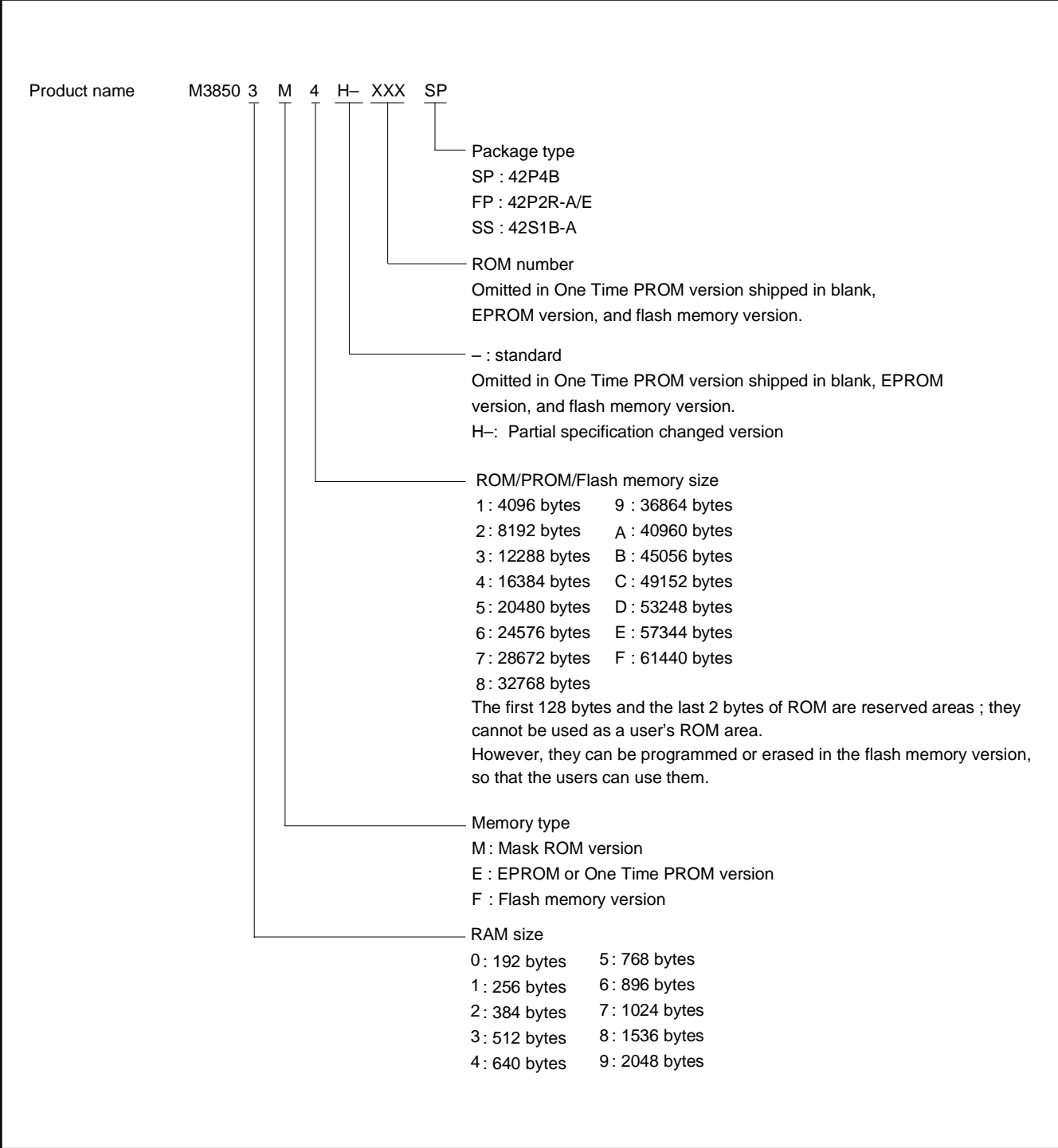


Fig. 3 Part numbering

GROUP EXPANSION

Mitsubishi plans to expand the 3850 group (spec. H) as follows.

Memory Type

Support for mask ROM, One Time PROM, and flash memory versions.

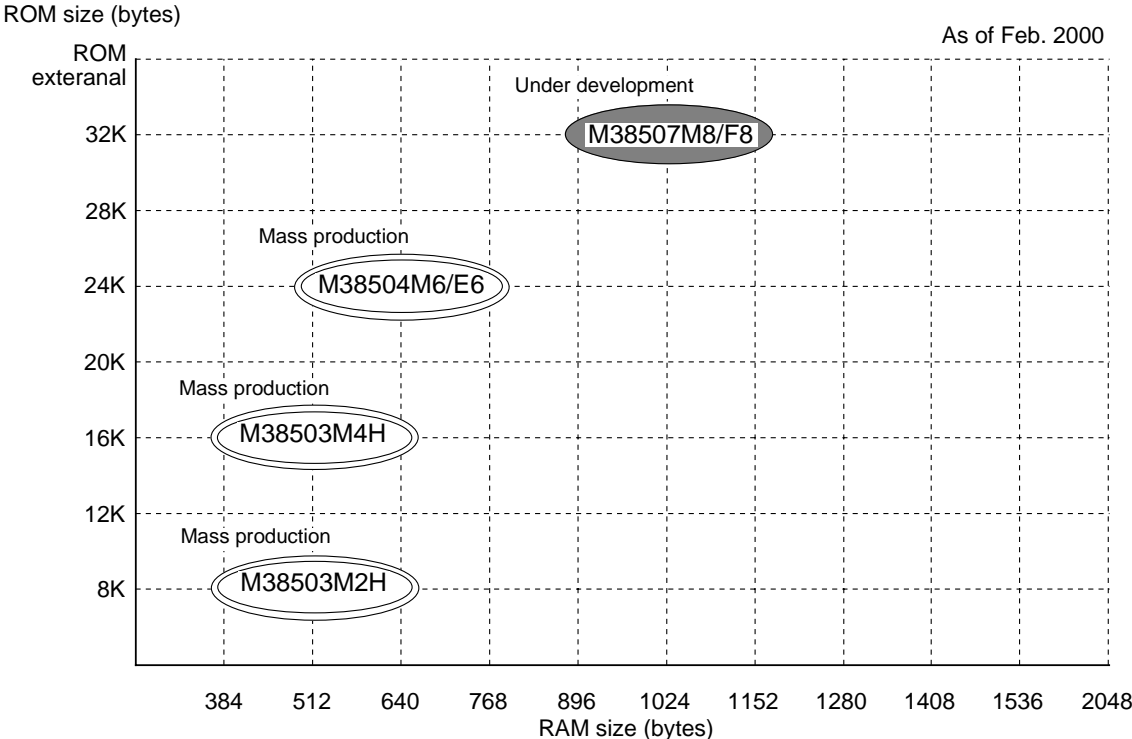
Memory Size

- Flash memory size 32 K bytes
- One Time PROM size 24 K bytes
- Mask ROM size 8 K to 32 K bytes
- RAM size 512 to 1 K bytes

Packages

- 42P4B 42-pin shrink plastic-molded DIP
- 42P2R-A/E 42-pin plastic-molded SOP
- 42S1B-A 42-pin shrink ceramic DIP (EPROM version)

Memory Expansion Plan



Products under development or planning: the development schedule and specification may be revised without notice. The development of planning products may be stopped.

Fig. 4 Memory expansion plan

Currently planning products are listed below.

Table 2 Support products

As of Feb. 2000

Product name	ROM size (bytes) ROM size for User in ()	RAM size (bytes)	Package	Remarks
M38503M2H-XXXSP	8192 (8062)	512	42P4B	Mask ROM version
M38503M2H-XXXFP			42P2R-A/E	Mask ROM version
M38503M4H-XXXSP	16384 (16254)	512	424P4B	Mask ROM version
M38503M4H-XXXFP			42P2R-A/E	Mask ROM version
M38504M6-XXXSP	24576 (24446)	640	424P4B	Mask ROM version
M38504E6-XXXSP				One Time PROM version
M388504E6SP				One Time PROM version (blank)
M388504E6SS			42S1B-A	EPROM version
M38504M6-XXXFP			42P2R-A/E	Mask ROM version
M38504E6-XXXFP				One Time PROM version
M38504E6FP				One Time PROM version (blank)
				One Time PROM version (blank)

Table 3 3850 group (standard) and 3850 group (spec. H) corresponding products

3850 group (standard)	3850 group (spec. H)
M38503M2-XXXFP/SP	M38503M2H-XXXFP/SP
M38503M4-XXXFP/SP	M38503M4H-XXXFP/SP
M38503E4-XXXFP/SP	M38504M6-XXXFP/SP
M38503E4FP/SP	M38504E6-XXXFP/SP
M38503E4SS	M38504E6FP/SP
	M38504E6SS
	M38507M8-XXXFP/SP
	M38507F8FP/SP

Table 4 Differences between 3850 group (standard) and 3850 group (spec. H)

	3850 group (standard)	3850 group (spec. H)
Serial I/O	1: Serial I/O (UART or Clock-synchronized)	2: Serial I/O1 (UART or Clock-synchronized) Serial I/O2 (Clock-synchronized)
A-D converter	Unserviceable in low-speed mode	Serviceable in low-speed mode
Large current port	5: P13-P17	8: P10-P17

Notes on differences between 3850 group (standard) and 3850 group (spec. H)

- (1) The absolute maximum ratings of 3850 group (spec. H) is smaller than that of 3850 group (standard).
 - Power source voltage $V_{cc} = -0.3$ to 6.5 V
 - CNVss input voltage $V_i = -0.3$ to $V_{cc} + 0.3$ V
- (2) The oscillation circuit constants of XIN-XOUT, XCIN-XCOUT may be some differences between 3850 group (standard) and 3850 group (spec. H).
- (3) Do not write any data to the reserved area and the reserved bit. (Do not change the contents after rest.)
- (4) Fix bit 3 of the CPU mode register to "1".
- (5) Be sure to perform the termination of unused pins.

**FUNCTIONAL DESCRIPTION
CENTRAL PROCESSING UNIT (CPU)**

The 3850 group (spec. H) uses the standard 740 Family instruction set. Refer to the table of 740 Family addressing modes and machine instructions or the 740 Family Software Manual for details on the instruction set.

Machine-resident 740 Family instructions are as follows:

- The FST and SLW instructions cannot be used.
- The STP, WIT, MUL, and DIV instructions can be used.

[Accumulator (A)]

The accumulator is an 8-bit register. Data operations such as data transfer, etc., are executed mainly through the accumulator.

[Index Register X (X)]

The index register X is an 8-bit register. In the index addressing modes, the value of the OPERAND is added to the contents of register X and specifies the real address.

[Index Register Y (Y)]

The index register Y is an 8-bit register. In partial instruction, the value of the OPERAND is added to the contents of register Y and specifies the real address.

[Stack Pointer (S)]

The stack pointer is an 8-bit register used during subroutine calls and interrupts. This register indicates start address of stored area (stack) for storing registers during subroutine calls and interrupts. The low-order 8 bits of the stack address are determined by the contents of the stack pointer. The high-order 8 bits of the stack address are determined by the stack page selection bit. If the stack page selection bit is "0", the high-order 8 bits becomes "0016". If the stack page selection bit is "1", the high-order 8 bits becomes "0116".

The operations of pushing register contents onto the stack and popping them from the stack are shown in Figure 6.

Store registers other than those described in Figure 6 with program when the user needs them during interrupts or subroutine calls.

[Program Counter (PC)]

The program counter is a 16-bit counter consisting of two 8-bit registers PCH and PCL. It is used to indicate the address of the next instruction to be executed.

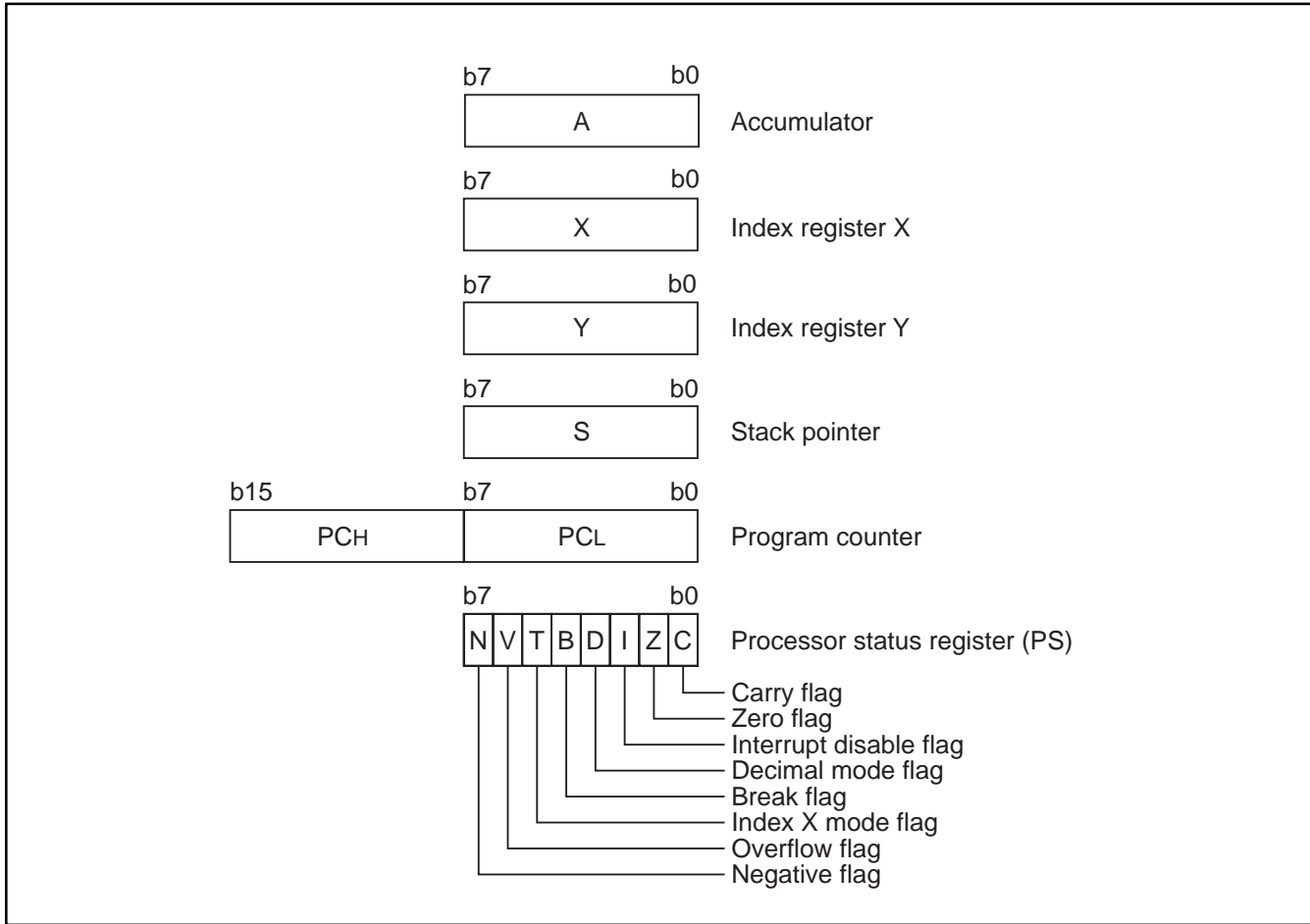


Fig. 5 740 Family CPU register structure

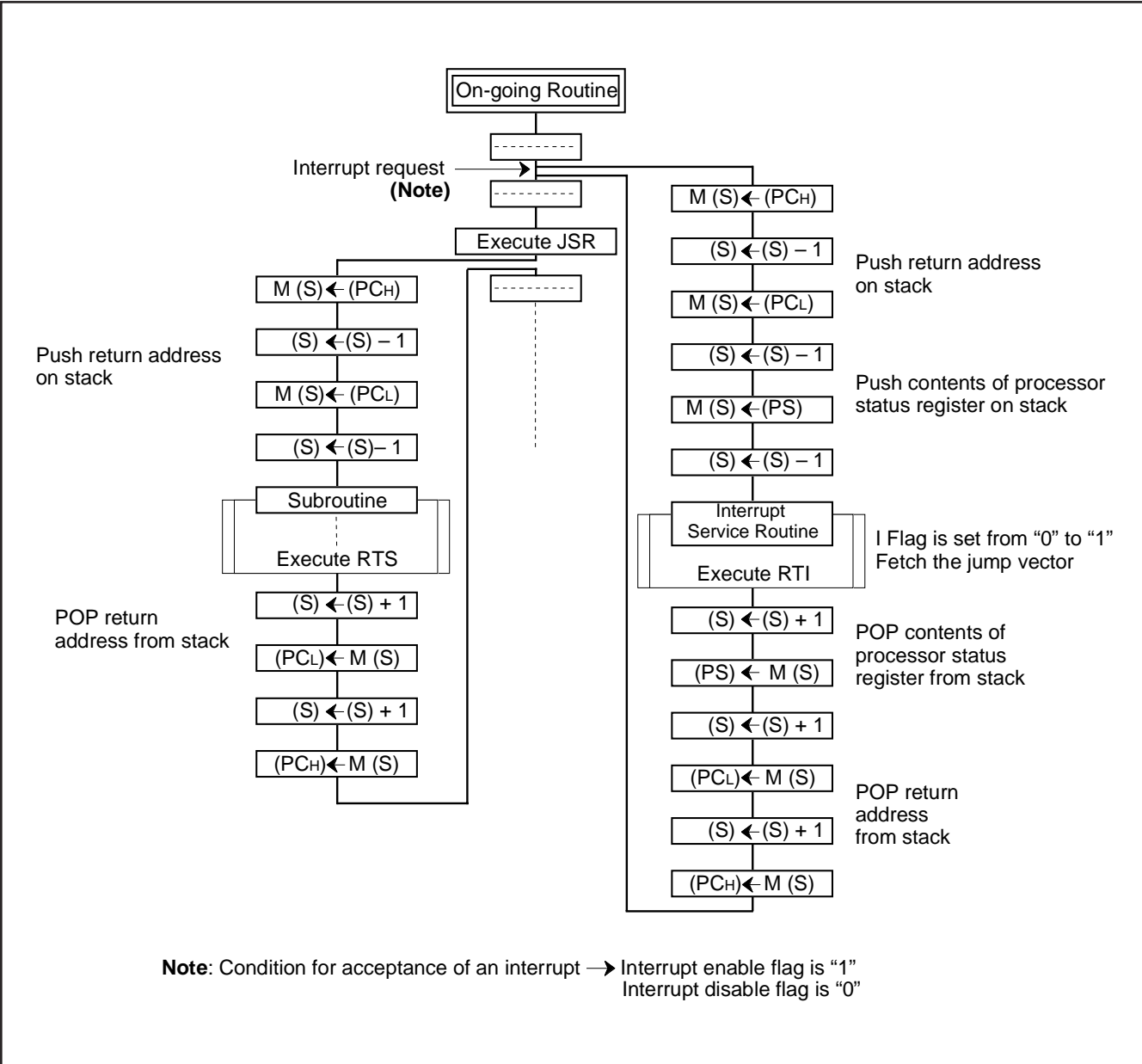


Fig. 6 Register push and pop at interrupt generation and subroutine call

Table 5 Push and pop instructions of accumulator or processor status register

	Push instruction to stack	Pop instruction from stack
Accumulator	PHA	PLA
Processor status register	PHP	PLP

[Processor status register (PS)]

The processor status register is an 8-bit register consisting of 5 flags which indicate the status of the processor after an arithmetic operation and 3 flags which decide MCU operation. Branch operations can be performed by testing the Carry (C) flag, Zero (Z) flag, Overflow (V) flag, or the Negative (N) flag. In decimal mode, the Z, V, N flags are not valid.

•Bit 0: Carry flag (C)

The C flag contains a carry or borrow generated by the arithmetic logic unit (ALU) immediately after an arithmetic operation. It can also be changed by a shift or rotate instruction.

•Bit 1: Zero flag (Z)

The Z flag is set if the result of an immediate arithmetic operation or a data transfer is "0", and cleared if the result is anything other than "0".

•Bit 2: Interrupt disable flag (I)

The I flag disables all interrupts except for the interrupt generated by the BRK instruction. Interrupts are disabled when the I flag is "1".

•Bit 3: Decimal mode flag (D)

The D flag determines whether additions and subtractions are executed in binary or decimal. Binary arithmetic is executed when this flag is "0"; decimal arithmetic is executed when it is "1". Decimal correction is automatic in decimal mode. Only the ADC and SBC instructions can be used for decimal arithmetic.

•Bit 4: Break flag (B)

The B flag is used to indicate that the current interrupt was generated by the BRK instruction. The BRK flag in the processor status register is always "0". When the BRK instruction is used to generate an interrupt, the processor status register is pushed onto the stack with the break flag set to "1".

•Bit 5: Index X mode flag (T)

When the T flag is "0", arithmetic operations are performed between accumulator and memory. When the T flag is "1", direct arithmetic operations and direct data transfers are enabled between memory locations.

•Bit 6: Overflow flag (V)

The V flag is used during the addition or subtraction of one byte of signed data. It is set if the result exceeds +127 to -128. When the BIT instruction is executed, bit 6 of the memory location operated on by the BIT instruction is stored in the overflow flag.

•Bit 7: Negative flag (N)

The N flag is set if the result of an arithmetic operation or data transfer is negative. When the BIT instruction is executed, bit 7 of the memory location operated on by the BIT instruction is stored in the negative flag.

Table 6 Set and clear instructions of each bit of processor status register

	C flag	Z flag	I flag	D flag	B flag	T flag	V flag	N flag
Set instruction	SEC	–	SEI	SED	–	SET	–	–
Clear instruction	CLC	–	CLI	CLD	–	CLT	CLV	–

[CPU Mode Register (CPUM)] 003B16

The CPU mode register contains the stack page selection bit, etc.
The CPU mode register is allocated at address 003B16.

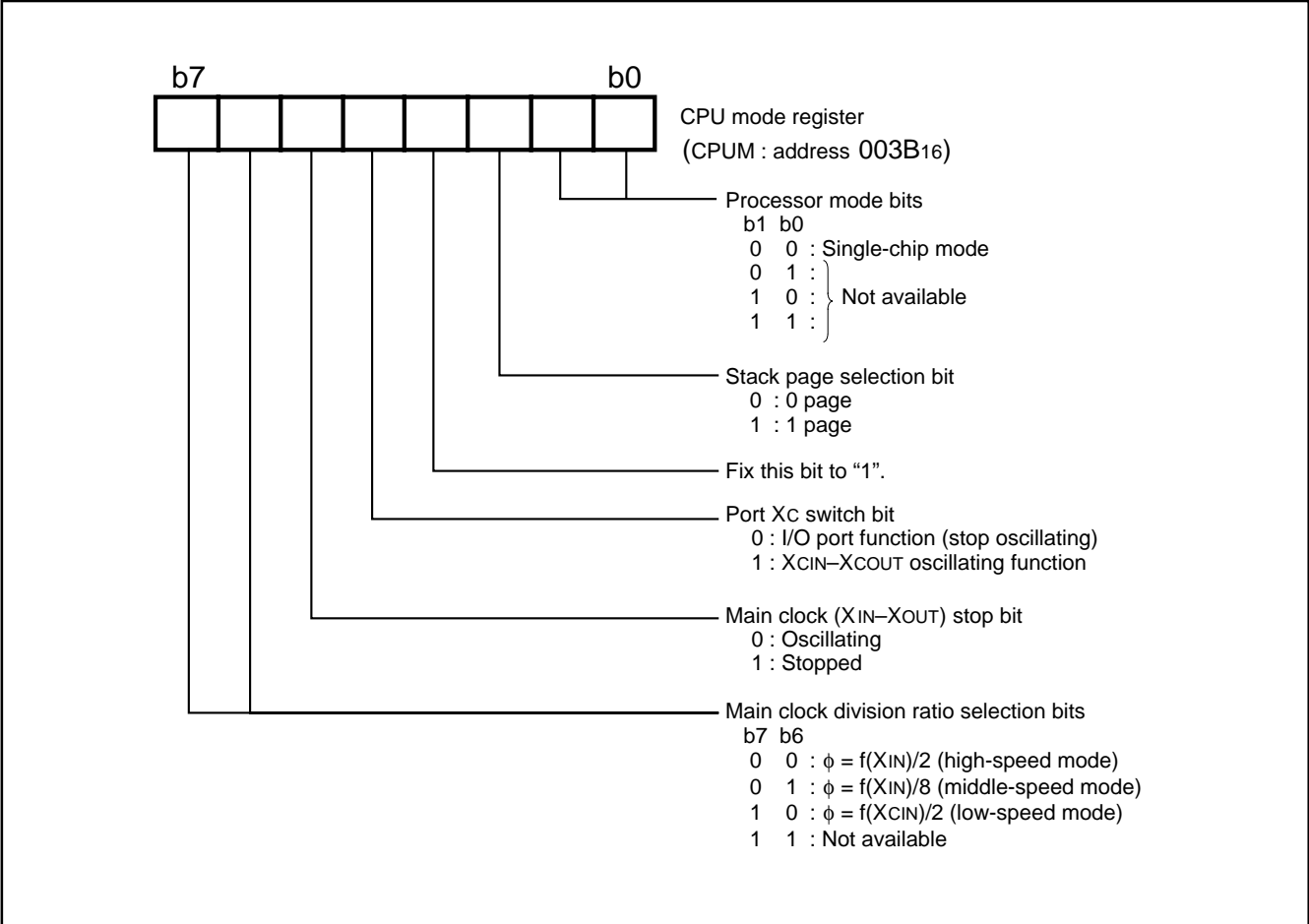


Fig. 7 Structure of CPU mode register

MEMORY

Special Function Register (SFR) Area

The Special Function Register area in the zero page contains control registers such as I/O ports and timers.

RAM

RAM is used for data storage and for stack area of subroutine calls and interrupts.

ROM

The first 128 bytes and the last 2 bytes of ROM are reserved for device testing and the rest is user area for storing programs.

Interrupt Vector Area

The interrupt vector area contains reset and interrupt vectors.

Zero Page

Access to this area with only 2 bytes is possible in the zero page addressing mode.

Special Page

Access to this area with only 2 bytes is possible in the special page addressing mode.

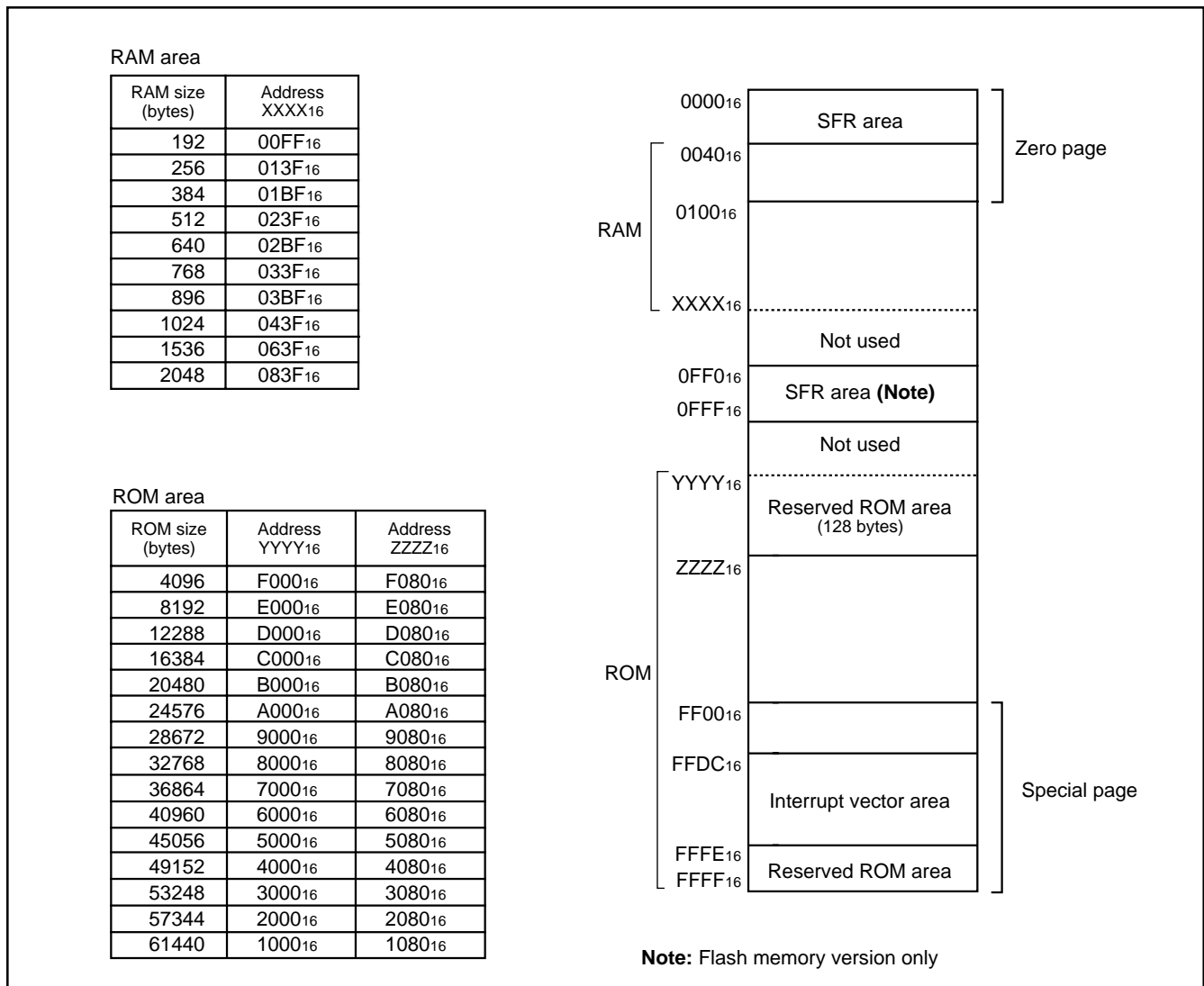


Fig. 8 Memory map diagram

0000 ₁₆	Port P0 (P0)	0020 ₁₆	Prescaler 12 (PRE12)
0001 ₁₆	Port P0 direction register (P0D)	0021 ₁₆	Timer 1 (T1)
0002 ₁₆	Port P1 (P1)	0022 ₁₆	Timer 2 (T2)
0003 ₁₆	Port P1 direction register (P1D)	0023 ₁₆	Timer XY mode register (TM)
0004 ₁₆	Port P2 (P2)	0024 ₁₆	Prescaler X (PREX)
0005 ₁₆	Port P2 direction register (P2D)	0025 ₁₆	Timer X (TX)
0006 ₁₆	Port P3 (P3)	0026 ₁₆	Prescaler Y (PREY)
0007 ₁₆	Port P3 direction register (P3D)	0027 ₁₆	Timer Y (TY)
0008 ₁₆	Port P4 (P4)	0028 ₁₆	Timer count source selection register (TCSS)
0009 ₁₆	Port P4 direction register (P4D)	0029 ₁₆	
000A ₁₆		002A ₁₆	
000B ₁₆		002B ₁₆	Reserved *
000C ₁₆		002C ₁₆	Reserved *
000D ₁₆		002D ₁₆	Reserved *
000E ₁₆		002E ₁₆	Reserved *
000F ₁₆		002F ₁₆	Reserved *
0010 ₁₆		0030 ₁₆	Reserved *
0011 ₁₆		0031 ₁₆	Reserved *
0012 ₁₆	Reserved *	0032 ₁₆	
0013 ₁₆	Reserved *	0033 ₁₆	
0014 ₁₆	Reserved *	0034 ₁₆	A-D control register (ADCON)
0015 ₁₆	Serial I/O2 control register 1 (SIO2CON1)	0035 ₁₆	A-D conversion low-order register (ADL)
0016 ₁₆	Serial I/O2 control register 2 (SIO2CON2)	0036 ₁₆	A-D conversion high-order register (ADH)
0017 ₁₆	Serial I/O2 register (SIO2)	0037 ₁₆	Reserved *
0018 ₁₆	Transmit/Receive buffer register (TB/RB)	0038 ₁₆	MISRG
0019 ₁₆	Serial I/O1 status register (SIOSTS)	0039 ₁₆	Watchdog timer control register (WDTCN)
001A ₁₆	Serial I/O1 control register (SIOCON)	003A ₁₆	Interrupt edge selection register (INTEDGE)
001B ₁₆	UART control register (UARTCON)	003B ₁₆	CPU mode register (CPUM)
001C ₁₆	Baud rate generator (BRG)	003C ₁₆	Interrupt request register 1 (IREQ1)
001D ₁₆	PWM control register (PWMCON)	003D ₁₆	Interrupt request register 2 (IREQ2)
001E ₁₆	PWM prescaler (PREPWM)	003E ₁₆	Interrupt control register 1 (ICON1)
001F ₁₆	PWM register (PWM)	003F ₁₆	Interrupt control register 2 (ICON2)

* Reserved : Do not write any data to this addresses, because these areas are reserved.

Fig. 9 Memory map of special function register (SFR)

I/O PORTS

The I/O ports have direction registers which determine the input/output direction of each individual pin. Each bit in a direction register corresponds to one pin, and each pin can be set to be input port or output port.

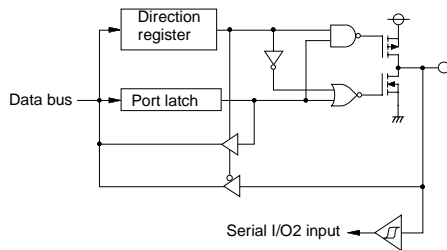
When "0" is written to the bit corresponding to a pin, that pin becomes an input pin. When "1" is written to that bit, that pin becomes an output pin.

If data is read from a pin which is set to output, the value of the port output latch is read, not the value of the pin itself. Pins set to input are floating. If a pin set to input is written to, only the port output latch is written to and the pin remains floating.

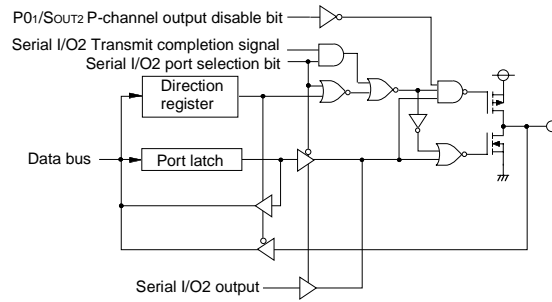
Table 5 I/O port function

Pin	Name	Input/Output	I/O Structure	Non-Port Function	Related SFRs	Ref.No.		
P00/SIN2	Port P0	Input/output, individual bits	CMOS compatible input level CMOS 3-state output	Serial I/O2 function I/O	Serial I/O2 control register	(1)		
P01/SOUT2						(2)		
P02/SCLK2						(3)		
P03/SRDY2						(4)		
P04–P07	Port P1						(5)	
P10–P17								
P20/XCOUT					Sub-clock generating circuit	CPU mode register	(6)	
P21/XCIN							(7)	
P22	Port P2			CMOS compatible input level N-channel open-drain output			(8)	
P23								
P24/RxD				CMOS compatible input level CMOS 3-state output	Serial I/O1 function I/O	Serial I/O1 control register	(9)	
P25/TxD							(10)	
P26/SCLK							(11)	
P27/CNTR0/ $\overline{\text{SRDY1}}$							(12)	
P30/AN0– P34/AN4	Port P3				A-D conversion input	A-D control register	(13)	
P40/CNTR1	Port P4							CMOS compatible input level CMOS 3-state output
P41/INT0			External interrupt input	Interrupt edge selection register	(15)			
P42/INT1		External interrupt input SCMP2 output				Interrupt edge selection register Serial I/O2 control register		
P43/INT2/SCMP2			External interrupt input PWM output	Interrupt edge selection register PWM control register	(17)			
P44/INT3/PWM								

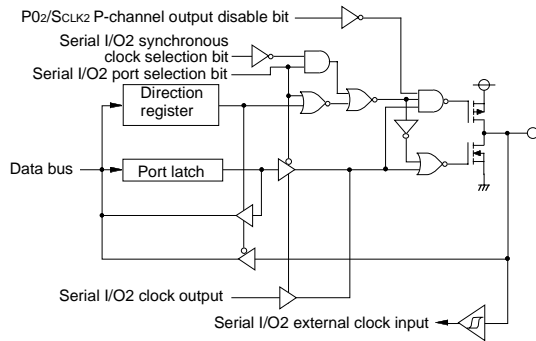
(1) Port P00



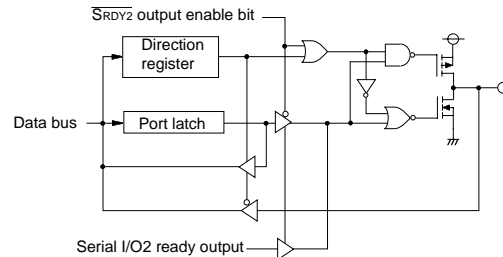
(2) Port P01



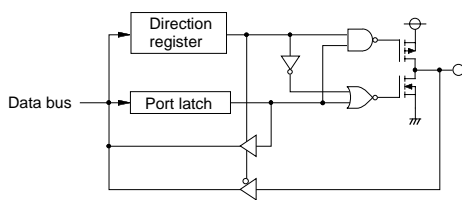
(3) Port P02



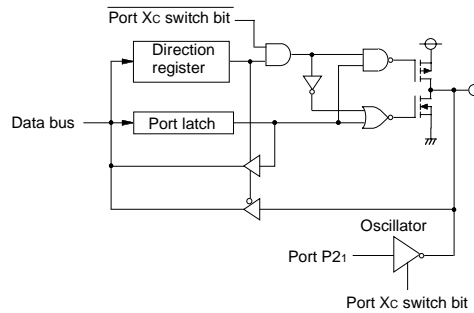
(4) Port P03



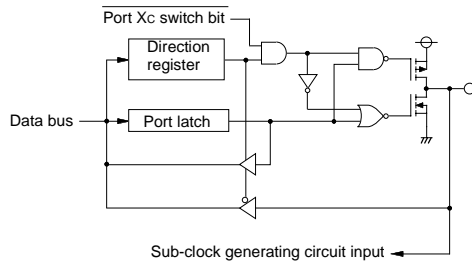
(5) Ports P04-P07, P1



(6) Port P20



(7) Port P21



(8) Ports P22, P23

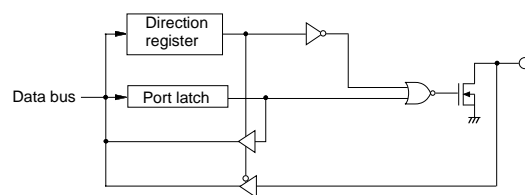


Fig. 10 Port block diagram (1)

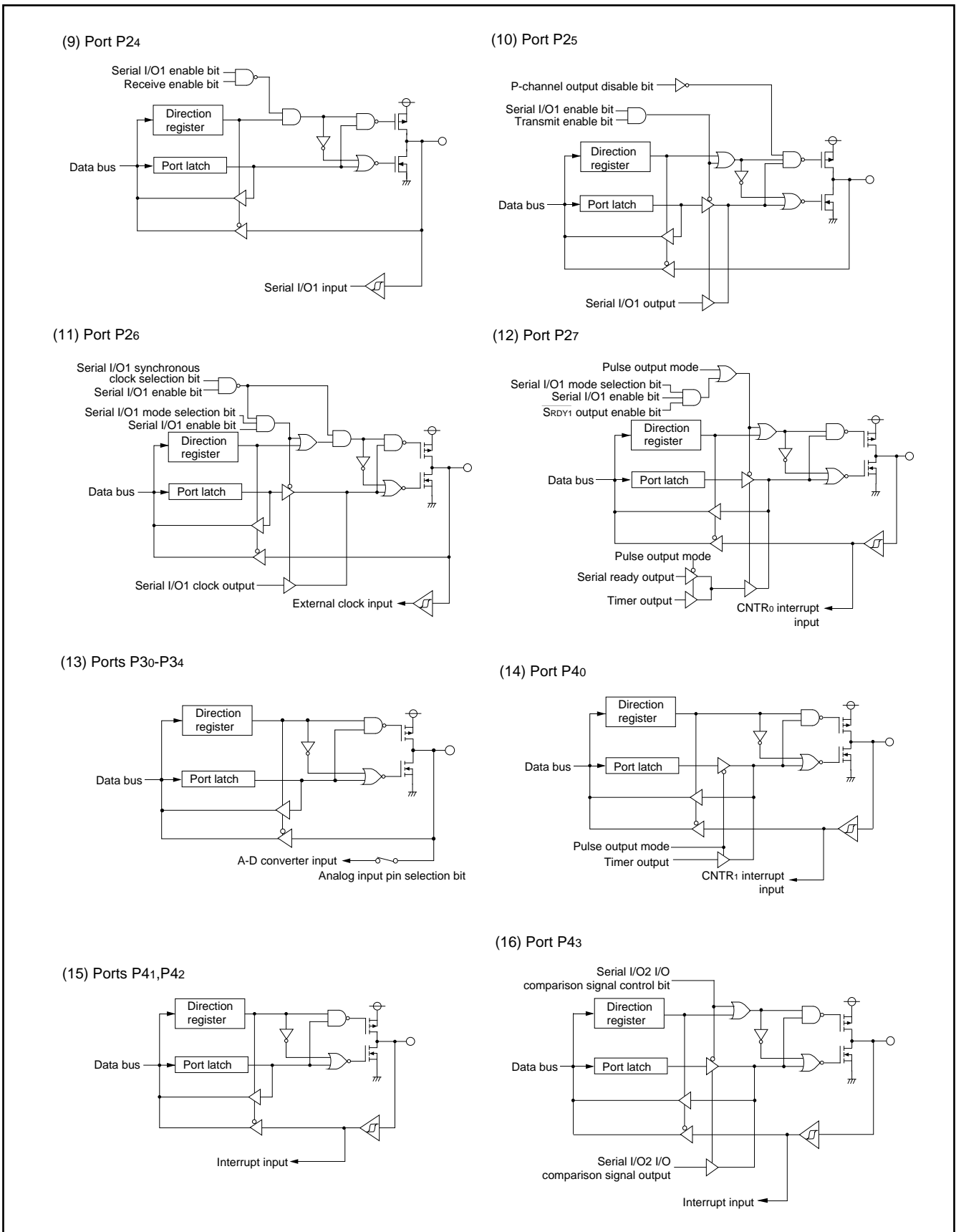


Fig. 11 Port block diagram (2)

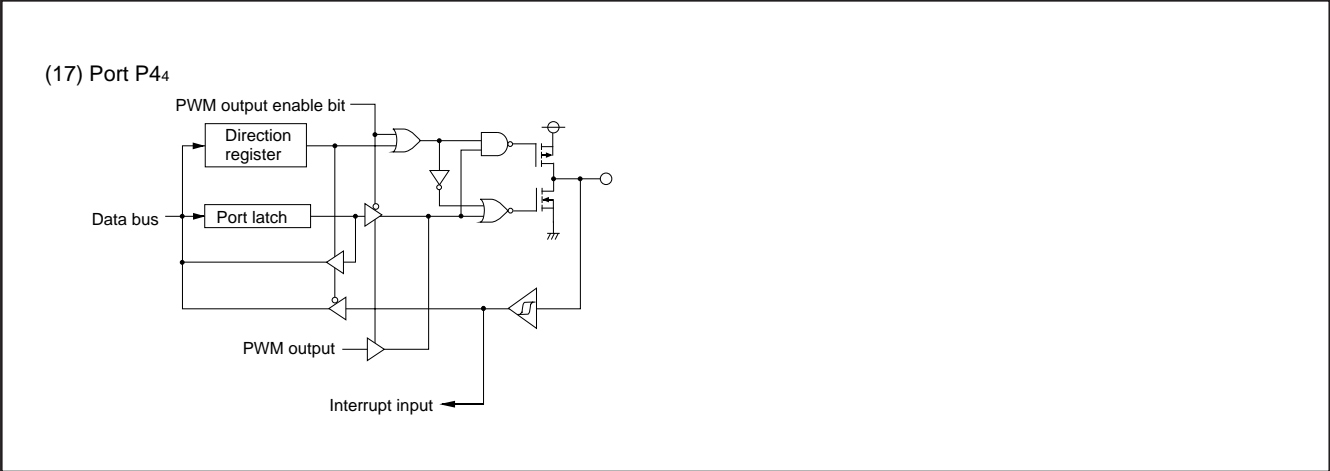


Fig. 12 Port block diagram (3)

INTERRUPTS

Interrupts occur by 14 sources among 14 sources: six external, seven internal, and one software.

Interrupt Control

Each interrupt is controlled by an interrupt request bit, an interrupt enable bit, and the interrupt disable flag except for the software interrupt set by the BRK instruction. An interrupt occurs if the corresponding interrupt request and enable bits are "1" and the interrupt disable flag is "0".

Interrupt enable bits can be set or cleared by software.

Interrupt request bits can be cleared by software, but cannot be set by software.

The BRK instruction cannot be disabled with any flag or bit. The I (interrupt disable) flag disables all interrupts except the BRK instruction interrupt.

When several interrupts occur at the same time, the interrupts are received according to priority.

Interrupt Operation

By acceptance of an interrupt, the following operations are automatically performed:

1. The contents of the program counter and the processor status register are automatically pushed onto the stack.
2. The interrupt disable flag is set and the corresponding interrupt request bit is cleared.
3. The interrupt jump destination address is read from the vector table into the program counter.

■Notes

When the active edge of an external interrupt (INT₀–INT₃, CNTR₀, CNTR₁) is set, the corresponding interrupt request bit may also be set. Therefore, take the following sequence:

1. Disable the interrupt
2. Change the interrupt edge selection register (the timer XY mode register for CNTR₀ and CNTR₁)
3. Clear the interrupt request bit to "0"
4. Accept the interrupt.

Table 8 Interrupt vector addresses and priority

Interrupt Source	Priority	Vector Addresses (Note 1)		Interrupt Request Generating Conditions	Remarks
		High	Low		
Reset (Note 2)	1	FFFD ₁₆	FFFC ₁₆	At reset	Non-maskable
INT ₀	2	FFFB ₁₆	FFFA ₁₆	At detection of either rising or falling edge of INT ₀ input	External interrupt (active edge selectable)
Reserved	3	FFF9 ₁₆	FFF8 ₁₆	Reserved	
INT ₁	4	FFF7 ₁₆	FFF6 ₁₆	At detection of either rising or falling edge of INT ₁ input	External interrupt (active edge selectable)
INT ₂	5	FFF5 ₁₆	FFF4 ₁₆	At detection of either rising or falling edge of INT ₂ input	External interrupt (active edge selectable)
INT ₃ / Serial I/O ₂	6	FFF3 ₁₆	FFF2 ₁₆	At detection of either rising or falling edge of INT ₃ input/ At completion of serial I/O ₂ data reception/transmission	External interrupt (active edge selectable) Switch by Serial I/O ₂ /INT ₃ interrupt source bit
Reserved	7	FFF1 ₁₆	FFF0 ₁₆	Reserved	
Timer X	8	FFEF ₁₆	FFEE ₁₆	At timer X underflow	
Timer Y	9	FFED ₁₆	FFEC ₁₆	At timer Y underflow	
Timer 1	10	FFEB ₁₆	FFEA ₁₆	At timer 1 underflow	STP release timer underflow
Timer 2	11	FFE9 ₁₆	FFE8 ₁₆	At timer 2 underflow	
Serial I/O ₁ reception	12	FFE7 ₁₆	FFE6 ₁₆	At completion of serial I/O ₁ data reception	Valid when serial I/O ₁ is selected
Serial I/O ₁ transmission	13	FFE5 ₁₆	FFE4 ₁₆	At completion of serial I/O ₁ transfer shift or when transmission buffer is empty	Valid when serial I/O ₁ is selected
CNTR ₀	14	FFE3 ₁₆	FFE2 ₁₆	At detection of either rising or falling edge of CNTR ₀ input	External interrupt (active edge selectable)
CNTR ₁	15	FFE1 ₁₆	FFE0 ₁₆	At detection of either rising or falling edge of CNTR ₁ input	External interrupt (active edge selectable)
A-D converter	16	FFDF ₁₆	FFDE ₁₆	At completion of A-D conversion	
BRK instruction	17	FFDD ₁₆	FFDC ₁₆	At BRK instruction execution	Non-maskable software interrupt

Notes 1: Vector addresses contain interrupt jump destination addresses.

2: Reset function in the same way as an interrupt with the highest priority.

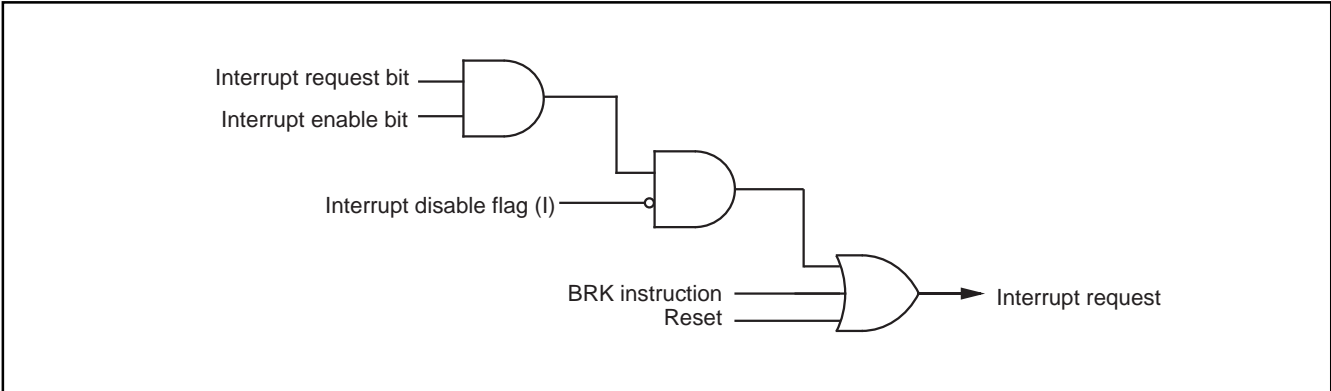


Fig. 13 Interrupt control

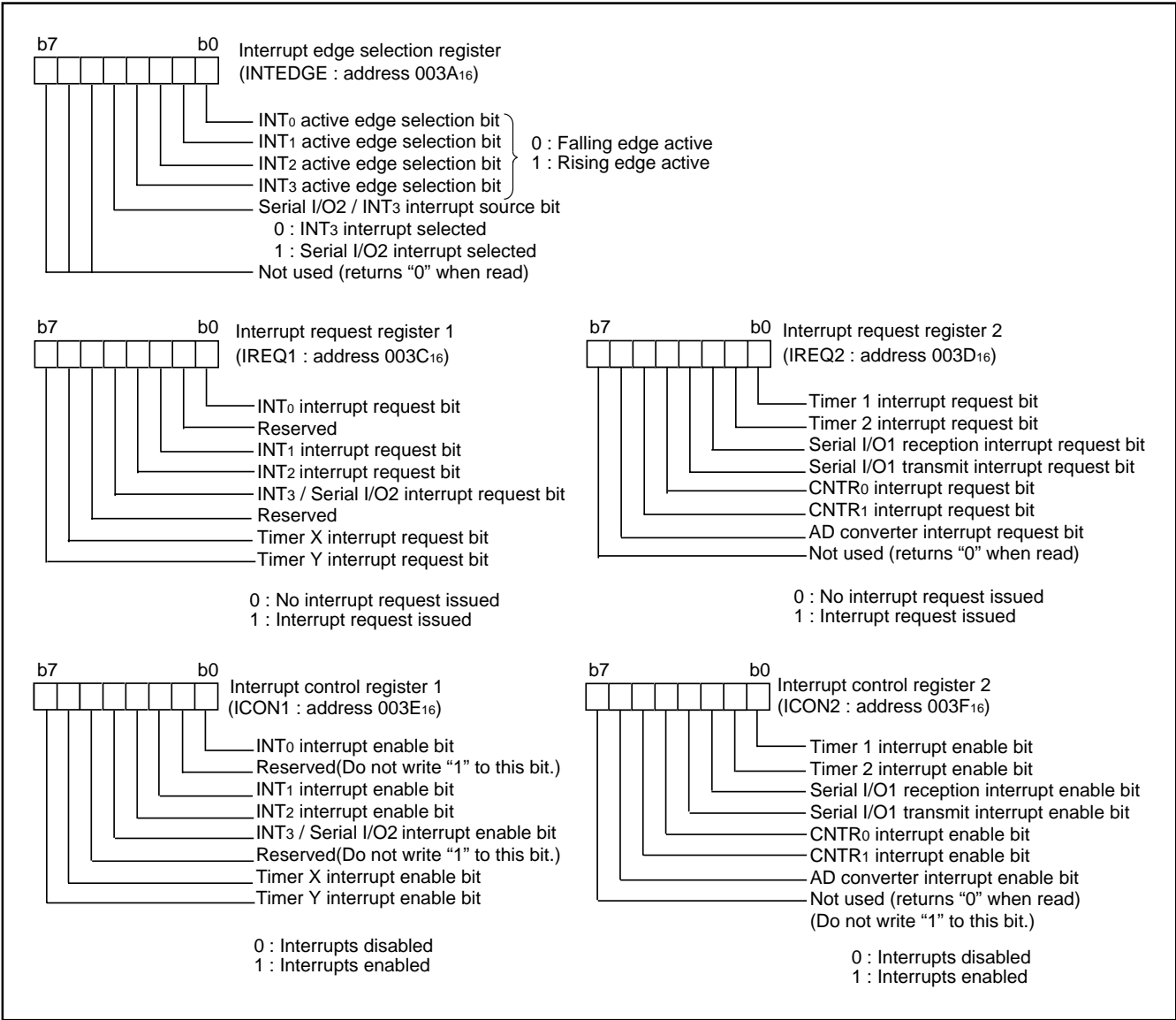


Fig. 14 Structure of interrupt-related registers

TIMERS

The 3850 group (spec. H) has four timers: timer X, timer Y, timer 1, and timer 2.

The division ratio of each timer or prescaler is given by 1/(n + 1), where n is the value in the corresponding timer or prescaler latch. All timers are count down. When the timer reaches "0016", an underflow occurs at the next count pulse and the corresponding timer latch is reloaded into the timer and the count is continued. When a timer underflows, the interrupt request bit corresponding to that timer is set to "1".

Timer 1 and Timer 2

The count source of prescaler 12 is the oscillation frequency which is selected by timer 12 count source selection bit. The output of prescaler 12 is counted by timer 1 and timer 2, and a timer underflow sets the interrupt request bit.

Timer X and Timer Y

Timer X and Timer Y can each select in one of four operating modes by setting the timer XY mode register.

(1) Timer Mode

The timer counts the count source selected by Timer count source selection bit.

(2) Pulse Output Mode

The timer counts the count source selected by Timer count source selection bit. Whenever the contents of the timer reach "0016", the signal output from the CNTR0 (or CNTR1) pin is inverted. If the CNTR0 (or CNTR1) active edge selection bit is "0", output begins at "H".

If it is "1", output starts at "L". When using a timer in this mode, set the corresponding port P27 (or port P40) direction register to output mode.

(3) Event Counter Mode

Operation in event counter mode is the same as in timer mode, except that the timer counts signals input through the CNTR0 or CNTR1 pin.

When the CNTR0 (or CNTR1) active edge selection bit is "0", the rising edge of the CNTR0 (or CNTR1) pin is counted.

When the CNTR0 (or CNTR1) active edge selection bit is "1", the falling edge of the CNTR0 (or CNTR1) pin is counted.

(4) Pulse Width Measurement Mode

If the CNTR0 (or CNTR1) active edge selection bit is "0", the timer counts the selected signals by the count source selection bit while the CNTR0 (or CNTR1) pin is at "H". If the CNTR0 (or CNTR1) active edge selection bit is "1", the timer counts it while the CNTR0 (or CNTR1) pin is at "L".

The count can be stopped by setting "1" to the timer X (or timer Y) count stop bit in any mode. The corresponding interrupt request bit is set each time a timer underflows.

Note

When switching the count source by the timer 12, X and Y count source bit, the value of timer count is altered in unconsiderable amount owing to generating of a thin pulses in the count input signals.

Therefore, select the timer count source before set the value to the prescaler and the timer.

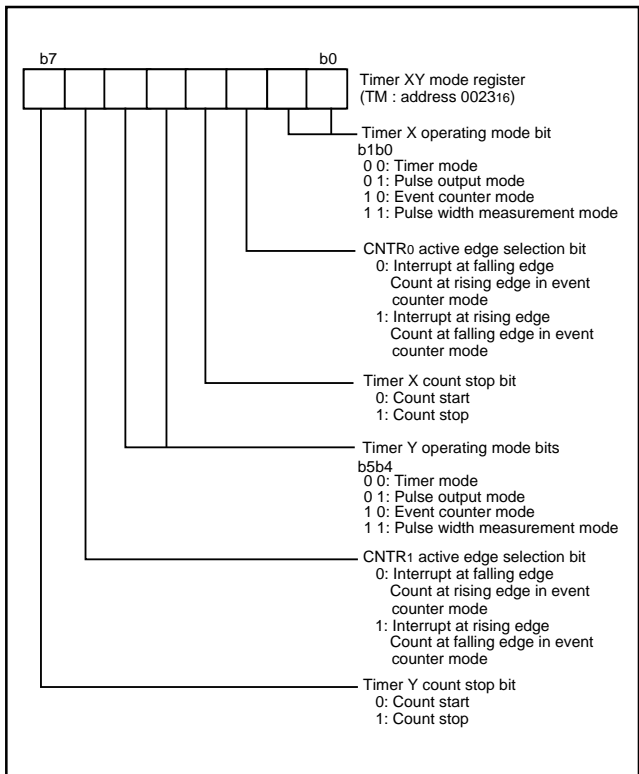


Fig. 15 Structure of timer XY mode register

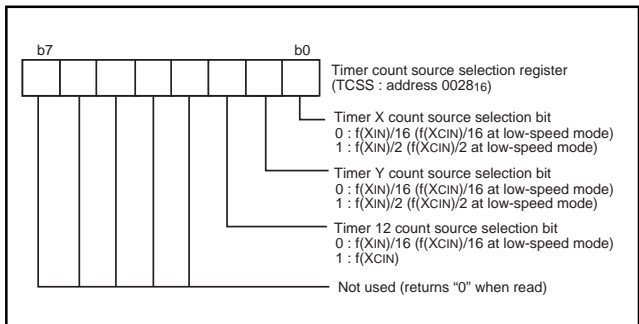


Fig. 16 Structure of timer count source selection register

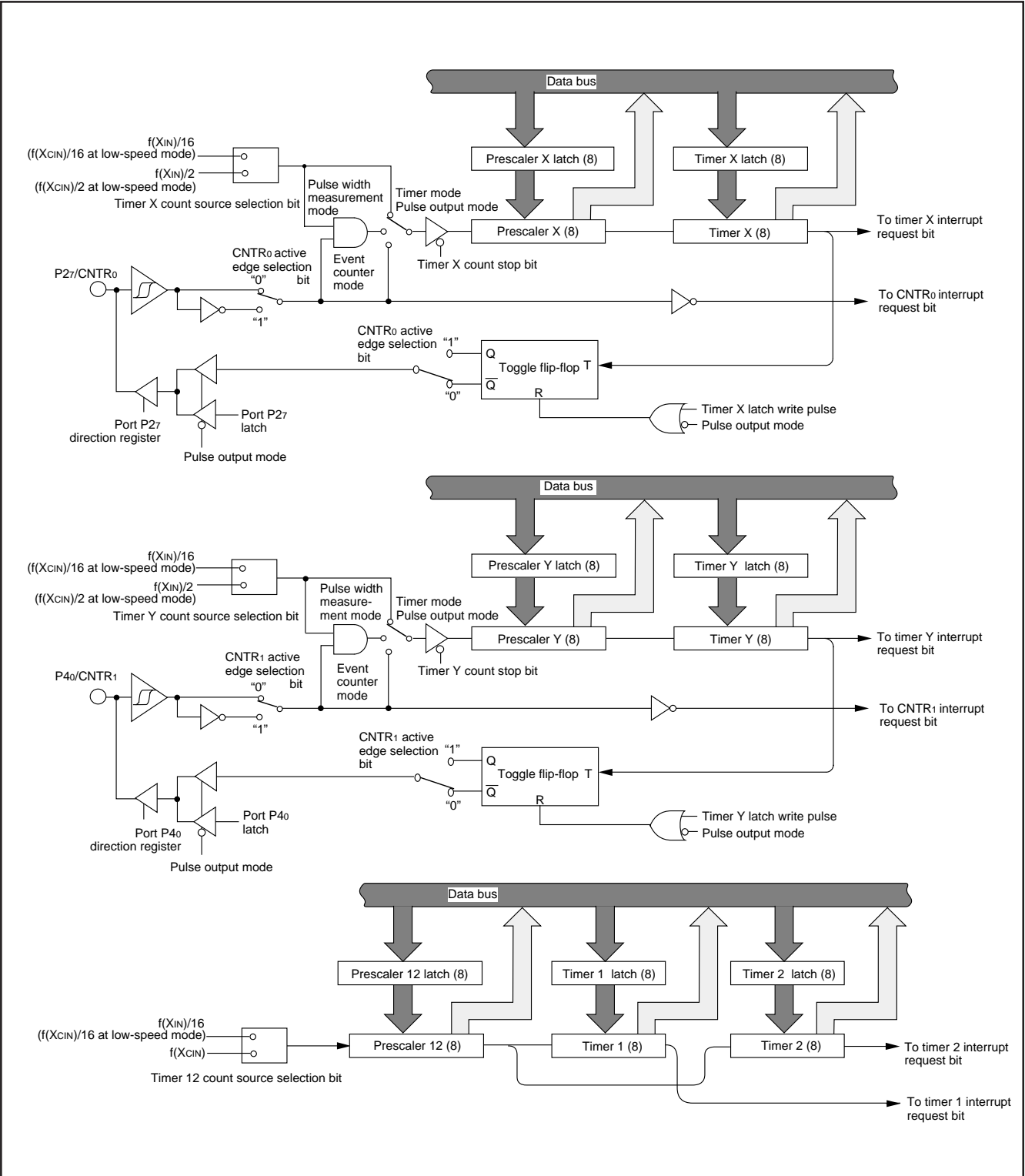


Fig. 17 Block diagram of timer X, timer Y, timer 1, and timer 2

SERIAL I/O1

Serial I/O1 can be used as either clock synchronous or asynchronous (UART) serial I/O. A dedicated timer is also provided for baud rate generation.

(1) Clock Synchronous Serial I/O Mode

Clock synchronous serial I/O mode can be selected by setting the serial I/O1 mode selection bit of the serial I/O1 control register (bit 6 of address 001A16) to "1".

For clock synchronous serial I/O, the transmitter and the receiver must use the same clock. If an internal clock is used, transfer is started by a write signal to the TB/RB.

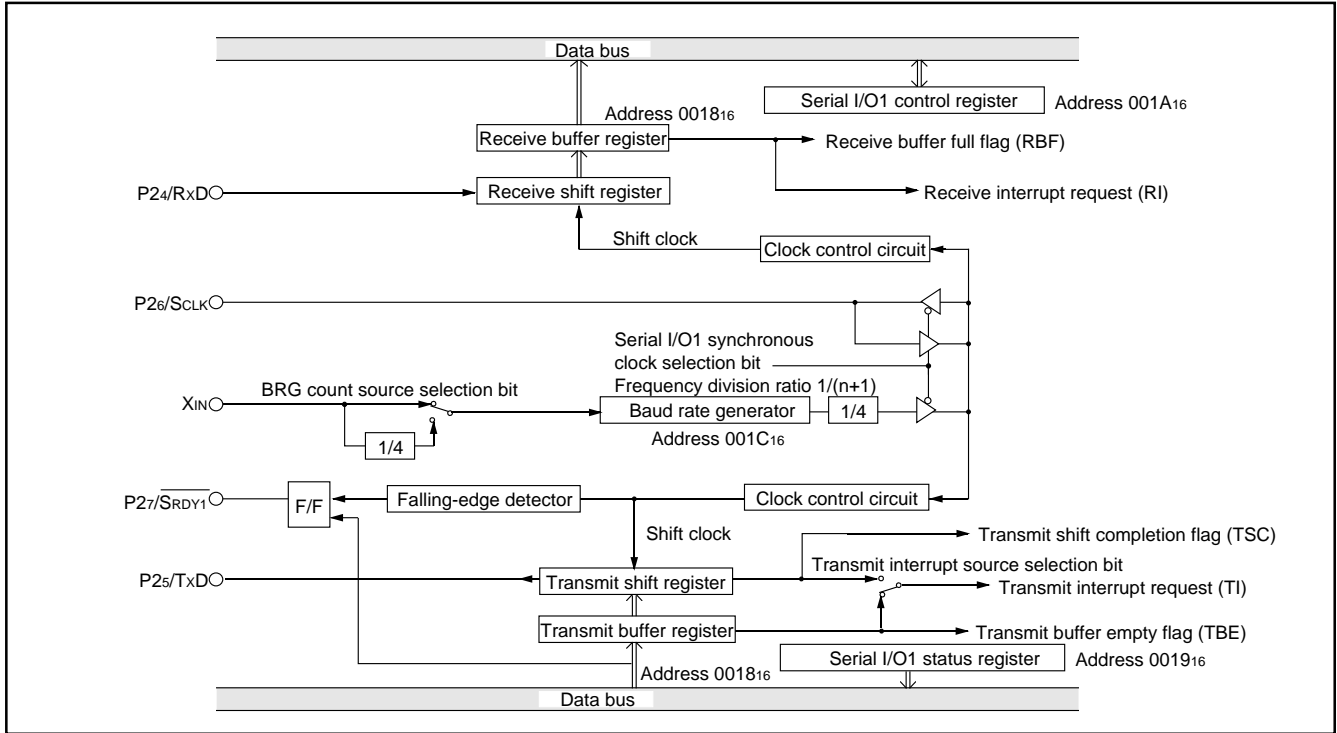


Fig. 18 Block diagram of clock synchronous serial I/O1

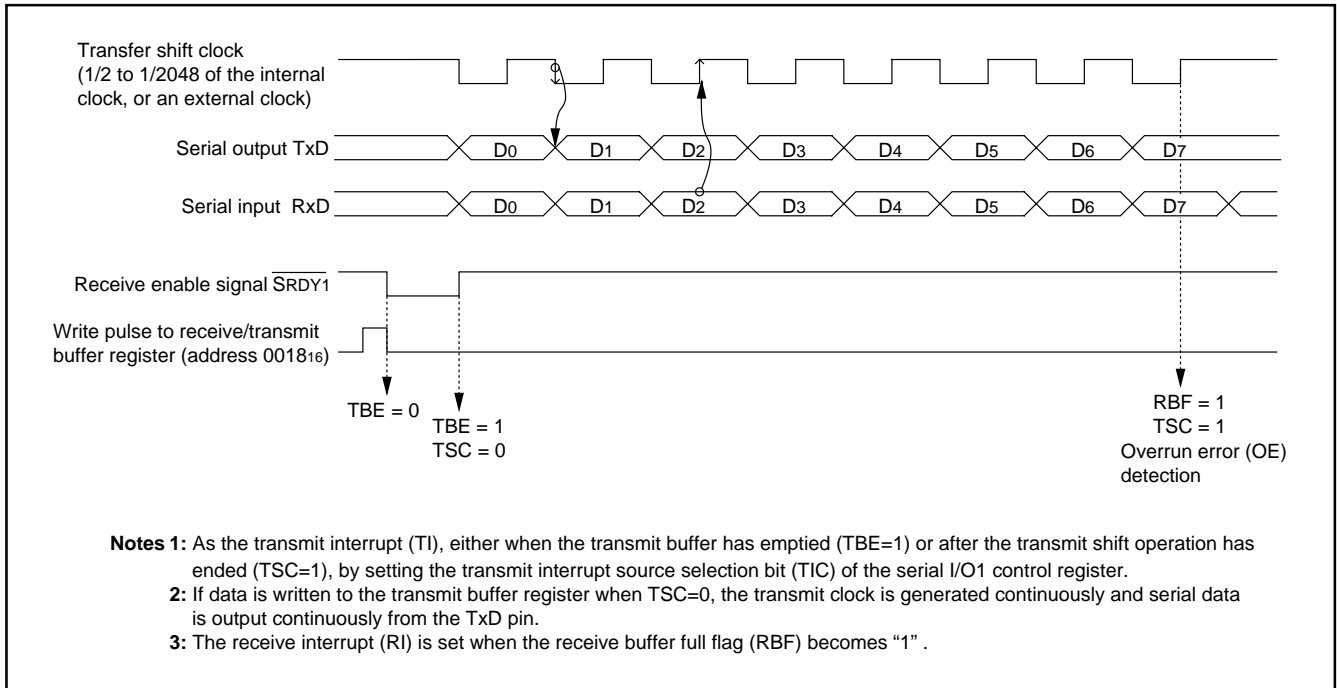


Fig. 19 Operation of clock synchronous serial I/O1 function

(2) Asynchronous Serial I/O (UART) Mode

Clock asynchronous serial I/O mode (UART) can be selected by clearing the serial I/O1 mode selection bit (b6) of the serial I/O1 control register to "0".

Eight serial data transfer formats can be selected, and the transfer formats used by a transmitter and receiver must be identical.

The transmit and receive shift registers each have a buffer, but the

two buffers have the same address in memory. Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer register, and receive data is read from the receive buffer register.

The transmit buffer register can also hold the next data to be transmitted, and the receive buffer register can hold a character while the next character is being received.

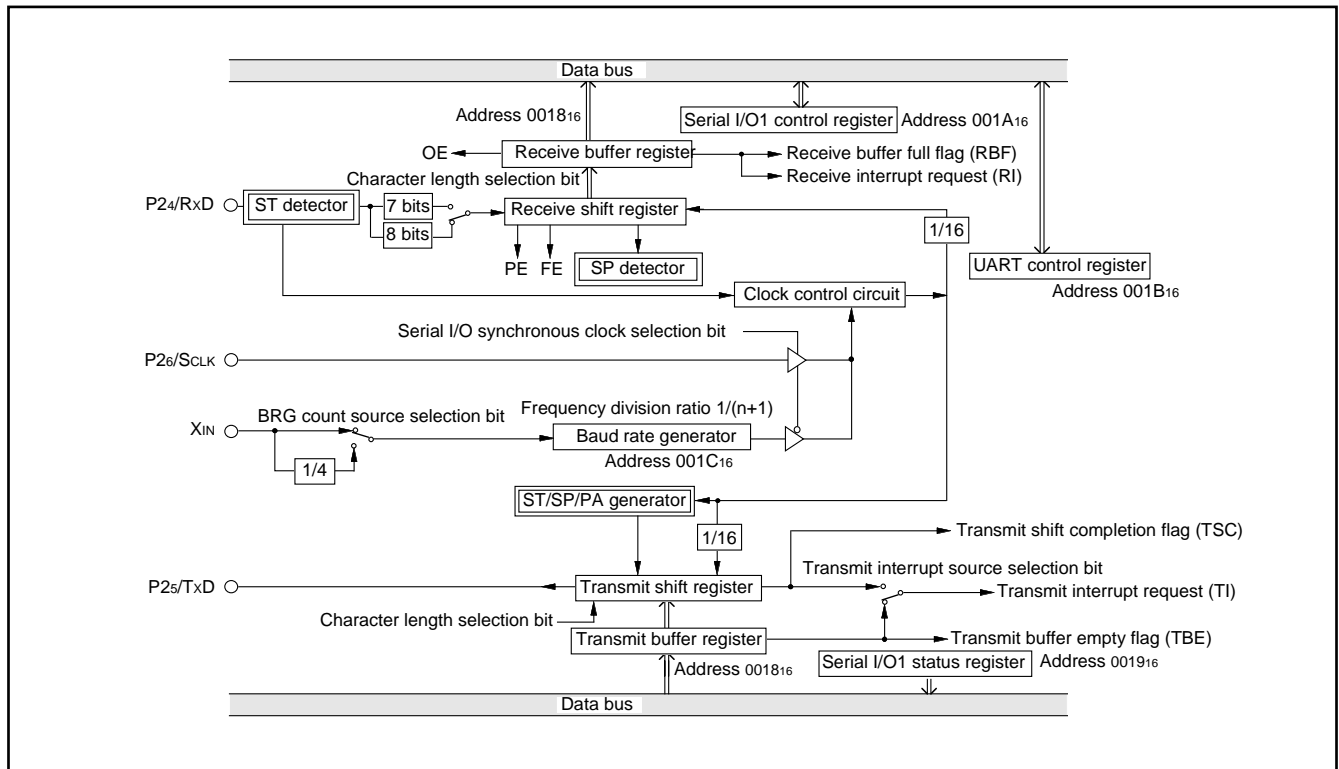


Fig. 20 Block diagram of UART serial I/O1

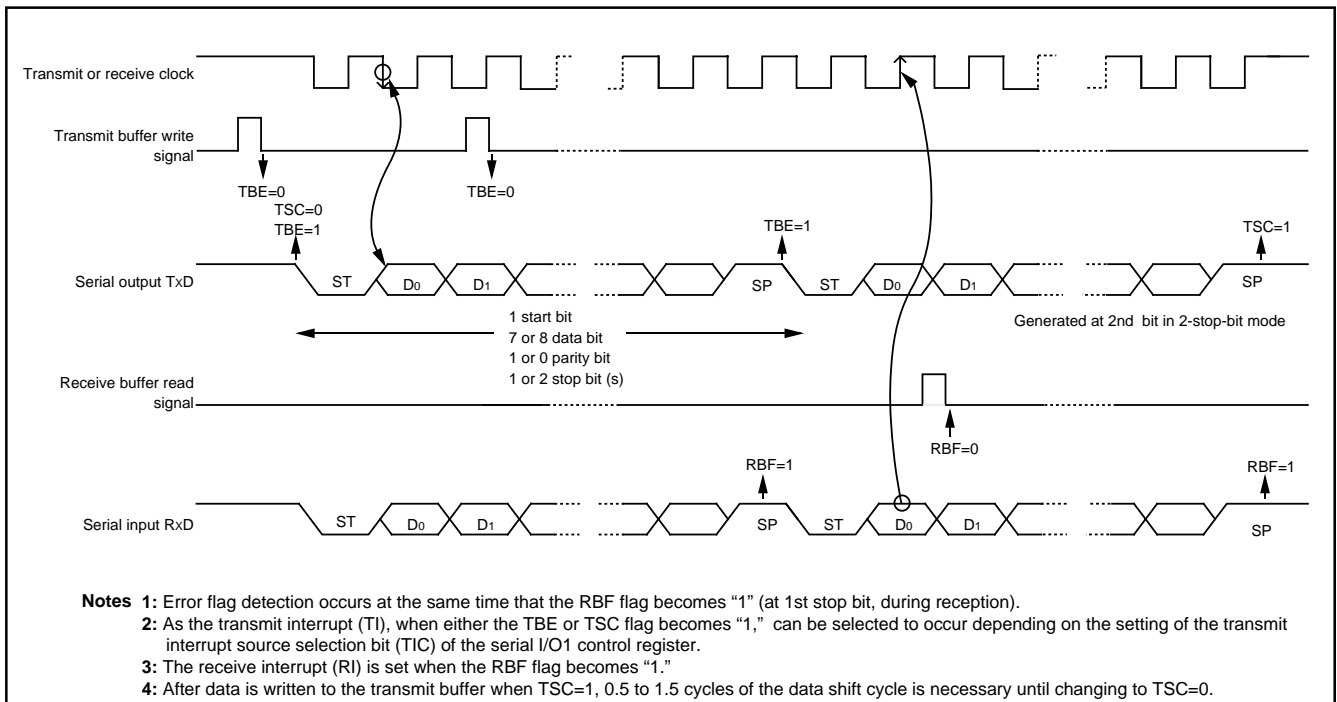


Fig. 21 Operation of UART serial I/O1 function

[Transmit Buffer Register/Receive Buffer Register (TB/RB)] 001816

The transmit buffer register and the receive buffer register are located at the same address. The transmit buffer is write-only and the receive buffer is read-only. If a character bit length is 7 bits, the MSB of data stored in the receive buffer is "0".

[Serial I/O1 Status Register (SIOSTS)] 001916

The read-only serial I/O1 status register consists of seven flags (bits 0 to 6) which indicate the operating status of the serial I/O1 function and various errors.

Three of the flags (bits 4 to 6) are valid only in UART mode.

The receive buffer full flag (bit 1) is cleared to "0" when the receive buffer register is read.

If there is an error, it is detected at the same time that data is transferred from the receive shift register to the receive buffer register, and the receive buffer full flag is set. A write to the serial I/O1 status register clears all the error flags OE, PE, FE, and SE (bit 3 to bit 6, respectively). Writing "0" to the serial I/O1 enable bit SIOE (bit 7 of the serial I/O1 control register) also clears all the status flags, including the error flags.

Bits 0 to 6 of the serial I/O1 status register are initialized to "0" at reset, but if the transmit enable bit (bit 4) of the serial I/O1 control register has been set to "1", the transmit shift completion flag (bit 2) and the transmit buffer empty flag (bit 0) become "1".

[Serial I/O1 Control Register (SIOCON)] 001A16

The serial I/O1 control register consists of eight control bits for the serial I/O1 function.

[UART Control Register (UARTCON)] 001B16

The UART control register consists of four control bits (bits 0 to 3) which are valid when asynchronous serial I/O is selected and set the data format of an data transfer and one bit (bit 4) which is always valid and sets the output structure of the P2₅/Tx/D pin.

[Baud Rate Generator (BRG)] 001C16

The baud rate generator determines the baud rate for serial transfer.

The baud rate generator divides the frequency of the count source by $1/(n + 1)$, where n is the value written to the baud rate generator.

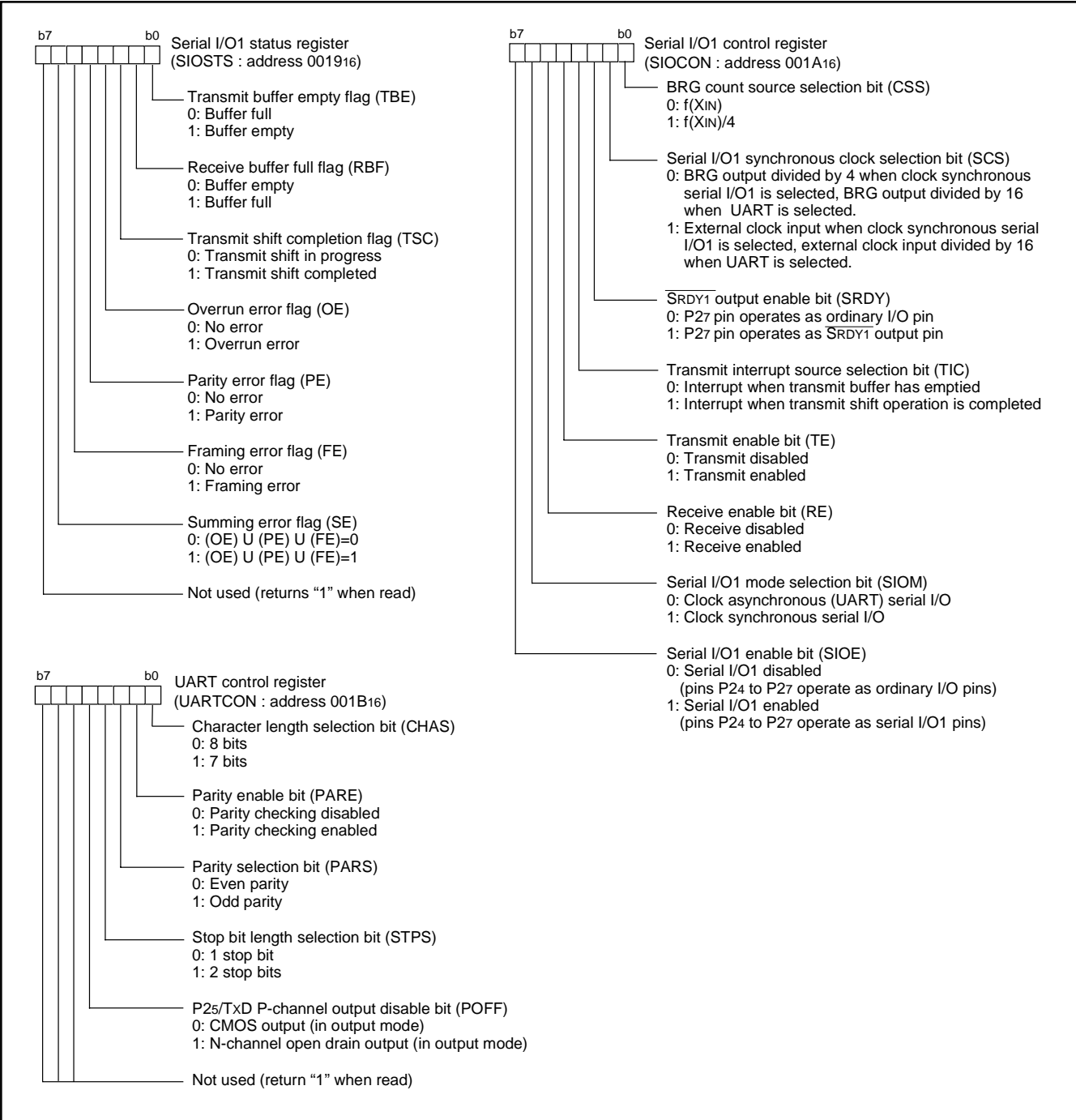


Fig. 22 Structure of serial I/O1 control registers

SERIAL I/O2

The serial I/O2 can be operated only as the clock synchronous type. As a synchronous clock for serial transfer, either internal clock or external clock can be selected by the serial I/O2 synchronous clock selection bit (b6) of serial I/O2 control register 1.

The internal clock incorporates a dedicated divider and permits selecting 6 types of clock by the internal synchronous clock selection bits (b2, b1, b0) of serial I/O2 control register 1.

Regarding SOUT2 and SCLK2 being output pins, either CMOS output format or N-channel open-drain output format can be selected by the P01/SOUT2, P02/SCLK2 P-channel output disable bit (b7) of serial I/O2 control register 1.

When the internal clock has been selected, a transfer starts by a write signal to the serial I/O2 register (address 001716). After completion of data transfer, the level of the SOUT2 pin goes to high impedance automatically but bit 7 of the serial I/O2 control register 2 is not set to "1" automatically.

When the external clock has been selected, the contents of the serial I/O2 register is continuously sifted while transfer clocks are input. Accordingly, control the clock externally. Note that the SOUT2 pin does not go to high impedance after completion of data transfer.

To cause the SOUT2 pin to go to high impedance in the case where the external clock is selected, set bit 7 of the serial I/O2 control register 2 to "1" when SCLK is "H" after completion of data transfer. After the next data transfer is started (the transfer clock falls), bit 7 of the serial I/O2 control register 2 is set to "0" and the SOUT2 pin is put into the active state.

Regardless of the internal clock to external clock, the interrupt request bit is set after the number of bits (1 to 8 bits) selected by the optional transfer bit is transferred. In case of a fractional number of bits less than 8 bits as the last data, the received data to be stored in the serial I/O2 register becomes a fractional number of bits close to MSB if the transfer direction selection bit of serial I/O2 control register 1 is LSB first, or a fractional number of bits close to LSB if the said bit is MSB first. For the remaining bits, the previously received data is shifted.

At transmit operation using the clock synchronous serial I/O, the SCMP2 signal can be output by comparing the state of the transmit pin SOUT2 with the state of the receive pin SIN2 in synchronization with a rise of the transfer clock. If the output level of the SOUT2 pin is equal to the input level to the SIN2 pin, "L" is output from the SCMP2 pin. If not, "H" is output. At this time, an INT2 interrupt request can also be generated. Select a valid edge by bit 2 of the interrupt edge selection register (address 003A16).

[Serial I/O2 Control Registers 1, 2 (SIO2CON1 / SIO2CON2)] 001516, 001616

The serial I/O2 control registers 1 and 2 are containing various selection bits for serial I/O2 control as shown in Figure 23.

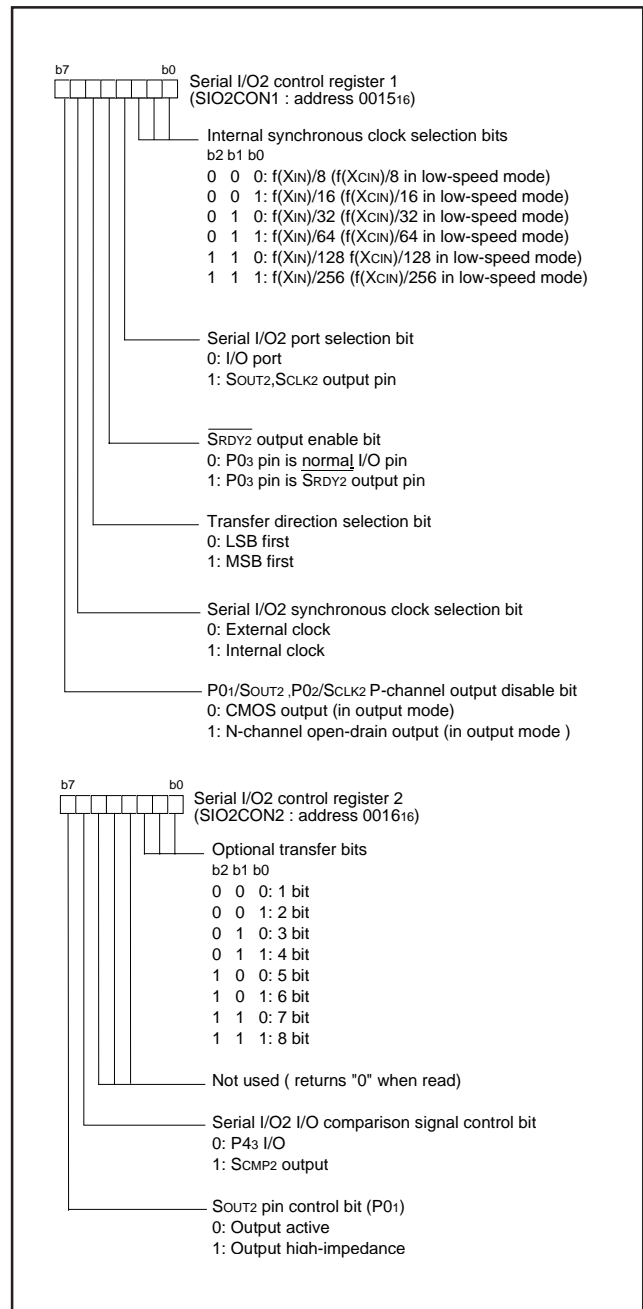


Fig. 23 Structure of Serial I/O2 control registers 1, 2

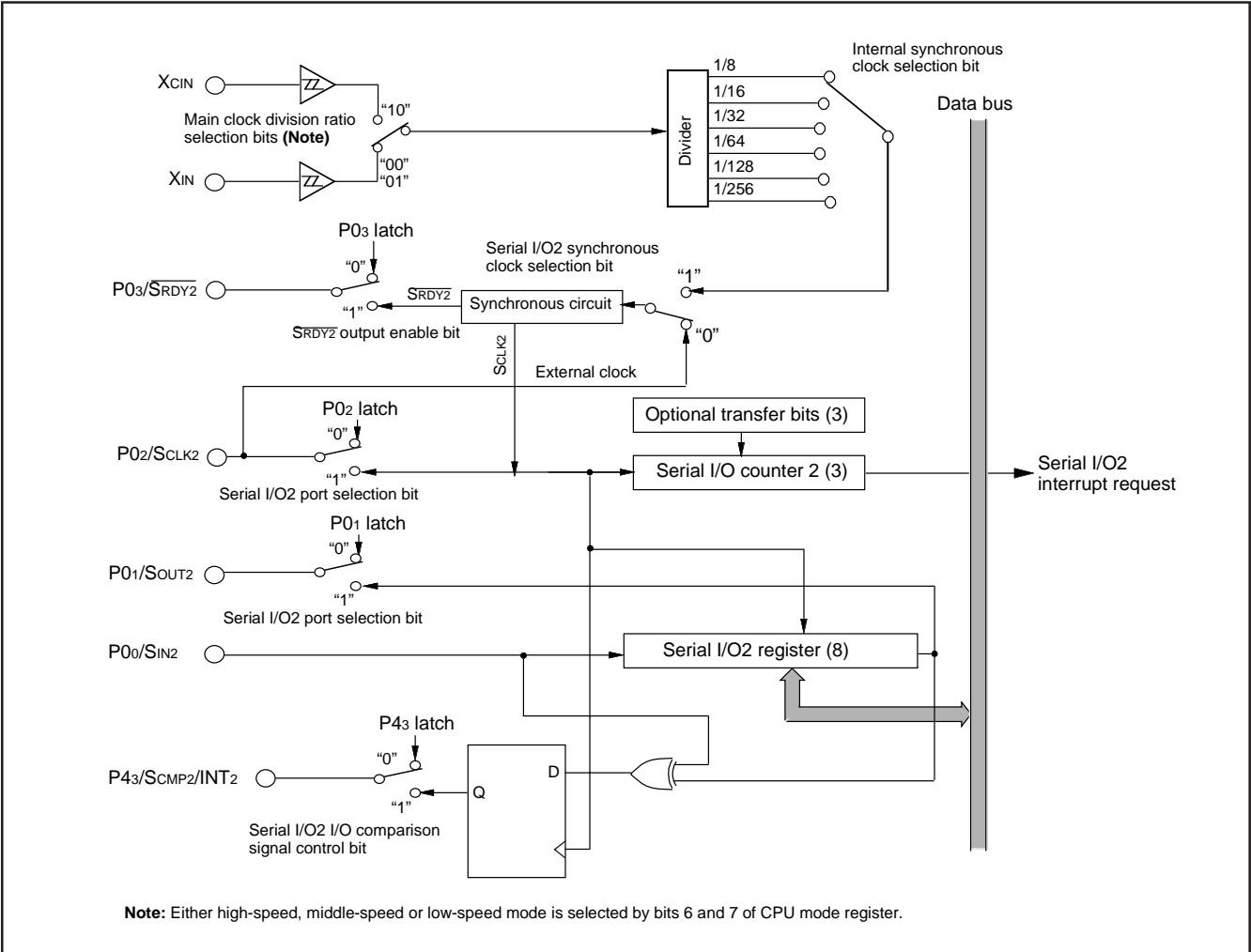


Fig. 24 Block diagram of Serial I/O2

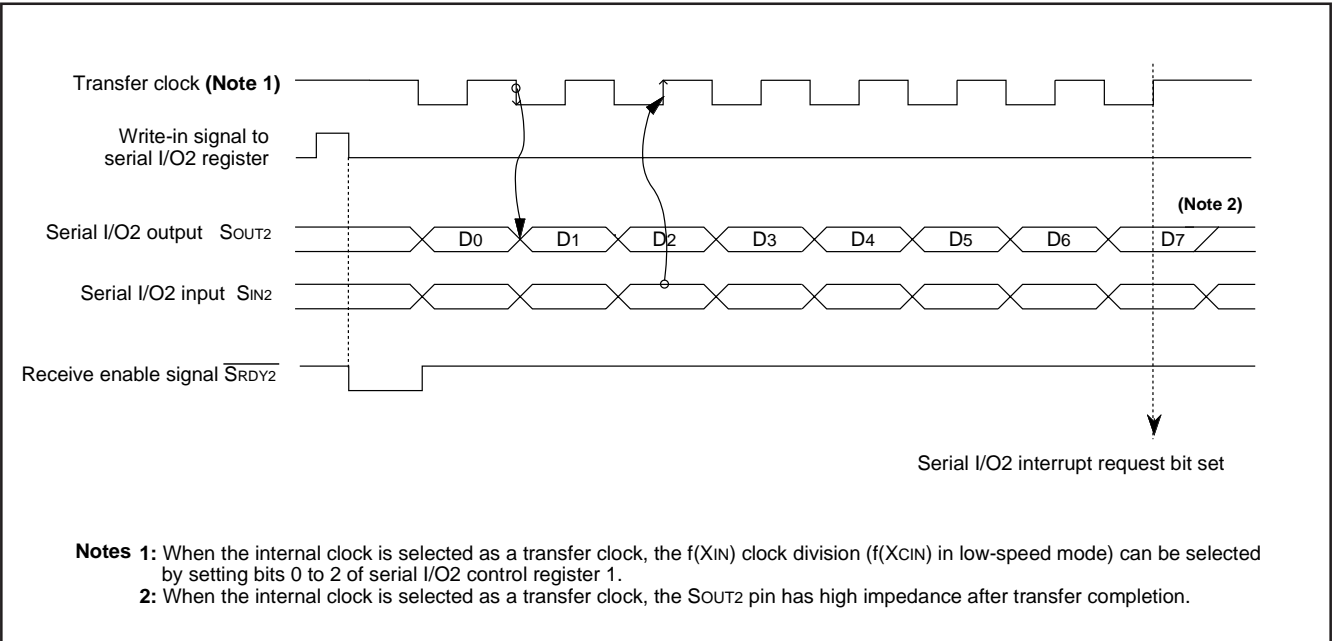


Fig. 25 Timing chart of Serial I/O2

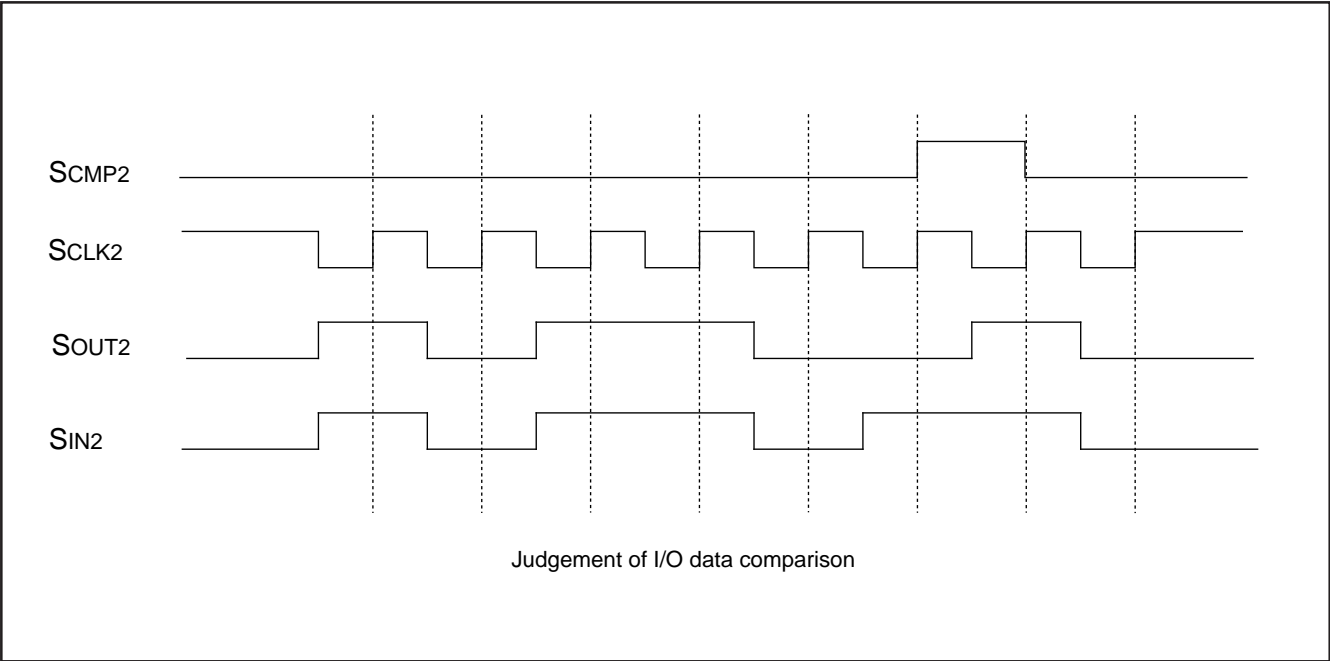


Fig. 26 SCMP2 output operation

PULSE WIDTH MODULATION (PWM)

The 3850 group (spec. H) has a PWM function with an 8-bit resolution, based on a signal that is the clock input X_{IN} or that clock input divided by 2.

Data Setting

The PWM output pin also functions as port P44. Set the PWM period by the PWM prescaler, and set the "H" term of output pulse by the PWM register.

If the value in the PWM prescaler is n and the value in the PWM register is m (where n = 0 to 255 and m = 0 to 255) :

$$\begin{aligned} \text{PWM period} &= 255 \times (n+1) / f(X_{IN}) \\ &= 31.875 \times (n+1) \mu\text{s} \\ &\quad (\text{when } f(X_{IN}) = 8 \text{ MHz, count source selection bit} = "0") \end{aligned}$$

$$\begin{aligned} \text{Output pulse "H" term} &= \text{PWM period} \times m / 255 \\ &= 0.125 \times (n+1) \times m \mu\text{s} \\ &\quad (\text{when } f(X_{IN}) = 8 \text{ MHz, count source selection bit} = "0") \end{aligned}$$

PWM Operation

When bit 0 (PWM enable bit) of the PWM control register is set to "1", operation starts by initializing the PWM output circuit, and pulses are output starting at an "H".

If the PWM register or PWM prescaler is updated during PWM output, the pulses will change in the cycle after the one in which the change was made.

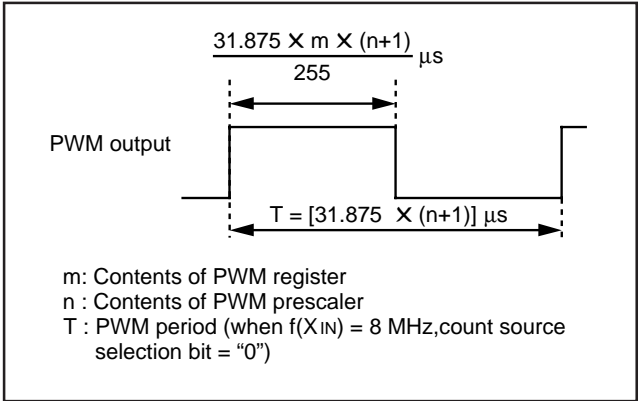


Fig. 27 Timing of PWM period

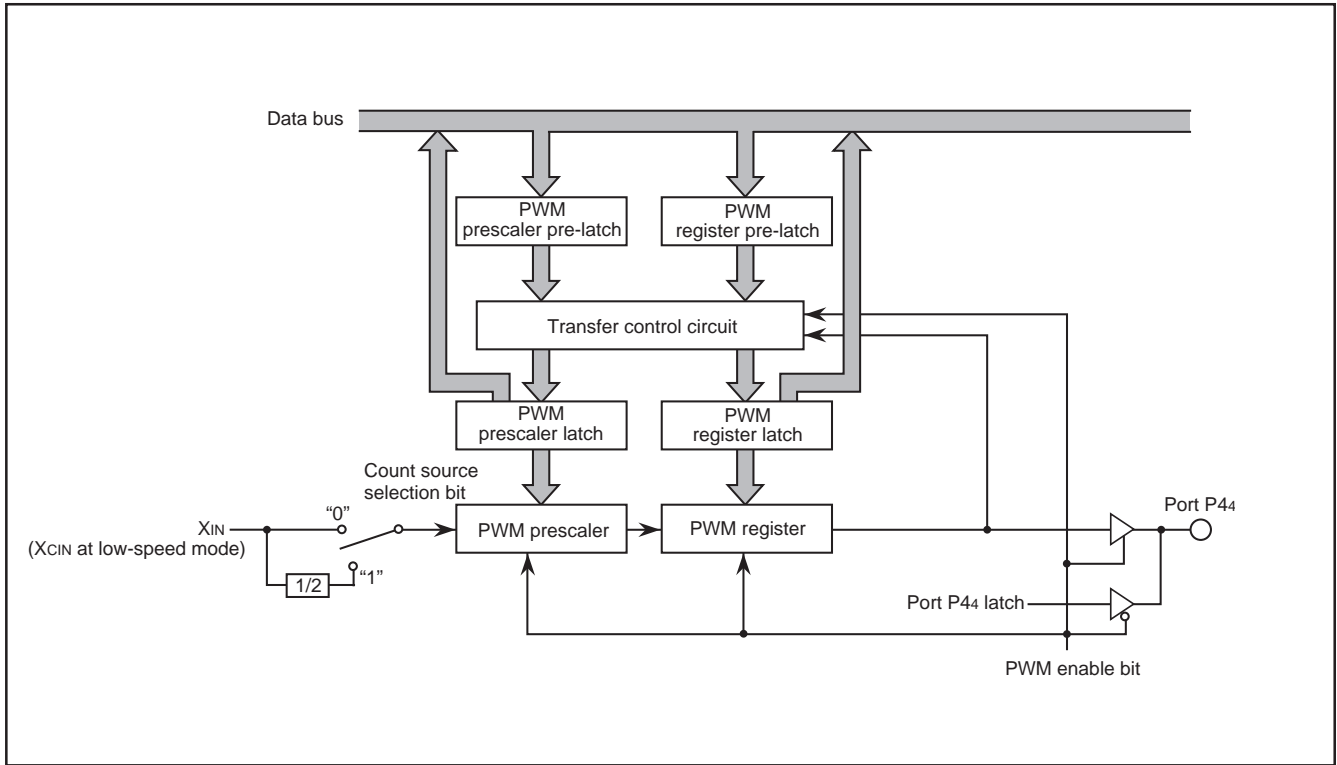


Fig. 28 Block diagram of PWM function

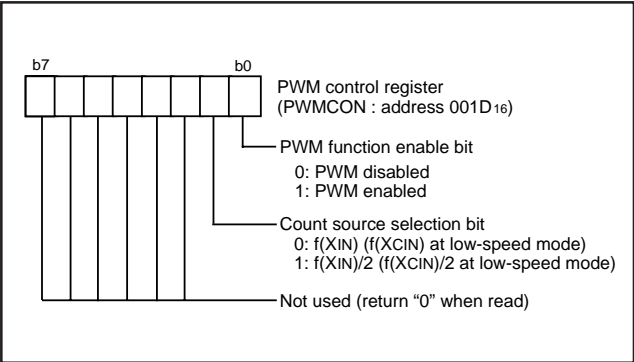


Fig. 29 Structure of PWM control register

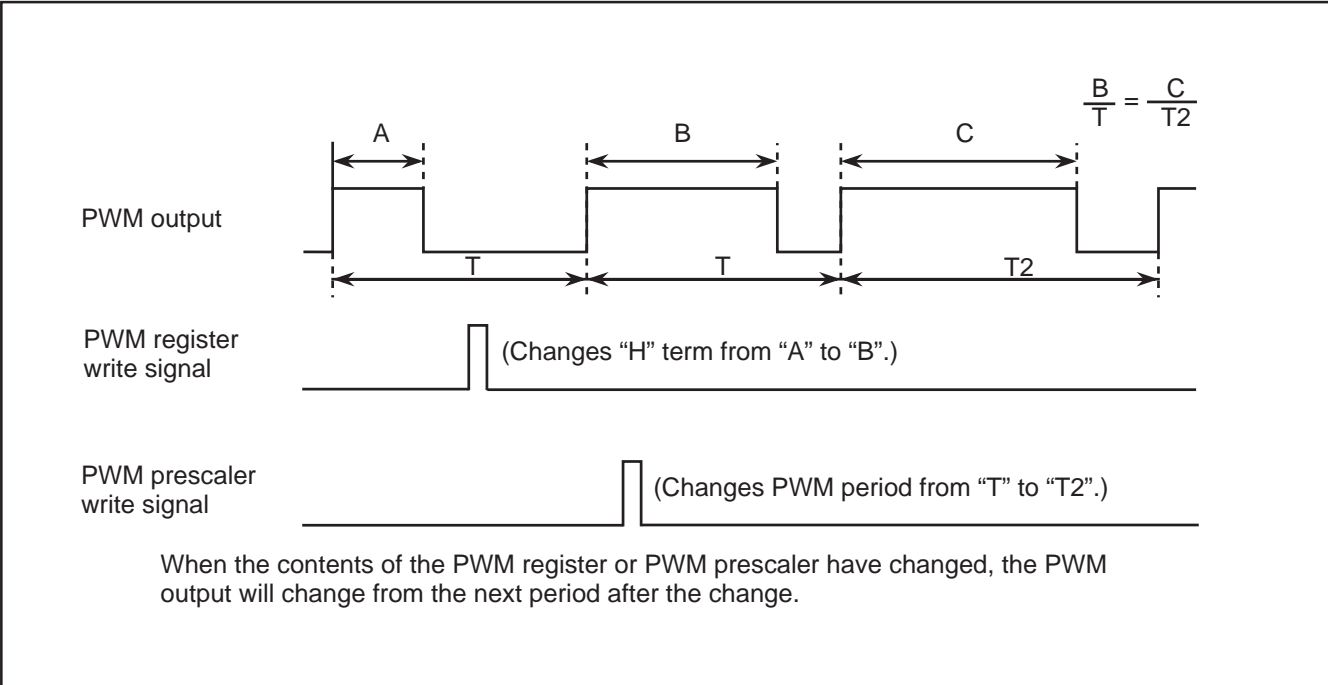


Fig. 30 PWM output timing when PWM register or PWM prescaler is changed

■Note

The PWM starts after the PWM function enable bit is set to enable and "L" level is output from the PWM pin. The length of this "L" level output is as follows:

$$\frac{n+1}{2 \cdot f(XIN)} \text{ sec} \quad (\text{Count source selection bit} = 0, \text{ where } n \text{ is the value set in the prescaler})$$

$$\frac{n+1}{f(XIN)} \text{ sec} \quad (\text{Count source selection bit} = 1, \text{ where } n \text{ is the value set in the prescaler})$$

A-D CONVERTER

[A-D Conversion Registers (ADL, ADH)] 003516, 003616

The A-D conversion registers are read-only registers that store the result of an A-D conversion. Do not read these registers during an A-D conversion.

[AD Control Register (ADCON)] 003416

The AD control register controls the A-D conversion process. Bits 0 to 2 select a specific analog input pin. Bit 4 indicates the completion of an A-D conversion. The value of this bit remains at "0" during an A-D conversion and changes to "1" when an A-D conversion ends. Writing "0" to this bit starts the A-D conversion.

Comparison Voltage Generator

The comparison voltage generator divides the voltage between AVSS and VREF into 1024 and outputs the divided voltages.

Channel Selector

The channel selector selects one of ports P30/AN0 to P34/AN4 and inputs the voltage to the comparator.

Comparator and Control Circuit

The comparator and control circuit compare an analog input voltage with the comparison voltage, and the result is stored in the A-D conversion registers. When an A-D conversion is completed, the control circuit sets the A-D conversion completion bit and the A-D interrupt request bit to "1".

Note that because the comparator consists of a capacitor coupling, set f(XIN) to 500 kHz or more during an A-D conversion. When the A-D converter is operated at low-speed mode, f(XIN) and f(XCIN) do not have the lower limit of frequency, because of the A-D converter has a built-in self-oscillation circuit.

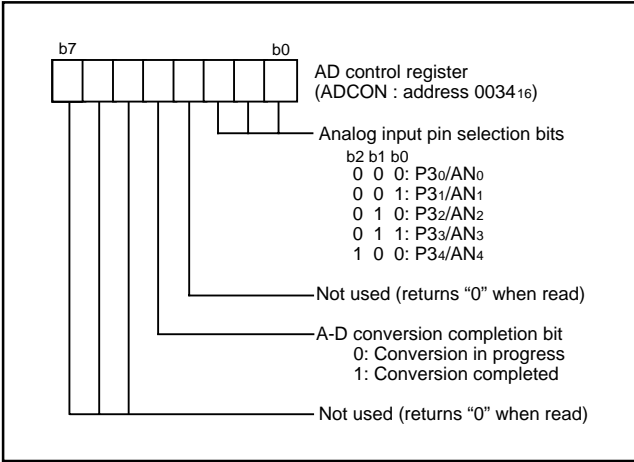


Fig. 31 Structure of AD control register

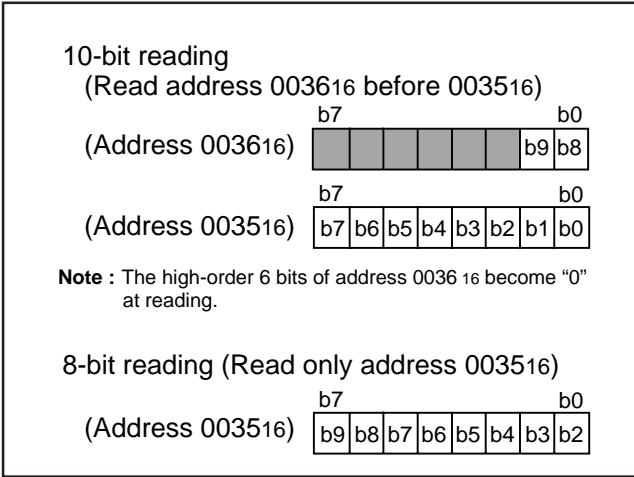


Fig. 32 Structure of A-D conversion registers

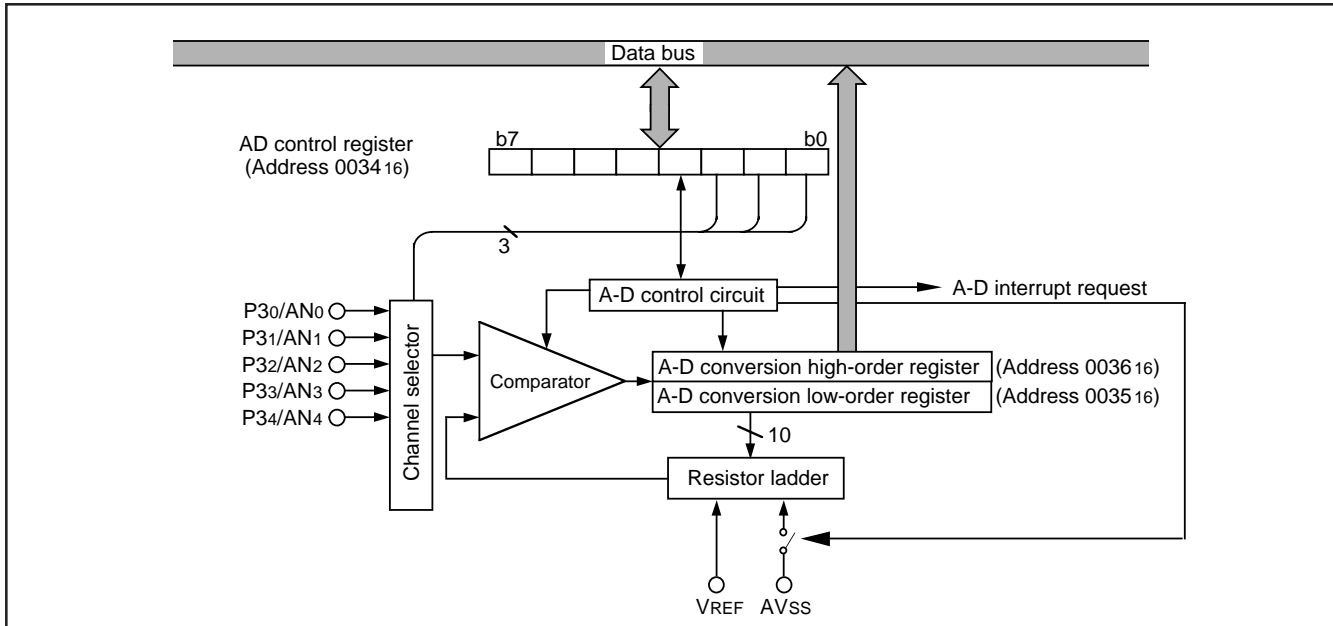


Fig. 33 Block diagram of A-D converter

WATCHDOG TIMER

The watchdog timer gives a mean of returning to the reset status when a program cannot run on a normal loop (for example, because of a software run-away). The watchdog timer consists of an 8-bit watchdog timer L and an 8-bit watchdog timer H.

Standard Operation of Watchdog Timer

When any data is not written into the watchdog timer control register (address 0039₁₆) after reset, the watchdog timer is in the stop state. The watchdog timer starts to count down by writing an optional value into the watchdog timer control register (address 0039₁₆) and an internal reset occurs at an underflow of the watchdog timer H.

Accordingly, programming is usually performed so that writing to the watchdog timer control register (address 0039₁₆) may be started before an underflow. When the watchdog timer control register (address 0039₁₆) is read, the values of the high-order 6 bits of the watchdog timer H, STP instruction disable bit, and watchdog timer H count source selection bit are read.

Initial value of watchdog timer

At reset or writing to the watchdog timer control register (address 0039₁₆), each watchdog timer H and L is set to "FF₁₆."

Watchdog timer H count source selection bit operation

Bit 7 of the watchdog timer control register (address 0039₁₆) permits selecting a watchdog timer H count source. When this bit is set to "0", the count source becomes the underflow signal of watchdog timer L. The detection time is set to 131.072 ms at f(X_{IN}) = 8 MHz frequency and 32.768 s at f(X_{CIN}) = 32 kHz frequency. When this bit is set to "1", the count source becomes the signal divided by 16 for f(X_{IN}) (or f(X_{CIN})). The detection time in this case is set to 512 μs at f(X_{IN}) = 8 MHz frequency and 128 ms at f(X_{CIN}) = 32 kHz frequency. This bit is cleared to "0" after reset.

Operation of STP instruction disable bit

Bit 6 of the watchdog timer control register (address 0039₁₆) permits disabling the STP instruction when the watchdog timer is in operation.

When this bit is "0", the STP instruction is enabled. When this bit is "1", the STP instruction is disabled, once the STP instruction is executed, an internal reset occurs. When this bit is set to "1", it cannot be rewritten to "0" by program. This bit is cleared to "0" after reset.

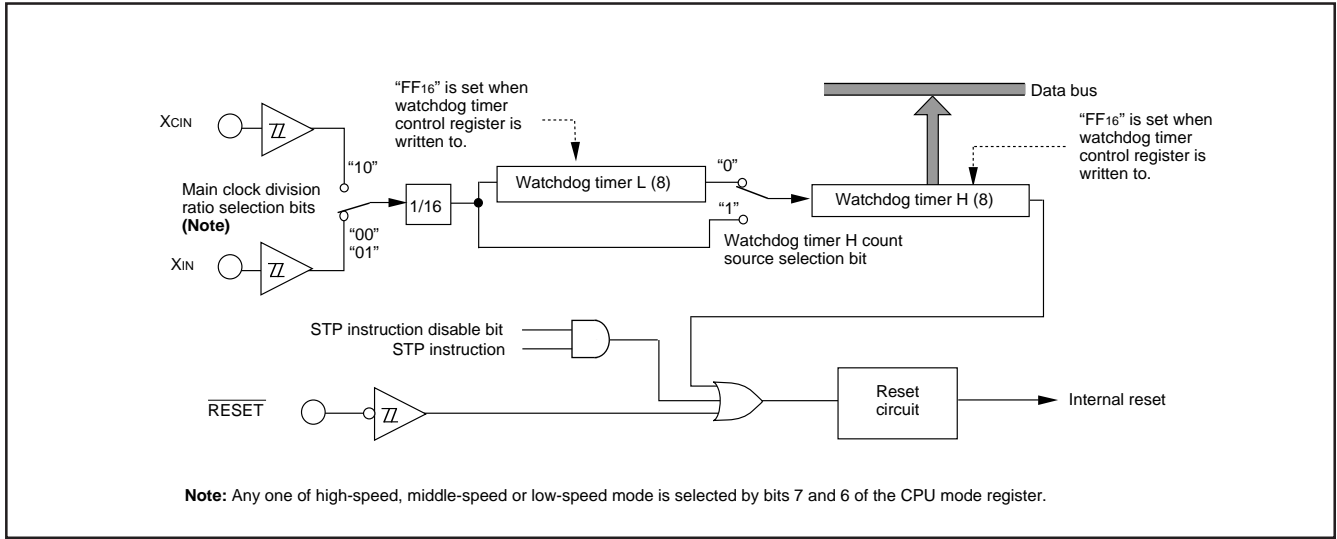


Fig. 34 Block diagram of Watchdog timer

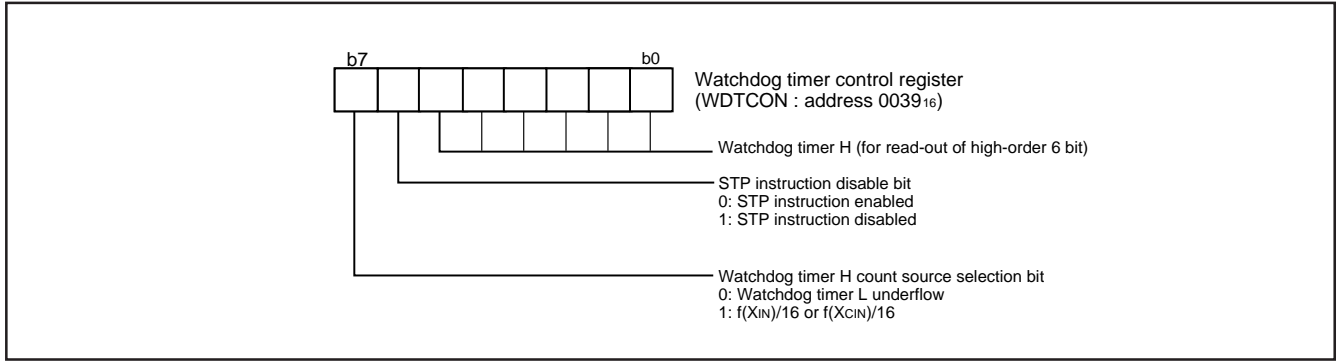


Fig. 35 Structure of Watchdog timer control register

RESET CIRCUIT

To reset the microcomputer, RESET pin must be held at an "L" level for 2 μs or more. Then the RESET pin is returned to an "H" level (the power source voltage must be between 2.7 V and 5.5 V, and the oscillation must be stable), reset is released. After the reset is completed, the program starts from the address contained in address FFFD16 (high-order byte) and address FFFC16 (low-order byte). Make sure that the reset input voltage is less than 0.54 V for Vcc of 2.7 V.

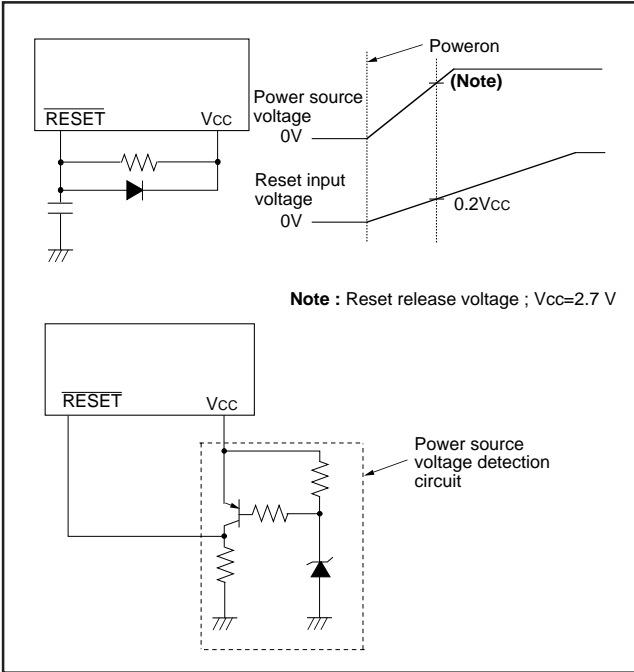


Fig. 36 Reset circuit example

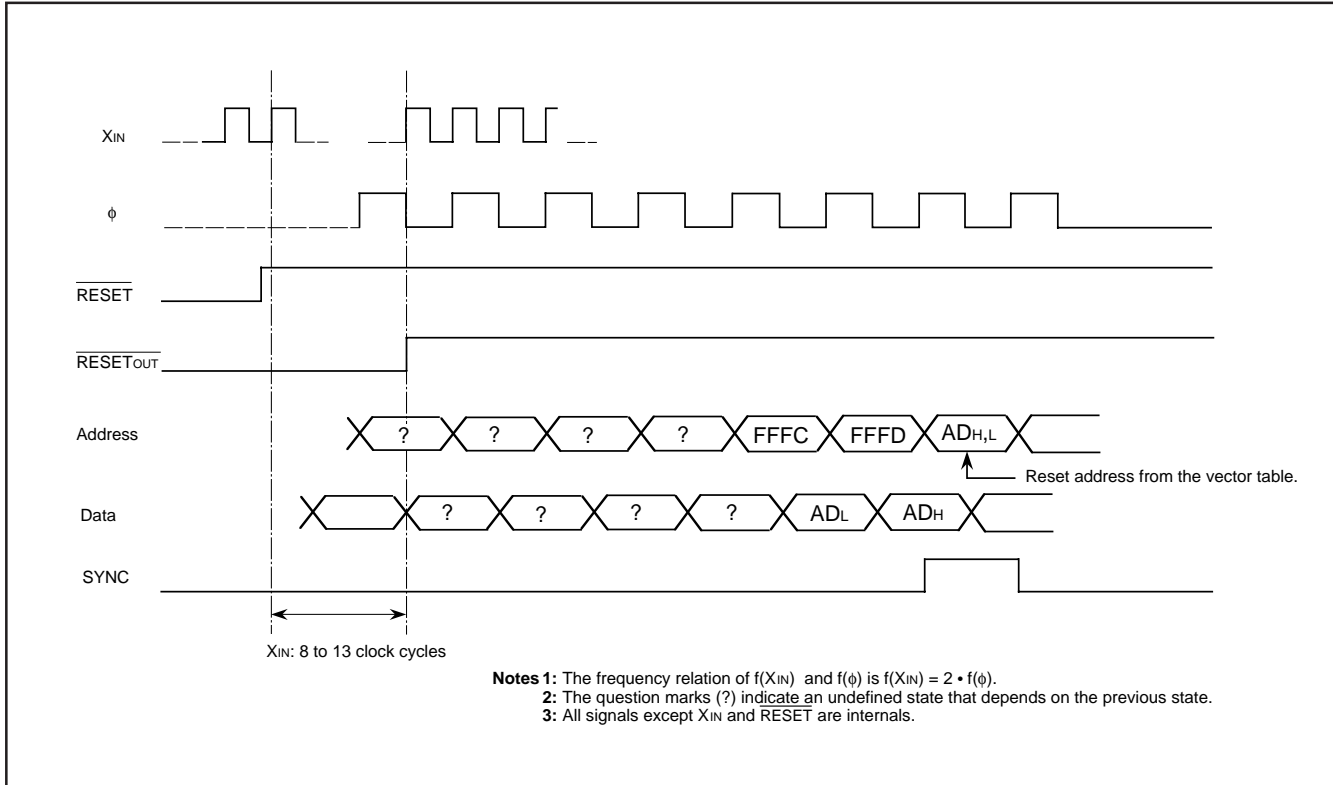


Fig. 37 Reset sequence

- Notes 1: The frequency relation of $f(X_{IN})$ and $f(\phi)$ is $f(X_{IN}) = 2 \cdot f(\phi)$.
- 2: The question marks (?) indicate an undefined state that depends on the previous state.
- 3: All signals except X_{IN} and RESET are internals.

	Address	Register contents		Address	Register contents
(1) Port P0 (P0)	0000 ₁₆	00 ₁₆	(34) MISRG	0038 ₁₆	00 ₁₆
(2) Port P0 direction register (P0D)	0001 ₁₆	00 ₁₆	(35) Watchdog timer control register (WDTCON)	0039 ₁₆	0 0 1 1 1 1 1 1
(3) Port P1 (P1)	0002 ₁₆	00 ₁₆	(36) Interrupt edge selection register (INTEDGE)	003A ₁₆	00 ₁₆
(4) Port P1 direction register (P1D)	0003 ₁₆	00 ₁₆	(37) CPU mode register (CPUM)	003B ₁₆	0 1 0 0 1 0 0 0
(5) Port P2 (P2)	0004 ₁₆	00 ₁₆	(38) Interrupt request register 1 (IREQ1)	003C ₁₆	00 ₁₆
(6) Port P2 direction register (P2D)	0005 ₁₆	00 ₁₆	(39) Interrupt request register 2 (IREQ2)	003D ₁₆	00 ₁₆
(7) Port P3 (P3)	0006 ₁₆	00 ₁₆	(40) Interrupt control register 1 (ICON1)	003E ₁₆	00 ₁₆
(8) Port P3 direction register (P3D)	0007 ₁₆	00 ₁₆	(41) Interrupt control register 2 (ICON2)	003F ₁₆	00 ₁₆
(9) Port P4 (P4)	0008 ₁₆	00 ₁₆	(42) Processor status register	(PS)	X X X X X 1 X X
(10) Port P4 direction register (P4D)	0009 ₁₆	00 ₁₆	(43) Program counter	(PC _H)	FFFD ₁₆ contents
(11) Serial I/O2 control register 1 (SIO2CON1)	0015 ₁₆	00 ₁₆		(PC _L)	FFFC ₁₆ contents
(12) Serial I/O2 control register 2 (SIO2CON2)	0016 ₁₆	0 0 0 0 0 1 1 1			
(13) Serial I/O2 register (SIO2)	0017 ₁₆	X X X X X X X X			
(14) Transmit/Receive buffer register (TB/RB)	0018 ₁₆	X X X X X X X X			
(15) Serial I/O1 status register (SIOSTS)	0019 ₁₆	1 0 0 0 0 0 0 0			
(16) Serial I/O1 control register (SIOCON)	001A ₁₆	00 ₁₆			
(17) UART control register (UARTCON)	001B ₁₆	1 1 1 0 0 0 0 0			
(18) Baud rate generator (BRG)	001C ₁₆	X X X X X X X X			
(19) PWM control register (PWMCON)	001D ₁₆	00 ₁₆			
(20) PWM prescaler (PREPWM)	001E ₁₆	X X X X X X X X			
(21) PWM register (PWM)	001F ₁₆	X X X X X X X X			
(22) Prescaler 12 (PRE12)	0020 ₁₆	FF ₁₆			
(23) Timer 1 (T1)	0021 ₁₆	01 ₁₆			
(24) Timer 2 (T2)	0022 ₁₆	00 ₁₆			
(25) Timer XY mode register (TM)	0023 ₁₆	00 ₁₆			
(26) Prescaler X (PREX)	0024 ₁₆	FF ₁₆			
(27) Timer X (TX)	0025 ₁₆	FF ₁₆			
(28) Prescaler Y (PREY)	0026 ₁₆	FF ₁₆			
(29) Timer Y (TY)	0027 ₁₆	FF ₁₆			
(30) Timer count source selection register (TCSS)	0028 ₁₆	00 ₁₆			
(31) A-D control register (ADCON)	0034 ₁₆	0 0 0 1 0 0 0 0			
(32) A-D conversion low-order register (ADL)	0035 ₁₆	X X X X X X X X			
(33) A-D conversion high-order register (ADH)	0036 ₁₆	0 0 0 0 0 0 X X			

Note : X : Not fixed
 Since the initial values for other than above mentioned registers and RAM contents are indefinite at reset, they must be set.

Fig. 38 Internal status at reset

CLOCK GENERATING CIRCUIT

The 3850 group (spec. H) has two built-in oscillation circuits. An oscillation circuit can be formed by connecting a resonator between XIN and XOUT (XCIN and XCOUT). Use the circuit constants in accordance with the resonator manufacturer's recommended values. No external resistor is needed between XIN and XOUT since a feed-back resistor exists on-chip. However, an external feed-back resistor is needed between XCIN and XCOUT. Immediately after power on, only the XIN oscillation circuit starts oscillating, and XCIN and XCOUT pins function as I/O ports.

Frequency Control

(1) Middle-speed mode

The internal clock ϕ is the frequency of XIN divided by 8. After reset, this mode is selected.

(2) High-speed mode

The internal clock ϕ is half the frequency of XIN.

(3) Low-speed mode

The internal clock ϕ is half the frequency of XCIN.

■Note

If you switch the mode between middle/high-speed and low-speed, stabilize both XIN and XCIN oscillations. The sufficient time is required for the sub-clock to stabilize, especially immediately after power on and at returning from the stop mode. When switching the mode between middle/high-speed and low-speed, set the frequency on condition that $f(XIN) > 3 \cdot f(XCIN)$.

(4) Low power dissipation mode

The low power consumption operation can be realized by stopping the main clock XIN in low-speed mode. To stop the main clock, set bit 5 of the CPU mode register to "1." When the main clock XIN is restarted (by setting the main clock stop bit to "0"), set sufficient time for oscillation to stabilize.

The sub-clock XCIN-XCOUT oscillating circuit can not directly input clocks that are generated externally. Accordingly, make sure to cause an external resonator to oscillate.

Oscillation Control

(1) Stop mode

If the STP instruction is executed, the internal clock ϕ stops at an "H" level, and XIN and XCIN oscillation stops. When the oscillation stabilizing time set after STP instruction released bit is "0," the prescaler 12 is set to "FF16" and timer 1 is set to "0116." When the oscillation stabilizing time set after STP instruction released bit is "1," set the sufficient time for oscillation of used oscillator to stabilize since nothing is set to the prescaler 12 and timer 1.

Either XIN or XCIN divided by 16 is input to the prescaler 12 as count source. Oscillator restarts when an external interrupt is received, but the internal clock ϕ is not supplied to the CPU (remains at "H") until timer 1 underflows. The internal clock ϕ is supplied for the first time, when timer 1 underflows. This ensures time for the clock oscillation using the ceramic resonators to be stabilized. When the oscillator is restarted by reset, apply "L" level to the RESET pin until the oscillation is stable since a wait time will not be generated.

(2) Wait mode

If the WIT instruction is executed, the internal clock ϕ stops at an "H" level, but the oscillator does not stop. The internal clock ϕ restarts at reset or when an interrupt is received. Since the oscillator does not stop, normal operation can be started immediately after the clock is restarted.

To ensure that the interrupts will be received to release the STP or WIT state, their interrupt enable bits must be set to "1" before executing of the STP or WIT instruction.

When releasing the STP state, the prescaler 12 and timer 1 will start counting the clock XIN divided by 16. Accordingly, set the timer 1 interrupt enable bit to "0" before executing the STP instruction.

■Note

When using the oscillation stabilizing time set after STP instruction released bit set to "1", evaluate time to stabilize oscillation of the used oscillator and set the value to the timer 1 and prescaler 12.

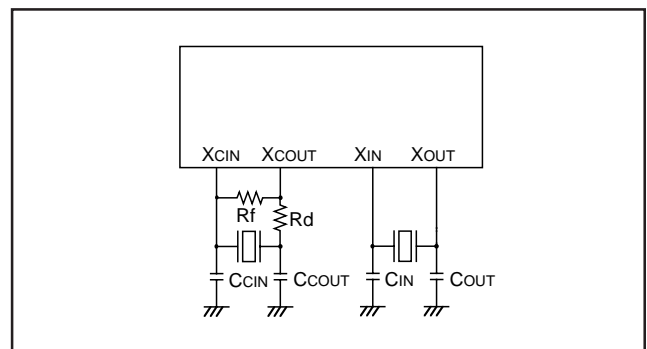


Fig. 39 Ceramic resonator circuit

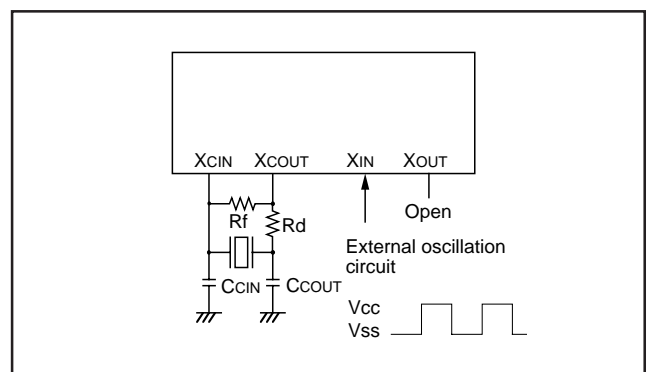


Fig. 40 External clock input circuit

[MISRG (MISRG)] 003816

MISRG consists of three control bits (bits 1 to 3) for middle-speed mode automatic switch and one control bit (bit 0) for oscillation stabilizing time set after STP instruction released.

By setting the middle-speed mode automatic switch start bit to "1" while operating in the low-speed mode and setting the middle-speed mode automatic switch set bit to "1", XIN oscillation automatically starts and the mode is automatically switched to the middle-speed mode.

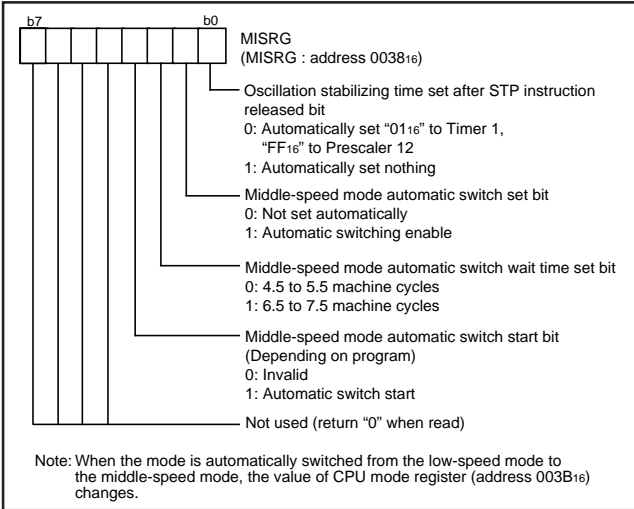


Fig. 41 Structure of MISRG

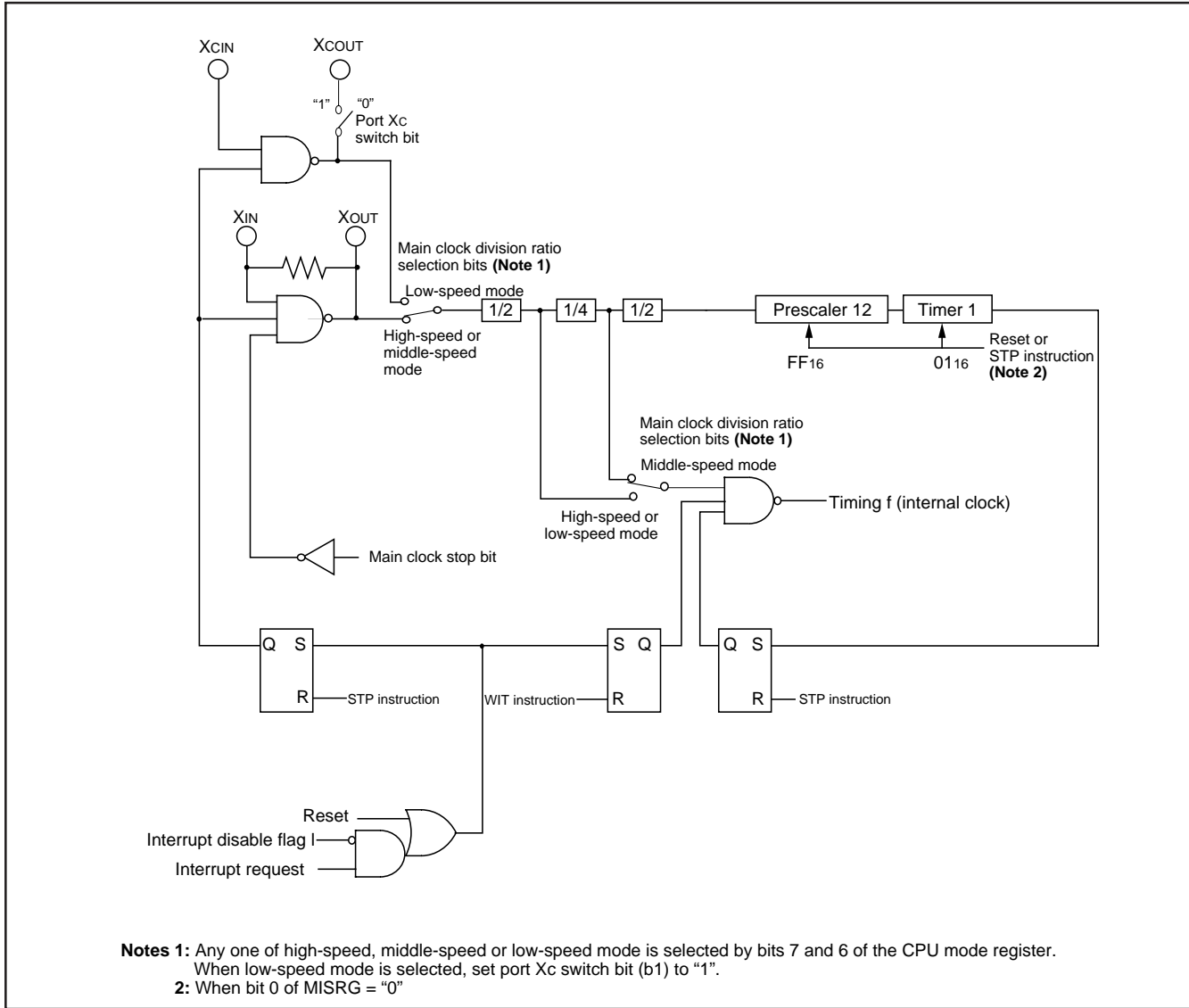
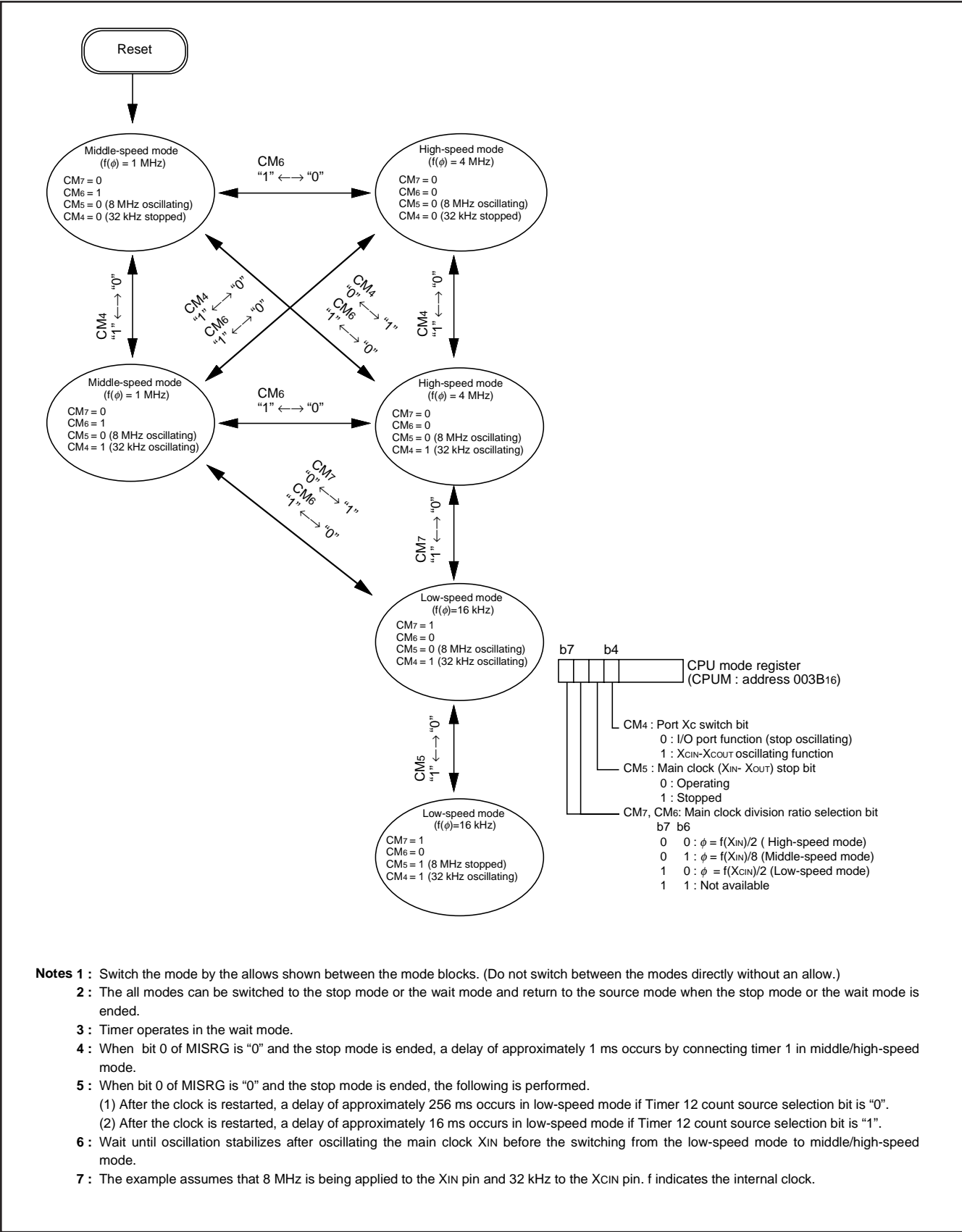


Fig. 42 System clock generating circuit block diagram (Single-chip mode)



- Notes 1 :** Switch the mode by the allows shown between the mode blocks. (Do not switch between the modes directly without an allow.)
- 2 :** The all modes can be switched to the stop mode or the wait mode and return to the source mode when the stop mode or the wait mode is ended.
- 3 :** Timer operates in the wait mode.
- 4 :** When bit 0 of MISRG is "0" and the stop mode is ended, a delay of approximately 1 ms occurs by connecting timer 1 in middle/high-speed mode.
- 5 :** When bit 0 of MISRG is "0" and the stop mode is ended, the following is performed.
 (1) After the clock is restarted, a delay of approximately 256 ms occurs in low-speed mode if Timer 12 count source selection bit is "0".
 (2) After the clock is restarted, a delay of approximately 16 ms occurs in low-speed mode if Timer 12 count source selection bit is "1".
- 6 :** Wait until oscillation stabilizes after oscillating the main clock XIN before the switching from the low-speed mode to middle/high-speed mode.
- 7 :** The example assumes that 8 MHz is being applied to the XIN pin and 32 kHz to the XCIN pin. f indicates the internal clock.

Fig. 43 State transitions of system clock

NOTES ON PROGRAMMING

Processor Status Register

The contents of the processor status register (PS) after a reset are undefined, except for the interrupt disable flag (I) which is "1." After a reset, initialize flags which affect program execution. In particular, it is essential to initialize the index X mode (T) and the decimal mode (D) flags because of their effect on calculations.

Interrupts

The contents of the interrupt request bits do not change immediately after they have been written. After writing to an interrupt request register, execute at least one instruction before performing a BBC or BBS instruction.

Decimal Calculations

- To calculate in decimal notation, set the decimal mode flag (D) to "1", then execute an ADC or SBC instruction. After executing an ADC or SBC instruction, execute at least one instruction before executing a SEC, CLC, or CLD instruction.
- In decimal mode, the values of the negative (N), overflow (V), and zero (Z) flags are invalid.

Timers

If a value n (between 0 and 255) is written to a timer latch, the frequency division ratio is $1/(n+1)$.

Multiplication and Division Instructions

- The index X mode (T) and the decimal mode (D) flags do not affect the MUL and DIV instruction.
- The execution of these instructions does not change the contents of the processor status register.

Ports

The contents of the port direction registers cannot be read. The following cannot be used:

- The data transfer instruction (LDA, etc.)
- The operation instruction when the index X mode flag (T) is "1"
- The addressing mode which uses the value of a direction register as an index
- The bit-test instruction (BBC or BBS, etc.) to a direction register
- The read-modify-write instructions (ROR, CLB, or SEB, etc.) to a direction register.

Use instructions such as LDM and STA, etc., to set the port direction registers.

Serial I/O

In clock synchronous serial I/O, if the receive side is using an external clock and it is to output the $\overline{\text{SRDY}}_1$ signal, set the transmit enable bit, the receive enable bit, and the $\overline{\text{SRDY}}_1$ output enable bit to "1."

Serial I/O1 continues to output the final bit from the TxD pin after transmission is completed.

SOUT2 pin for serial I/O2 goes to high impedance after transmission is completed.

When an external clock is used as synchronous clock in serial I/O1 or serial I/O2, write transmission data to the transmit buffer register or serial I/O2 register while the transfer clock is "H."

A-D Converter

The comparator uses capacitive coupling amplifier whose charge will be lost if the clock frequency is too low.

Therefore, make sure that $f(\text{XIN})$ in the middle/high-speed mode is at least on 500 kHz during an A-D conversion.

Do not execute the STP or WIT instruction during an A-D conversion.

Instruction Execution Time

The instruction execution time is obtained by multiplying the frequency of the internal clock ϕ by the number of cycles needed to execute an instruction.

The number of cycles required to execute an instruction is shown in the list of machine instructions.

The frequency of the internal clock ϕ is half of the XIN frequency in high-speed mode.

NOTES ON USAGE

Differences between 3850 group (standard) and 3850 group (spec. H)

- (1) The absolute maximum ratings of 3850 group (spec. H) is smaller than that of 3850 group (standard).
 - Power source voltage $V_{CC} = -0.3$ to 6.5 V
 - CNVss input voltage $V_I = -0.3$ to $V_{CC} + 0.3$ V
- (2) The oscillation circuit constants of XIN-XOUT, XCIN-XCOUT may be some differences between 3850 group (standard) and 3850 group (spec. H).
- (3) Do not write any data to the reserved area and the reserved bit. (Do not change the contents after rest.)
- (4) Fix bit 3 of the CPU mode register to "1".
- (5) Be sure to perform the termination of unused pins.

Handling of Source Pins

In order to avoid a latch-up occurrence, connect a capacitor suitable for high frequencies as bypass capacitor between power source pin (V_{CC} pin) and GND pin (V_{SS} pin) and between power source pin (V_{CC} pin) and analog power source input pin (AV_{SS} pin). Besides, connect the capacitor to as close as possible. For bypass capacitor which should not be located too far from the pins to be connected, a ceramic capacitor of 0.01 μF –0.1 μF is recommended.

ELECTRICAL CHARACTERISTICS

Table 7 Absolute maximum ratings

Symbol	Parameter	Conditions	Ratings	Unit	
V _{CC}	Power source voltage		-0.3 to 6.5	V	
V _I	Input voltage	All voltages are based on V _{SS} . Output transistors are cut off.	-0.3 to V _{CC} +0.3	V	
V _I	Input voltage				P00–P07, P10–P17, P20, P21, P24–P27, P30–P34, P40–P44, VREF
V _I	Input voltage		P22, P23	-0.3 to 5.8	V
V _I	Input voltage		RESET, XIN	-0.3 to V _{CC} +0.3	V
V _I	Input voltage		CNV _{SS}	-0.3 to V _{CC} +0.3	V
V _O	Output voltage		P00–P07, P10–P17, P20, P21, P24–P27, P30–P34, P40–P44, XOUT	-0.3 to V _{CC} +0.3	V
V _O	Output voltage	P22, P23	-0.3 to 5.8	V	
P _d	Power dissipation	T _a = 25 °C	1000 (Note)	mW	
T _{opr}	Operating temperature		-20 to 85	°C	
T _{stg}	Storage temperature		-40 to 125	°C	

Note : The rating becomes 300mW at the 42P2R-A/E package.

Table 8 Recommended operating conditions (1)

(V_{CC} = 2.7 to 5.5 V, T_a = -20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
V _{CC}	Power source voltage	8 MHz (high-speed mode)	4.0	5.0	5.5	V
		8 MHz (middle-speed mode), 4 MHz (high-speed mode)	2.7	5.0	5.5	
V _{SS}	Power source voltage			0		V
VREF	A-D convert reference voltage		2.0		V _{CC}	V
AV _{SS}	Analog power source voltage			0		V
V _{IA}	Analog input voltage	AN0–AN4	AV _{SS}		V _{CC}	V
V _{IH}	“H” input voltage	P00–P07, P10–P17, P20–P27, P30–P34, P40–P44	0.8V _{CC}		V _{CC}	V
V _{IH}	“H” input voltage	RESET, XIN, CNV _{SS}	0.8V _{CC}		V _{CC}	V
V _{IL}	“L” input voltage	P00–P07, P10–P17, P20–P27, P30–P34, P40–P44	0		0.2V _{CC}	V
V _{IL}	“L” input voltage	RESET, CNV _{SS}	0		0.2V _{CC}	V
V _{IL}	“L” input voltage	XIN	0		0.16V _{CC}	V
ΣIOH(peak)	“H” total peak output current	P00–P07, P10–P17, P30–P34 (Note)			-80	mA
ΣIOH(peak)	“H” total peak output current	P20, P21, P24–P27, P40–P44 (Note)			-80	mA
ΣIOL(peak)	“L” total peak output current (Note)	P00–P07, P30–P34			80	mA
ΣIOL(peak)	“L” total peak output current (Note)	P10–P17			120	mA
ΣIOL(peak)	“L” total peak output current	P20–P27, P40–P44 (Note)			80	mA
ΣIOH(avg)	“H” total average output current	P00–P07, P10–P17, P30–P34 (Note)			-40	mA
ΣIOH(avg)	“H” total average output current	P20, P21, P24–P27, P40–P44 (Note)			-40	mA
ΣIOL(avg)	“L” total average output current (Note)	P00–P07, P30–P34			40	mA
ΣIOL(avg)	“L” total average output current (Note)	P10–P17			60	mA
ΣIOL(avg)	“L” total average output current	P20–P27, P40–P44 (Note)			40	mA

Note : The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.

Table 9 Recommended operating conditions (2)
(VCC = 2.7 to 5.5 V, Ta = -20 to 85 °C, unless otherwise noted)

Symbol		Parameter	Limits			Unit
			Min.	Typ.	Max.	
IOH(peak)	"H" peak output current	P00-P07, P10-P17, P20, P21, P24-P27, P30-P34, P40-P44 (Note 1)			-10	mA
IOL(peak)	"L" peak output current (Note 1)	P00-P07, P20-P27, P30-P34, P40-P44			10	mA
IOL(peak)	"L" peak output current (Note 1)	P10-P17			20	mA
IOH(avg)	"H" average output current	P00-P07, P10-P17, P20, P21, P24-P27, P30-P34, P40-P44 (Note 2)			-5	mA
IOL(avg)	"L" average output current (Note 2)	P00-P07, P20-P27, P30-P34, P40-P44			5	mA
IOL(avg)	"L" average output current (Note 2)	P10-P17			15	mA
f(XIN)	Internal clock oscillation frequency (VCC = 4.0 to 5.5V) (Note 3)				8	MHz
f(XIN)	Internal clock oscillation frequency (VCC = 2.7 to 5.5V) (Note 3)				4	MHz

Notes 1: The peak output current is the peak current flowing in each port.

2: The average output current IOL(avg), IOH(avg) are average value measured over 100 ms.

3: When the oscillation frequency has a duty cycle of 50%.

Table 10 Electrical characteristics (1)

(V_{CC} = 2.7 to 5.5 V, V_{SS} = 0 V, T_a = -20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V _{OH}	"H" output voltage P00-P07, P10-P17, P20, P21, P24-P27, P30-P34, P40-P44 (Note)	I _{OH} = -10 mA V _{CC} = 4.0-5.5 V	V _{CC} -2.0			V
		I _{OH} = -1.0 mA V _{CC} = 2.7-5.5 V	V _{CC} -1.0			V
V _{OL}	"L" output voltage P00-P07, P20-P27, P30-P34, P40-P44	I _{OL} = 10 mA V _{CC} = 4.0-5.5 V			2.0	V
		I _{OL} = 1.0 mA V _{CC} = 2.7-5.5 V			1.0	V
V _{OL}	"L" output voltage P10-P17	I _{OL} = 20 mA V _{CC} = 4.0-5.5 V			2.0	V
		I _{OL} = 10 mA V _{CC} = 2.7-5.5 V			1.0	V
V _{T+} -V _{T-}	Hysteresis CNTR0, CNTR1, INT0-INT3			0.4		V
V _{T+} -V _{T-}	Hysteresis RxD, SCLK			0.5		V
V _{T+} -V _{T-}	Hysteresis RESET			0.5		V
I _{IH}	"H" input current P00-P07, P10-P17, P20, P21, P24-P27, P30-P34, P40-P44	V _I = V _{CC}			5.0	μA
I _{IH}	"H" input current RESET, CNV _{SS}	V _I = V _{CC}			5.0	μA
I _{IH}	"H" input current X _{IN}	V _I = V _{CC}		4		μA
I _{IL}	"L" input current P00-P07, P10-P17, P20-P27, P30-P34, P40-P44	V _I = V _{SS}			-5.0	μA
I _{IL}	"L" input current RESET, CNV _{SS}	V _I = V _{SS}			-5.0	μA
I _{IL}	"L" input current X _{IN}	V _I = V _{SS}		-4		μA
VRAM	RAM hold voltage	When clock stopped	2.0		5.5	V

Note: P25 is measured when the P25/TxD P-channel output disable bit of the UART control register (bit 4 of address 001B16) is "0".

Table 11 Electrical characteristics (2)
 (VCC = 2.7 to 5.5 V, VSS = 0 V, Ta = -20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit	
			Min.	Typ.	Max.		
ICC	Power source current	High-speed mode f(XIN) = 8 MHz f(XCIN) = 32.768 kHz Output transistors "off"		6.8	13	mA	
		High-speed mode f(XIN) = 8 MHz (in WIT state) f(XCIN) = 32.768 kHz Output transistors "off"		1.6		mA	
		Low-speed mode f(XIN) = stopped f(XCIN) = 32.768 kHz Output transistors "off"		60	200	μA	
		Low-speed mode f(XIN) = stopped f(XCIN) = 32.768 kHz (in WIT state) Output transistors "off"		20	40	μA	
		Low-speed mode (VCC = 3 V) f(XIN) = stopped f(XCIN) = 32.768 kHz Output transistors "off"		20	55	μA	
		Low-speed mode (VCC = 3 V) f(XIN) = stopped f(XCIN) = 32.768 kHz (in WIT state) Output transistors "off"		5.0	10.0	μA	
		Middle-speed mode f(XIN) = 8 MHz f(XCIN) = stopped Output transistors "off"		4.0	7.0	mA	
		Middle-speed mode f(XIN) = 8 MHz (in WIT state) f(XCIN) = stopped Output transistors "off"		1.5		mA	
		Increment when A-D conversion is executed f(XIN) = 8 MHz		800		μA	
		All oscillation stopped (in STP state) Output transistors "off"	Ta = 25 °C		0.1	1.0	μA
			Ta = 85 °C			10	μA

Table 12 A-D converter characteristics

(VCC = 2.7 to 5.5 V, VSS = AVSS = 0 V, Ta = -20 to 85 °C, f(XIN) = 8 MHz, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
-	Resolution					10	bit
-	Absolute accuracy (excluding quantization error)					±4	LSB
tCONV	Conversion time		High-speed mode, Middle-speed mode			61	2tc(XIN)
			Low-speed mode		40		μs
RLADDER	Ladder resistor				35		kΩ
IVREF	Reference power source input current	VREF "on"	VREF = 5.0 V	50	150	200	μA
		VREF "off"				5.0	
II(AD)	A-D port input current				0.5	5.0	μA

TIMING REQUIREMENTS

Table 13 Timing requirements (1)

(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, T_a = -20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t _w ($\overline{\text{RESET}}$)	Reset input "L" pulse width	2			μs
t _c (X _{IN})	External clock input cycle time	125			ns
t _{WH} (X _{IN})	External clock input "H" pulse width	50			ns
t _{WL} (X _{IN})	External clock input "L" pulse width	50			ns
t _c (CNTR)	CNTR ₀ , CNTR ₁ input cycle time	200			ns
t _{WH} (CNTR)	CNTR ₀ , CNTR ₁ input "H" pulse width	80			ns
t _{WL} (CNTR)	CNTR ₀ , CNTR ₁ input "L" pulse width	80			ns
t _{WH} (INT)	INT ₀ to INT ₃ input "H" pulse width	80			ns
t _{WL} (INT)	INT ₀ to INT ₃ input "L" pulse width	80			ns
t _c (SCLK1)	Serial I/O1 clock input cycle time (Note)	800			ns
t _{WH} (SCLK1)	Serial I/O1 clock input "H" pulse width (Note)	370			ns
t _{WL} (SCLK1)	Serial I/O1 clock input "L" pulse width (Note)	370			ns
t _{su} (RxD-SCLK1)	Serial I/O1 input setup time	220			ns
t _h (SCLK1-RxD)	Serial I/O1 input hold time	100			ns
t _c (SCLK2)	Serial I/O2 clock input cycle time	1000			ns
t _{WH} (SCLK2)	Serial I/O2 clock input "H" pulse width	400			ns
t _{WL} (SCLK2)	Serial I/O2 clock input "L" pulse width	400			ns
t _{su} (SIN2-SCLK2)	Serial I/O2 clock input setup time	200			ns
t _h (SCLK2-SIN2)	Serial I/O2 clock input hold time	200			ns

Note : When f(X_{IN}) = 8 MHz and bit 6 of address 001A₁₆ is "1" (clock synchronous).
Divide this value by four when f(X_{IN}) = 8 MHz and bit 6 of address 001A₁₆ is "0" (UART).

Table 14 Timing requirements (2)

(V_{CC} = 2.7 to 5.5 V, V_{SS} = 0 V, T_a = -20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t _w ($\overline{\text{RESET}}$)	Reset input "L" pulse width	2			μs
t _c (X _{IN})	External clock input cycle time	250			ns
t _{WH} (X _{IN})	External clock input "H" pulse width	100			ns
t _{WL} (X _{IN})	External clock input "L" pulse width	100			ns
t _c (CNTR)	CNTR ₀ , CNTR ₁ input cycle time	500			ns
t _{WH} (CNTR)	CNTR ₀ , CNTR ₁ input "H" pulse width	230			ns
t _{WL} (CNTR)	CNTR ₀ , CNTR ₁ input "L" pulse width	230			ns
t _{WH} (INT)	INT ₀ to INT ₃ input "H" pulse width	230			ns
t _{WL} (INT)	INT ₀ to INT ₃ input "L" pulse width	230			ns
t _c (SCLK1)	Serial I/O1 clock input cycle time (Note)	2000			ns
t _{WH} (SCLK1)	Serial I/O1 clock input "H" pulse width (Note)	950			ns
t _{WL} (SCLK1)	Serial I/O1 clock input "L" pulse width (Note)	950			ns
t _{su} (RxD-SCLK1)	Serial I/O1 input setup time	400			ns
t _h (SCLK1-RxD)	Serial I/O1 input hold time	200			ns
t _c (SCLK2)	Serial I/O2 clock input cycle time	2000			ns
t _{WH} (SCLK2)	Serial I/O2 clock input "H" pulse width	950			ns
t _{WL} (SCLK2)	Serial I/O2 clock input "L" pulse width	950			ns
t _{su} (SIN2-SCLK2)	Serial I/O2 clock input setup time	400			ns
t _h (SCLK2-SIN2)	Serial I/O2 clock input hold time	300			ns

Note : When f(X_{IN}) = 4 MHz and bit 6 of address 001A₁₆ is "1" (clock synchronous).
Divide this value by four when f(X_{IN}) = 4 MHz and bit 6 of address 001A₁₆ is "0" (UART).

Table 15 Switching characteristics (1)

(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, T_a = -20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
t _{WH} (SCLK1)	Serial I/O1 clock output "H" pulse width	Fig.44	t _C (SCLK1)/2-30			ns
t _{WL} (SCLK1)	Serial I/O1 clock output "L" pulse width		t _C (SCLK1)/2-30			ns
t _d (SCLK1-TXD)	Serial I/O1 output delay time (Note 1)				140	ns
t _v (SCLK1-TXD)	Serial I/O1 output valid time (Note 1)		-30			ns
t _r (SCLK1)	Serial I/O1 clock output rising time				30	ns
t _f (SCLK1)	Serial I/O1 clock output falling time				30	ns
t _{WH} (SCLK2)	Serial I/O2 clock output "H" pulse width		t _C (SCLK2)/2-160			ns
t _{WL} (SCLK2)	Serial I/O2 clock output "L" pulse width		t _C (SCLK2)/2-160			ns
t _d (SCLK2-SOUT2)	Serial I/O2 output delay time (Note 2)				200	ns
t _v (SCLK2-SOUT2)	Serial I/O2 output valid time (Note 2)		0			ns
t _f (SCLK2)	Serial I/O2 clock output falling time				30	ns
t _r (CMOS)	CMOS output rising time (Note 3)			10	30	ns
t _f (CMOS)	CMOS output falling time (Note 3)			10	30	ns

Notes 1: When the P25/TXD P-channel output disable bit of the UART control register (bit 4 of address 001B16) is "0".

2: When the P01/SOUT2 and P02/SCLK2 P-channel output disable bit of the Serial I/O2 control register 1 (bit 7 of address 001516) is "0".

3: The XOUT pin is excluded.

Table 16 Switching characteristics (2)

(V_{CC} = 2.7 to 5.5 V, V_{SS} = 0 V, T_a = -20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
t _{WH} (SCLK1)	Serial I/O1 clock output "H" pulse width	Fig.44	t _C (SCLK1)/2-50			ns
t _{WL} (SCLK1)	Serial I/O1 clock output "L" pulse width		t _C (SCLK1)/2-50			ns
t _d (SCLK1-TXD)	Serial I/O1 output delay time (Note 1)				350	ns
t _v (SCLK1-TXD)	Serial I/O1 output valid time (Note 1)		-30			ns
t _r (SCLK1)	Serial I/O1 clock output rising time				50	ns
t _f (SCLK1)	Serial I/O1 clock output falling time				50	ns
t _{WH} (SCLK2)	Serial I/O2 clock output "H" pulse width		t _C (SCLK2)/2-240			ns
t _{WL} (SCLK2)	Serial I/O2 clock output "L" pulse width		t _C (SCLK2)/2-240			ns
t _d (SCLK2-SOUT2)	Serial I/O2 output delay time (Note 2)				400	ns
t _v (SCLK2-SOUT2)	Serial I/O2 output valid time (Note 2)		0			ns
t _f (SCLK2)	Serial I/O2 clock output falling time				50	ns
t _r (CMOS)	CMOS output rising time (Note 3)			20	50	ns
t _f (CMOS)	CMOS output falling time (Note 3)			20	50	ns

Notes 1: When the P25/TXD P-channel output disable bit of the UART control register (bit 4 of address 001B16) is "0".

2: When the P01/SOUT2 and P02/SCLK2 P-channel output disable bit of the Serial I/O2 control register 1 (bit 7 of address 001516) is "0".

3: The XOUT pin is excluded.

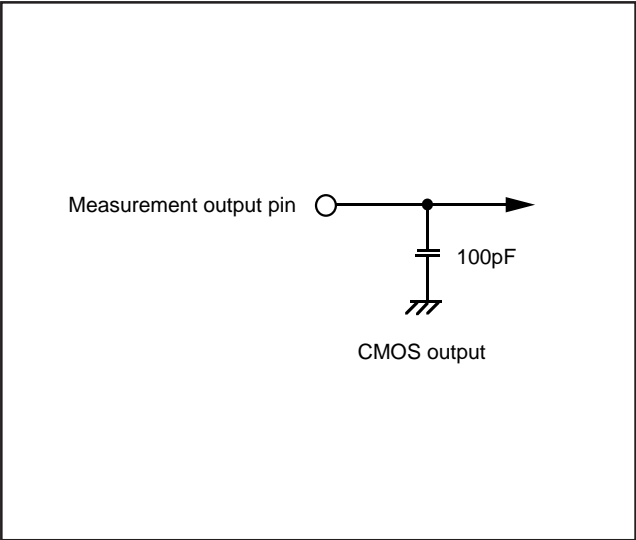


Fig. 44 Circuit for measuring output switching characteristics

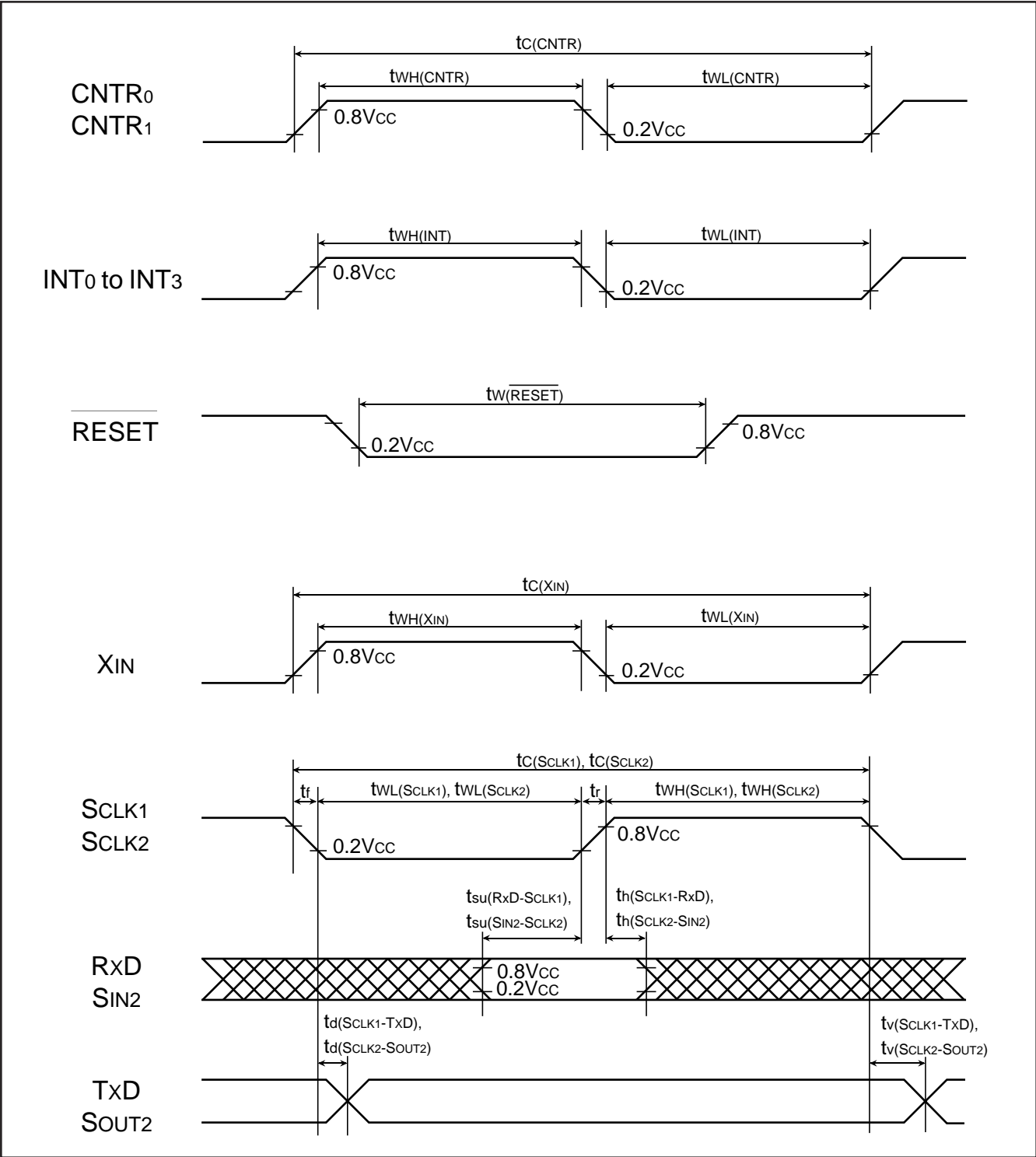


Fig. 45 Timing diagram

PACKAGE OUTLINE

42P4B

Plastic 42pin 600mil SDIP

EIAJ Package Code SDIP42-P-600-1.78	JEDEC Code -	Weight(g) 4.1	Lead Material Alloy 42/Cu Alloy
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Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	-	-	5.5
A1	0.51	-	-
A2	-	3.8	-
b	0.35	0.45	0.55
b1	0.9	1.0	1.3
b2	0.63	0.73	1.03
c	0.22	0.27	0.34
D	36.5	36.7	36.9
E	12.85	13.0	13.15
e	-	1.778	-
e1	-	15.24	-
L	3.0	-	-
θ	0°	-	15°

42P2R-A/E

Plastic 42pin 450mil SSOP

EIAJ Package Code SSOP42-P-450-0.80	JEDEC Code -	Weight(g) 0.63	Lead Material Alloy 42
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Recommended Mount Pad

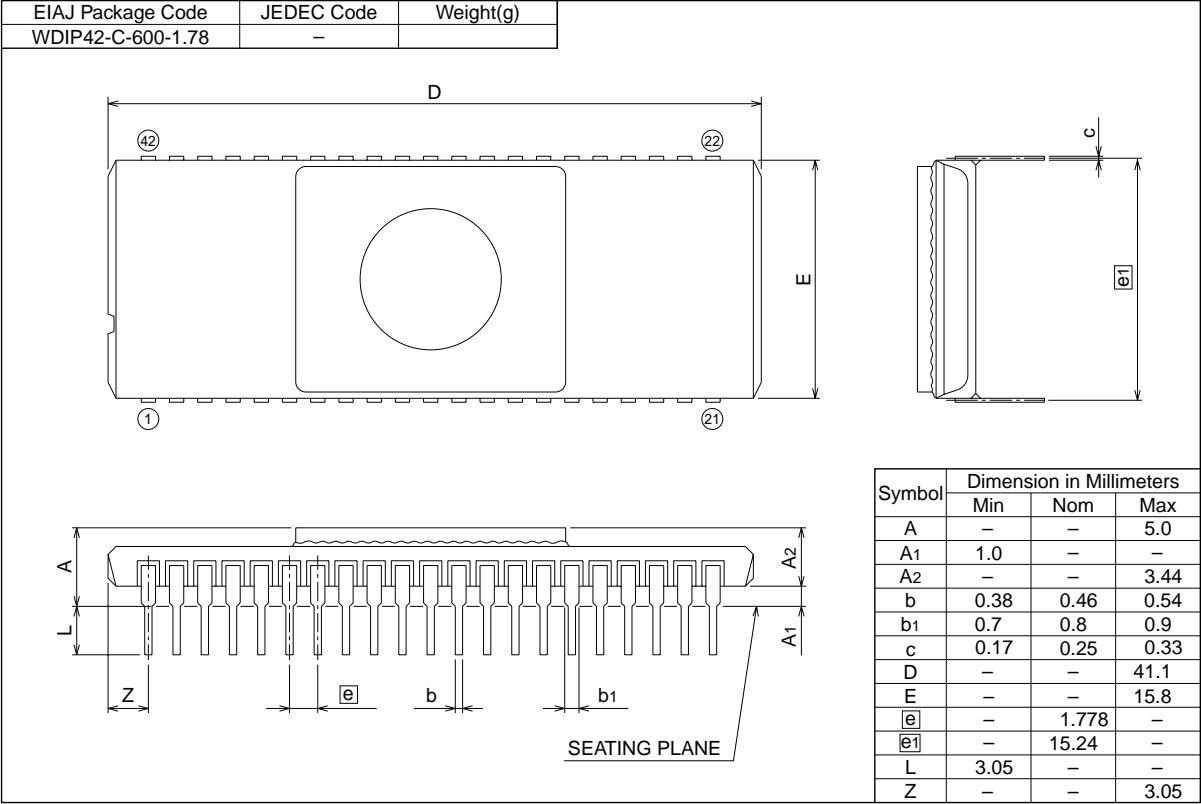
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	-	-	2.4
A1	0.05	-	-
A2	-	2.0	-
b	0.25	0.3	0.4
c	0.13	0.15	0.2
D	17.3	17.5	17.7
E	8.2	8.4	8.6
e	-	0.8	-
HE	11.63	11.93	12.23
L	0.3	0.5	0.7
L1	-	1.765	-
Z	-	0.75	-
Z1	-	-	0.9
y	-	-	0.15
θ	0°	-	10°
b2	-	0.5	-
e1	-	11.43	-
l2	1.27	-	-

3850 Group (Spec. H)

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

42S1B-A

Metal seal 42pin 600mil DIP





MITSUBISHI ELECTRIC CORPORATION

HEAD OFFICE: 2-2-3, MARUNOUCHI, CHIYODA-KU, TOKYO 100-8310, JAPAN

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REVISION DESCRIPTION LIST

3850 GROUP (SPEC. H) DATA SHEET

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1.0	First Edition	000309
1.1	Font errors are revised.	000322