Am2130/Am2140

1024x8 Dual-Port Static Random-Access Memories

DISTINCTIVE CHARACTERISTICS

- True dual port operation
- Access time as fast as 55 ns
- Master device (Am2130) has on-chip arbitration
- Expandable data bus width in multiples of 8 bits using one master (Am2130) and required number of slave devices (Am2140)
- Automatic power-down feature
- All inputs and outputs are TTL-compatible
- 48-pin DIP or 52-pin PLCC
- Single +5-volt power supply
- Advanced N-MOS technology

GENERAL DESCRIPTION

The Am2130 and the Am2140 are members of the 1K x 8 dual-port static RAM family. The Am2130 is designated as the master and the Am2140 as the slave device. The master provides the necessary control signal to the slave devices to facilitate implementing a wider data bus in a system. The master/slave concept allows expansion with minimal external logic.

Both devices have two independent ports called Left and Right port. Each port consists of an 8-bit bidirectional data bus and a 10-bit address input bus and necessary control signals.

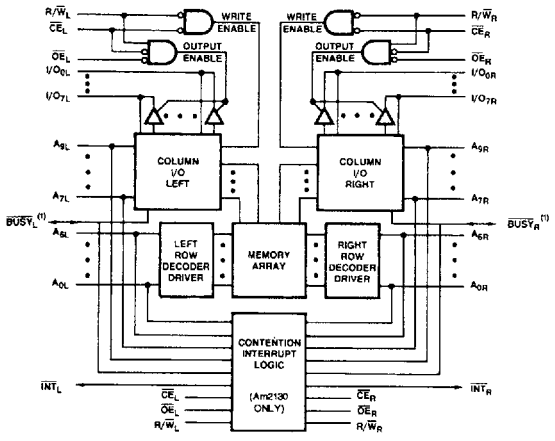
The Am2130 has an on-board arbiter to resolve contention between the left and right ports. When contention between ports occurs, one port is given priority while the other port receives a busy indication.

The Am2130 also contains on-chip facilities for supporting semaphores. Addresses $(3FE)_H$ and $(3FF)_H$ serve as interrupt generators. If any data is written at the address $(3FF)_H$ from the left port, an interrupt signal becomes active for the right port. The interrupt signal is deactivated by reading from the right port at the same address. The address $(3FE)_H$ is used in a similar fashion by the right port to activate the interrupt signal for the left port.

The Am2130/Am2140 also have two chip enable signals corresponding to the left and right ports. Before any transaction on a port takes place, the corresponding chip enable input must be activated. If a chip enable signal is not active, the circuitry corresponding to its side automatically powers down and enters standby mode.

The Am2130/Am2140 are packaged in 48-pin DIPs or 52-pin plastic leaded chip carrier. All inputs and outputs are TTL-compatible and the devices operate from a single +5-volt power supply.

BLOCK DIAGRAM

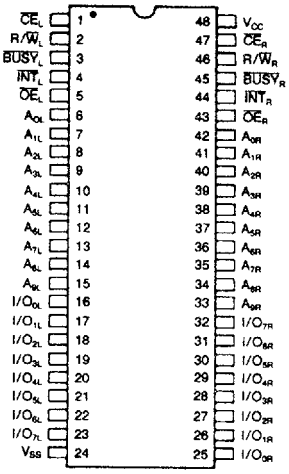


BD005085

Notes: 1. Am2130 (Master): BUSY is open-drain output and requires pull-up resistor.
Am2140 (Slave): BUSY is an input.

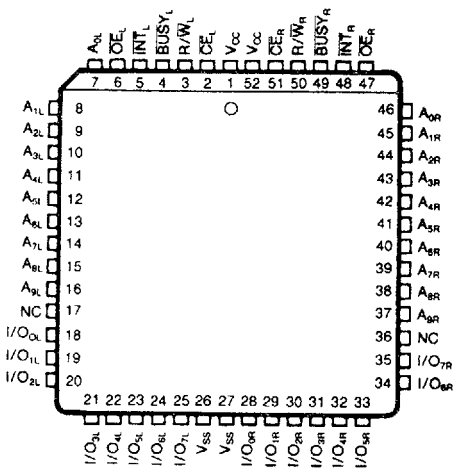
CONNECTION DIAGRAMS
Top View

DIP



CD005813

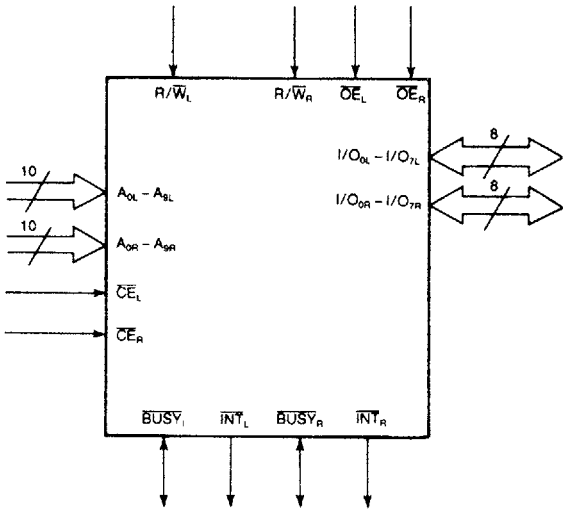
PLCC



CD009600

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



LS002232

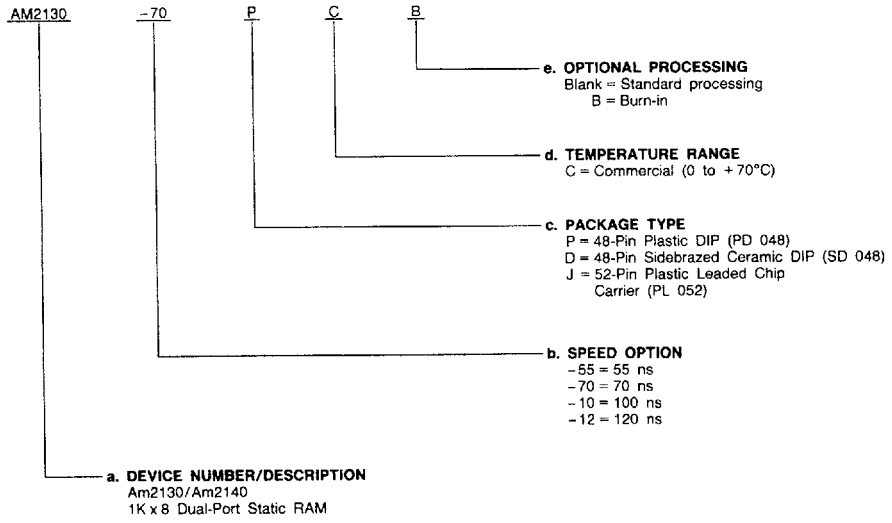
V_{CC} = +5-V Power Supply
V_{SS} = Ground

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ORDERING INFORMATION

Standard Products

AMD products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM2130-55	PC, PCB, DC, DCB, JC, JCB
AM2130-70	
AM2130-10	
AM2130-12	
AM2140-55	
AM2140-70	
AM2140-10	
AM2140-12	

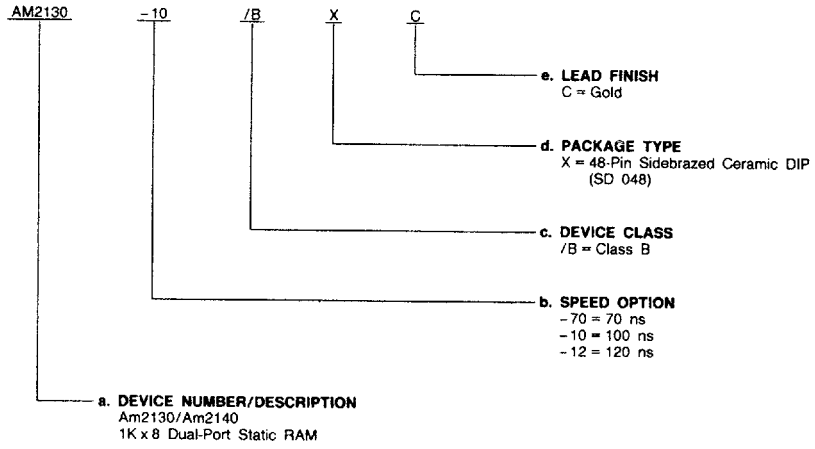
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult MSIS sales department to confirm availability of specific valid combinations, and to obtain additional data on MSIS's standard military grade products.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
AM2130-70	/BXC
AM2130-10	
AM2130-12	
AM2140-70	
AM2140-10	
AM2140-12	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult MSIS sales department to confirm availability of specific valid combinations, and to obtain additional data on MSIS's standard military grade products.

Group A Tests

Group A Tests consist of subgroups 1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

Am2130

$A_{0L} - A_{9L}$ Left Port Address (Inputs)
These 10 inputs constitute the memory address for the left port. A_0 is the least significant bit position and A_9 is the most significant position. A HIGH level on any of these inputs represents a logic 1 at that position and LOW represents a logic 0. The sequence of events and related timing for the address inputs during read and write operations will be discussed in later sections of this data sheet.

If a write operation is performed using $(3FF)_H$, an interrupt signal is activated for the right port (see $\overline{INT}_R$ pin description).

If a read operation is performed using $(3FE)_H$, the $\overline{INT}_L$ signal will be deactivated (see $\overline{INT}_L$ description).

$A_{0R} - A_{9R}$ Right Port Address (Inputs)
These 10 inputs constitute the memory address for the right port. A_0 is the least significant bit position and A_9 is the most significant position. A HIGH level on any of these inputs represents a logic 1 at that position and LOW represents a logic 0. The sequence of events and related timing for the address inputs during read and write operations will be discussed in later sections of this data sheet.

If a write operation is performed using $(3FE)_H$, an interrupt signal is activated for the left port (see $\overline{INT}_L$ pin description).

If a read operation is performed using $(3FF)_H$, the $\overline{INT}_R$ signal will be deactivated (see $\overline{INT}_R$ description).

$\overline{BUSY}_L$ Left Port Busy Flag (Output; Open Drain)
This open-drain output requires a pull-up resistor for proper operation. A LOW on this output indicates that the on-chip arbitration logic detected a contention between the left and right ports and the right port is given priority. All left port signals must be held stable until a HIGH on this output is indicated.

The $\overline{BUSY}_L$ signal generation is a logical function of the left and right port address inputs and the $\overline{CE}_L$ and $\overline{CE}_R$ inputs. The transient behavior of the $\overline{BUSY}_L$ output is not assured while the inputs are changing.

$\overline{BUSY}_R$ Right Port Busy Flag (Output; Open Drain)
This open-drain output requires a pull-up resistor for proper operation. A LOW on this output indicates that the on-chip arbitration logic detected a contention between the left and right ports and the left port is given priority. All right port signals must be held stable until a HIGH on this output is indicated.

The $\overline{BUSY}_R$ signal generation is a logical function of the left and right port address inputs and the $\overline{CE}_L$ and $\overline{CE}_R$ inputs. The transient behavior of the $\overline{BUSY}_R$ output is not assured while the inputs are changing.

$\overline{CE}_L$ Left Port Chip Enable (Input)
This input must be LOW before any transaction from the left port and remain LOW for the duration of the transaction. When this input goes HIGH, left port logic circuits enter standby power mode and remain in this mode as long as this input remains HIGH. It should be noted that powering down the left port to standby mode does not affect the $\overline{INT}_L$ or $\overline{INT}_R$ outputs. This input going HIGH also initializes the internal arbitration latch. It is recommended that $\overline{CE}_L$ go HIGH after completing a transaction (see discussion on arbitration).

$\overline{CE}_R$ Right Port Chip Enable (Input)
Operation of this input is identical to $\overline{CE}_L$ except that the $\overline{CE}_R$ input controls the right port.

GND (V_{SS}) Ground

$I/O_{0L} - I/O_{7L}$ Left Port Input/Output Bus (Input/Output; Three State)
These eight lines constitute the data bus for the left port. If a read operation is performed using the left port, data from the location addressed by the left port address will be available on these lines. Similarly, to perform a write operation using the left port, data to be written into the memory must be presented on these lines. The drivers on the chip to drive these lines are enabled only when the $\overline{CE}_L$ is LOW, $\overline{OE}_L$ is LOW and $R/\overline{W}_L$ is HIGH.

$I/O_{0R} - I/O_{7R}$ Right Port Input/Output Bus (Input/Output; Three State)
These eight lines constitute the data bus for the right port. If a read operation is performed using the right port, data from the location addressed by the right port address will be available on these lines. Similarly, to perform a write operation using the right port, data to be written into the memory must be presented on these lines. The drivers on the chip to drive these lines are enabled only when the $\overline{CE}_R$ is LOW, $\overline{OE}_R$ is LOW and $R/\overline{W}_R$ is HIGH.

$\overline{INT}_L$ Left Port Interrupt Flag (Output; Open Drain)
This open-drain output requires a pull-up resistor for proper operation. If the right port performs any write operation using address $(3FE)_H$, then this output goes LOW. It will remain LOW until the left port successfully completes any read operation using the address $(3FE)_H$. It should be noted that powering down the ports has no effect on this output.

$\overline{INT}_R$ Right Port Interrupt Flag (Output; Open Drain)
This open-drain output requires a pull-up resistor for proper operation. If the left port performs any write operation using address $(3FF)_H$, then this output goes LOW. It will remain LOW until the right port successfully completes any read operation using the address $(3FF)_H$. It should be noted that powering down the ports has no effect on this output.

$\overline{OE}_L$ Output Enable Left I/O Port (Input)
When this input is HIGH, the left port I/O bus lines are in high impedance state. If this input is LOW and $\overline{CE}_L$ is LOW and $R/\overline{W}_L$ is HIGH, the left port drivers are enabled and data from the location addressed by the $A_{0L} - A_{9L}$ inputs will be available on the I/O bus lines of the left port. It may be of interest to note that the $\overline{OE}_L$ input has no effect on the $\overline{BUSY}_L$ or $\overline{BUSY}_R$ or $\overline{INT}_L$ or $\overline{INT}_R$ signals. Even though the left port I/O port drivers are disabled when the $R/\overline{W}_L$ input goes LOW (write operation), it is recommended that the $\overline{OE}_L$ signal be kept HIGH during write operations to the left port.

$\overline{OE}_R$ Output Enable Right I/O Port (Input)
When this input is HIGH, the right port I/O bus lines are in high impedance state. If this input is LOW and $\overline{CE}_R$ is LOW and $R/\overline{W}_R$ is HIGH, the right port drivers are enabled and data from the location addressed by the $A_{0R} - A_{9R}$ inputs will be available on the I/O bus lines of the right port. It may be of interest to note that the $\overline{OE}_R$ input has no effect on the $\overline{BUSY}_L$ or $\overline{BUSY}_R$ or $\overline{INT}_L$ or $\overline{INT}_R$ signals. Even though the left port I/O port drivers are disabled when the $R/\overline{W}_R$ input goes LOW (write operation), it is recommended that the $\overline{OE}_R$ signal be kept HIGH during write operations to the right port.

$R/\overline{W}_L$ Left Port Read/$\overline{\text{Write}}$ Enable (Input)
This input is used to specify the left port function to be performed. HIGH indicates a read and LOW indicates a write function.

When the $\overline{CE}_L$ is LOW and the $\overline{OE}_L$ is LOW and the $R/\overline{W}_L$ is HIGH, data from the location addressed by the $A_{0L} - A_{9L}$ will be available on the $I/O_{0L} - I/O_{7L}$ lines. As mentioned earlier, reading from the left port at the location $(3FE)_H$ disables the $\overline{INT}_L$ output.

When the $\overline{CE}_L$ is LOW and the $R/\overline{W}_L$ goes LOW, data present on the $I/O_{0L} - I/O_{7L}$ lines will be written into the location addressed by the $A_{0L} - A_{9L}$ inputs. It should be noted that the write operation is not affected by the $\overline{OE}_L$ input. However, it is recommended that the $\overline{OE}_L$ input be held HIGH during a write operation. As mentioned earlier, performing a write operation from the left port at the address $(3FF)_H$ causes the $\overline{INT}_R$ output to go LOW.

It should be noted that even though $R/\overline{W}_L$ is LOW, writing is internally inhibited if the right port is given priority by the arbiter. Discussion on arbitration can be found in a later section.

$R/\overline{W}_R$ Right Port Read/$\overline{\text{Write}}$ Enable (Input)
This input is used to specify the right port function to be performed. HIGH indicates a read and LOW indicates a write function.

When the $\overline{CE}_R$ is LOW and the $\overline{OE}_R$ is LOW and the $R/\overline{W}_R$ is HIGH, data from the location addressed by the $A_{0R} - A_{9R}$ will be available on the $I/O_{0R} - I/O_{7R}$ lines. As mentioned earlier, reading from the right port at the location $(3FF)_H$ disables the $\overline{INT}_R$ output.

When the $\overline{CE}_R$ is LOW and the $R/\overline{W}_R$ goes LOW, data present on the $I/O_{0R} - I/O_{7R}$ lines will be written into the location addressed by the $A_{0R} - A_{9R}$ inputs. It should be noted that the write operation is not affected by the $\overline{OE}_R$ input. However, it is recommended that the $\overline{OE}_R$ input be held HIGH during a write operation. As mentioned earlier, performing a write operation from the left port at the address $(3FE)_H$ causes the $\overline{INT}_L$ output to go LOW.

It should be noted that even though $R/\overline{W}_R$ is LOW, writing is internally inhibited if the left port is given priority by the arbiter. Discussion on arbitration can be found in a later section.

V_{CC} +5-Volt Power Supply

Am2140

The Am2140 is functionally very similar to the Am2130. The Am2140 differs from the Am2130 in two signals only — $\overline{BUSY}_L$ and $\overline{BUSY}_R$. In the case of the Am2140 they are used as inputs and play a significant role in expanding the word width.

$\overline{BUSY}_L$ Left Port $\overline{\text{Busy}}$ Flag (Input)
If this input is LOW, a write enable signal to the left side of the memory array is internally disabled. In expanded systems where an Am2130 is used as the master, this input is connected to the $\overline{BUSY}_L$ output of the Am2130.

$\overline{BUSY}_R$ Right Port $\overline{\text{Busy}}$ Flag (Output; Open Drain)
If this input is LOW, a write enable signal to the right side of the memory array is internally disabled. In expanded systems where an Am2130 is used as the master, this input is connected to the $\overline{BUSY}_R$ output of the Am2130.

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FUNCTIONAL DESCRIPTION

As shown in the block diagram, the Am2130/Am2140 is a true 1K x 8 dual-port RAM. It consists of a memory array with two sets of address decoders and associated logic. This arrangement allows the accessing of every word in the memory array from two independent sources. We call these sources left side and right side for convenience. Data accessed by the left-side address inputs appears on the left-side data lines of the array and is connected to the left-side I/O pins through the associated three-state buffers. The enable control signal for these buffers is generated using the R/$\overline{W}_L$, $\overline{CE}_L$ and $\overline{OE}_L$ inputs. If the I/O buffers are disabled on the chip, the I/O pins can be used as inputs. Data to be written from the left port is presented on these inputs. Writing into the memory array from the left side is controlled by the left write enable signal generated on the chip using the R/$\overline{W}_L$ and $\overline{CE}_L$ inputs. An identical arrangement exists for the right side also. In addition, there is on-chip arbitration logic to give priority to one port over the other in case of a contention, and interrupt flag logic.

Contention Arbitration

Two independent access facilities are provided in a dual-port memory to eliminate physical interference between signals. However, there are two significant possibilities of "logical" interference which are not tolerable: when one port is reading from a location while the other port is writing into the same location at the same time. In this case, data received by the reading port may not be predictable. Similarly, consider the situation when both ports write information into the same location simultaneously. The resultant data that finally ends up in the memory location may not be valid. These two situations are commonly called contention. The Am2130 has on-chip logic to detect contention and give priority to one port over the other. In a true dual-port RAM, simultaneous reading from both ports at the same address does not corrupt the data. Hence, it can be construed that no contention occurs. However, for the sake of simplicity and compatibility with the industry standard practices, the Am2130 arbitration is based purely on addresses. Hence, in the case of a simultaneous read from both ports at the same address, the arbitration logic will sense contention and give priority to one of the ports. The other port will receive a busy indication.

Figure 1 is a conceptual logic diagram of contention arbitration logic. It consists of two equality comparators. The left comparator compares the left port address inputs to the delayed version of the right port address. Similarly, the right comparator compares the right-port address to the delayed version of the left port address. The output of the comparators is connected to a latch formed by two cross-coupled NAND gates as shown in Figure 1. The chip enable signals, $\overline{CE}_L$ and $\overline{CE}_R$, are also inputs to this latch as shown. The $\overline{BUSY}_L$ and $\overline{BUSY}_R$ outputs are generated by gating the latch output with the proper chip enable signal as shown. Also note that the latch outputs are used internally for left and right write inhibit signals. For example, if the right side write inhibit signal in Figure 1 is LOW, writing into the memory does not occur even if the R/$\overline{W}_R$ input of the Am2130 is LOW.

The operation of the arbitration circuit can now be explained. Assume that the left port address had been stable and $\overline{CE}_L$ is LOW. Both Q and Q' outputs of the latch will be HIGH because the output of both comparators is LOW (addresses are different). So the $\overline{BUSY}$ output on both sides is HIGH. Now assume that the right address changes and becomes equal to the left address. The right address comparator output goes HIGH and the Q' output of the latch goes LOW. Eventually the output of the left comparator also goes HIGH, but because of the cross coupling of the Q' into the gate generating the Q output, Q output remains HIGH. As soon as the $\overline{CE}_R$ input goes LOW, $\overline{BUSY}_R$ becomes LOW. Thus, the arbitrator gave priority to the left port by indicating a busy signal to the right port. Thus in this example, the left port is the winner and the right port is the loser in the contention for the memory. Sooner or later the left port will finish its transaction at the contended location and change the address or its chip enable will go HIGH. Thus when the contention is over the Q output of the latch will become HIGH and $\overline{BUSY}_R$ will go HIGH. A similar reasoning can be used to understand the operation of the left side. It should be clear then, in cases of contention, the arbiter will decide one port as the winner and the losing port must wait for the winner to complete the use of the memory. The winning port must indicate to the arbiter that it has completed its operation either by changing the address or making its chip enable input HIGH. Without such an indication, the arbiter will not remove the busy indication to the losing port.

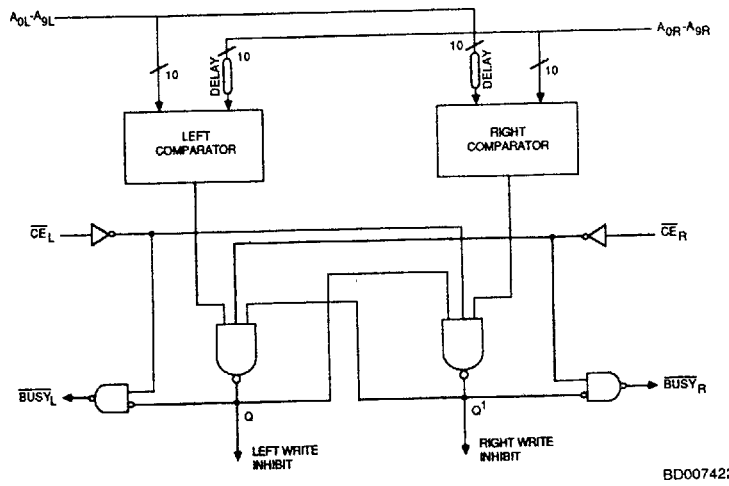


Figure 1. Conceptual Arbitration Logic

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Read/Write Operations

Performing read/write operations when there is no contention is relatively straightforward. The sequence of events for a read is listed below. The timing relationships between various signals can be found in later sections of this data sheet.

1. Establish HIGH on the R/$\overline{W}$ and LOW on the $\overline{CE}$ input of the desired port.
2. Establish the desired address on the desired port address lines.
3. Make the $\overline{OE}$ input of the desired port LOW.
4. The I/O lines of the selected port will contain the data after the access time has elapsed.
5. Make the output enable and chip enable inputs HIGH to complete the read operation.

Performing write operations when there is no contention is equally straightforward. The sequence of events for a write is listed below. The timing relationships between various signals can be found in later sections of this data sheet.

1. Establish LOW on the $\overline{CE}$ input of the desired port.
2. Establish the desired address on the desired port address lines.
3. Establish the desired data on the I/O lines of the port.
4. Make the R/$\overline{W}$ input of the port LOW and bring it HIGH after the specified amount of time.
5. Make the $\overline{CE}$ input HIGH to complete the operation.

When a read or write operation is initiated by a port and contention from the other port occurs, the implications are very simple. The losing port will see its $\overline{BUSY}$ line go LOW. The port must wait until a HIGH is indicated on the $\overline{BUSY}$ line. Thus in this case of contention, the operation did not really start when the port initiated it. Instead, the operation actually started when the $\overline{BUSY}$ line went HIGH. See the timing diagram for details.

Interrupts

Each port has an associated output called interrupt. The interrupt outputs are activated and deactivated by the on-chip logic when read and write operations occur with a particular address location. For example, if a write operation is performed by the left port with address $(3FF)_H$, an on-chip latch is set. This latch drives the $\overline{INT}_R$ output LOW. The latch is cleared only when a read operation from the right port using the address $(3FF)_H$ takes place. Similarly, if a write operation from the right port using the address $(3FE)_H$ occurs, a latch is set to drive the $\overline{INT}_L$ output LOW. The $\overline{INT}_L$ will go HIGH (latch is cleared) only after a read operation from the left port using the address $(3FE)_H$ occurs. As mentioned before, powering down a port to standby mode does not affect these outputs.

Depth Expansion Using Multiple Am2130s

The Am2130 has an intrinsic storage capacity of 1K bytes. However, it is simple to expand the storage capacity by using multiple devices. Figure 2 is a conceptual diagram of a 2K byte dual port memory system using two Am2130 devices. The principle behind such expansion is obvious: all that needs to be done is to decode the most significant system address to generate the individual $\overline{CE}$ inputs for the Am2130s. For example in Figure 2, A_{10} is the most significant address bit. When this signal is LOW and $\overline{CE}$ input is LOW, the chip enable input of the upper Am2130 goes LOW. Thus, the first 1K locations are selected for transactions. On the other hand, if A_{10} is HIGH and $\overline{CE}$ is LOW, the chip enable input of the lower Am2130 goes LOW selecting the second 1K locations. As depicted in the figure, the address inputs of both Am2130 devices are bussed together. Similarly, the I/O signals are also bussed to create the overall data bus. Also note that the other control signals are connected between the two devices.

In this example, we have not used the interrupt outputs. However, it should be noted that depth expansion using multiple devices does not change the operation of the interrupt outputs. The interrupt output of each device behaves as described before. Hence, the user must decide which interrupt output from which device will be used in his system.

Width Expansion

The intrinsic width of the data word of the Am2130 is eight bits. However, it is possible to realize wider data words (multiples of 8) by using multiple devices. The instinctive solution of taking the required number of the devices and assigning the data bits to individual devices is potentially unreliable. As we know, the Am2130 has arbitration logic on the chip, and hence is called the master. When several of these masters are present, device-to-device variations and other factors may cause one device to give priority to one port, while another device gives priority to the other port. In essence both ports are busy! This is an undesirable situation and should not be allowed in operation. The most elegant way to avoid the situation is to allow only one device to arbitrate the contention. It is recommended that when expanding the width of the data words, the Am2130 be used as the master and a number of Am2140s be used as slave devices. The Am2140 does not have the arbitration capability; instead it accepts the $\overline{BUSY}$ outputs generated by the Am2130 as inputs.

Figure 3 is a conceptual diagram of a 16-bit system using one Am2130 and one Am2140. As can be seen, using master/slave devices avoids external logic for expansion. For the sake of completeness of this discussion, it may be noted that it is indeed possible to expand the width using Am2130s only. However, external logic must be provided to prevent every device of the system from arbitrating. We want only one device to be the arbitrator. As explained in Figure 1, arbitration can be defeated by suitable control of the $\overline{CE}$ input of the Am2130.

Figure 4 shows a conceptual diagram of a 16-bit system using two Am2130s. Device 1 in this figure behaves as the master. The external logic shown in the figure ensures that the $\overline{CE}$ input of Device 2 is HIGH if the corresponding $\overline{BUSY}$ output of Device 1 is LOW. Thus the arbitration logic of Device 2 is prevented from taking part in resolving contention.

Simultaneous Width and Depth Expansion

By combining the depth and width expansion schemes discussed, it is possible to build systems with greater depth (multiples of 1K) and wider words (multiples of 8). Figure 5 shows a conceptual diagram of a 2K x 16 system. The operation of this scheme is understood by suitably combining the explanation of Figure 2 and Figure 3 and hence is not repeated here.

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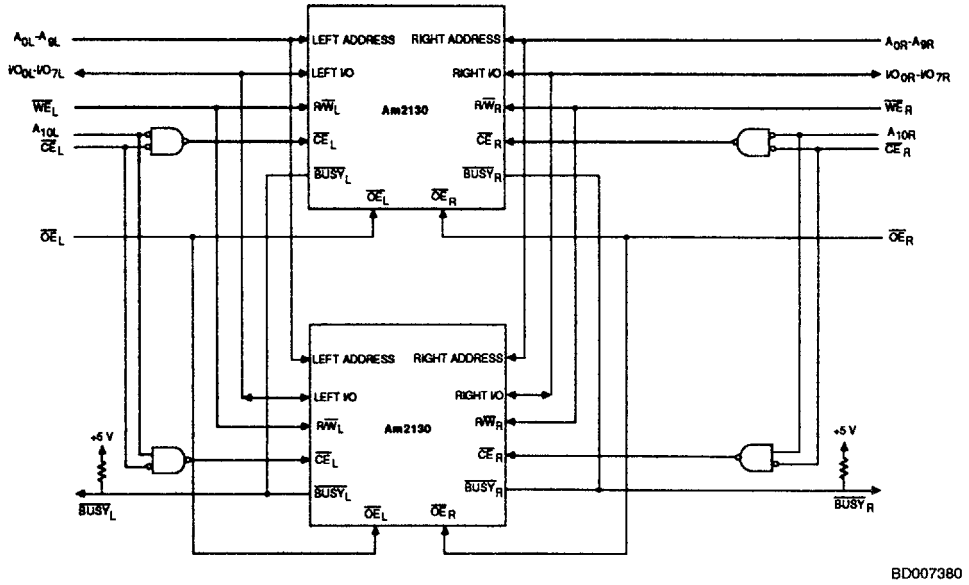


Figure 2. Conceptual Depth Expansion

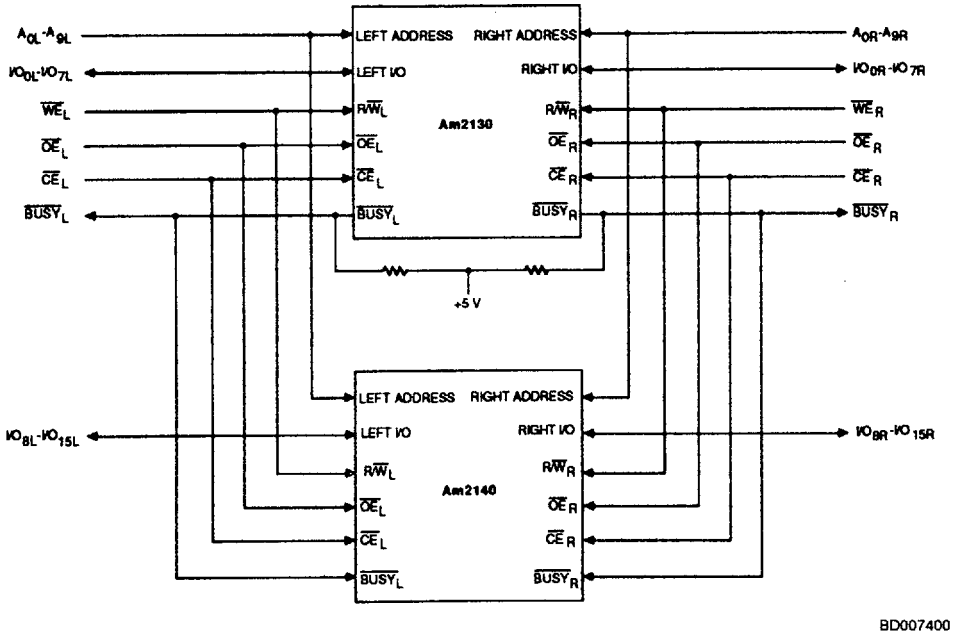


Figure 3. Width Expansion with Master/Slave

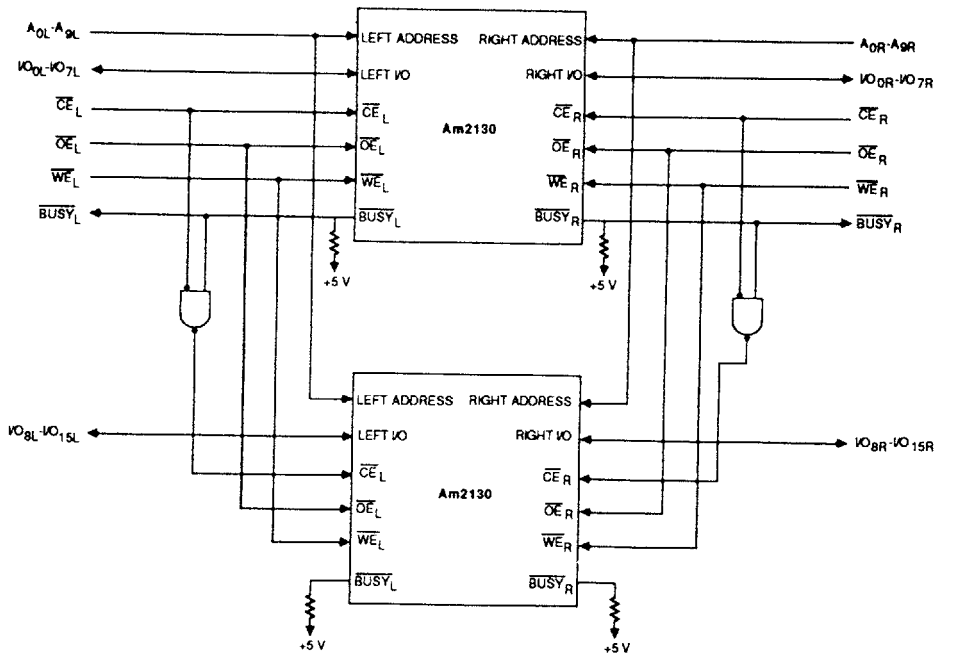


Figure 4. Width Expansion with Master

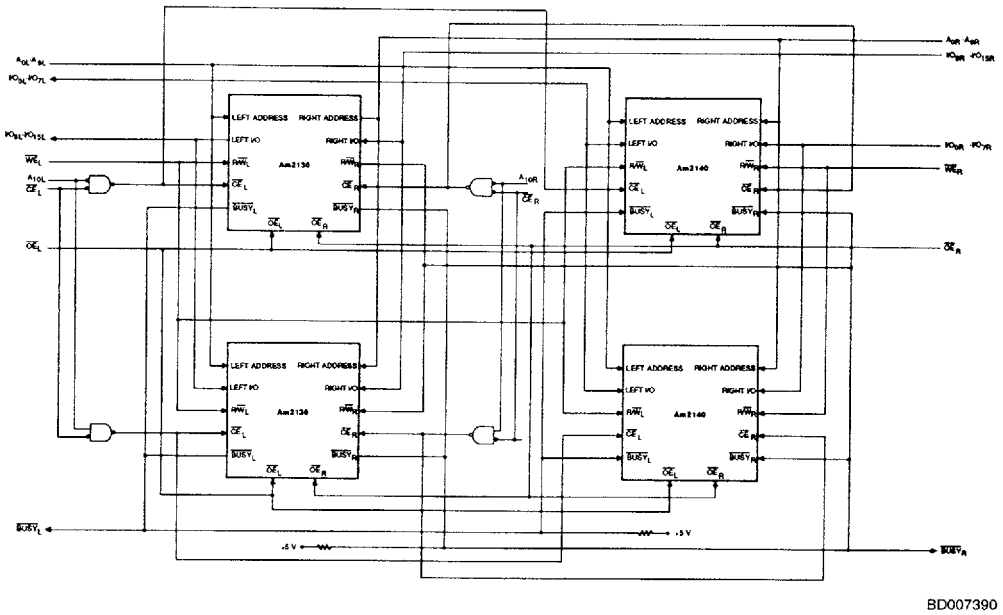


Figure 5. Conceptual Diagram of a 2K x 16 System Using Master/Slave

TABLE 1. NON-CONTENTION READ/WRITE CONTROL

	Left Port Inputs			Right Port Inputs				Left Flags		Right Flags		
$R/\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	$A_{0L}-A_{9L}$	$R/\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	$A_{0R}-A_{9R}$	$\overline{BUSY}_L$	$\overline{INT}_L$	$\overline{BUSY}_R$	$\overline{INT}_R$	Function
X	H	X	X	X	X	X	X	H	X	H	X	Left port in power-down mode
X	X	X	X	X	H	X	X	H	X	H	X	Right port in power-down mode
L	L	X	X	X	X	X	X	H	X	X	X	Data on left port written to memory location $A_{0L}-A_{9L}$
H	L	L	X	X	X	X	X	H	X	X	X	Data in memory location $A_{0L}-A_{9L}$ output on left port
X	X	X	X	L	L	X	X	X	X	H	X	Data on right port written to memory location $A_{0R}-A_{9R}$
X	X	X	X	H	L	L	X	X	X	H	X	Data in memory location $A_{0R}-A_{9R}$ output on right port
L	L	X	3FF	X	X	X	X	H	X	H	L	Left port flags right port to read memory location 3FF
X	X	X	X	L	L	X	3FE	H	L	H	X	Right port flags left port to read memory location 3FE

TABLE 2. BUSY ARBITRATION OF ADDRESS CONTENTION

Left Port				Right Port				Flags (Note 1)		
$R/\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	$A_{0L}-A_{9L}$	$R/\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	$A_{0R}-A_{9R}$	$\overline{BUSY}_L$	$\overline{BUSY}_R$	Function
X	L (LIV)	X	Match	X	L	X	Match	L	H	Right-Port operation only is permitted. (Note 3)
X	L	X	Match (LIV)	X	L	X	Match	L	H	
X	L	X	Match	X	L (LIV)	X	Match	H	L	Left-port operation only is permitted. (Note 4)
X	L	X	Match	X	L	X	Match (LIV)	H	L	

TABLE 3. INTERRUPT FLAG

Left Port					Right Port					
$R/\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	$A_{0L}-A_{9L}$	$\overline{INT}_L$	$R/\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	$A_{0R}-A_{9R}$	$\overline{INT}_R$	Function
L	L	X	3FF	X	X	X	X	X_1	L	Set $\overline{INT}_R$
X	X	X	X_1	X	H	L	L	3FF	H	Reset $\overline{INT}_R$
X	X	X	X_1	L	L	L	X	3FE	X	Set $\overline{INT}_L$
H	L	L	3FE	H	X	X	X	X_1	X	Reset $\overline{INT}_L$

Key: H = HIGH
L = LOW
LIV = Last Input Valid; meets t_{APS} spec (Note 2)
X = Don't Care
X_1 = No Match, or
Same port deselected, or
Opposite port has priority

Notes: 1. INT Flags = X
2. If LIV violates t_{APS} spec then one of the two ports receives priority, and the remaining port's $\overline{BUSY}$ Flag goes LOW. However, there is an extremely rare metastable event which can occur when the arbitration circuitry cannot determine which port was "first" at the matching address. On this rare occurrence, both ports may momentarily receive $\overline{BUSY}$ = LOW signals until the metastable state is resolved (usually within a few nanoseconds). Thereafter, one port's $\overline{BUSY}$ remains LOW while the other completes its operation and resumes normal operation.
3. A Left-Port Read operation is also permitted if the Right-Port is also reading.
4. A Right-Port Read operation is also permitted if the Left-Port is also reading.

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ABSOLUTE MAXIMUM RATINGS (Note 15)

Storage Temperature ..... −65 to +150°C
Ambient Temperature
with Power Applied ..... −55 to +125°C
Supply Voltage
with Respect to Ground ..... −0.5 to +7.0 V
All Signal Voltages ..... −3.5 to +7.0 V
Power Dissipation ..... 1.2 W

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES (Note 8)

Commercial (C) Devices
Temperature (T_A) ..... 0 to +70°C
Supply Voltage (V_{CC}) ..... +4.5 to +5.5 V

Military (M) Devices
Temperature (T_A) ..... −55 to +125°C
Supply Voltage (V_{CC}) ..... +4.5 to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions		Am2130/Am2140 Min.	Am2130/Am2140 Max.	Units
I_{LI}	Input Load Current (All Input Pins)	V_{CC} = Max., V_{IN} = GND to V_{CC}			10	µA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{CC} = Max., V_{OUT} = GND to V_{CC}			10	µA
I_{CC}	Power Supply Current (Both Ports Active)	V_{CC} = Max., $\overline{CE}$ = V_{IL} Outputs Open	C Devices		170	mA
			M Devices		185	
I_{SB1}	Standby Current (Both Ports Standby)	V_{CC} = Min. to Max., $\overline{CE_L}$ and $\overline{CE_R}$ = V_{IH}	C Devices		30	mA
			M Devices		40	
I_{SB2}	Standby Current (One Port Standby)	V_{CC} = Max., $\overline{CE_L}$ = V_{IL} and $\overline{CE_R}$ = V_{IH} or $\overline{CE_L}$ = V_{IH} and $\overline{CE_R}$ = V_{IL}	C Devices		110	mA
			M Devices		125	
V_{IL}	Input LOW Voltage			−0.5	0.8	V
V_{IH}	Input HIGH Voltage			2.2	6.0	V
V_{OL1}	Output LOW Voltage (I/O_0 − I/O_7)	I_{OL} = 3.2 mA			0.4	V
V_{OL2}	Open-Drain Output LOW Voltage ($\overline{BUSY}$ (Note 14), $\overline{INT}$)	I_{OL} = 4 mA (Note 7)			0.5	V
V_{OH}	Output HIGH Voltage	I_{OH} = −1.0 mA (Note 7)		2.4		V

CAPACITANCE (Note 9)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Units
C_{OUT}	Output Capacitance			10	pF
C_{IN}	Input Capacitance			10	

Notes: See notes following Switching Waveforms.

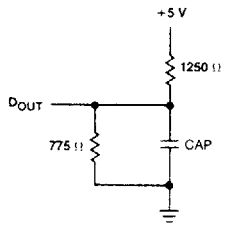
SWITCHING CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 7, 8, 9, 10, 11 are tested unless otherwise noted)

No.	Parameter Symbol	Parameter Description	Test Conditions	Am2130/Am2140								Units
				-55		-70		-10		-12		
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE (Note 10)												
1	t_{RC}	Read Cycle Time		55		70		100		120		ns
2	t_{AA}	Address Access Time			55		70		100		120	ns
3	t_{ACE}	Chip Enable Access Time			55		70		100		120	ns
4	t_{AOE}	Output Enable Access Time			30		35		40		60	ns
5	t_{OH}	Output Hold from Address Change		5		5		5		5		ns
6	t_{LZ}	Output Low Z Time	(Notes 5 & 9)	5		5		5		5		ns
7	t_{HZ}	Output High Z Time	(Notes 5 & 9)	0	25	0	30	0	40	0	40	ns
8	t_{PU}	Chip Enable to Power Up Time	(Note 9)	0		0		0		0		ns
9	t_{PD}	Chip Disable to Power Down Time	(Note 9)			35	35		50		60	ns
WRITE CYCLE (Note 10)												
10	t_{WC}	Write Cycle Time		55		70		100		120		ns
11	t_{EW}	Chip Enable to End of Write		55		65		90		100		ns
12	t_{AW}	Address Valid to End of Write		50		65		90		100		ns
13	t_{AS}	Address Setup Time		0		0		0		0		ns
14	t_{WP}	Write Pulse Width		45		50		60		70		ns
15	t_{WR}	Write Recovery Time		0		0		0		0		ns
16	t_{DW}	Data Valid to End of Write		30		35		40		40		ns
17	t_{DH}	Data Hold Time		0		0		0		0		ns
18	t_{WZ}	Write Enabled to Output in High Z	(Notes 5 & 9)	0	25	0	30	0	40	0	50	ns
19	t_{OW}	Output Active from End of Write	(Notes 5 & 9)	0		0		0		0		ns
$\overline{BUSY}$ FLAG TIMING (Notes 7 & 14)												
20	t_{RC}	Read Cycle Time		55		70		100		120		ns
21	t_{WC}	Write Cycle Time		55		70		100		120		ns
22	t_{BW}	$\overline{BUSY}$ to Write	(Note 13)	-5		-5		-5		-5		ns
23	t_{WH}	Write Hold After $\overline{BUSY}$	(Note 13)	20		20		20		20		ns
24	t_{BAA}	$\overline{BUSY}$ Access Time to Address	(Note 9)		45		45		50		60	ns
25	t_{BDA}	$\overline{BUSY}$ Disable Time to Address	(Note 9)		40		45		50		60	ns
26	t_{BAC}	$\overline{BUSY}$ Access Time to Chip Enable or Chip Select	(Note 9)		40		45		50		60	ns
27	t_{BDC}	$\overline{BUSY}$ Disable Time to Chip E nable or Chip Select	(Note 9)		40		45		50		60	ns
28	t_{APS}	Arbitration Priority Setup Time		10		10		10		10		ns
INTERRUPT TIMING (Note 7)												
29	t_{WINS}	$\overline{WE}$ to Interrupt Set Time			30		30		35		45	ns
30	t_{EINS}	$\overline{CE}$ to Interrupt Set Time			50		55		60		70	ns
31	t_{INS}	Address to Interrupt Set Time			50		55		60		70	ns
32	t_{OINR}	Output Enable to Interrupt Reset Time			30		30		35		45	ns
33	t_{INR}	Address to Interrupt Reset Time			50		55		60		70	ns
34	t_{EINR}	Chip Enable to Interrupt Reset Time			50		55		60		70	ns

Notes: See notes following Switching Waveforms.

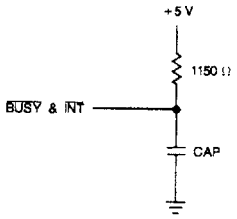
8077984 0000094 T49

SWITCHING TEST CIRCUITS



TC002201

Test Loads A and B



TC002222

Test Loads C and D

TEST OUTPUT LOADS	
Test Load	**CAP**
A	5 pF (Note 1)
B	100 pF
C	50 pF
D	5 pF (Note 1)

Notes: 1. Includes Scope and Jig Capacitance.

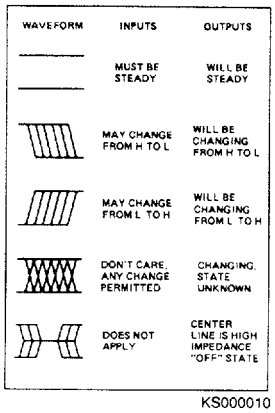
SWITCHING TEST WAVEFORM

AC Test Conditions	
Input Levels	GND to 3.0 V
Input Rise and Fall Times	5 ns
Input Timing Reference Levels	1.5 V
Output Reference Levels	1.5 V
Test Output Load	See Test Output Loads Table

4

SWITCHING WAVEFORMS

KEY TO SWITCHING WAVEFORMS

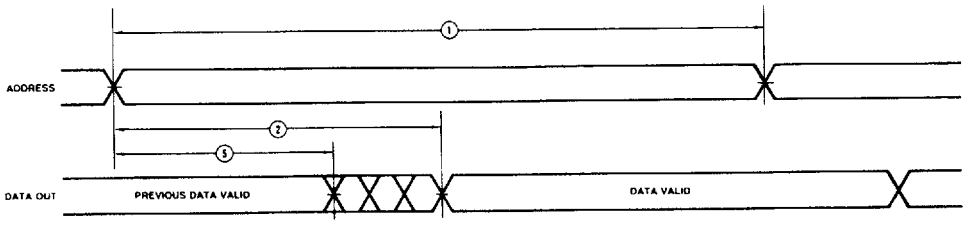


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8077984 0000095 985

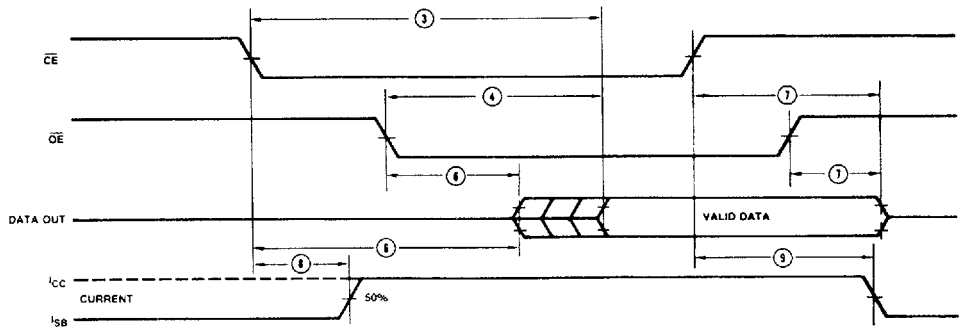
SWITCHING WAVEFORMS (Cont'd.)

READ CYCLE
(Either Side)



WF009391

Address Access
(Notes 1 & 2)

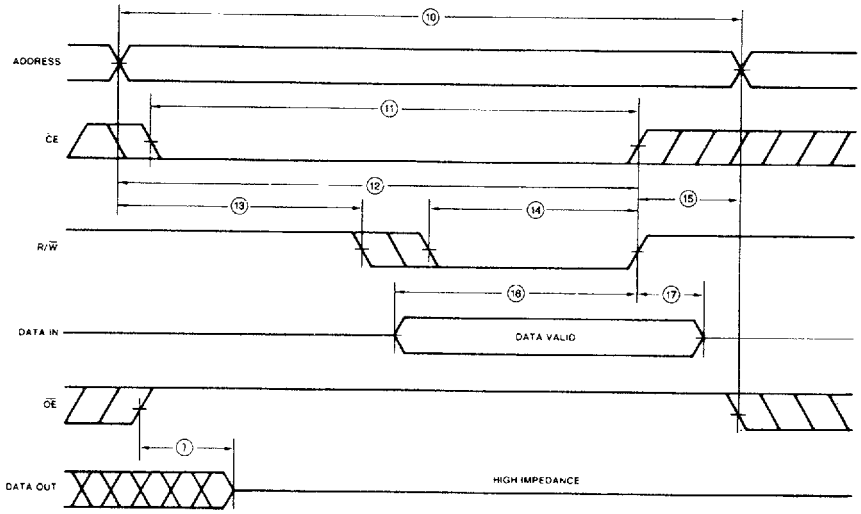


WF009401

$\overline{CE}$ and $\overline{OE}$-Controlled Access
(Notes 1 & 3)

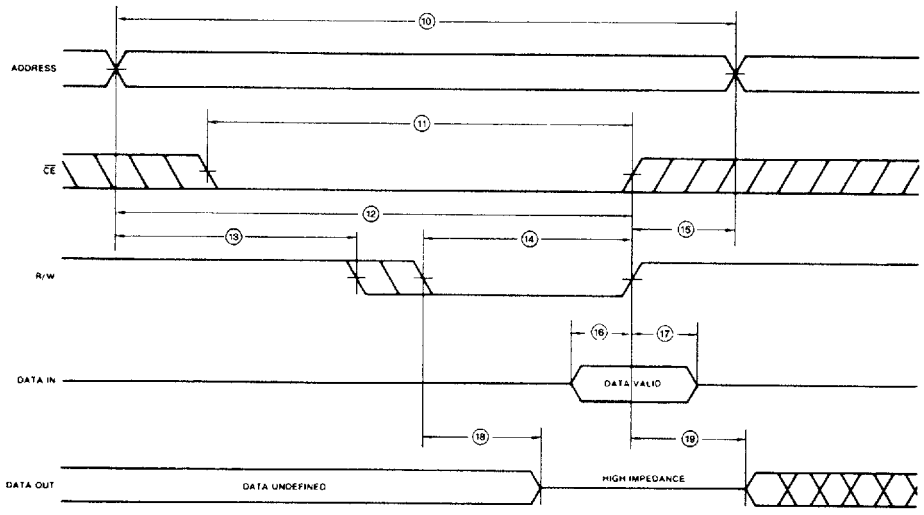
SWITCHING WAVEFORMS (Cont'd.)

WRITE CYCLE
(Either Side — Note 4)



WF009411

OE-Controlled Data Out

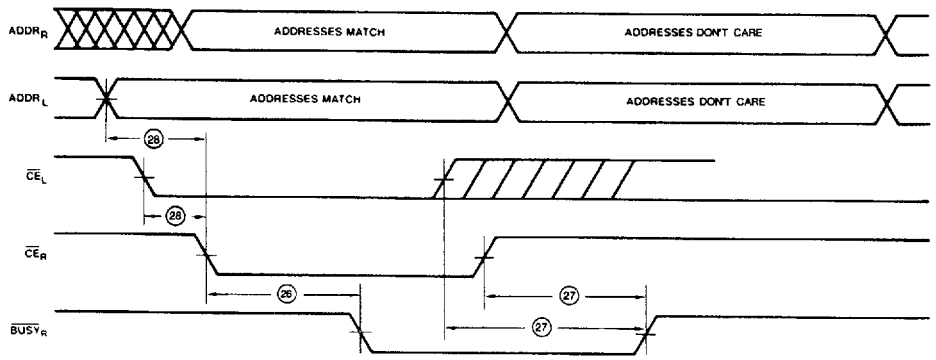


WF009421

WE-Controlled Data Out
($\overline{OE}$ = V_{IL})

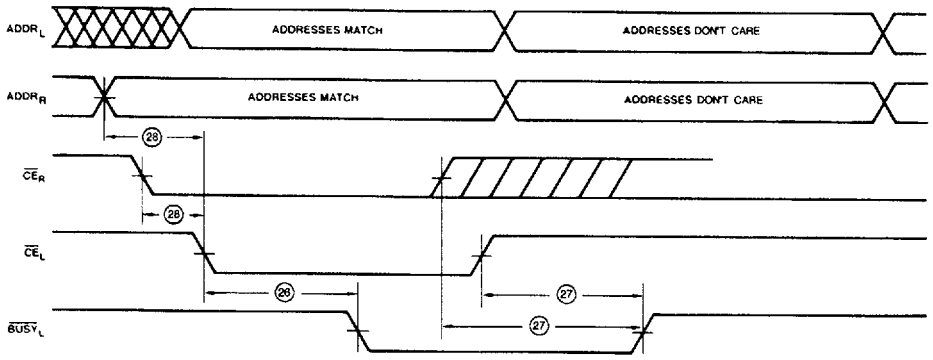
SWITCHING WAVEFORMS (Cont'd.)

$\overline{BUSY}$ FLAG TIMING (1 of 2) (Note 12)
(Chip Enable Arbitration)



WF009433

$\overline{CE}_R$ Valid Last

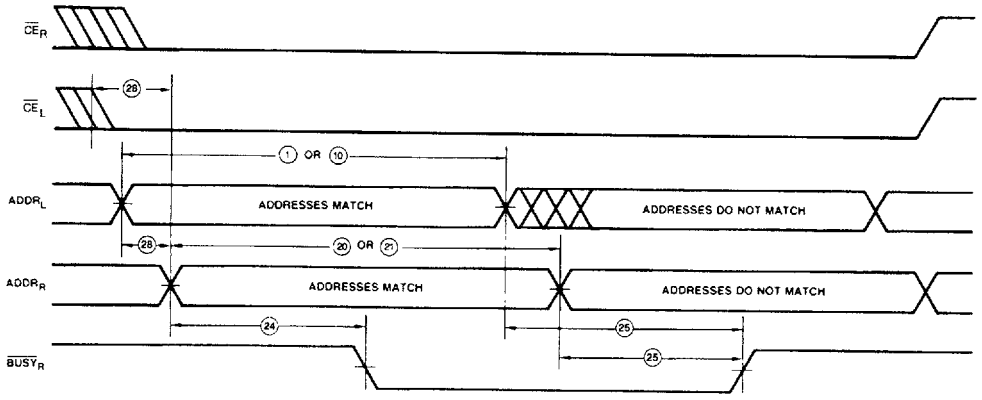


WF009434

$\overline{CE}_L$ Valid Last

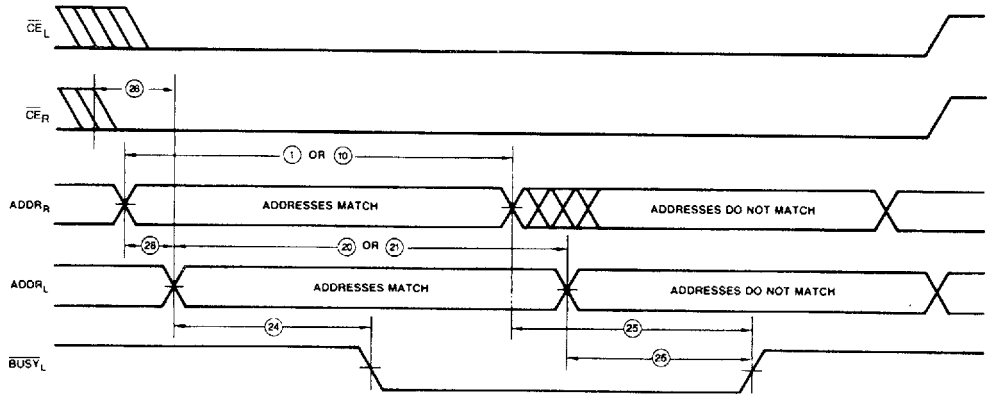
SWITCHING WAVEFORMS (Cont'd.)

$\overline{BUSY}$ FLAG TIMING (2 of 2)
(Address Arbitration)



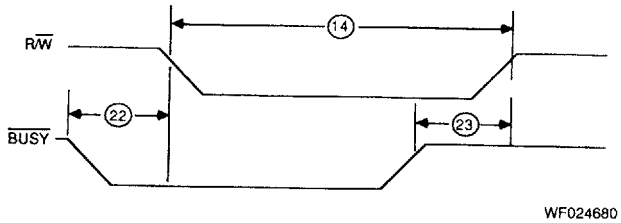
WF009443

$ADDR_R$ Valid Last



WF009444

$ADDR_L$ Valid Last

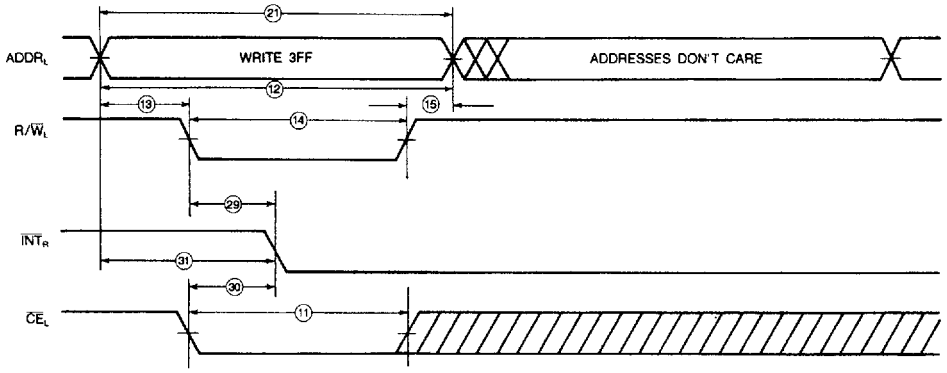


WF024680

For Am2140 Only

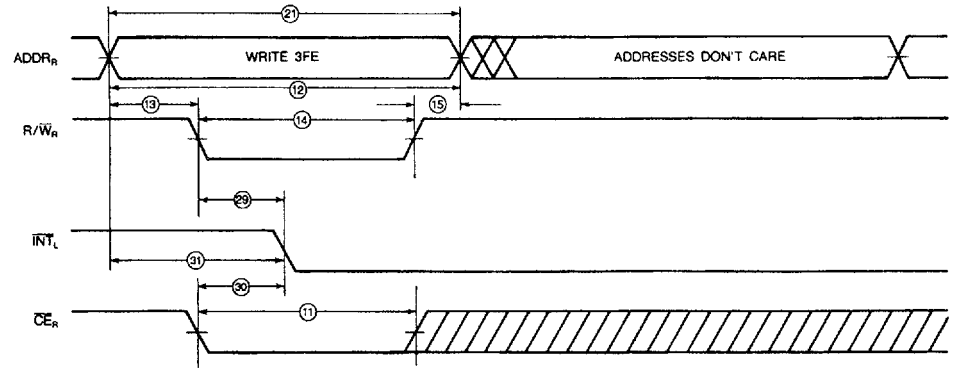
SWITCHING WAVEFORMS (Cont'd.)

INTERRUPT TIMING (1 of 2)
(Set $\overline{INT}$ Flag — Note 11)



WF009486

Left Side Flags Right Side

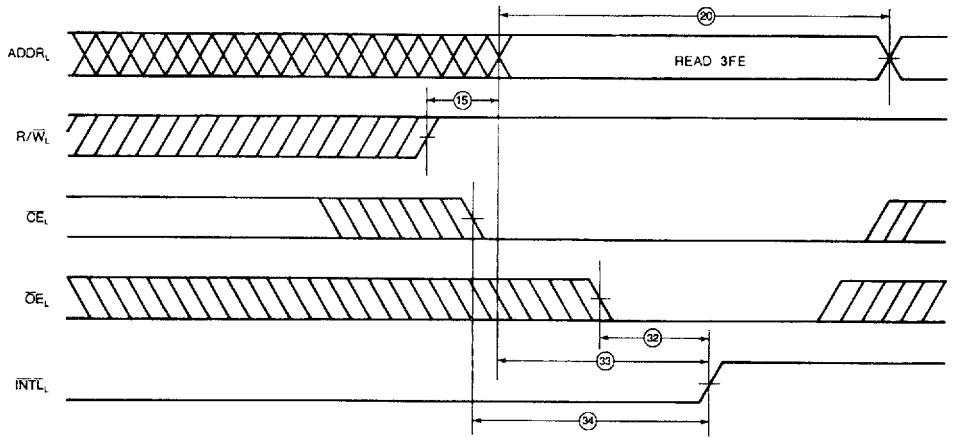


WF009487

Right Side Flags Left Side

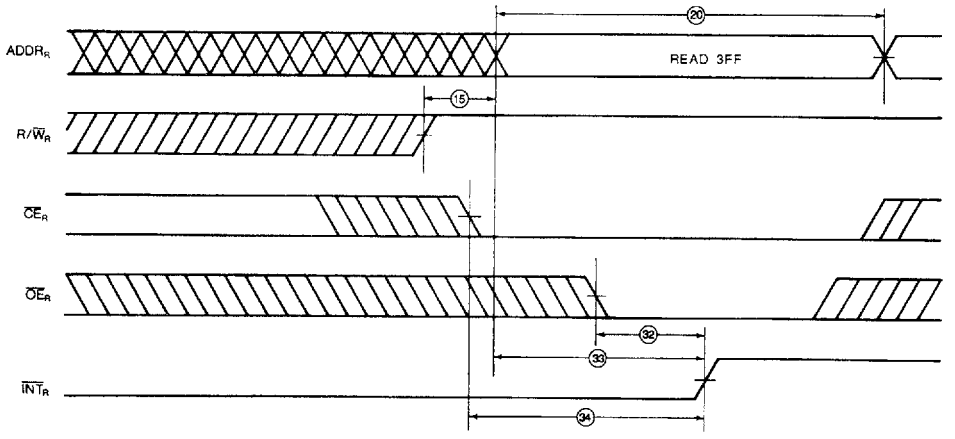
SWITCHING WAVEFORMS (Cont'd.)

INTERRUPT TIMING (2 of 2)
(Clear $\overline{INT}$ Flag)



WF009489

Left Side Clears $\overline{INT}_L$



WF009488

Right Side Clears $\overline{INT}_R$

4

Notes*

1. R/$\overline{W}$ is HIGH for Read Cycles.
2. Device is continuously enabled, $\overline{CE} = V_{IL}$, $\overline{OE} = V_{IL}$.
3. Addresses valid prior to or coincident with $\overline{CE}$ transition LOW.
4. If $\overline{CE}$ and R/$\overline{W}$ go HIGH simultaneously, the outputs remain in the high-impedance state.
5. Transition is measured at 1.5 V on the input to VOH – 500 mV and VOL + 500 mV on the outputs using the Load shown in Load A.
6. $\overline{CE}_L = \overline{CE}_R = V_{IL}$.
7. The $\overline{BUSY}$ and $\overline{INT}$ outputs are open drain. A pull-up resistor is required for system operation. For measurement purposes, Load C is used for HIGH-to-LOW transitions; output reference level is 1.5 V. Load D is used for LOW-to-HIGH transitions; output reference level is +500 mV from the output LOW voltage level.
8. For test and correlation purposes, ambient temperature is defined as the instant-on case temperature.
9. This parameter is guaranteed by design but is not 100% tested.
10. Except where indicated, I/O pins use Load B.
11. For a given port to Set or Clear an Interrupt Flag, 1) that port must have priority if addresses match and both $\overline{CE}_L = \overline{CE}_R$ = LOW; or 2) Addresses do not match.
12. If the last input valid transition, which would ordinarily cause a match, occurs at the same time that the opposite port address or $\overline{CE}$ changes to a no-match condition, then $\overline{BUSY}$ will remain HIGH (i.e., if there is never a match, then $\overline{BUSY}$ remains HIGH).
13. For Slave Am2140 only.
14. For Master Am2130 only.
15. Absolute Maximum Ratings are intended for user guidelines and are not tested.

* Notes listed correspond to reference made in the following sections:
  - Operating Ranges
  - DC Characteristics table
  - Switching Characteristics table
  - Switching Waveforms