SLOS407A – FEBRUARY 2003 – MARCH 2003

12-W STEREO CLASS-D AUDIO POWER AMPLIFIER WITH DC VOLUME CONTROL

FEATURES

- **12-W/Ch Into an 8-Ω Load From 15-V Supply**
- **Efficient, Class-D Operation Eliminates Heatsinks and Reduces Power Supply Requirements**
- **32-Step DC Volume Control From –40 dB to 36 dB**
- **Line Outputs For External Headphone Amplifier With Volume Control**
- **Regulated 5-V Supply Output for Powering TPA6110A2**
- **Space-Saving, Thermally-Enhanced PowerPAD™ Packaging**
- **Thermal and Short-Circuit Protection**

APPLICATIONS

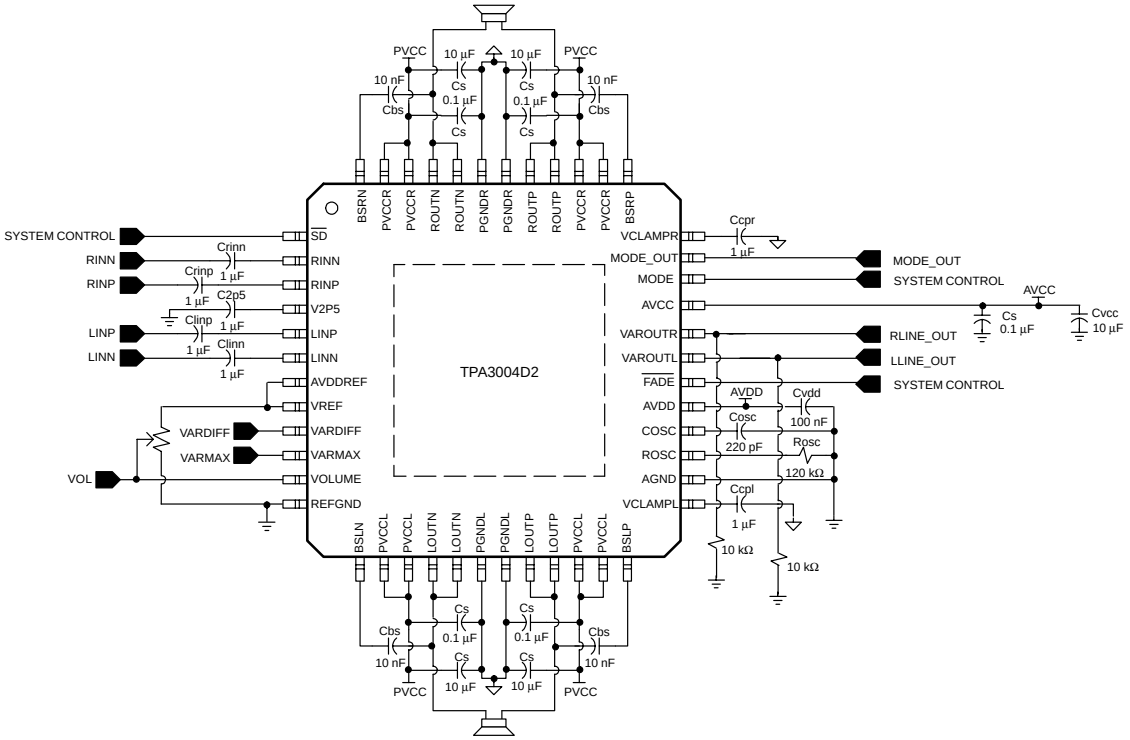
- **LCD Monitors and TVs**
- **Powered Speakers**

DESCRIPTION

The TPA3004D2 is a 12-W (per channel) efficient, Class-D audio amplifier for driving bridged-tied stereo speakers. The TPA3004D2 can drive stereo speakers as low as 4 Ω. The high efficiency of the TPA3004D2 eliminates the need for external heatsinks when playing music.

Stereo speaker volume is controlled with a dc voltage applied to the volume control terminal offering a range of gain from –40 dB to 36 dB. Line outputs, for driving external headphone amplifier inputs, are also dc voltage controlled with a range of gain from –56 dB to 20 dB.

An integrated 5-V regulated supply is provided for powering an external headphone amplifier.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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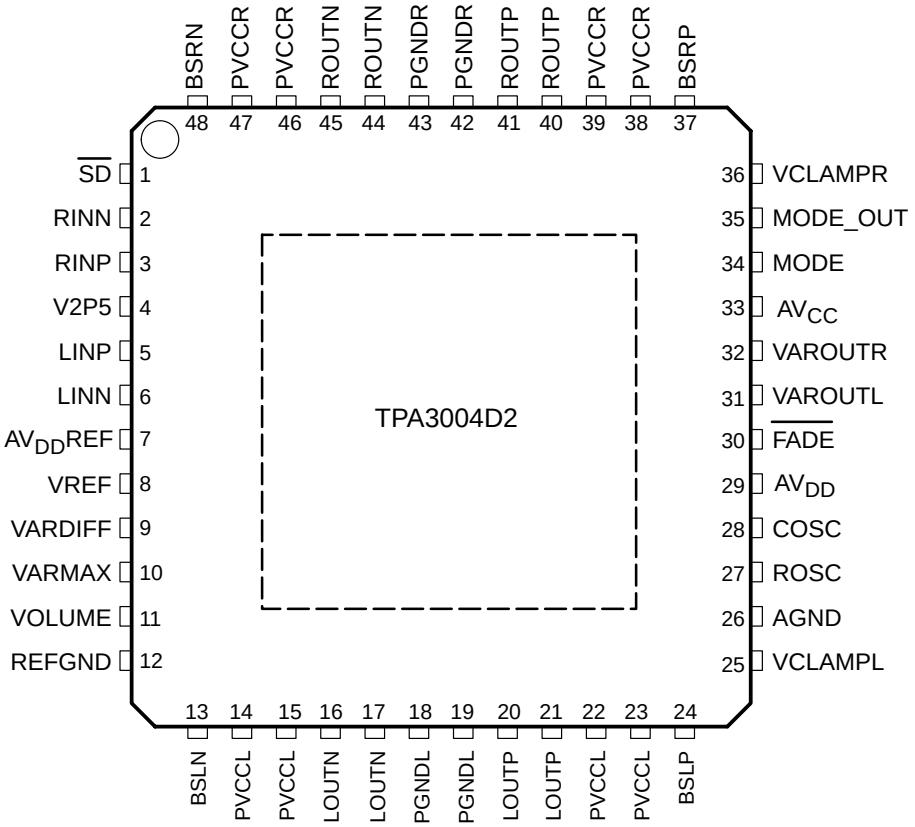
AVAILABLE OPTIONS

T_A	PACKAGED DEVICE
	48-PIN HTQFP (PHP)†
–40°C to 85°C	TPA3004D2PHP

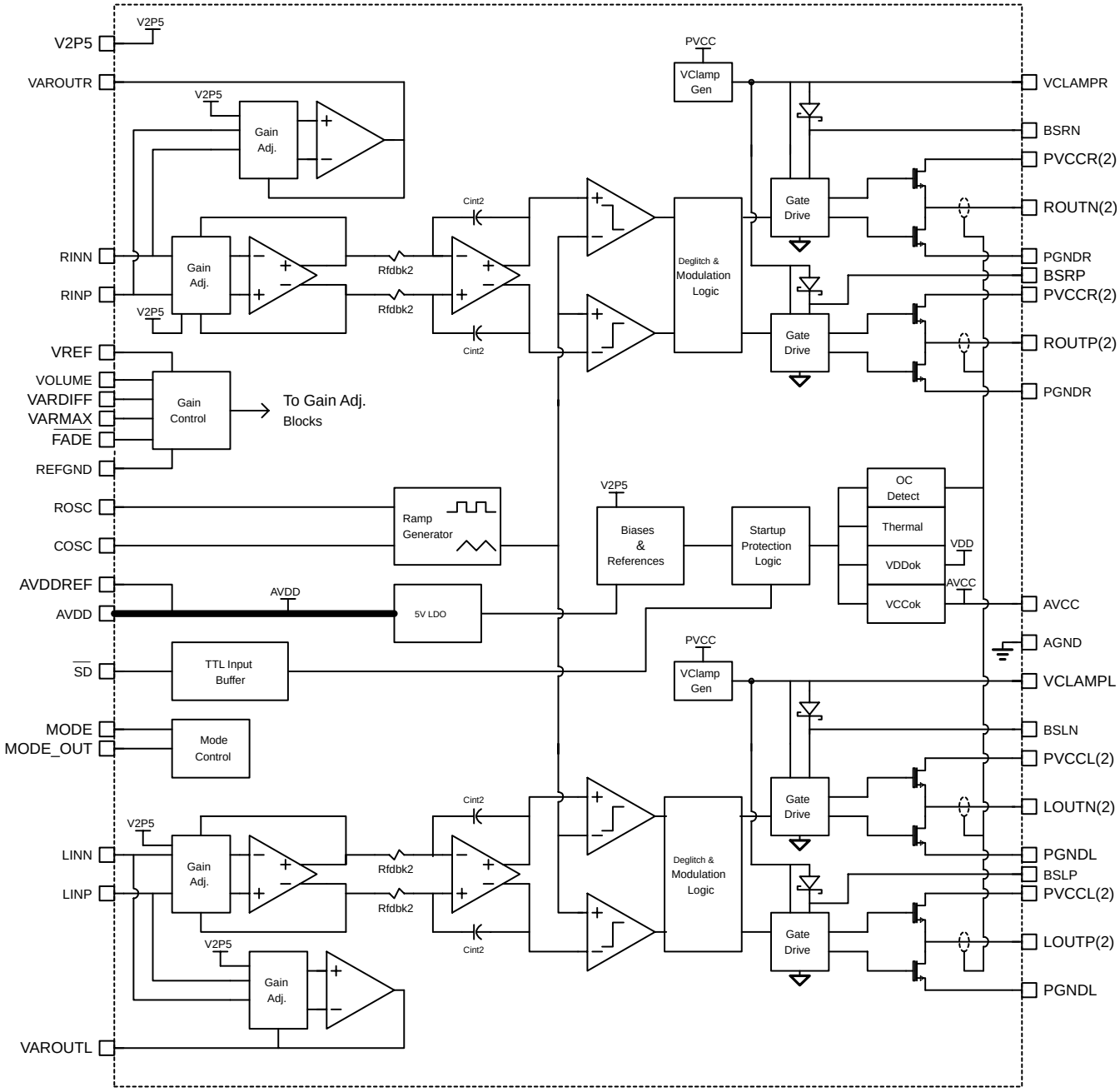
† The PHP package is available taped and reeled. To order a taped and reeled part, add the suffix R to the part number (e.g., TPA3004D2PHPR).

PHP PACKAGE

(TOP VIEW)



functional block diagram



Terminal Functions

TERMINAL NO.	TERMINAL NAME	I/O	DESCRIPTION
AGND	26	–	Analog ground for digital/analog cells in core
AV_{CC}	33	–	High-voltage analog power supply (8.5 V to 18 V)
AV_{DD}	29	O	5-V Regulated output capable of 100-mA output
AV_{DD}REF	7	O	5-V Reference output—provided for connection to adjacent VREF terminal.
BSLN	13	I/O	Bootstrap I/O for left channel, negative high-side FET
BSLP	24	I/O	Bootstrap I/O for left channel, positive high-side FET
BSRN	48	I/O	Bootstrap I/O for right channel, negative high-side FET
BSRP	37	I/O	Bootstrap I/O for right channel, positive high-side FET
COSC	28	I/O	I/O for charge/discharging currents onto capacitor for ramp generator triangle wave biased at V2P5
$\overline{\text{FADE}}$	30	I	Input for controlling volume ramp rate. A logic low on this pin places the amplifier in fade mode. A logic high on this pin allows a quick transition to the desired volume setting when cycling $\overline{\text{SD}}$ or during power-up.
LINN	6	I	Negative differential audio input for left channel
LINP	5	I	Positive differential audio input for left channel
LOUTN	16, 17	O	Class-D 1/2-H-bridge negative output for left channel
LOUTP	20, 21	O	Class-D 1/2-H-bridge positive output for left channel
MODE	34	I	Input for MODE control. A logic high on this pin places the amplifier in the variable output mode and the Class-D outputs are disabled. A logic low on this pin places the amplifier in the Class-D mode and Class-D stereo outputs are enabled. Variable outputs (VAROUTL and VAROUTR) are still enabled in Class-D mode to be used as line-level outputs for external amplifiers.
MODE_OUT	35	O	Output for control of the variable output amplifiers. When the MODE pin (34) is a logic high, the MODE_OUT pin is driven low. When the MODE pin (34) is a logic low, the MODE_OUT pin is driven high. This pin is intended for MUTE control of an external headphone amplifier. Leave unconnected when not used for headphone amplifier control.
PGNDL	18, 19	–	Power ground for left channel H-bridge
PGNDR	42, 43	–	Power ground for right channel H-bridge
PVCCL	14, 15	–	Power supply for left channel H-bridge (tied to pins 22 and 23 internally), not connected to PVCCR or AV_{CC}.
PVCCL	22, 23	–	Power supply for left channel H-bridge (tied to pins 14 and 15 internally), not connected to PVCCR or AV_{CC}.
PVCCR	38,39	–	Power supply for right channel H-bridge (tied to pins 46 and 47 internally), not connected to PVCCL or AV_{CC}.
PVCCR	46, 47	–	Power supply for right channel H-bridge (tied to pins 38 and 39 internally), not connected to PVCCL or AV_{CC}.
REFGND	12	–	Ground for gain control circuitry. Connect to AGND. If using a DAC to control the volume, connect the DAC ground to this terminal.
RINP	3	I	Positive differential audio input for right channel
RINN	2	I	Negative differential audio input for right channel
ROSC	27	I/O	Current setting resistor for ramp generator. Nominally equal to 1/8*V_{CC}
ROUTN	44, 45	O	Class-D 1/2-H-bridge negative output for right channel
ROUTP	40, 41	O	Class-D 1/2-H-bridge positive output for right channel
$\overline{\text{SD}}$	1	I	Shutdown signal for IC (low = shutdown, high = operational). TTL logic levels with compliance to V_{CC}.
VARDIFF	9	I	DC voltage to set the difference in gain between the Class-D and VAROUT outputs. Connect to GND or AV_{DD}REF if VAROUT outputs are unconnected.
VARMAX	10	I	DC voltage that sets the maximum gain for the VAROUT outputs. Connect to GND or AV_{DD}REF if VAROUT outputs are unconnected.
VAROUTL	31	O	Variable output for left channel audio. Line level output for driving external HP amplifier.

Terminal Functions (Continued)

TERMINAL NO.	TERMINAL NAME	I/O	DESCRIPTION
VAROUTR	32	O	Variable output for right channel audio. Line level output for driving external HP amplifier.
VCLAMPL	25	–	Internally generated voltage supply for left channel bootstrap capacitors.
VCLAMPR	36	–	Internally generated voltage supply for right channel bootstrap capacitors.
VOLUME	11	I	DC voltage that sets the gain of the Class-D and VAROUT outputs.
VREF	8	I	Analog reference for gain control section.
V2P5	4	O	2.5-V Reference for analog cells, as well as reference for unused audio input when using single-ended inputs.
—	Thermal Pad	–	Connect to AGND and PGND—should be center point for both grounds.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range: AV_{CC}, PV_{CC} . . . . . –0.3 V to 20 V
Load impedance, R_L . . . . . ≥ 3.6 Ω
Input voltage range, V_I: MODE, VREF, VARDIFF, VARMAX, VOLUME, $\overline{FADE}$ . . . . . 0 V to 5.5 V
$\overline{SD}$ . . . . . –0.3 V to V_{CC} + 0.3 V
RINN, RINP, LINN, LINP . . . . . –0.3 V to 7 V
Supply current: AV_{DD} . . . . . 120 mA
AVDDREF . . . . . 10 mA
Output current, VAROUTL, VAROUTR . . . . . 20 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . –40°C to 85°C
Operating junction temperature range, T_J‡ . . . . . –40°C to 150°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ The (TPA3004D2) incorporates an exposed PowerPAD on the underside of the chip. This acts as a heatsink and must be connected to a thermally dissipating plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature that couldm permanently damage the device. See TI Technical Brief SLMA002 for more information about utilizing the PowerPAD thermally enhanced package.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$	DERATING FACTOR	$T_A = 70°C$	$T_A = 85°C$
PHP	4.3 W	34.7 mW/°C§	2.7 W	2.2 W

§ The PowerPAD must be soldered to a thermal land on the printed circuit board. Please refer to the *PowerPAD Thermally Enhanced Package* application note (SLMA002).

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{CC}	PV_{CC}, AV_{CC}; $R_L \geq 3.6\ \Omega$	8.5	18	V
Volume reference voltage	VREF	3.0	5.5	V
Volume control pins, input voltage	VARDIFF, VARMAX, VOLUME		5.5	V
High-level input voltage, V_{IH}	$\overline{SD}$	2		V
	MODE	3.5		
	$\overline{FADE}$	4.0		
Low-level input voltage, V_{IL}	$\overline{SD}$		0.8	V
	MODE, $\overline{FADE}$		2	
High-level output voltage, V_{OH}	MODE_OUT, I_{OH} = 1 mA	AV_{DD}–100mV		V
Low-level output voltage, V_{OL}	MODE_OUT, I_{OL} = –1 mA		AGND+100mV	V
High-level input current, I_{IH}	MODE,V_I= 5 V, V_{CC} = 18 V		1	uA
	$\overline{FADE}$, V_I= 18 V, V_{CC} = 18 V		150	
	$\overline{SD}$, V_I= 18 V, V_{CC} = 18 V		50	
Low-level input current, I_{IL}	MODE, $\overline{FADE}$, V_I= 0 V, V_{CC} = 18 V		1	uA
	$\overline{SD}$, V_I= 0 V, V_{CC} = 18 V		1	uA
Oscillator frequency, f_{OSC}		225	275	kHz
Operating free-air temperature, T_A		–40	85	°C
Operating junction temperature, T_J†			125	°C

† Continuous operation above the recommended junction temperature may result in reduced reliability and/or lifetime of the device. The junction temperature is controlled by the thermal design of the application and should be carefully considered in high power dissipation applications. See the *thermal considerations* section on pages 33–35 for recommendations on improving the thermal performance of your application.

dc characteristics, T_A = 25°C, V_{CC} = 12 V, R_L = 8 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$\lvert V_{OS} \rvert$	Class-D Output offset voltage (measured differentially)	INN and INP connected together, Gain = 36 dB			10	65	mV
V2P5 (terminal 4)	2.5-V Bias voltage	No load		0.45x AV_{DD}	0.5x AV_{DD}	0.55x AV_{DD}	V
AV_{DD}	5-V Regulated output	I_O = 0 to 100 mA, $\overline{SD}$ = 2 V, V_{CC} = 8.5 V to 18 V		4.5	5.0	5.5	V
PSRR	Class-D power supply rejection ratio	V_{CC} = 11.5 V to 12.5 V			–80		dB
$I_{CC(class-D)}$	Class-D mode quiescent current	MODE = 2 V, $\overline{SD}$ = 2 V, V_{CC} = 18 V			16	28.5	mA
$I_{CC(varout)}$	Variable output mode quiescent current	MODE = 3.5 V, $\overline{SD}$ = 2 V, V_{CC} = 18 V			7	9	mA
$I_{CC(class-D – max power)}$	Class-D mode RMS current at max power	R_L = 8 Ω, P_O = 12 W, V_{CC} = 15 V to 18 V			2		A
$I_{CC(SD)}$	Supply current in shutdown mode	$\overline{SD}$ = 0.8 V, V_{CC} = 12 V			1	10	uA
		$\overline{SD}$ = 0.8 V, V_{CC} = 18 V				160	
$r_{ds(on)}$	Drain-source on-state resistance	V_{CC} = 12 V, I_O = 1 A, T_J = 25°C	High side		300		mΩ
			Low side		250		
			Total		550	650	

ac characteristics for Class-D outputs, T_A = 25°C, V_{CC} = 12 V, R_L = 8 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
k_{SVR}	Supply ripple rejection ratio	V_{CC} = 11.5 V to 12.5 V from 10 Hz to 1 kHz, Gain = 36 dB		–67		dB
$P_{O(max)}$	Maximum continuous output power (thermally limited)	R_L = 4 Ω		7.5		W
		R_L = 8 Ω		12		W
V_n	Output integrated noise floor	20 Hz to 22 kHz, No weighting filter, Gain = 0.5 dB		–82		dBV
	Crosstalk, Class-D–Left → Class-D–Right	Gain = 13.2 dB, P_O = 1 W, R_L = 8 Ω		–77		dB
	Crosstalk, Class-D → VAROUT	Maximum output at THD < 0.5%, Gain = 36 dB		–63		dB
SNR	Signal-to-noise ratio	Maximum output at THD+N < 0.5%, f= 1 kHz, Gain = 0.5 dB		102		dB
	Thermal trip point			150		°C
	Thermal hystersis			20		°C

characteristics for VAROUT outputs

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
$\|V_{OS}\|$	Output offset voltage	Measured between V2P5 and VAROUT, Gain = 20 dB, R_L = 10 kΩ		10	65	mV
THD+N	Total harmonic distortion + noise	A_V = 7.3 dB, f = 1 kHz, P_O = 6 mW, R_L = 32 Ω		0.025%		
		A_V = 7.3 dB, f = 1 kHz, R_L = 2 kΩ, V_O = 1 V_{rms}		0.002%		
PSRR	DC power supply rejection ratio	Gain = 20 dB		–74		dB
k_{SVR}	Supply ripple rejection ratio	Gain = 20 dB, f = 1 kHz		–95		dB
	Crosstalk, VAROUTL → VAROUTR	Maximum output at THD < 0.5%, Gain = 20 dB		–60		dB
	Crosstalk, VAROUT → Class-D	Maximum output at THD < 0.5%, Gain = 20 dB		–74		dB
V_n	Output integrated noise floor	20 Hz to 22 kHz, Gain = 20 dB		75		μV
		20 Hz to 22 kHz, Gain = –0.3 dB		15		

Table 1. DC Volume Control for Class-D Outputs

VOLTAGE ON THE VOLUME PIN AS A PERCENTAGE OF VREF (INCREASING VOLUME OR FIXED GAIN)	VOLTAGE ON THE VOLUME PIN AS A PERCENTAGE OF VREF (DECREASING VOLUME)	GAIN OF CLASS-D AMPLIFIER
%	%	dB
0 – 4.5	0 – 2.9	–75†
4.5 – 6.7	2.9 – 5.1	–40.0
6.7 – 8.91	5.1 – 7.2	–37.5
8.9 – 11.1	7.2 – 9.4	–35.0
11.1 – 13.3	9.4 – 11.6	–32.4
13.3 – 15.5	11.6 – 13.8	–29.9
15.5 – 17.7	13.8 – 16.0	–27.4
17.7 – 19.9	16.0 – 18.2	–24.8
19.9 – 22.1	18.2 – 20.4	–22.3
22.1 – 24.3	20.4 – 22.6	–19.8
24.3 – 26.5	22.6 – 24.8	–17.2
26.5 – 28.7	24.8 – 27.0	–14.7
28.7 – 30.9	27.0 – 29.1	–12.2
30.9 – 33.1	29.1 – 31.3	–9.6
33.1 – 35.3	31.3 – 33.5	–7.1
35.3 – 37.5	33.5 – 35.7	–4.6
37.5 – 39.7	35.7 – 37.9	–2.0
39.7 – 41.9	37.9 – 40.1	0.5†
41.9 – 44.1	40.1 – 42.3	3.1
44.1 – 46.4	42.3 – 44.5	5.6
46.4 – 48.6	44.5 – 46.7	8.1
48.6 – 50.8	46.7 – 48.9	10.7
50.8 – 53.0	48.9 – 51.0	13.2
53.0 – 55.2	51.0 – 53.2	15.7
55.2 – 57.4	53.2 – 55.4	18.3
57.4 – 59.6	55.4 – 57.6	20.8
59.6 – 61.8	57.6 – 59.8	23.3
61.8 – 64.0	59.8 – 62.0	25.9
64.0 – 66.2	62.0 – 64.2	28.4
66.2 – 68.4	64.2 – 66.4	30.9
68.4 – 70.6	66.4 – 68.6	33.5
> 70.6	>68.6	36.0†

† Tested in production. Remaining steps are specified by design.

Table 2. DC Volume Control for VAROUT Outputs

VAROUT_VOLUME (V)† – FROM FIGURE 24 – AS A PERCENTAGE OF VREF (INCREASING VOLUME OR FIXED GAIN)	VAROUT_VOLUME (V) – FROM FIGURE 24 – AS A PERCENTAGE OF VREF (DECREASING VOLUME)	GAIN OF VAROUT AMPLIFIER
%	%	dB
0 – 4.5	0 – 2.9	–66†
4.5 – 6.7	2.9 – 5.1	–56.0
6.7 – 8.91	5.1 – 7.2	–53.5
8.9 – 11.1	7.2 – 9.4	–50.9
11.1 – 13.3	9.4 – 11.6	–48.4
13.3 – 15.5	11.6 – 13.8	–45.9
15.5 – 17.7	13.8 – 16.0	–43.3
17.7 – 19.9	16.0 – 18.2	–40.8
19.9 – 22.1	18.2 – 20.4	–38.3
22.1 – 24.3	20.4 – 22.6	–35.7
24.3 – 26.5	22.6 – 24.8	–33.2
26.5 – 28.7	24.8 – 27.0	–30.7
28.7 – 30.9	27.0 – 29.1	–28.1
30.9 – 33.1	29.1 – 31.3	–25.6
33.1 – 35.3	31.3 – 33.5	–23.1
35.3 – 37.5	33.5 – 35.7	–20.5
37.5 – 39.7	35.7 – 37.9	–18.0
39.7 – 41.9	37.9 – 40.1	–15.5
41.9 – 44.1	40.1 – 42.3	–13.0‡
44.1 – 46.4	42.3 – 44.5	–10.4
46.4 – 48.6	44.5 – 46.7	–7.9
48.6 – 50.8	46.7 – 48.9	–5.3
50.8 – 53.0	48.9 – 51.0	–2.8
53.0 – 55.2	51.0 – 53.2	–0.3
55.2 – 57.4	53.2 – 55.4	2.3
57.4 – 59.6	55.4 – 57.6	4.8
59.6 – 61.8	57.6 – 59.8	7.3
61.8 – 64.0	59.8 – 62.0	9.9
64.0 – 66.2	62.0 – 64.2	12.4
66.2 – 68.4	64.2 – 66.4	14.9
68.4 – 70.6	66.4 – 68.6	17.5
> 70.6	>68.6	20.0†

† VAROUT_VOLUME (V) = VOLUME (V) – VARDIFF (V), see pages 25 – 27.
‡ Tested in production. Remaining steps are specified by design.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
	Class-D Efficiency	vs Output power	1
P_O	Class-D Output power	vs Load resistance	2
		vs Supply voltage	3
I_{CC}	Class-D Supply current	vs Supply voltage	4
		vs Output Power	5
$I_{O(sd)}$	Shutdown supply current	vs Supply voltage	6
	Class-D Input impedance	vs Gain	7
THD+N	Class-D Total harmonic distortion + noise	vs Frequency	8 – 12
		vs Output power	13 – 17
k_{SVR}	Class-D Supply ripple rejection ratio	vs Frequency	18
	Class-D Closed loop response		19
	Class-D Intermodulation performance		20
	Class-D Input offset voltage	vs Common-mode input voltage	21
	Class-D Crosstalk	vs Frequency	22
	Class-D Mute attenuation	vs Frequency	23
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	Class-D Common-mode rejection ratio	vs Frequency	25
	VAROUT Input resistance	vs Gain	26
	VAROUT Noise	vs Frequency	27
	VAROUT Closed Loop Response		28
	VAROUT Common-mode rejection ratio	vs Frequency	29
	VAROUT Crosstalk	vs Frequency	30
THD+N	VAROUT Total harmonic distortion + noise	vs Output power	31
		vs Output voltage	32
		vs Frequency	33
k_{SVR}	VAROUT Supply ripple rejection ratio	vs Frequency	34

TYPICAL CHARACTERISTICS

EFFICIENCY vs OUTPUT POWER

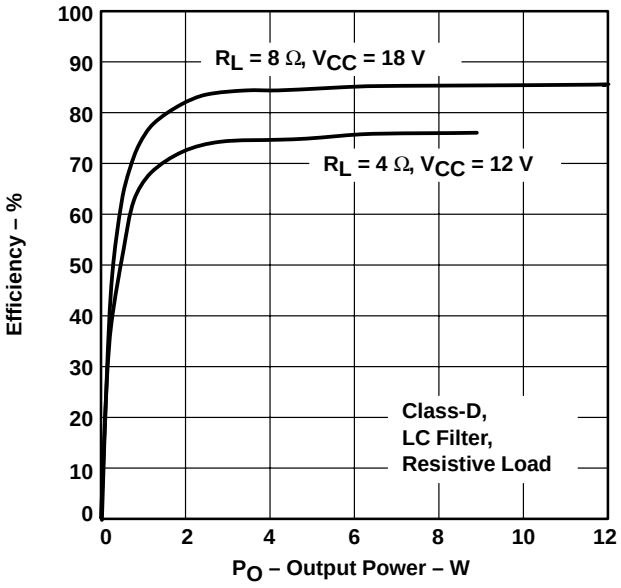


Figure 1

OUTPUT POWER vs LOAD RESISTANCE

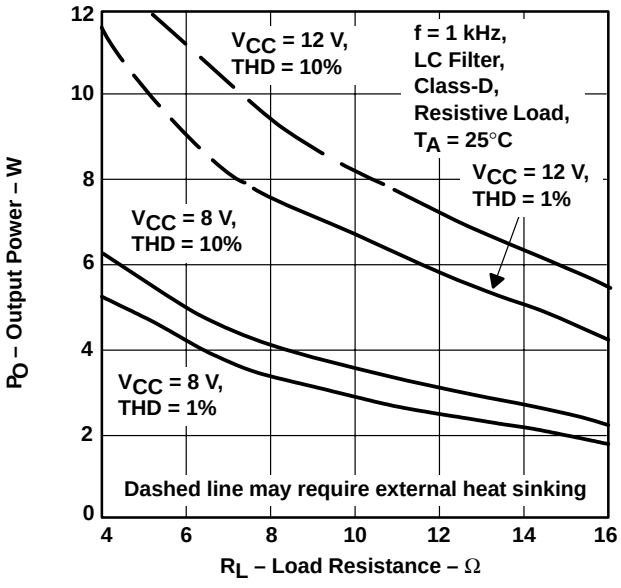


Figure 2

OUTPUT POWER vs SUPPLY VOLTAGE

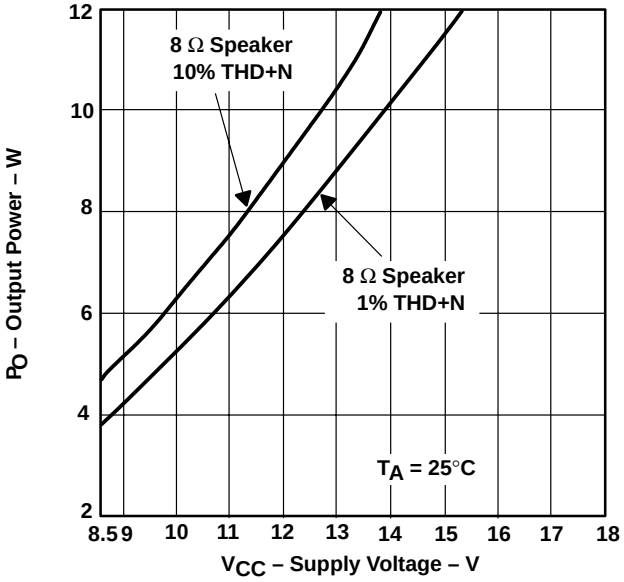


Figure 3

SUPPLY CURRENT vs SUPPLY VOLTAGE

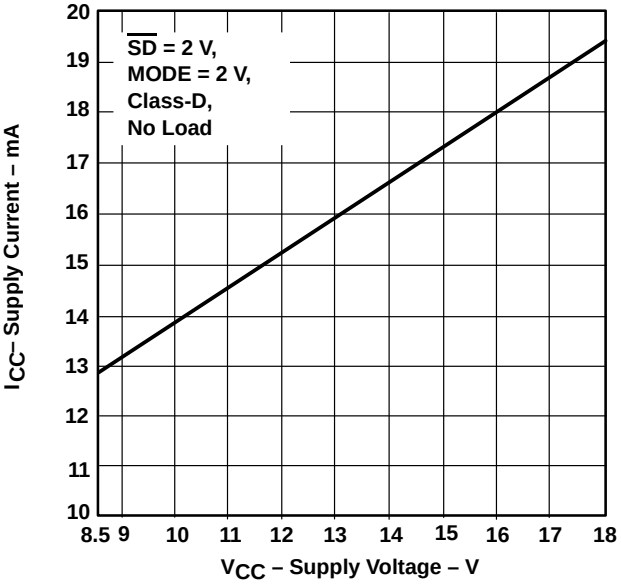


Figure 4

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs OUTPUT POWER

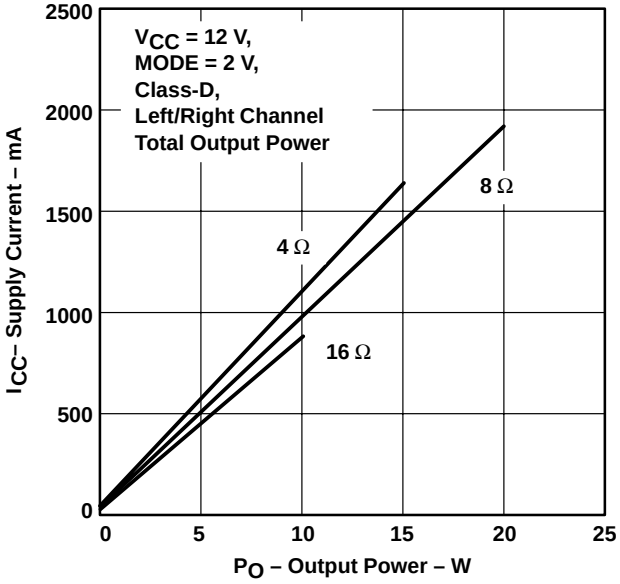


Figure 5

SHUTDOWN SUPPLY CURRENT vs SUPPLY VOLTAGE

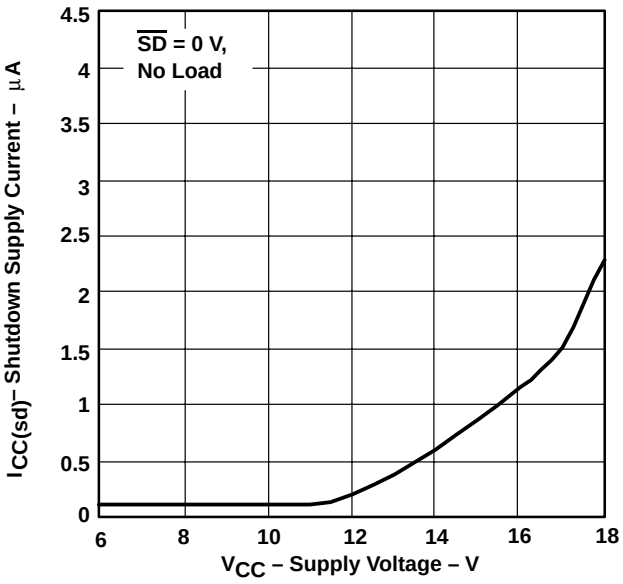


Figure 6

INPUT IMPEDANCE vs GAIN

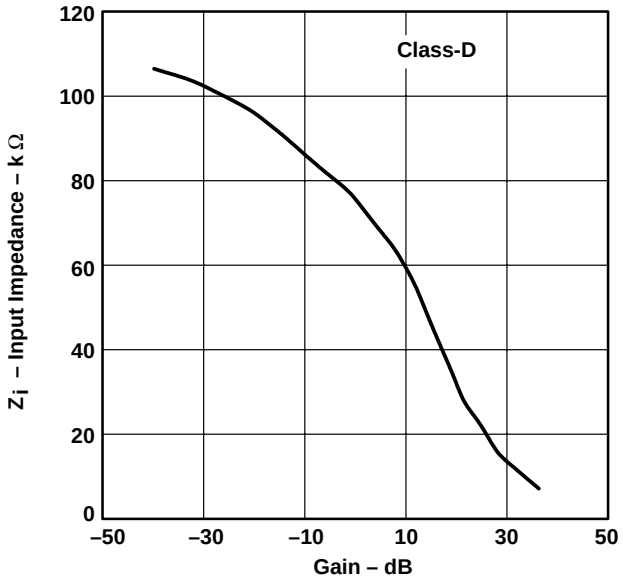


Figure 7

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

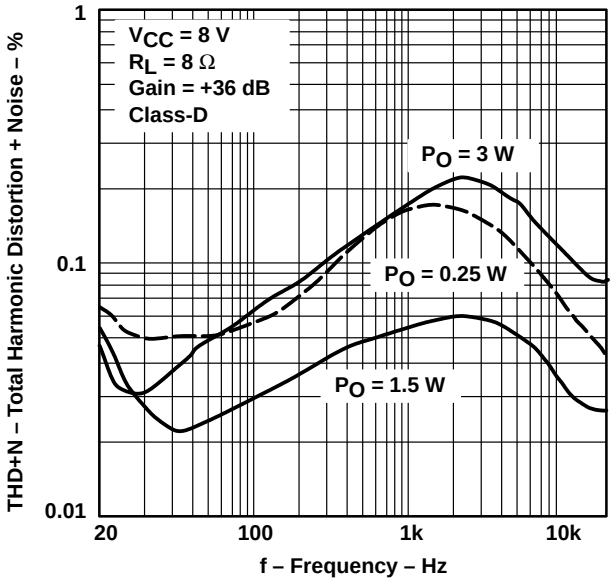


Figure 8

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION + NOISE
vs
FREQUENCY

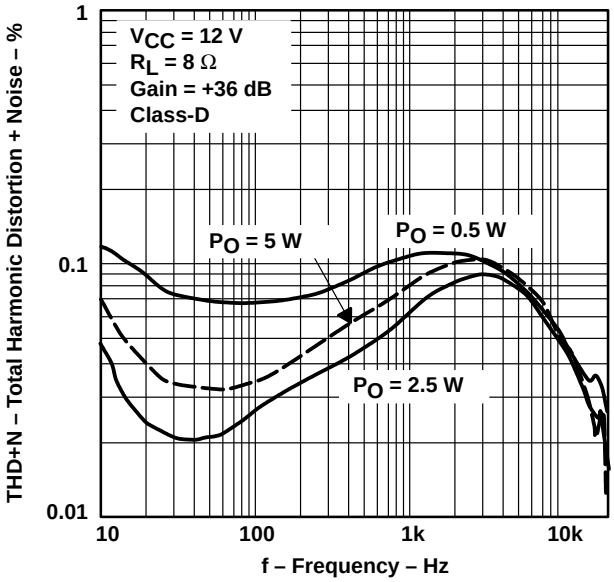


Figure 9

TOTAL HARMONIC DISTORTION + NOISE
vs
FREQUENCY

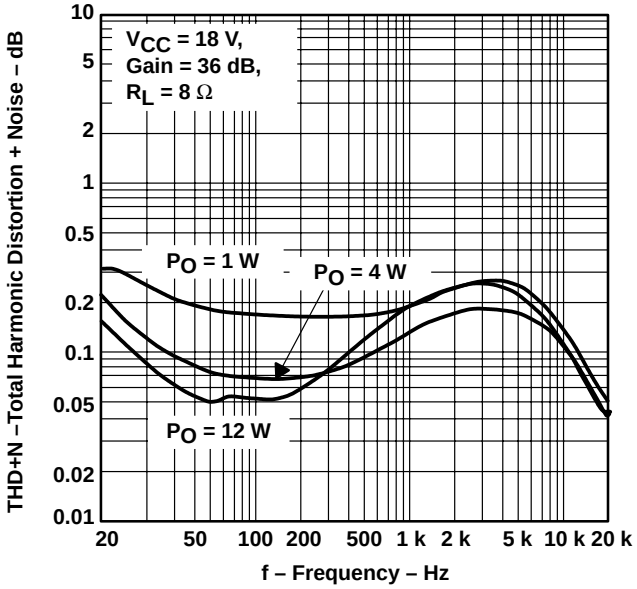


Figure 10

TOTAL HARMONIC DISTORTION + NOISE
vs
FREQUENCY

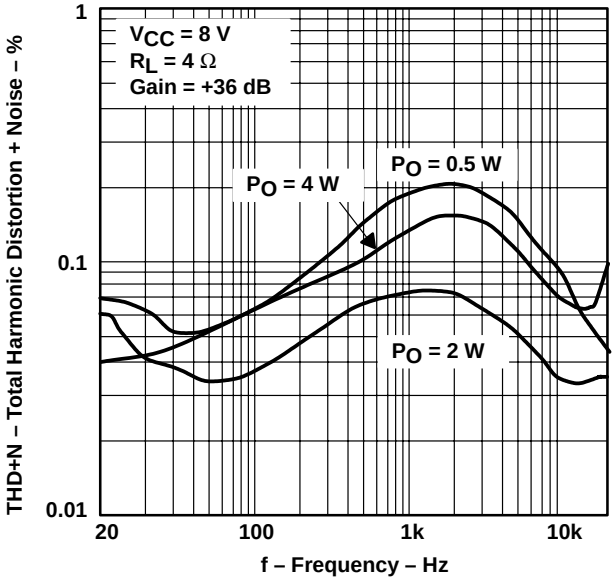


Figure 11

TOTAL HARMONIC DISTORTION + NOISE
vs
FREQUENCY

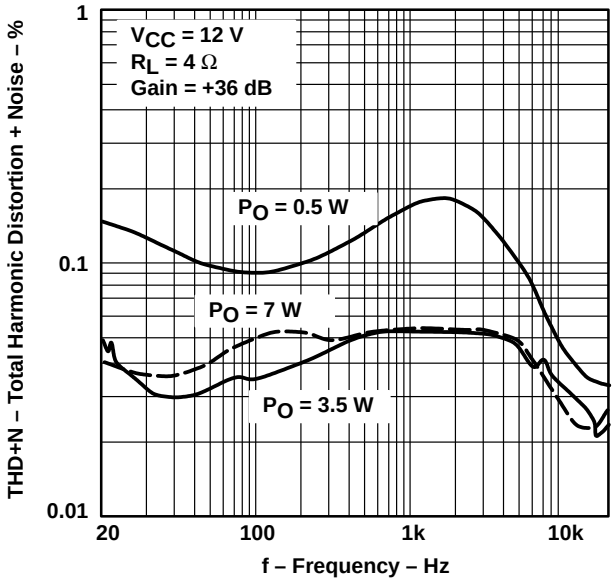


Figure 12

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

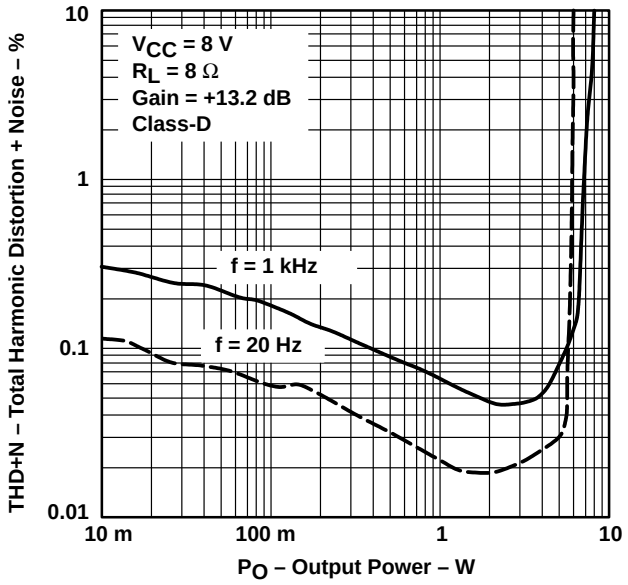


Figure 13

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

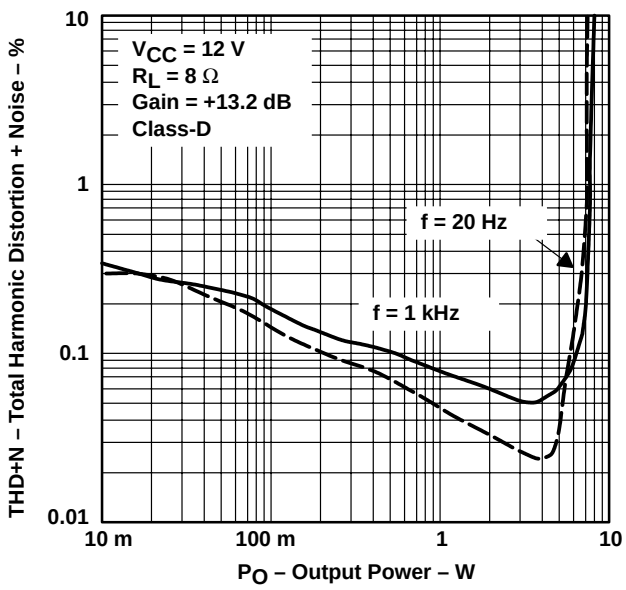


Figure 14

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

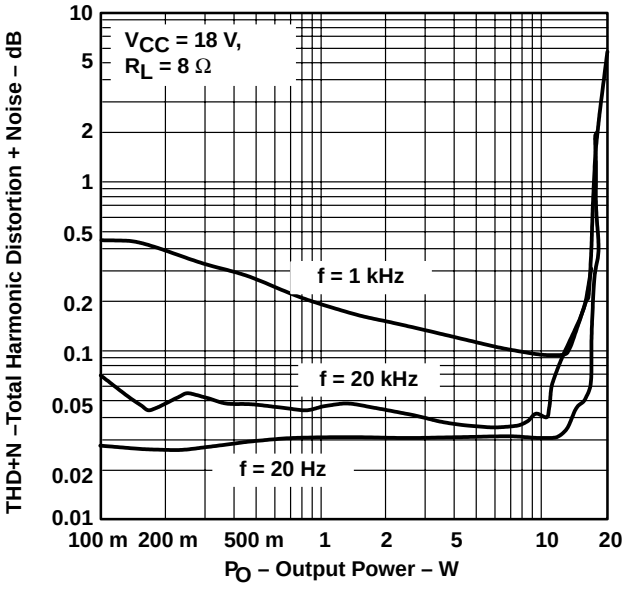


Figure 15

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

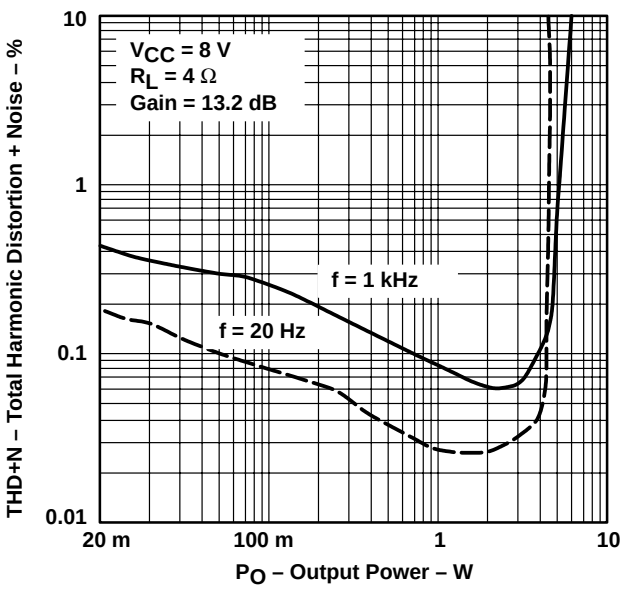


Figure 16

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

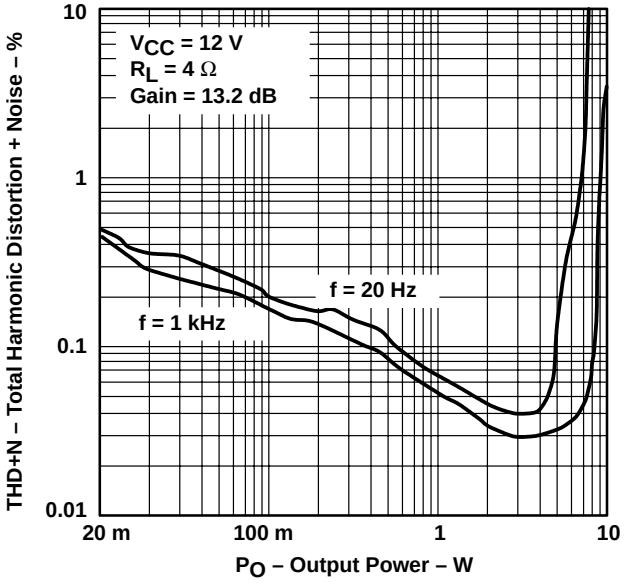


Figure 17

SUPPLY RIPPLE REJECTION RATIO vs FREQUENCY

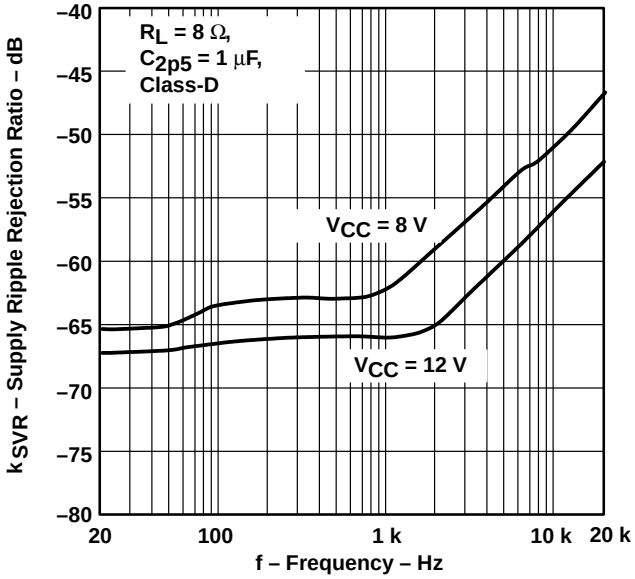


Figure 18

CLOSED LOOP RESPONSE

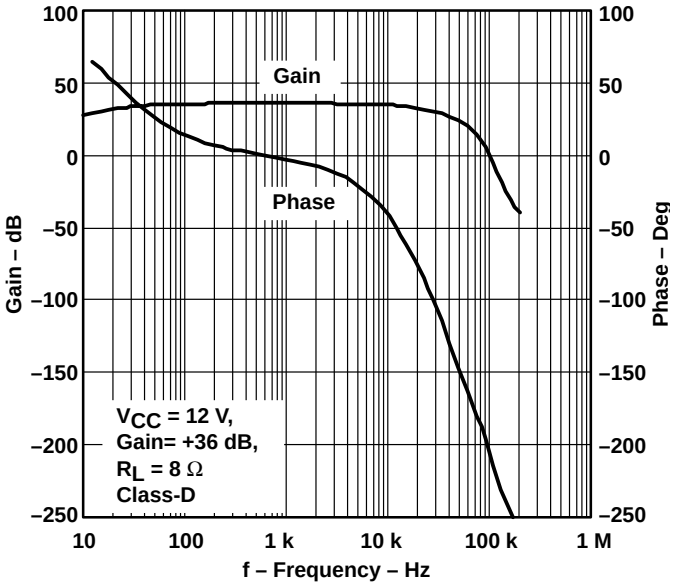


Figure 19

INTERMODULATION PERFORMANCE

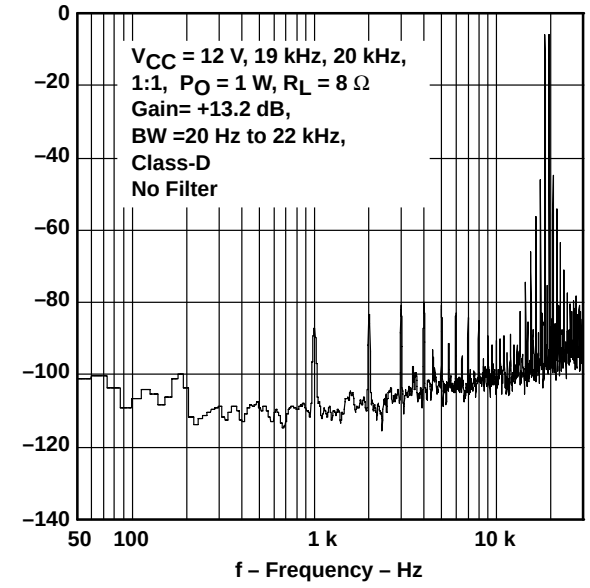


Figure 20

TYPICAL CHARACTERISTICS

INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE

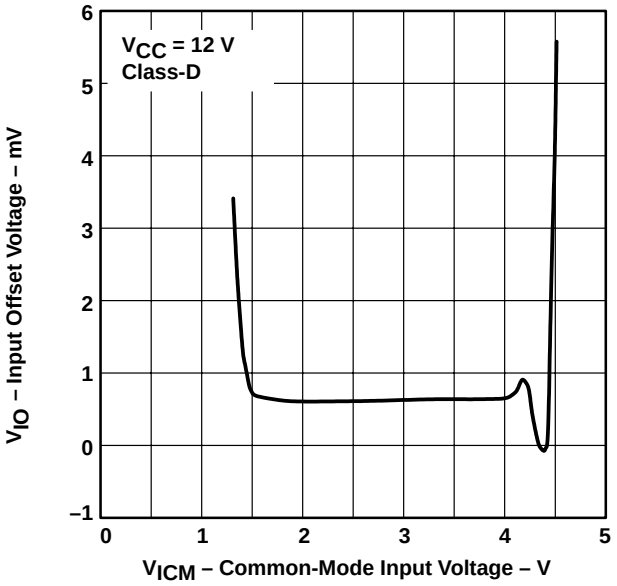


Figure 21

CROSSTALK vs FREQUENCY

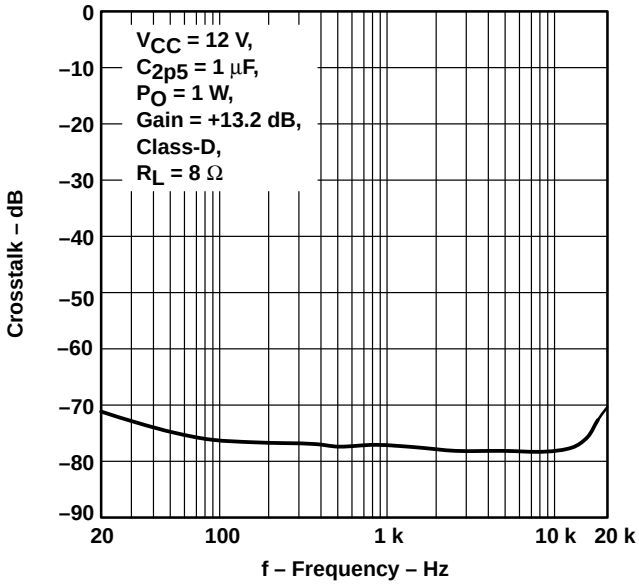


Figure 22

MUTE ATTENUATION vs FREQUENCY

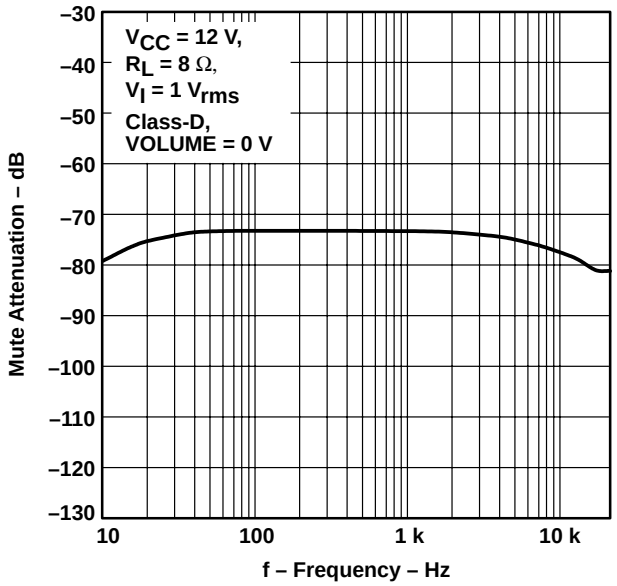


Figure 23

SHUTDOWN ATTENUATION vs FREQUENCY

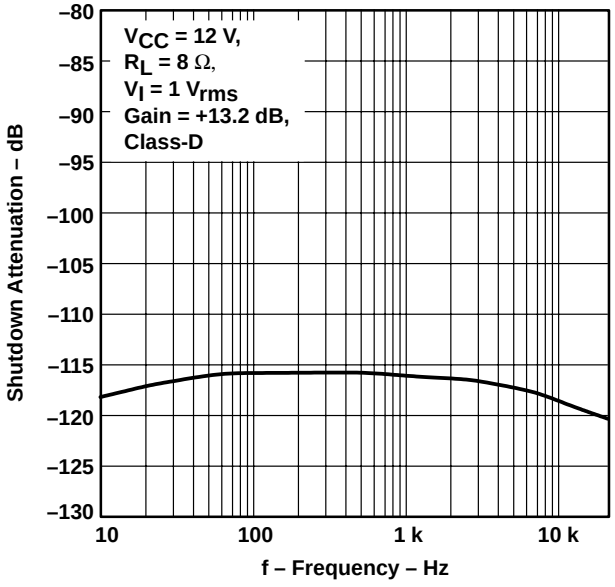


Figure 24

TYPICAL CHARACTERISTICS

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

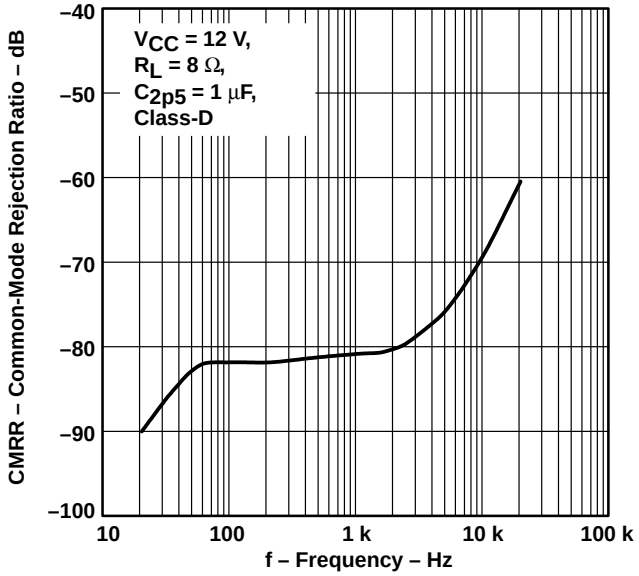


Figure 25

INPUT RESISTANCE
vs
GAIN

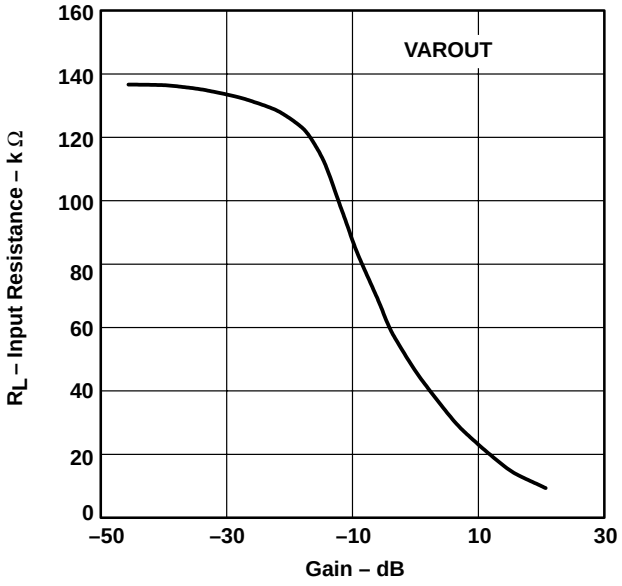


Figure 26

NOISE
vs
FREQUENCY

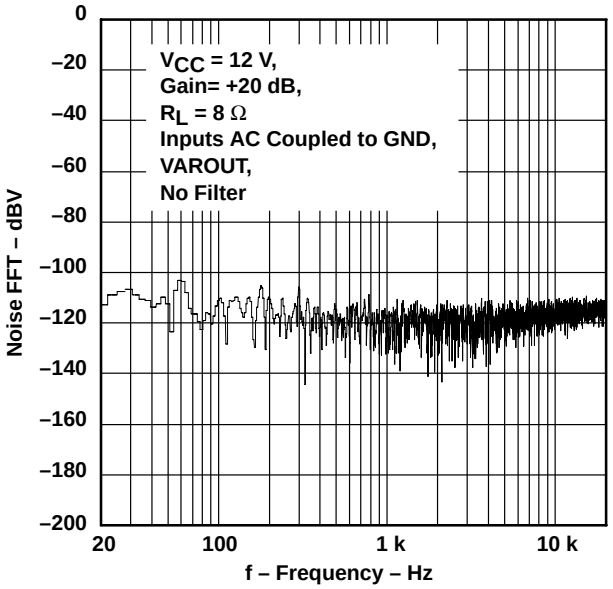


Figure 27

CLOSED LOOP RESPONSE

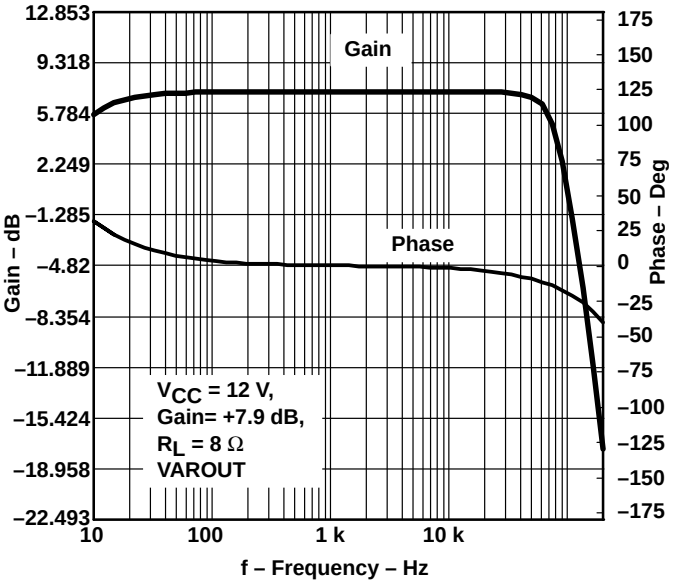


Figure 28

TYPICAL CHARACTERISTICS

COMMON-MODE REJECTION RATIO vs FREQUENCY

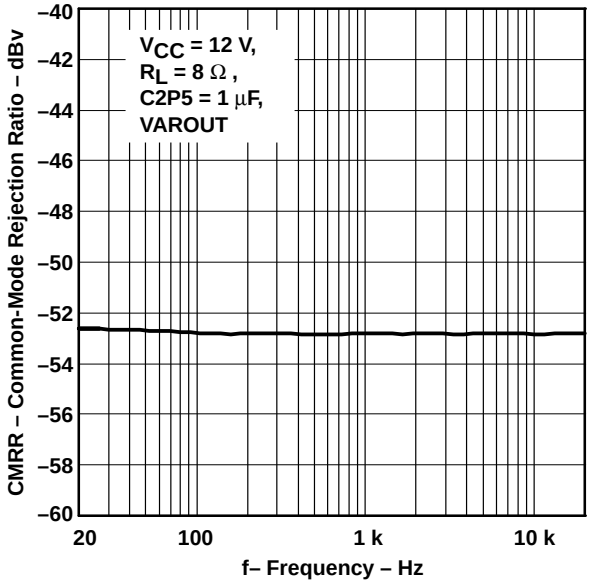


Figure 29

CROSSTALK (VAROUTL-TO-VAROUTR) vs FREQUENCY

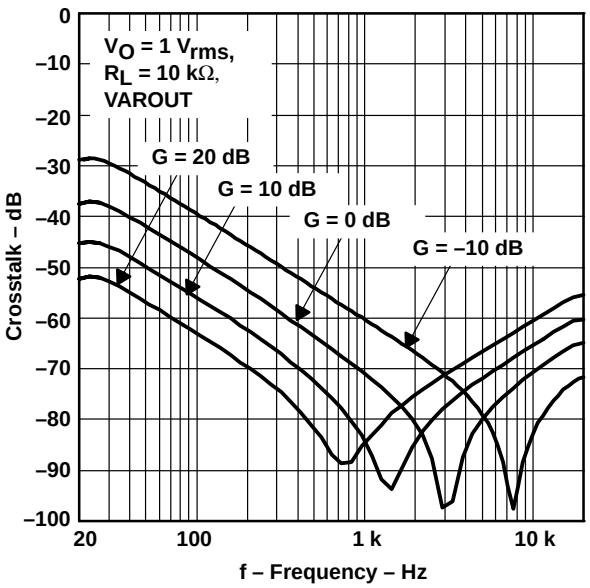


Figure 30

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

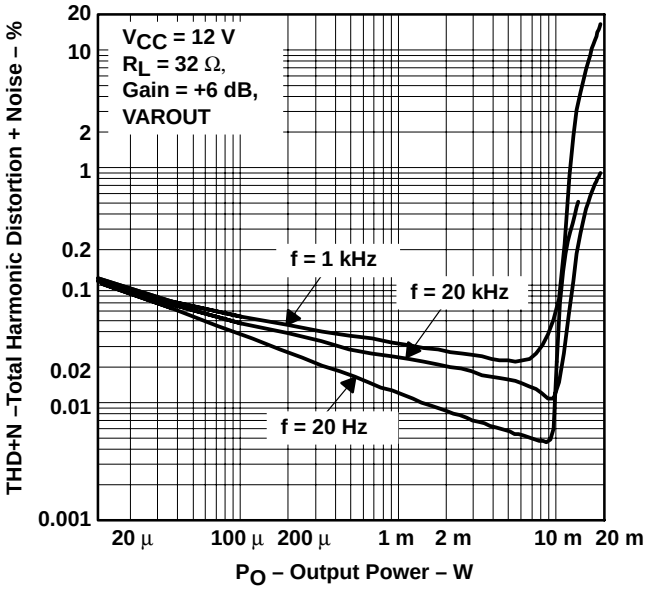


Figure 31

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT VOLTAGE

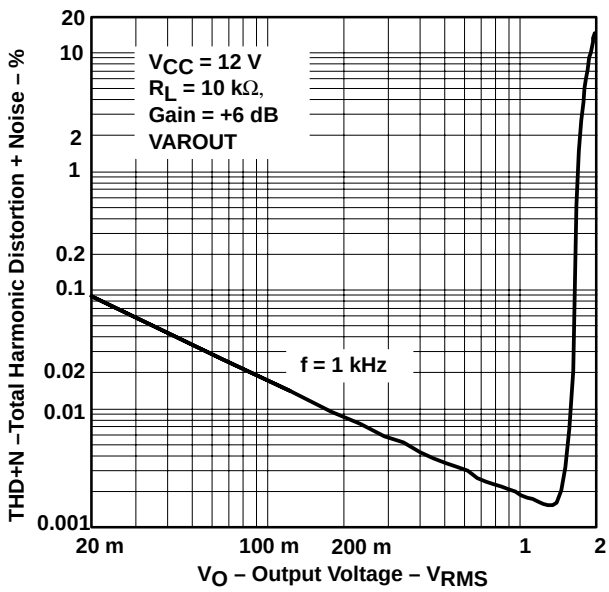


Figure 32

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

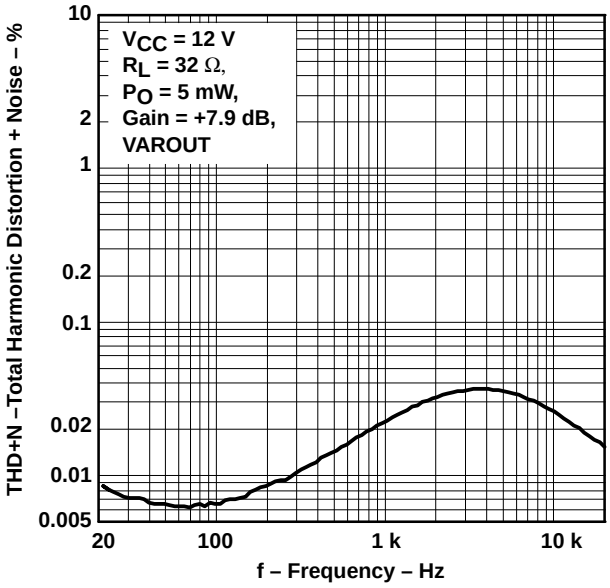


Figure 33

SUPPLY RIPPLE REJECTION RATIO vs FREQUENCY

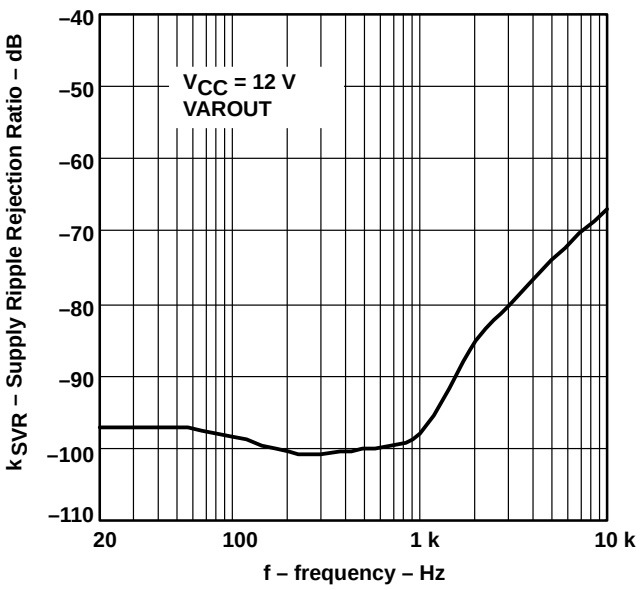


Figure 34

APPLICATION INFORMATION

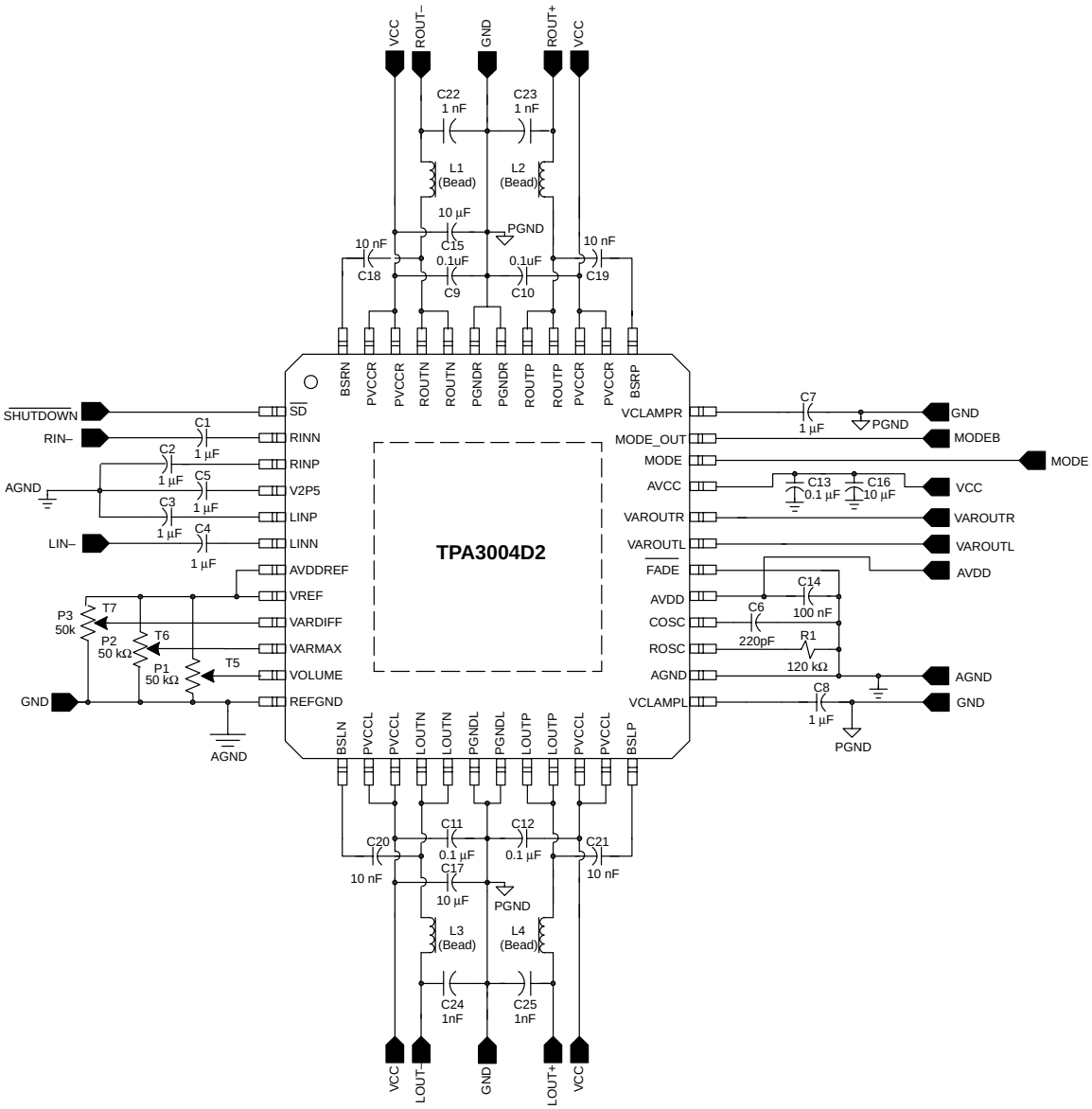


Figure 35. Stereo Class-D With Single-Ended Inputs

APPLICATION INFORMATION

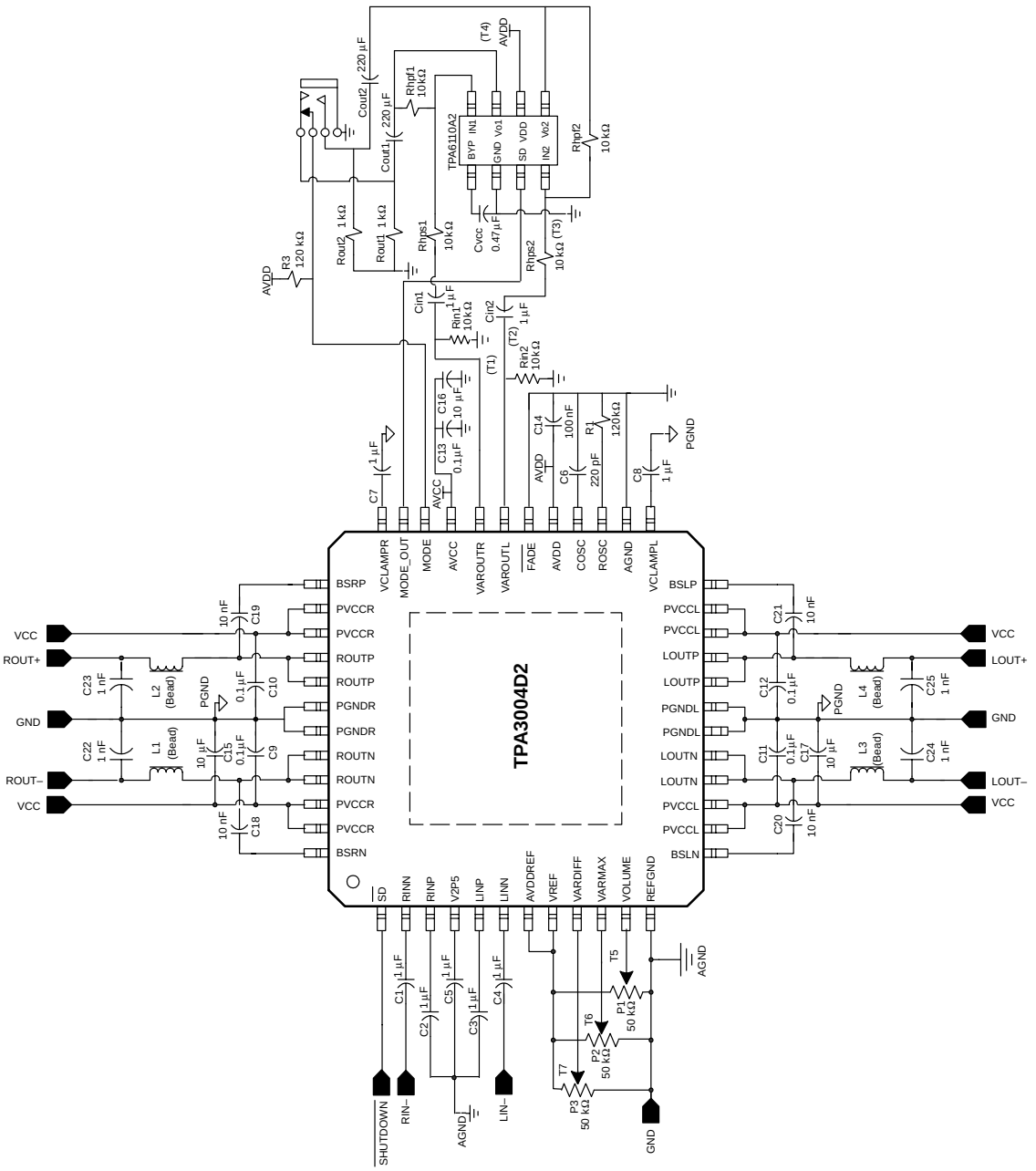


Figure 36. Stereo Class-D With Single-Ended Inputs and Stereo Headphone Amplifier Interface

APPLICATION INFORMATION

class-D operation

This section focuses on the class-D operation of the TPA3004D2.

traditional class-D modulation scheme

The traditional class-D modulation scheme, which is used in the TPA032D0x family, has a differential output where each output is 180 degrees out of phase and changes from ground to the supply voltage, V_{CC}. Therefore, the differential prefiltered output varies between positive and negative V_{CC}, where filtered 50% duty cycle yields 0 V across the load. The traditional class-D modulation scheme with voltage and current waveforms is shown in Figure 37. Note that even at an average of 0 V across the load (50% duty cycle), the current to the load is high, causing high loss, thus causing a high supply current.

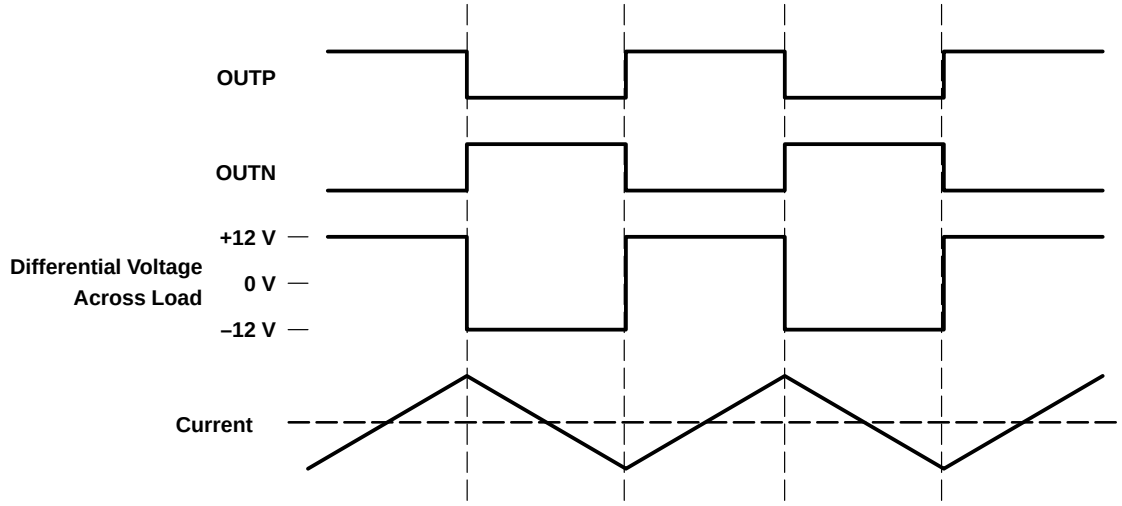


Figure 37. Traditional Class-D Modulation Scheme's Output Voltage and Current Waveforms Into an Inductive Load With No Input

TPA3004D2 modulation scheme

The TPA3004D2 uses a modulation scheme that still has each output switching from 0 to the supply voltage. However, OUTP and OUTN are now in phase with each other with no input. The duty cycle of OUTP is greater than 50% and OUTN is less than 50% for positive output voltages. The duty cycle of OUTP is less than 50% and OUTN is greater than 50% for negative output voltages. The voltage across the load sits at 0 V throughout most of the switching period, greatly reducing the switching current, which reduces any I^2R losses in the load.

APPLICATION INFORMATION

TPA3004D2 modulation scheme (continued)

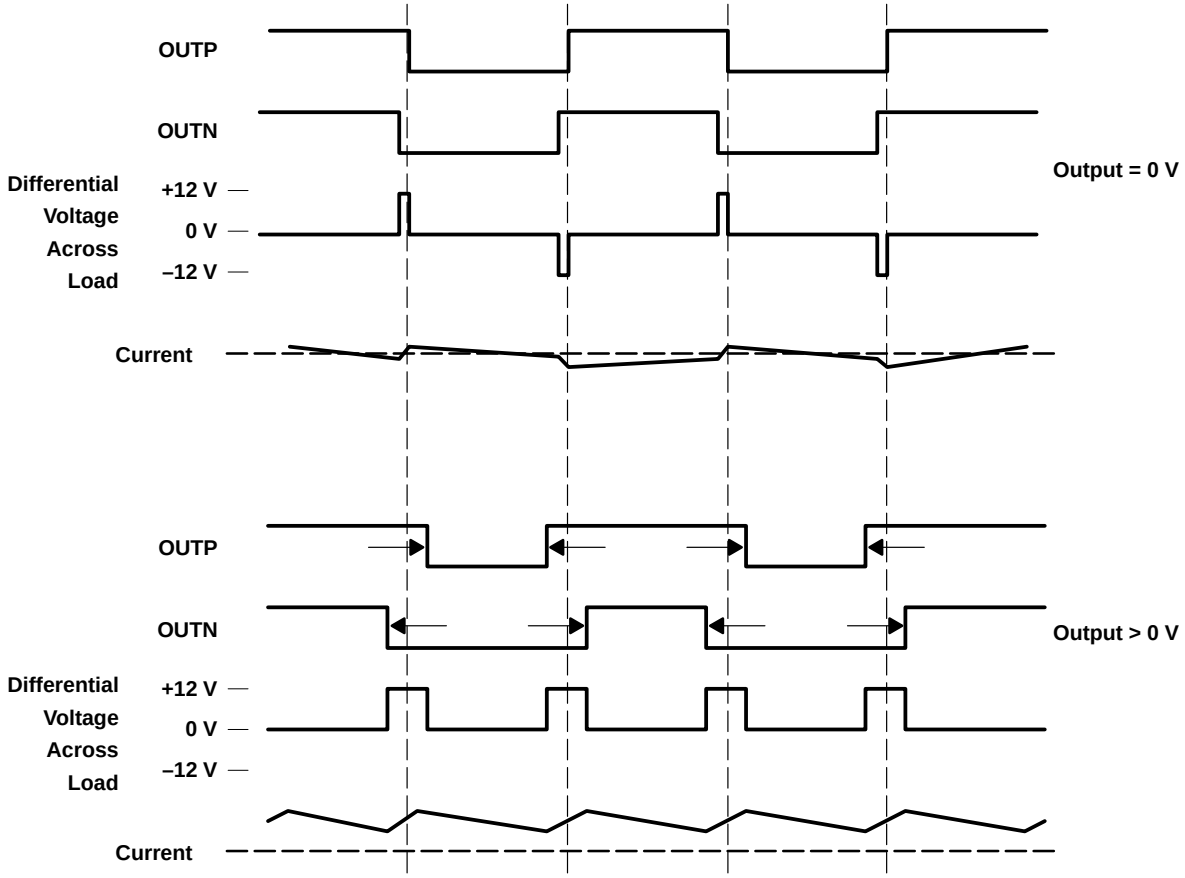


Figure 38. The TPA3004D2 Output Voltage and Current Waveforms Into an Inductive Load

efficiency: LC filter required with the traditional class-D modulation scheme

The main reason that the traditional class-D amplifier needs an output filter is that the switching waveform results in maximum current flow. This causes more loss in the load, which causes lower efficiency. The ripple current is large for the traditional modulation scheme, because the ripple current is proportional to voltage multiplied by the time at that voltage. The differential voltage swing is $2 \times V_{CC}$, and the time at each voltage is half the period for the traditional modulation scheme. An ideal LC filter is needed to store the ripple current from each half cycle for the next half cycle, while any resistance causes power dissipation. The speaker is both resistive and reactive, whereas an LC filter is almost purely reactive.

The TPA3004D2 modulation scheme has very little loss in the load without a filter because the pulses are very short and the change in voltage is V_{CC} instead of $2 \times V_{CC}$. As the output power increases, the pulses widen, making the ripple current larger. Ripple current could be filtered with an LC filter for increased efficiency, but for most applications the filter is not needed.

An LC filter with a cutoff frequency less than the class-D switching frequency allows the switching current to flow through the filter instead of the load. The filter has less resistance than the speaker, which results in less power dissipation, therefore increasing efficiency.

APPLICATION INFORMATION

effects of applying a square wave into a speaker

Audio specialists have advised for years not to apply a square wave to speakers. If the amplitude of the waveform is high enough and the frequency of the square wave is within the bandwidth of the speaker, the square wave could cause the voice coil to jump out of the air gap and/or scar the voice coil. A 250-kHz switching frequency, however, does not significantly move the voice coil, as the cone movement is proportional to $1/f^2$ for frequencies beyond the audio band.

Damage may occur if the voice coil cannot handle the additional heat generated from the high-frequency switching current. The amount of power dissipated in the speaker may be estimated by first considering the overall efficiency of the system. If the on-resistance ($r_{ds(on)}$) of the output transistors is considered to cause the dominant loss in the system, then the maximum theoretical efficiency for the TPA3004D2 with an 8-Ω load is as follows:

$$\text{Efficiency (theoretical, \%)} = R_L / \left(R_L + r_{ds(on)} \right) \times 100\% = 8/(8 + 0.58) \times 100\% = 93.24\% \quad (1)$$

The maximum measured output power is approximately 7.5 W with an 12-V power supply. The total theoretical power supplied ($P_{(total)}$) for this worst-case condition would therefore be as follows:

$$P_{(total)} = P_O / \text{Efficiency} = 7.5 \text{ W} / 0.9324 = 8.04 \text{ W} \quad (2)$$

The efficiency measured in the lab using an 8-Ω speaker was 89%. The power not accounted for as dissipated across the $r_{ds(on)}$ may be calculated by simply subtracting the theoretical power from the measured power:

$$\text{Other losses} = P_{(total)}\text{(measured)} - P_{(total)}\text{ (theoretical)} = 8.43 - 8.04 = 0.387 \text{ W} \quad (3)$$

The quiescent supply current at 14 V is measured to be 14.3 mA. It can be assumed that the quiescent current encapsulates all remaining losses in the device, i.e., biasing and switching losses. It may be assumed that any remaining power is dissipated in the speaker and is calculated as follows:

$$P_{(dis)} = 0.387 \text{ W} - (14 \text{ V} \times 14.3 \text{ mA}) = 0.19 \text{ W} \quad (4)$$

Note that these calculations are for the worst-case condition of 7.5 W delivered to the speaker. Since the 0.19 W is only 2.5% of the power delivered to the speaker, it may be concluded that the amount of power actually dissipated in the speaker is relatively insignificant. Furthermore, this power dissipated is well within the specifications of most loudspeaker drivers in a system, as the power rating is typically selected to handle the power generated from a clipping waveform.

when to use an output filter

Design the TPA3004D2 without the filter if the traces from amplifier to speaker are short (< 1 inch). Powered speakers, where the speaker is in the same enclosure as the amplifier, is a typical application for class-D without a filter.

Most applications require a ferrite bead filter. The ferrite filter reduces EMI around 1 MHz and higher (FCC and CE only test radiated emissions greater than 30 MHz). When selecting a ferrite bead, choose one with high impedance at high frequencies, but very low impedance at low frequencies.

Use a LC output filter if there are low frequency (<1 MHz) EMI sensitive circuits and/or there are long wires from the amplifier to the speaker.

APPLICATION INFORMATION

when to use an output filter (continued)

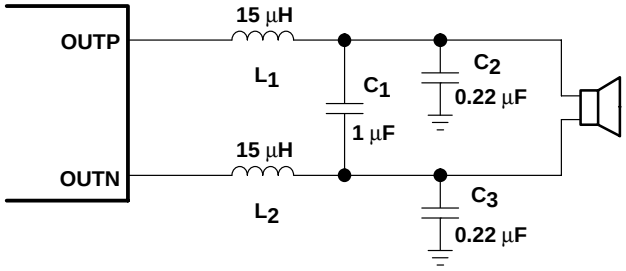


Figure 39. Typical LC Output Filter, Cutoff Frequency of 41 kHz, Speaker Impedance = 4 Ω

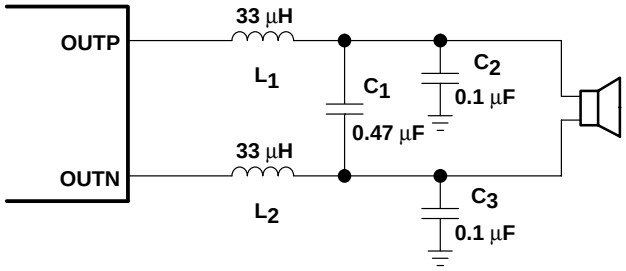


Figure 40. Typical LC Output Filter, Cutoff Frequency of 41 kHz, Speaker Impedance = 8 Ω

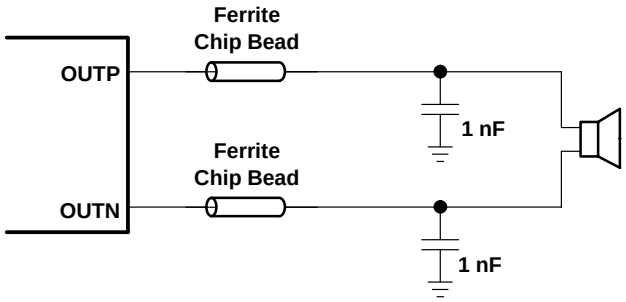


Figure 41. Typical Ferrite Chip Bead Filter (Chip bead example: Fair-Rite 2512067007Y3)

volume control operation

Three pins labeled VOLUME, VARDIFF, and VARMAX control the class-D volume when driving speakers and the VAROUT volume. All of these pins are controlled with a dc voltage, which should not exceed VREF.

When driving speakers in class-D mode, the VOLUME pin is the only pin that controls the gain. Table 1 lists the gain in class-D mode as determined by the voltage on the VOLUME pin in reference to the voltage on VREF.

If using a resistor divider to fix the gain of the amplifier, the VREF terminal can be directly connected to AVDDREF and a resistor divider can be connected across VREF and REFGND. (See Figure 35 in the Application Information section). For fixed gain, calculate the resistor divider values necessary to center the voltage between the two percentage points given in the first column of Table 1. For example, if a gain of 10.7 dB is desired, the resistors in the divider network can both be 10 kΩ. With these resistor values, a voltage of 50%*VREF will be present at the VOLUME pin and result in a class-D gain of 10.7 dB.

APPLICATION INFORMATION

volume control operation (continued)

If using a DAC to control the class-D gain, VREF and REFGND should be connected to the reference voltage for the DAC and the GND terminal of the DAC, respectively. For the DAC application, AVDDREF would be left unconnected. The reference voltage of the DAC provides the reference to the internal gain circuitry through the VREF input and any fluctuations in the DAC output voltage will not affect the TPA3004D2 gain. The percentages in the first column of Table 1 should be used for setting the voltages of the DAC when the voltage on the VOLUME terminal is increased. The percentages in the second column should be used for the DAC voltages when decreasing the voltage on the VOLUME terminal. Two lookup tables should be used in software to control the gain based on an increase or decrease in the desired system volume. This is explained further in a section below.

If using an analog potentiometer to control the gain, it should be connected between VREF and REFGND. VREF can be connected to AVDDREF or an external voltage source, if desired. The first and second column in Table 1 should be used to determine the point at which the gain changes depending on the direction that the potentiometer is turned. If the voltage on the center tap of the potentiometer is increasing, the first column in Table 1 should be referenced to determine the trip points. If the voltage is decreasing, the trip points in the second column should be referenced.

The trip point, where the gain actually changes, is different depending on whether the voltage on the VOLUME terminal is increasing or decreasing as a result of hysteresis about each trip point. The hysteresis ensures that the gain control is monotonic and does not oscillate from one gain step to another. A pictorial representation of the volume control can be found in Figure 43. The graph focuses on three gain steps with the trip points defined in the first and second columns of Table 1 for class–D gain. The dotted lines represent the hysteresis about each gain step.

The timing of the volume control circuitry is controlled by an internal 60 Hz clock. This clock determines the rate at which the gain changes when adjusting the voltage on the external volume control pins. The gain updates every 4 clock cycles (nominally 67 ms based on a 60 Hz clock) to the next step until the final desired gain is reached. For example, if the TPA3004D2 is currently in the +0.53 db class-D gain step and the VOLUME pin is adjusted for maximum gain at +36 dB, the time required for the gain to reach 36dB is 14 steps x 67ms/step = 0.938 seconds. Referencing table 1, there are 14 steps between the +0.53 dB gain step and the maximum gain step of +36 dB.

VARDIFF and VARMAX operation

The TPA3004D2 allows the user to specify a difference between the class–D gain and VAROUT gain. This is desirable to avoid any listening discomfort when plugging in headphones. When interfacing with the variable outputs, the VARDIFF and VARMAX pins control the VAROUT channel gain proportional to the gain set by the voltage on the VOLUME pin. When VARDIFF=0 V, the difference between the class–D gain and the VAROUT gain is 16 dB. As the voltage on the VARDIFF terminal is increased, the VAROUT channel gain decreases. Internal to the TPA3004D2 device, the voltage on the VARDIFF terminal is subtracted from the voltage on the VOLUME terminal and this value is used to determine the VAROUT gain.

Some audio systems require that the gain be limited in the VAROUT mode to a level that is comfortable for headphone listening. The VARMAX terminal controls the maximum gain for the VAROUT channels.

The functionality of the VARDIFF and VARMAX pin are combined to fix the VAROUT channel gain. A block diagram of the combined functionality is shown in Figure 42. The value obtained from the block diagram for VAROUT_VOLUME is a DC voltage that can be used in conjunction with Table 2 to determine the VAROUT channel gain. Table 2 lists the gain in VAROUT mode as determined by the VAROUT_VOLUME voltage in reference to the voltage on VREF.

APPLICATION INFORMATION

VARDIFF and VARMAX operation (continued)

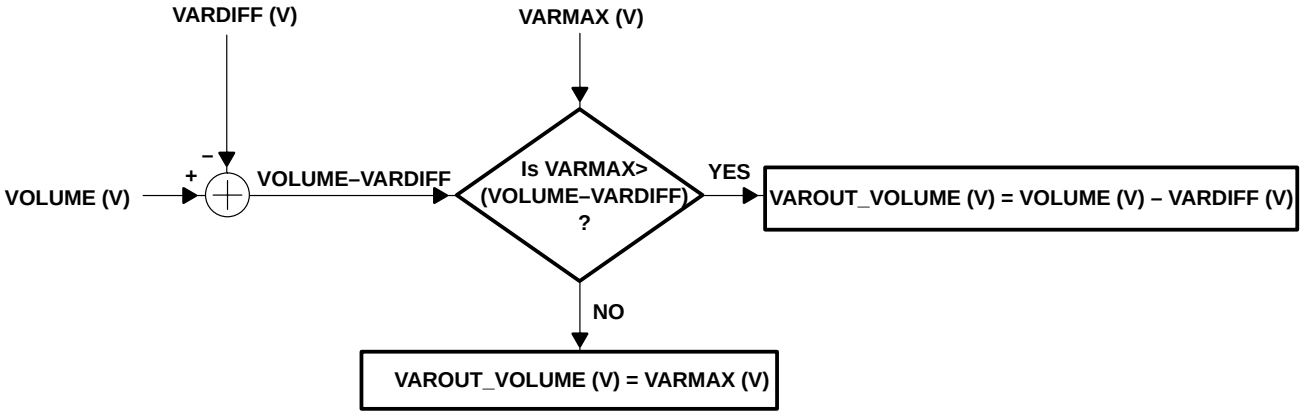


Figure 42. Block Diagram of VAROUT Volume Control

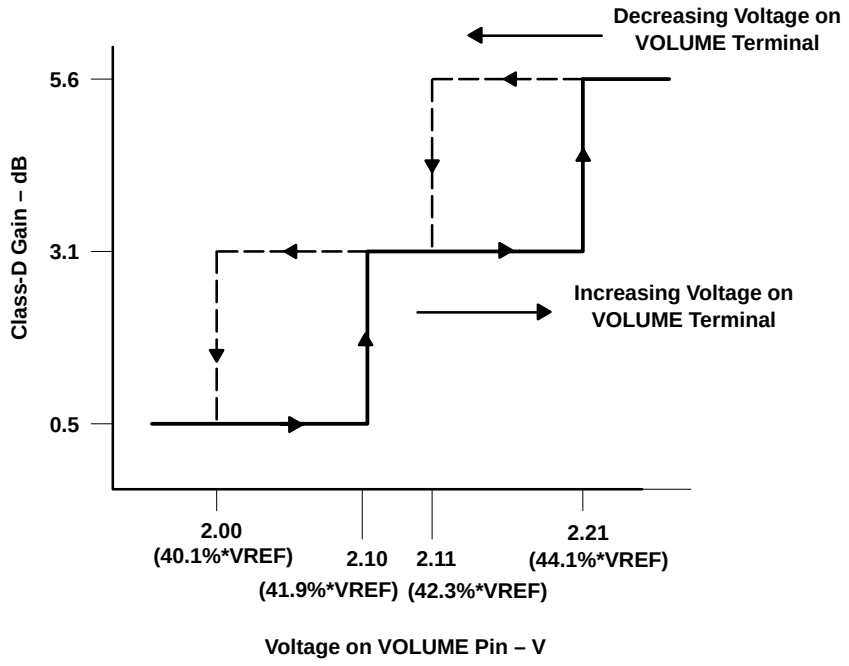


Figure 43. DC Volume Control Operation, VREF = 5 V

APPLICATION INFORMATION

MODE operation

The MODE pin is an input for controlling the output mode of the TPA3004D2. A logic HIGH on this pin disables the Class-D outputs. A logic LOW on this pin enables the class-D outputs. The VAROUT outputs are active in both modes and can be used as line level inputs to an external powered subwoofer while driving internal stereo speakers with the class-D outputs. The trip levels are defined in the specifications table.

For interfacing with an external headphone amplifier like the TPA6110A2, the MODE pin can be connected to the switch on a headphone jack. When configured like Figure 36, the class-D outputs will be disabled when a headphone plug is inserted into the headphone jack.

MODE_OUT operation

The MODE_OUT pin is an output for controlling the SHUTDOWN pin on an external headphone amplifier like the TPA6110A2 or for interfacing with other logic. The output voltages for a given load condition are given in the specifications table.

This output is controlled by the MODE pin logic. When the MODE input is driven to a logic low, the MODE_OUT output drives to a logic high. Conversely, when the MODE pin is driven to a logic high, the MODE_OUT output drives LOW. The MODE_OUT output is simply the inverted state of the MODE input.

It is designed in this manner because the TPA6110A2 SHUTDOWN input is active high. This allows the TPA3004D2 to place the TPA6110A2 into the shutdown state when driving internal speakers in the Class–D mode. Conversely, the MODE_OUT pin drives low to enable the TPA6110A2 headphone amplifier when headphones are plugged into the headphone jack and the MODE input is driven high.

$\overline{\text{FADE}}$ operation

The $\overline{\text{FADE}}$ terminal is a logic input that controls the operation of the volume control circuitry during transitions to and from the shutdown state and during power-up.

A logic low on this terminal, places the amplifier in the fade mode. During power-up or recovering from the shutdown state (a logic high is applied to the $\overline{\text{SD}}$ terminal), the volume is smoothly ramped up from the mute state, –75 dB, to the desired volume setting determined by the voltage on the volume control terminals. Conversely, the volume is smoothly ramped down from the current state to the mute state when a logic low is applied to the $\overline{\text{SD}}$ terminal. The timing of the volume control circuitry is controlled by an internal 60-Hz clock. This clock determines the rate at which the gain changes when adjusting the voltage on the external volume control pins. The gain updates every 4 clock cycles (nominally 67 ms based on a 60 Hz clock) to the next step until the final desired gain is reached. For example, if the TPA3004D2 is currently in the +0.53 db class-D gain step and the VOLUME pin is adjusted for maximum gain at +36 dB, the time required for the gain to reach 36 dB is 14 steps x 67 ms/step = 0.938 seconds. Referencing table 1, there are 14 steps between the +0.53 dB gain step and the maximum gain step of +36 dB.

Figure 44 shows a scope capture of the differential output (measured across OUT+ and OUT–) with the amplifier in the fade mode. A 1 V_{pp} dc voltage was applied across the differential inputs and a logic low was applied to the $\overline{\text{SD}}$ terminal at the time defined in the figure. The figure depicts the outputs transitioning from one gain step to the next lower step at approximately 67 ms/step.

A logic high on this pin disables the volume fade effect during transitions to and from the shutdown state and during power-up. During power-up or recovering from the shutdown state (a logic high is applied to the $\overline{\text{SD}}$ terminal), the transition from the mute state, –75 dB, to the desired volume setting is less than 1 ms. Conversely, the volume ramps down from current state to the mute state within 1 ms when a logic low is applied to the $\overline{\text{SD}}$ terminal.

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Figure 45 shows a scope capture of the differential output with the fade effect disabled. The outputs transition to the lowest gain state within 1ms of applying a logic low to the $\overline{SD}$ terminal.

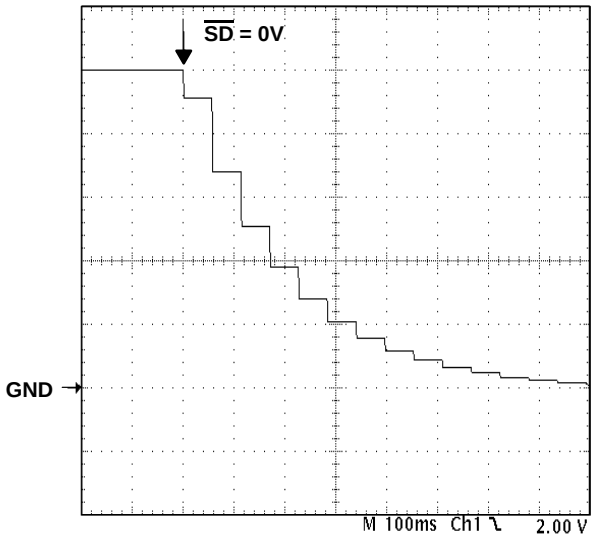


Figure 44. Differential Output With $\overline{FADE}$ (Terminal 30) Held Low

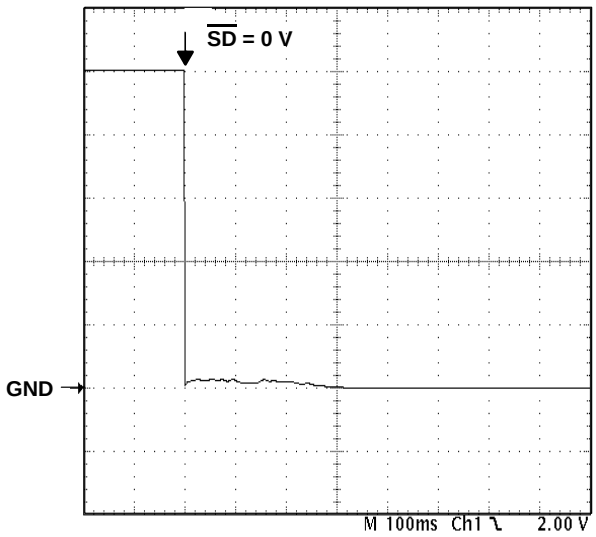


Figure 45. Differential Output With $\overline{FADE}$ Terminal Held High

APPLICATION INFORMATION

selection of COSC and ROSC

The switching frequency is determined using the values of the components connected to ROSC (pin 20) and COSC (pin 21) and may be calculated with the following equation:

$$f_{OSC} = 6.6 / (R_{OSC} * C_{OSC})$$

The frequency may be varied from 225 kHz to 275 kHz by adjusting the values chosen for R_{OSC} and C_{OSC}. The recommended values are C_{OSC} = 220 pF, R_{OSC}=120 kΩ for a switching frequency of 250 kHz.

internal 2.5-V bias generator capacitor selection

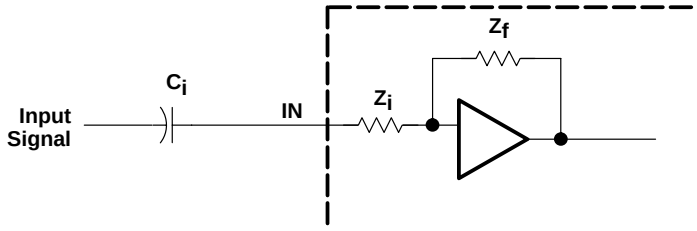
The internal 2.5-V bias generator (V2P5) provides the internal bias for the preamplifier stages on both the class-D amplifiers and the variable amplifiers. The external input capacitors and this internal reference allow the inputs to be biased within the optimal common-mode range of the input preamplifiers.

The selection of the capacitor value on the V2P5 terminal is critical for achieving the best device performance. During startup or recovery from the shutdown state, the V2P5 capacitor determines the rate at which the amplifier starts up. When the voltage on the V2P5 capacitor equals 0.75xV2P5, or 75% of its final value, the device turns on and the class-D outputs start switching. The startup time is not critical for the best depop performance since any pop sound that is heard is the result of the class-D outputs switching on and not the startup time. However, at least a 0.47-μF capacitor is recommended for the V2P5 capacitor.

A secondary function of the V2P5 capacitor is to filter high frequency noise on the internal 2.5-V bias generator.

input resistance

Each gain setting is achieved by varying the input resistance of the amplifier, which can range from its smallest value to over six times that value. As a result, if a single capacitor is used in the input high-pass filter, the –3 dB or cutoff frequency also changes by over six times.



The –3-dB frequency can be calculated using equation 5. Input impedance (Z_i) vs Gain can be found in Figure 7.

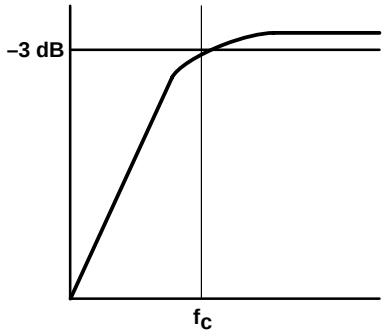
$$f_{-3dB} = \frac{1}{2\pi Z_i C_i} \quad (5)$$

APPLICATION INFORMATION

input capacitor, C_i

In the typical application an input capacitor (C_i) is required to allow the amplifier to bias the input signal to the proper dc level (V2P5)for optimum operation. In this case, C_i and the input impedance of the amplifier (Z_i) form a high-pass filter with the corner frequency determined in equation 6.

$$f_c = \frac{1}{2\pi Z_i C_i} \quad (6)$$



The value of C_i is important, as it directly affects the bass (low frequency) performance of the circuit. Consider the example where Z_i is 20 kΩ and the specification calls for a flat bass response down to 20 Hz. Equation 6 is reconfigured as equation 7.

$$C_i = \frac{1}{2\pi Z_i f_c} \quad (7)$$

In this example, C_i is 0.4 μF, so one would likely choose a value in the range of 0.47 μF to 1 μF. If the gain is known and will be constant, use Z_i from Figure 7 (Input Impedance vs Gain) to calculate C_i. Calculations for C_i should be based off the impedance at the lowest gain step intended for use in the system. A further consideration for this capacitor is the leakage path from the input source through the input network (C_i) and the feedback network to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at 2.5 V, which is likely higher than the source dc level. Note that it is important to confirm the capacitor polarity in the application.

power supply decoupling, C_S

The TPA3004D2 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 μF placed as close as possible to the device V_{CC} lead works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 μF or greater placed near the audio power amplifier is recommended. The 10-μF capacitor also serves as local storage capacitor for supplying current during large signal transients on the amplifier outputs.

BSN and BSP capacitors

The full H-bridge output stages use only NMOS transistors. They therefore require bootstrap capacitors for the high side of each output to turn on correctly. A 10-nF ceramic capacitor, rated for at least 25 V, must be connected from each output to its corresponding bootstrap input. Specifically, one 10-nF capacitor must be connected from xOUTP to xBSP, and one 10-nF capacitor must be connected from xOUTN to xBSN. (See the application circuit diagram in Figure 35.)

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VCLAMP capacitors

To ensure that the maximum gate-to-source voltage for the NMOS output transistors is not exceeded, two internal regulators clamp the gate voltage. Two 1-µF capacitors must be connected from VCLAMPL (pin 25) and VCLAMPR (pin 36) to ground and must be rated for at least 25 V. The voltages at the VCLAMP terminals vary with V_{CC} and may not be used for powering any other circuitry.

internal regulated 5-V supply (AV_{DD})

The AV_{DD} terminal (pin 29) is the output of an internally-generated 5-V supply, used for the oscillator, preamplifier, and volume control circuitry. It requires a 0.1-µF to 1-µF capacitor, placed very close to the pin, to ground to keep the regulator stable. The regulator may be used to power an external headphone amplifier or other circuitry, up to a current limit specified in the specification table.

AV_{DD} – POWER-UP RESPONSE

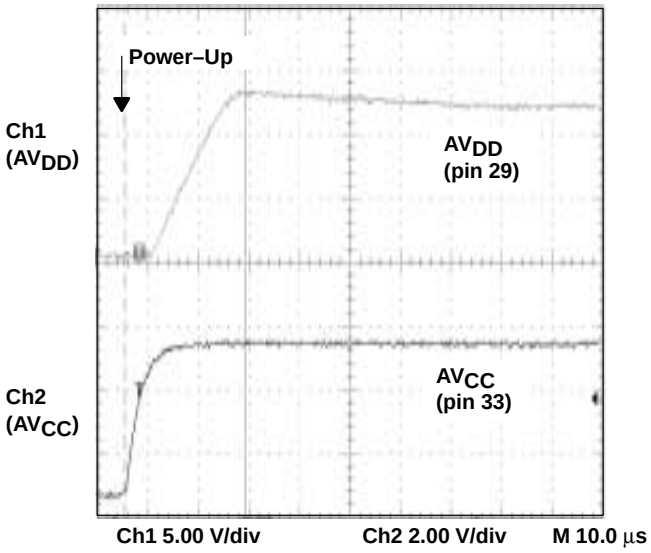


Figure 46. Power-Up Response

differential input

The differential input stage of the amplifier cancels any noise that appears on both input lines of the channel. To use the TPA3004D2 EVM with a differential source, connect the positive lead of the audio source to the INP input and the negative lead from the audio source to the INN input. To use the TPA3004D2 with a single-ended source, ac ground the INP input through a capacitor equal in value to the input capacitor on INN and apply the audio source to the INN input. In a single-ended input application, the INP input should be ac-grounded at the audio source instead of at the device input for best noise performance.

$\overline{SD}$ operation

The TPA3004D2 employs a shutdown mode of operation designed to reduce supply current (I_{CC}) to the absolute minimum level during periods of nonuse for power conservation. The $\overline{SD}$ input terminal should be held high (see specification table for trip point)during normal operation when the amplifier is in use. Pulling $\overline{SD}$ low causes the outputs to mute and the amplifier to enter a low-current state, $I_{CC(SD)}$ = 10 µA. $\overline{SD}$ should never be left unconnected, because amplifier operation would be unpredictable.

For the best power-off pop performance, the amplifier should be placed in the shutdown mode prior to removing the power supply voltage.

APPLICATION INFORMATION

using low-ESR capacitors

Low-ESR capacitors are recommended throughout this application section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves like an ideal capacitor.

short-circuit protection

The TPA3004D2 has short circuit protection circuitry on the outputs that prevents damage to the device during output-to-output shorts, output-to-GND shorts, and output-to-V_{CC} shorts. When a short-circuit is detected on the outputs, the part immediately disables the output drive. This is a latched fault and must be reset by cycling the voltage on the $\overline{SD}$ pin to a logic low and back to the logic high state for normal operation. This will clear the short-circuit flag and allow for normal operation if the short was removed. If the short was not removed, the protection circuitry will again activate. The trip-point for the short-circuit protection is nominally set at 8 A.

thermal protection

Thermal protection on the TPA3004D2 prevents damage to the device when the internal die temperature exceeds 150°C. There is a ±15 degree tolerance on this trip point from device to device. Once the die temperature exceeds the thermal set point, the device enters into the shutdown state and the outputs are disabled. This is not a latched fault. The thermal fault is cleared once the temperature of the die is reduced by 20°C. The device begins normal operation at this point with no external system interaction.

thermal considerations: output power and maximum ambient temperature

To calculate the maximum ambient temperature, the following equation may be used:

$$T_{Amax} = T_J - \Theta_{JA} P_{Dissipated}$$

where: $T_J = 125°C$

$\Theta_{JA} = 19°C/W$ (2-Layer PCB, 5 sq. in. copper, see Figure 47) (8)

(The derating factor for the 48-pin PHP package is given in the dissipation rating table.)

To estimate the power dissipation, the following equation may be used:

$$P_{Dissipated} = P_{O(average)} \times ((1 / Efficiency) - 1)$$

Efficiency = ~85% for an 8-Ω load

= ~75% for a 4-Ω load (9)

Example. What is the maximum ambient temperature for an application that requires the TPA3004D2 to drive 10 W into an 8-Ω speaker (stereo)?

$P_{Dissipated} = 20 W \times ((1 / 0.85) - 1) = 3.5 W$ ($P_O = 10 W * 2$)

$T_{Amax} = 125°C - (19°C/W \times 3.5 W) = 58.5°C$

APPLICATION INFORMATION

thermal considerations: output power and maximum ambient temperature (continued)

This calculation shows that the TPA3004D2 can drive 10 W of continuous RMS power per channel into an 8-Ω speaker up an ambient temperature of 58.5°C.

Figures 47 and 48 show the results of several thermal experiments conducted with the TPA3004D2. Both figures show that the best thermal performance can be achieved with more copper area for heat dissipation and an adequate number of thermal vias.

Figure 47 shows two curves for a 2–layer and 4–layer PCB. The 2–layer PCB layout was tightly controlled with a fixed amount of 2 oz. copper on the bottom layer of the PCB. The amount of copper is shown on the x–axis. Nine thermal vias of 13 mil (0.33mm) diameter were drilled under the PowerPad and connected to the bottom layer. The top layer only consisted of traces for signal routing.

The 4–layer PCB layout was also tightly controlled with a fixed amount of 2 oz. copper in middle GND layer. The top layer only consisted of traces for signal routing. The bottom and other middle layer were left blank. Nine thermal vias of 0.33mm diameter were drilled under the PowerPad and connected to the middle layer.

Figure 48 shows the effect of the number of thermal vias drilled under the PowerPad on the thermal performance of the PCB. The experiment was conducted with a 2–layer PCB and 3 square inches of copper on the bottom layer. For the best thermal performance, at least 16 vias in a 4x4 pattern should be used under the PowerPad. Refer to the TPA3004D2 EVM User's Manual, SLOU115, for an example layout with a 4x4 via pattern. PCB gerber files are available at request.

printed circuit board (PCB) layout

Because the TPA3004D2 is a class-D amplifier that switches at a high frequency, the layout of the printed circuit board (PCB) should be optimized according to the following guidelines for the best possible performance.

- Decoupling capacitors — As described on page 31, the high-frequency 0.1-uF decoupling capacitors should be placed as close to the PVCC (pin 14, 15, 22, 23, 38, 39, 46, 47) and AV_{CC} (pin 33) terminals as possible. The V2P5 (pin 4) capacitor, AV_{DD} (pin 29) capacitor, and VCLAMP (pins 25, 36) capacitor should also be placed as close to the device as possible. Large (10 uF or greater) bulk power supply decoupling capacitors should be placed near the TPA3004D2 on the PVCCL, PVCCR, and AV_{CC} terminals.
- Grounding — The AV_{CC} (pin 33) decoupling capacitor, AV_{DD} (pin 29) capacitor, V2P5 (pin 4) capacitor, COSC (pin 28) capacitor, and ROSC (pin 27) resistor should each be grounded to analog ground (AGND, pin 26 and pin 30). The PVCC (pin 9 and pin 16) decoupling capacitors should each be grounded to power ground (PGND, pins 18, 19, 42, 43). Analog ground and power ground may be connected at the PowerPAD, which should be used as a central ground connection or star ground for the TPA3004D2. Basically, an island should be created with a single connection to PGND at the PowerPAD.
- Output filter — The ferrite EMI filter (Figure 41, page 25) should be placed as close to the output terminals as possible for the best EMI performance. The LC filter (Figure 40, page 25 should be placed close to the outputs. The capacitors used in both the ferrite and LC filters should be grounded to power ground.
- PowerPAD — The PowerPAD must be soldered to the PCB for proper thermal performance and optimal reliability. The dimensions of the PowerPAD thermal land should be 5 mm by 5 mm (197 mils by 197 mils). The PowerPAD size measures 4.55 x 4.55 mm. Four rows of solid vias (four vias per row, 0.3302 mm or 13 mils diameter) should be equally spaced underneath the thermal land. The vias should connect to a solid copper plane, either on an internal layer or on the bottom layer of the PCB. The vias must be solid vias, not thermal relief or webbed vias. For additional information, please refer to the *PowerPAD Thermally Enhanced Package* application note, TI literature number SLMA002.

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For an example layout, please refer to the TPA3004D2 Evaluation Module (TPA3004D2EVM) User Manual, TI literature number SLOU158. Both the EVM user manual and the PowerPAD application note are available on the TI web site at http://www.ti.com.

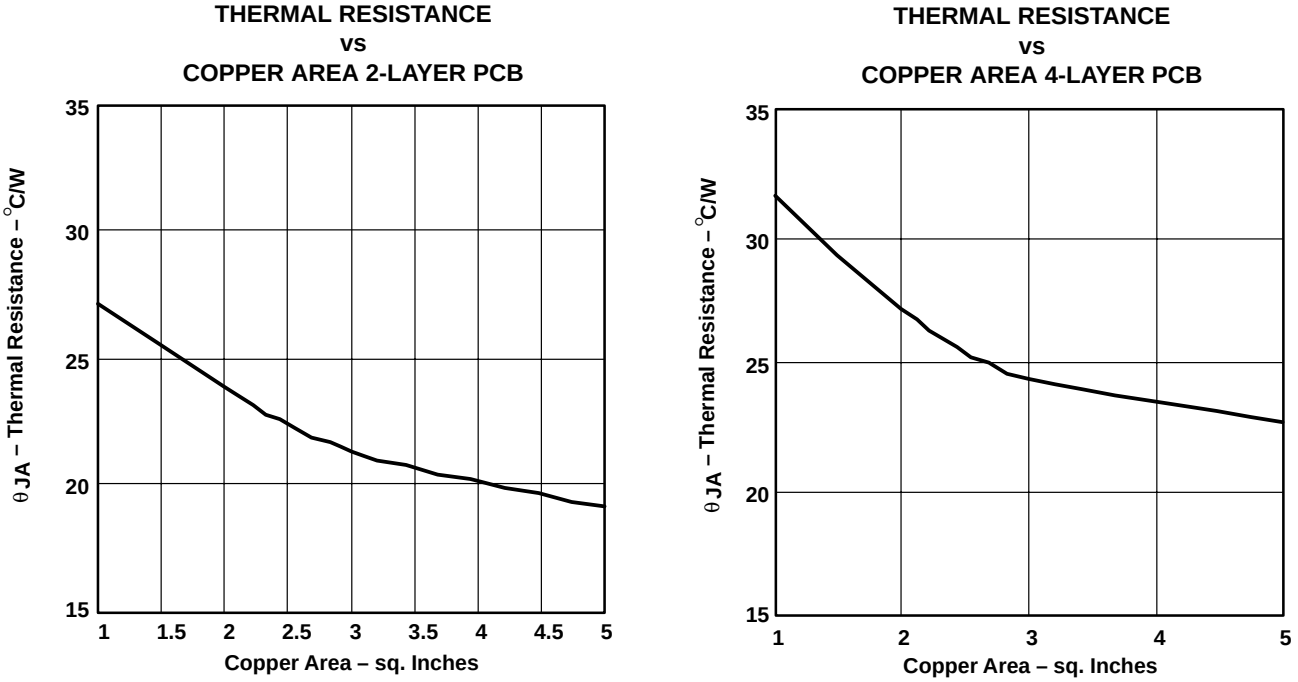


Figure 47. Thermal Resistance

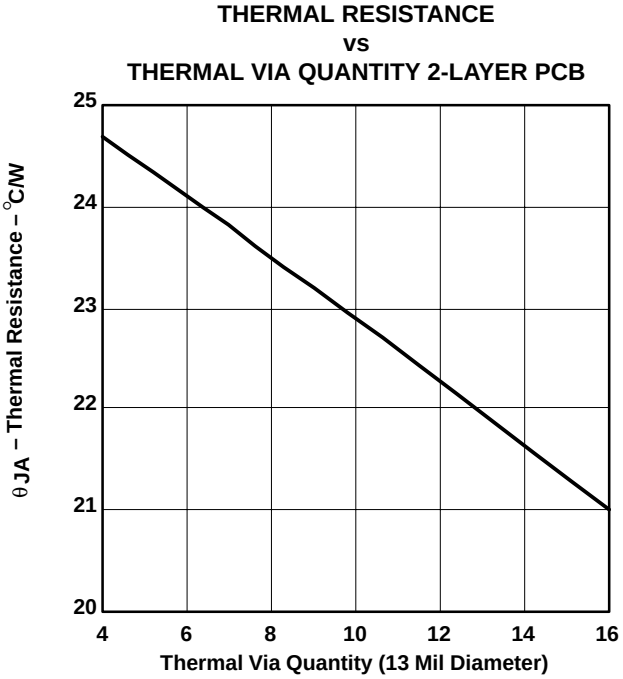


Figure 48. Thermal Resistance

APPLICATION INFORMATION

basic measurement system

This application note focuses on methods that use the basic equipment listed below:

- Audio analyzer or spectrum analyzer
- Digital multimeter (DMM)
- Oscilloscope
- Twisted pair wires
- Signal generator
- Power resistor(s)
- Linear regulated power supply
- Filter components
- EVM or other complete audio circuit

Figure 49 shows the block diagrams of basic measurement systems for class-AB and class-D amplifiers. A sine wave is normally used as the input signal since it consists of the fundamental frequency only (no other harmonics are present). An analyzer is then connected to the APA output to measure the voltage output. The analyzer must be capable of measuring the entire audio bandwidth. A regulated dc power supply is used to reduce the noise and distortion injected into the APA through the power pins. A System Two audio measurement system (AP-II) (Reference 1) by Audio Precision includes the signal generator and analyzer in one package.

The generator output and amplifier input must be ac-coupled. However, the EVMs already have the ac-coupling capacitors, (C_{IN}), so no additional coupling is required. The generator output impedance should be low to avoid attenuating the test signal, and is important since the input resistance of APAs is not very high (about 10 kΩ). Conversely the analyzer-input impedance should be high. The output impedance, R_{OUT}, of the APA is normally in the hundreds of milliohms and can be ignored for all but the power-related calculations.

Figure 49(a) shows a class-AB amplifier system, which is relatively simple because these amplifiers are linear their output signal is a linear representation of the input signal. They take analog signal input and produce analog signal output. These amplifier circuits can be directly connected to the AP-II or other analyzer input.

This is not true of the class-D amplifier system shown in Figure 49(b), which requires low pass filters in most cases in order to measure the audio output waveforms. This is because it takes an analog input signal and converts it into a pulse-width modulated (PWM) output signal that is not accurately processed by some analyzers.

APPLICATION INFORMATION

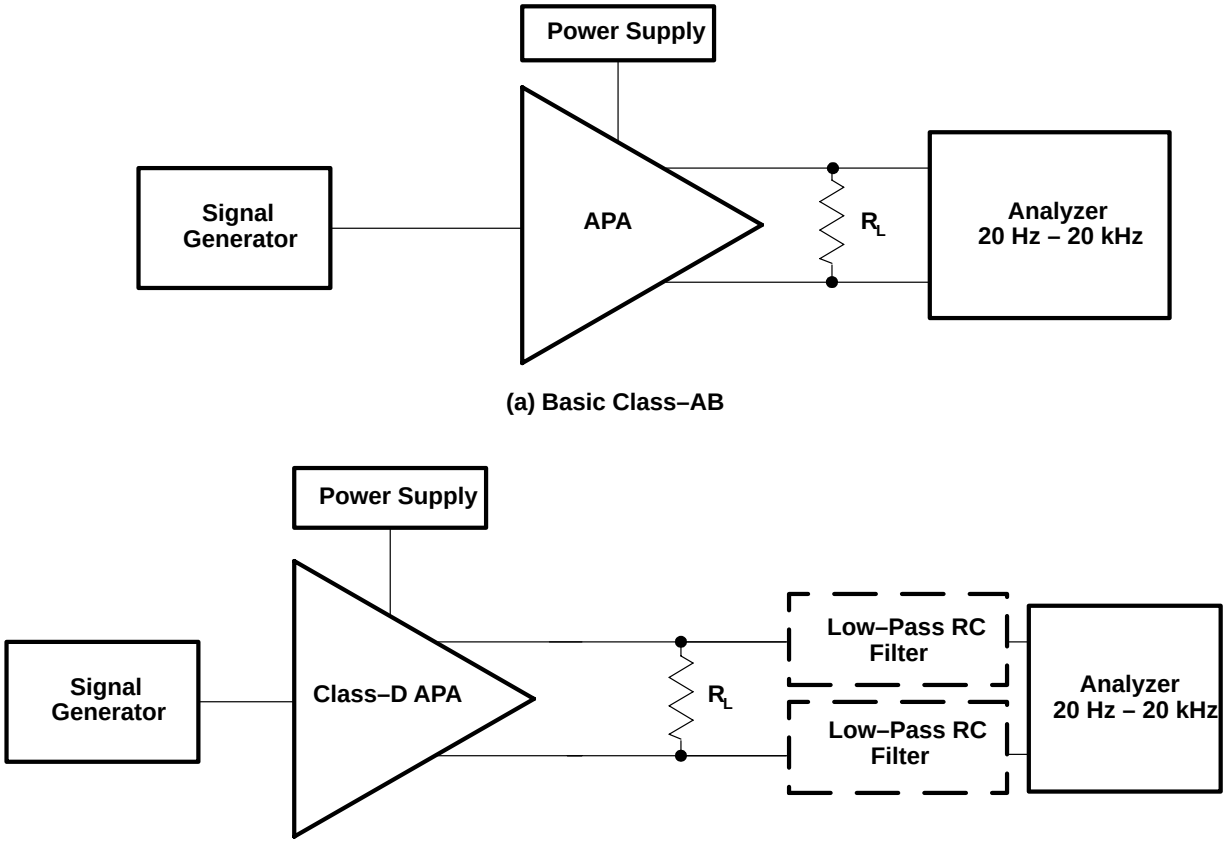


Figure 49. Audio Measurement Systems

The TPA3004D2 uses a modulation scheme that does not require an output filter for operation, but they do sometimes require an RC low-pass filter when making measurements. This is because some analyzer inputs cannot accurately process the rapidly changing square-wave output and therefore record an extremely high level of distortion. The RC low-pass measurement filter is used to remove the modulated waveforms so the analyzer can measure the output sine wave.

APPLICATION INFORMATION

differential input and BTL output

All of the class-D APAs and many class-AB APAs have differential inputs and bridge-tied load (BTL) outputs. Differential inputs have two input pins per channel and amplify the difference in voltage between the pins. Differential inputs reduce the common-mode noise and distortion of the input circuit. BTL is a term commonly used in audio to describe differential outputs. BTL outputs have two output pins providing voltages that are 180 degrees out of phase. The load is connected between these pins. This has the added benefits of quadrupling the output power to the load and eliminating a dc blocking capacitor.

A block diagram of the measurement circuit is shown in Figure 50. The differential input is a balanced input, meaning the positive (+) and negative (–) pins will have the same impedance to ground. Similarly, the BTL output equates to a balanced output.

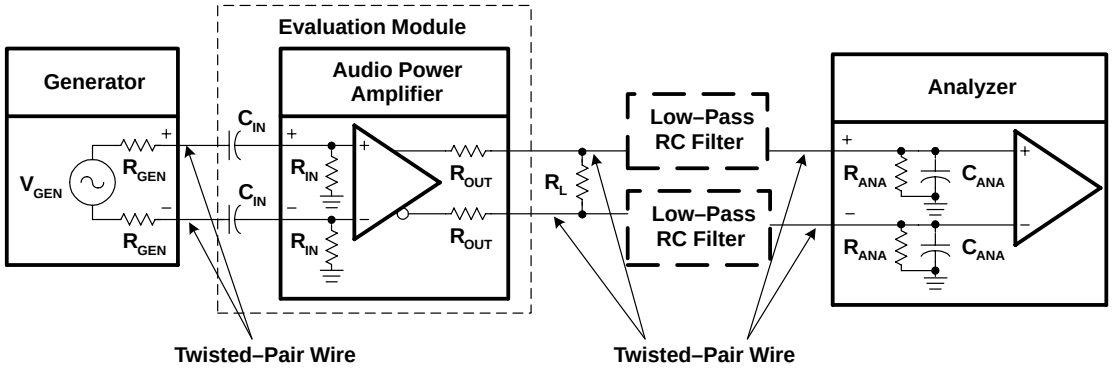


Figure 50. Differential Input—BTL output Measurement Circuit

The generator should have balanced outputs and the signal should be balanced for best results. An unbalanced output can be used, but it may create a ground loop that will affect the measurement accuracy. The analyzer must also have balanced inputs for the system to be fully balanced, thereby cancelling out any common mode noise in the circuit and providing the most accurate measurement.

The following general rules should be followed when connecting to APAs with differential inputs and BTL outputs:

- Use a balanced source to supply the input signal.
- Use an analyzer with balanced inputs.
- Use twisted-pair wire for all connections.
- Use shielding when the system environment is noisy.
- Ensure the cables from the power supply to the APA, and from the APA to the load, can handle the large currents (see Table 3).

Table 3 shows the recommended wire size for the power supply and load cables of the APA system. The real concern is the dc or ac power loss that occurs as the current flows through the cable. These recommendations are based on 12-inch long wire with a 20-kHz sine-wave signal at 25°C.

APPLICATION INFORMATION

Table 3. Recommended Minimum Wire Size for Power Cables

P_{OUT} (W)	R_L (Ω)	AWG SIZE		DC POWER LOSS (MW)		AC POWER LOSS (MW)	
10	4	18	22	16	40	18	42
2	4	18	22	3.2	8.0	3.7	8.5
1	8	22	28	2.0	8.0	2.1	8.1
< 0.75	8	22	28	1.5	6.1	1.6	6.2

Class-D RC low-pass filter

An RC filter is used to reduce the square-wave output when the analyzer inputs cannot process the pulse-width modulated class-D output waveform. This filter has little effect on the measurement accuracy because the cutoff frequency is set above the audio band. The high frequency of the square wave has negligible impact on measurement accuracy because it is well above the audible frequency range and the speaker cone cannot respond at such a fast rate. The RC filter is not required when an LC low-pass filter is used, such as with the class-D APAs that employ the traditional modulation scheme (TPA032D0x, TPA005Dxx).

The component values of the RC filter are selected using the equivalent output circuit as shown in Figure 51. R_L is the load impedance that the APA is driving for the test. The analyzer input impedance specifications should be available and substituted for R_{ANA} and C_{ANA}. The filter components, R_{FILT} and C_{FILT}, can then be derived for the system. The filter should be grounded to the APA near the output ground pins or at the power supply ground pin to minimize ground loops.

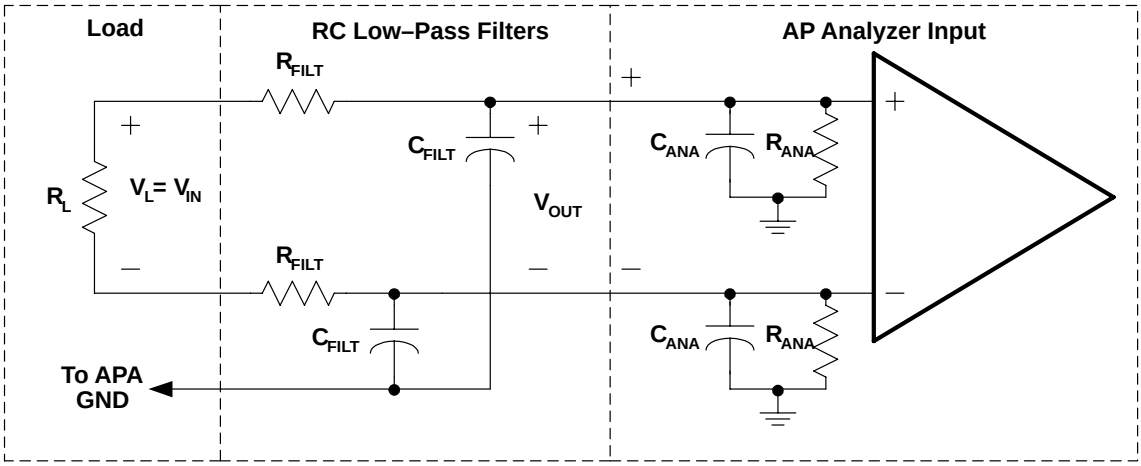


Figure 51. Measurement Low-Pass Filter Derivation Circuit—Class-D APAs

APPLICATION INFORMATION

The transfer function for this circuit is shown in equation (10) where $\omega_O = R_{EQ}C_{EQ}$, $R_{EQ} = R_{FILT} \| R_{ANA}$ and $C_{EQ} = (C_{FILT} + C_{ANA})$. The filter frequency should be set above f_{MAX}, the highest frequency of the measurement bandwidth, to avoid attenuating the audio signal. Equation (11) provides this cutoff frequency, f_C. The value of R_{FILT} must be chosen large enough to minimize current that is shunted from the load, yet small enough to minimize the attenuation of the analyzer-input voltage through the voltage divider formed by R_{FILT} and R_{ANA}. A rule of thumb is that R_{FILT} should be small (~100 Ω) for most measurements. This reduces the measurement error to less than 1% for $R_{ANA} \geq 10$ kΩ.

$$\left(\frac{V_{OUT}}{V_{IN}}\right) = \frac{\left(\frac{R_{ANA}}{R_{ANA} + R_{FILT}}\right)}{1 + j\left(\frac{\omega}{\omega_O}\right)} \tag{10}$$

$$f_C = \sqrt{2} \times f_{MAX} \tag{11}$$

An exception occurs with the efficiency measurements, where R_{FILT} must be increased by a factor of ten to reduce the current shunted through the filter. C_{FILT} must be decreased by a factor of ten to maintain the same cutoff frequency. See Table 2 for the recommended filter component values.

Once f_C is determined and R_{FILT} is selected, the filter capacitance is calculated using equation (11). When the calculated value is not available, it is better to choose a smaller capacitance value to keep f_C above the minimum desired value calculated in equation (12).

$$C_{FILT} = \frac{1}{2\pi \times f_C \times R_{FILT}} \tag{12}$$

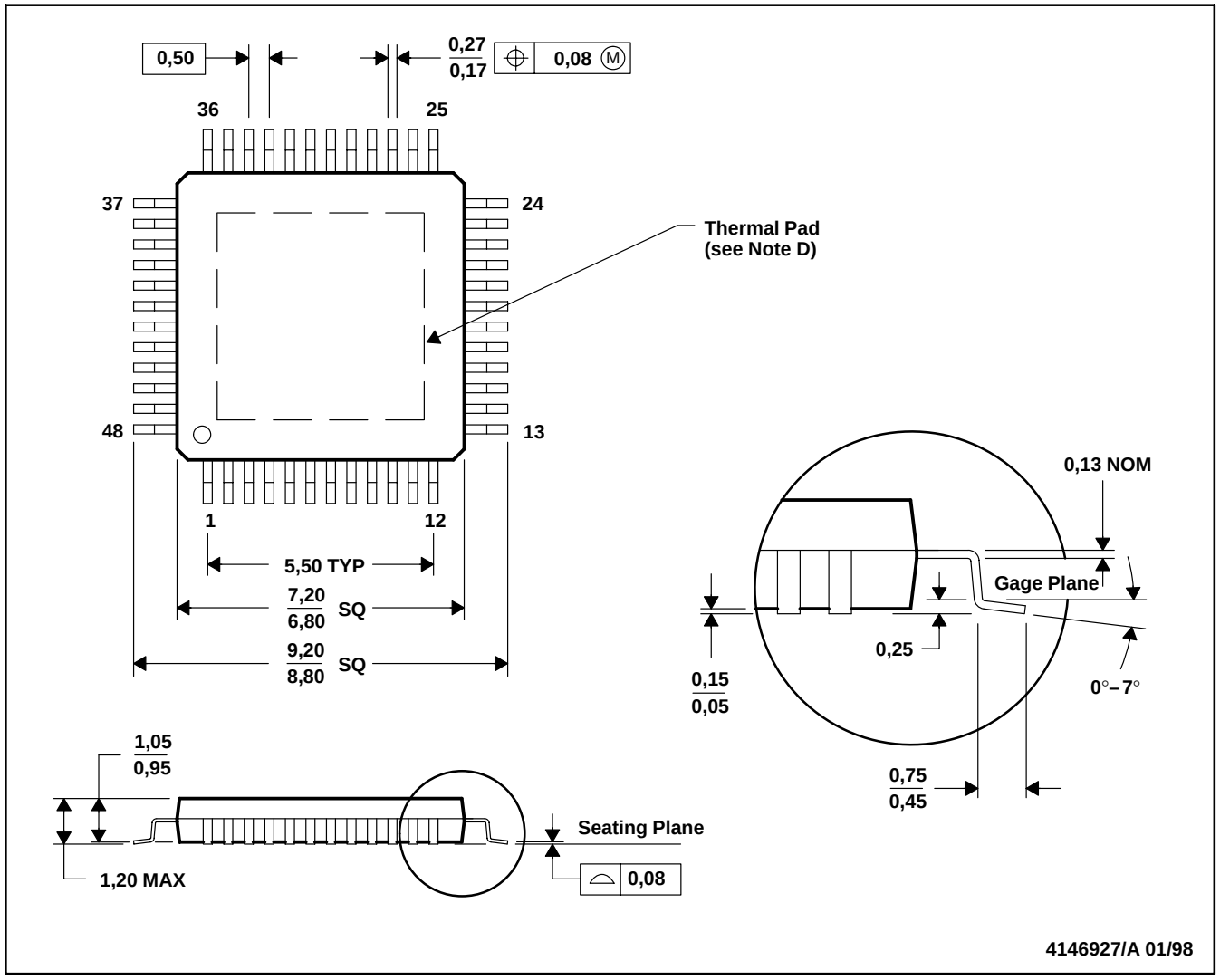
Table 4 shows recommended values of R_{FILT} and C_{FILT} based on common component values. The value of f_C was originally calculated to be 28 kHz for an f_{MAX} of 20 kHz. C_{FILT}, however, was calculated to be 57000 pF, but the nearest values of 56000 pF and 51000 pF were not available. A 47000 pF capacitor was used instead, and f_C is 34 kHz, which is above the desired value of 28 kHz.

Table 4. Typical RC Measurement Filter Values

MEASUREMENT	R_{FILT}	C_{FILT}
Efficiency	1 000 Ω	5 600 pF
All other measurements	100 Ω	56 000 pF

MECHANICAL DATA

PHP (S-PQFP-G48) **PowerPAD™ PLASTIC QUAD FLATPACK**

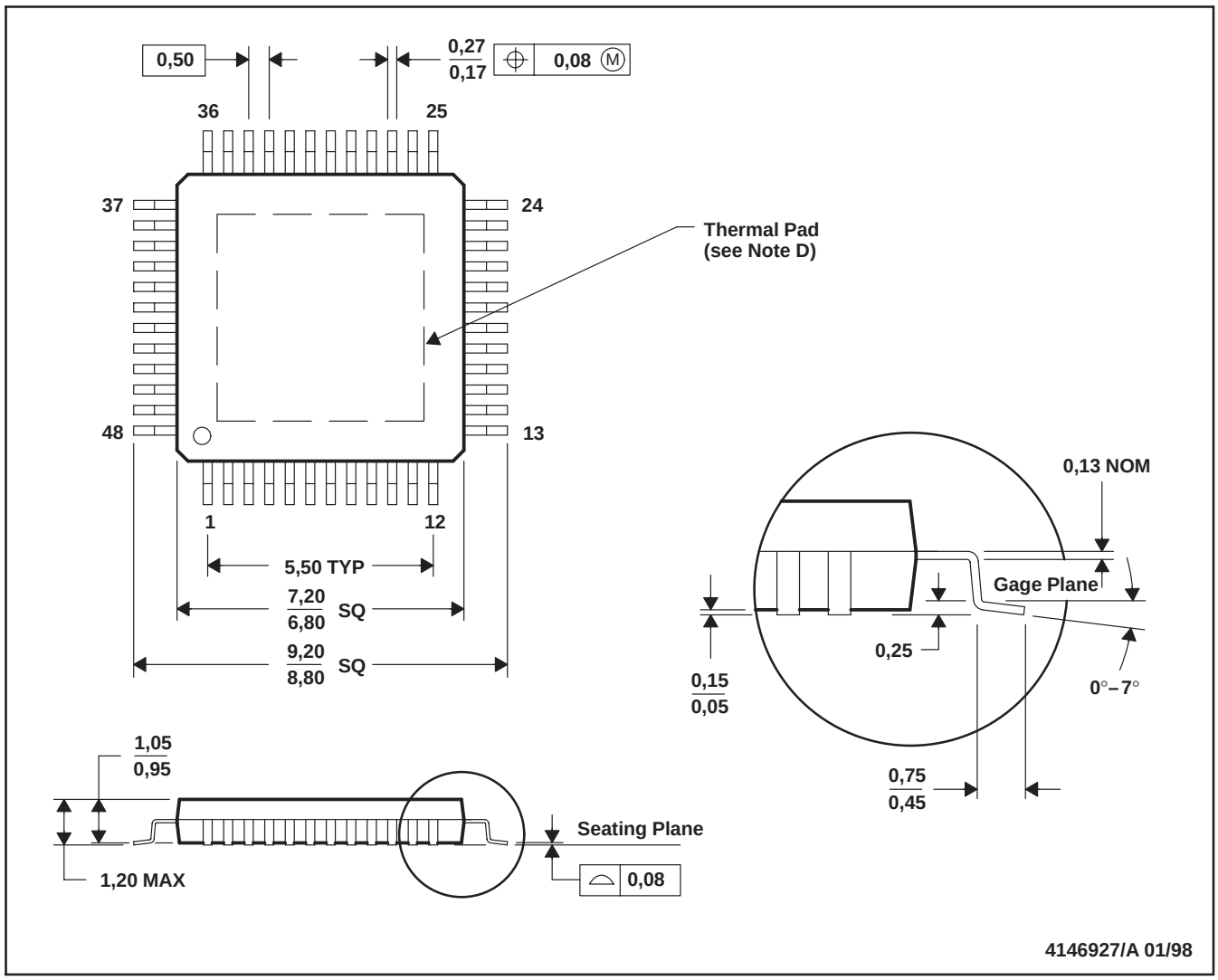


NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MS-026

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PHP (S-PQFP-G48) **PowerPAD™ PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
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Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

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