MULTI-PROTOCOL FULLY INTEGRATED 13.56-MHz RFID/NEAR FIELD COMMUNICATION (NFC) TRANSCEIVER IC

Check for Samples: TRF7970A

1 Introduction

1.1 Features

- **Supports Near Field Communication (NFC) Standards NFCIP-1 (ISO/IEC 18092) and NFCIP-2 (ISO/IEC 21481)**
- **Completely Integrated Protocol Handling for ISO15693, ISO18000-3, ISO14443A/B, and FeliCa**
- **Integrated Encoders, Decoders, and Data Framing for NFC Initiator, Active and Passive Target Operation for All Three Bit Rates (106 kbps, 212 kbps, 424 kbps) and Card Emulation**
- **RF Field Detector With Programmable Wake-Up Levels for NFC Passive Transponder Emulation Operation**
- **RF Field Detector for NFC Physical Collision Avoidance.**
- **Integrated State Machine for ISO14443A Anticollision (Broken Bytes) Operation (Transponder Emulation or NFC Passive Target)**
- **Input Voltage Range: 2.7 VDC to 5.5 VDC**
- **Programmable Output Power: +20 dBm (100 mW), +23 dBm (200 mW)**
- **Programmable I/O Voltage Levels From 1.8 VDC to 5.5 VDC**
- **Programmable System Clock Frequency Output (RF, RF/2, RF/4) from 13.56-MHz or 27.12-MHz Crystal or Oscillator**
- **Integrated Voltage Regulator Output for Other System Components (MCU, Peripherals, Indicators), 20 mA (Max)**
- **Programmable Modulation Depth**
- **Dual Receiver Architecture With RSSI for Elimination of "Read Holes" and Adjacent Reader System or Ambient In-Band Noise Detection**
- **Programmable Power Modes for Ultra Low-Power System Design (Power Down <1 µA)**
- **Parallel or SPI Interface (With 128-Byte FIFO)**
- **Temperature Range: -40°C to 110°C**
- **32-Pin QFN Package (5 mm x 5 mm)**

1.2 Applications

- **Mobile Devices (Tablets, Handsets)**
- **Secure Pairing (Bluetooth, WiFi, Other Paired Wireless Networks)**
- **Public Transport or Event Ticketing**
- **Passport or Payment (POS) Reader Systems**
- **Short-Range Wireless Communication Tasks (Firmware Updates)**
- **Product Identification or Authentication**
- **Medical Equipment or Consumables**
- **Access Control, Digital Door Locks**
- **Sharing of Electronic Business Cards**

1.3 Description

The TRF7970A is an integrated analog front end and data-framing device for a 13.56-MHz RFID/Near Field Communication system. Built-in programming options make it suitable for a wide range of applications for proximity and vicinity identification systems.

It can perform in one of three modes: RFID/NFC Reader, NFC Peer, or in Card Emulation mode. Built-in user-configurable programming options make it suitable for a wide range of applications.

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The TRF7970A is configured by selecting the desired protocol in the control registers. Direct access to all control registers allows fine tuning of various reader parameters as needed.

Documentation, reference designs, EVM, and TI MCU (MSP430, ARM) source code are available.

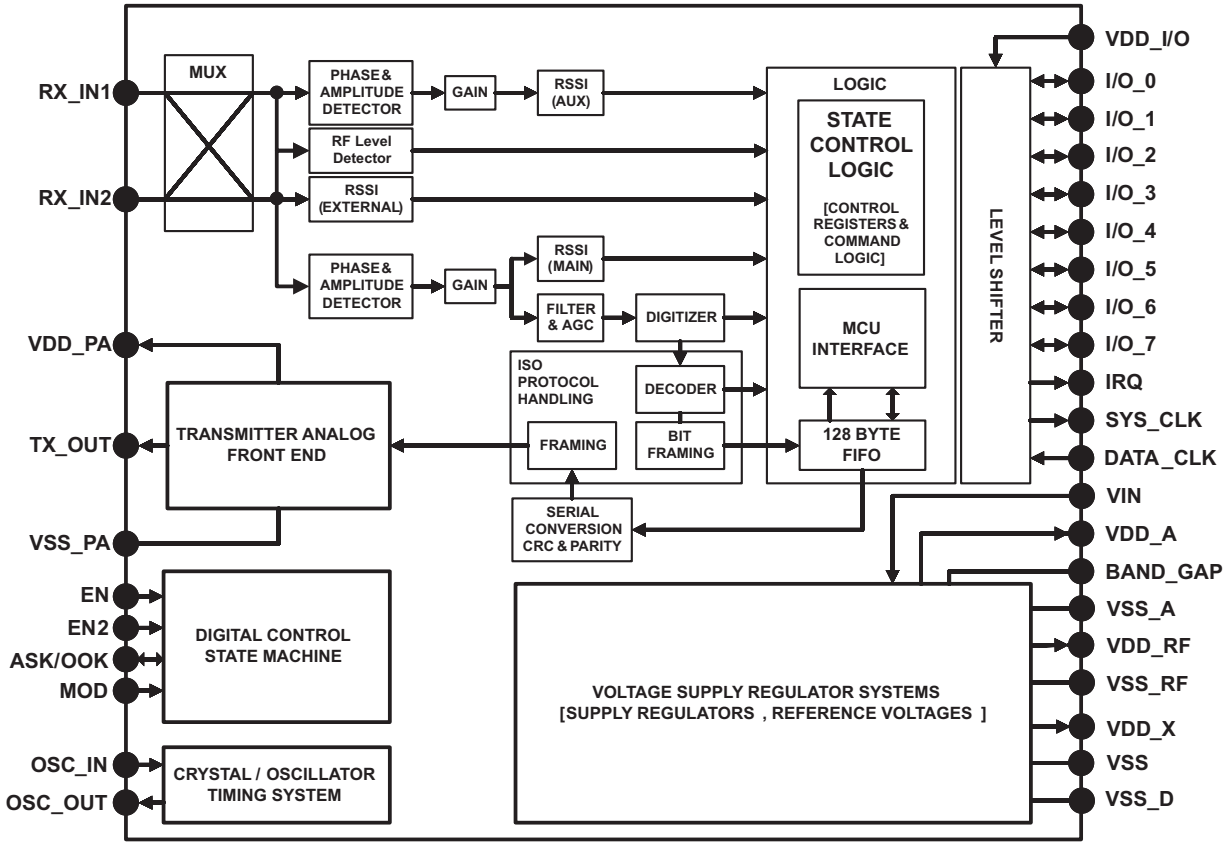


Figure 1-1. Block Diagram

1.3.1 Detailed Description

RFID/NFC Operation – Reader/Writer

The TRF7970A is a high performance 13.56-MHz HF RFID/NFC Transceiver IC composed of an integrated analog front end (AFE) and a built-in data framing engine for ISO15693, ISO14443A, ISO14443B, and FeliCa. This includes data rates up to 848 kbps for ISO14443 with all framing and synchronization tasks on board (in default mode). The TRF7970A also supports NFC Tag Type 1, 2, 3, and 4 operations. This architecture enables the customer to build a complete cost-effective yet high-performance multi-protocol 13.56-MHz RFID/NFC system together with a low-cost microcontroller (for example, MSP430).

Other standards and even custom protocols can be implemented by using two of the Direct Modes that the device offers. These Direct Modes (0 and 1) allow the user to fully control the analog front end (AFE) and also gain access to the raw subcarrier data or the unframed but already ISO formatted data and the associated (extracted) clock signal.

The receiver system has a dual input receiver architecture. The receivers also include various automatic and manual gain control options. The received input bandwidth can be selected to cover a broad range of input subcarrier signal options.

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The received signal strength from transponders, ambient sources, or internal levels is available through the RSSI register. The receiver output is selectable among a digitized subcarrier signal and any of the integrated subcarrier decoders. The selected subcarrier decoder delivers the data bit stream and the data clock as outputs.

The TRF7970A also includes a receiver framing engine. This receiver framing engine performs the CRC or parity check, removes the EOF and SOF settings, and organizes the data in bytes for ISO14443-A/B, ISO15693, and FeliCa protocols. Framed data is then accessible to the microcontroller (MCU) through a 128-byte FIFO register.

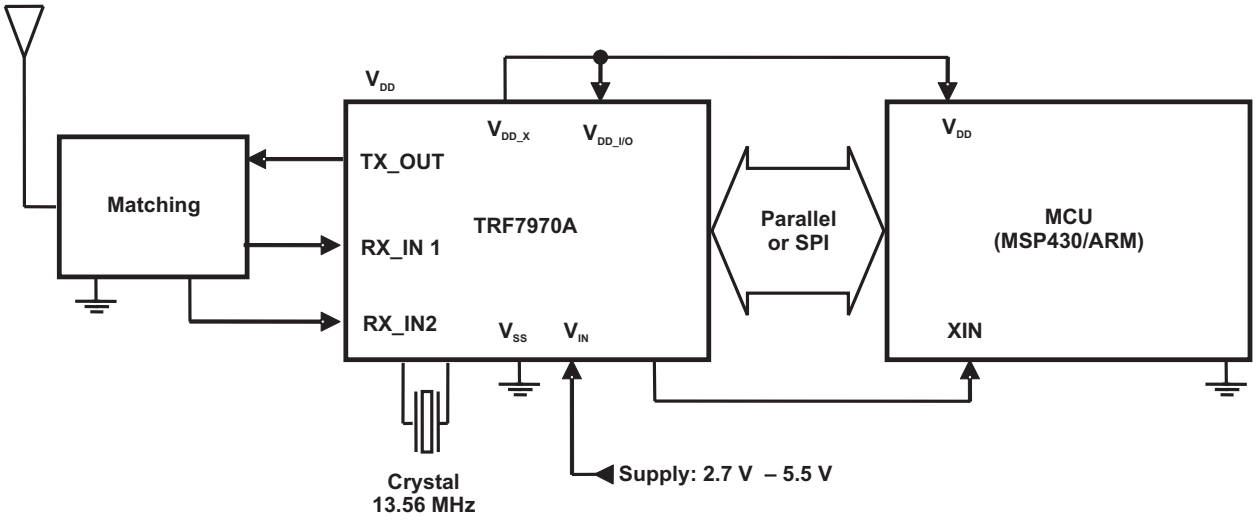


Figure 1-2. Application Block Diagram

A parallel or serial interface (SPI) can be used for the communication between the MCU and the TRF7970A reader. When the built-in hardware encoders and decoders are used, transmit and receive functions use a 128-byte FIFO register. For direct transmit or receive functions, the encoders and decoders can be bypassed so that the MCU can process the data in real time. The TRF7970A supports data communication levels from 1.8 V to 5.5 V for the MCU I/O interface. The transmitter has selectable output-power levels of 100 mW (+20 dBm) or 200 mW (+23 dBm) equivalent into a 50-Ω load when using a 5-V supply.

The transmitter supports OOK and ASK modulation with selectable modulation depth. The TRF7970A also includes a data transmission engine that comprises low-level encoding for ISO15693, ISO14443A/B and FeliCa. Included with the transmit data coding is the automatic generation of Start Of Frame (SOF), End Of Frame (EOF), Cyclic Redundancy Check (CRC), or parity bits.

Several integrated voltage regulators ensure a proper power-supply noise rejection for the complete reader system. The built-in programmable auxiliary voltage regulator V_{DD_X} (pin 32), is able to deliver up to 20 mA to supply a microcontroller and additional external circuits within the reader system.

NFC Device Operation – Initiator

The desired system of operation (bit rate) is achieved by selecting the option bits in control registers in the same way as for RFID reader operation. Also the communication to external MCU and data exchange is identical.

The transmitting system comprises an RF level detector (programmable level) which is used for initial (or response) RF collision avoidance. The RF collision avoidance sequence is started by sending a direct command. If successful, the NFC initiator can send the data or commands, the MCU has loaded in the FIFO register. The coding of this data is done by hardware coders either in ISO14443A/B format or in FeliCa format. The coders also provide CRC and parity bits (if required) and automatically add preambles, SOF, EOF, and synchronization bytes as defined by selected protocol.

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The receiver system offers same analog features (AGC, AM/PM, bandwidth selection, etc.) as described previously in RFID/NFC reader/writer description. The system comprises integrated decoders for passive targets (ISO14443A/B tag or FeliCa) or active targets (ISO14443A/B reader or FeliCa). For all this options, the system also supports framing including CRC and parity check and removal of SOF, EOF, and synchronization bytes as specified by the selected protocol.

NFC Device Operation – Target

The desired system of operation (bit rate) is achieved by selecting the option bits in control registers in the same way as for RFID reader or NFC initiator operation. Also the communication to external MCU and data exchange is identical.

The activation of NFC target is done when a sufficient RF field level is detected on the antenna. The level needed for wake-up is selectable and is stored in non-volatile register.

When the activation occurs, the system performs automatic power-up and waits for the first command to be received. Based on this command, the system knows if it should operate as passive or active target and at what bit rate. After activation, the receiver system offers the same analog features (for example, AGC, AM/PM, and bandwidth selection) as in the case of an RFID reader.

When used as the NFC target, the chip is typically in a power down or standby mode. If EN2 = H, the chip keeps the supply system on. If EN2 = L and EN = L, the chip is in complete power down. To operate as NFC target or Tag emulator, the MCU must load a value different than zero (0) in Target Detection Level register (B0-B2) to enable the RF measurement system (supplied by VEXT, so it can operate also during complete power down and consumes only 3.5 µA). The RF measurement constantly monitors the RF signal on the antenna input. When the RF level on the antenna input exceeds the level defined in the in Target Detection Level register, the chip is automatically activated (EN is internally forced high).

When the voltage supply system and the oscillator are started and are stable, osc_ok goes high (B6 of RSSI Level and Oscillator Status register) and IRQ is sent with bit B2 = 1 of IRQ register (field change). Bit B7 NFC Target Protocol in register directly displays the status of RF level detection (running constantly also during normal operation). This informs the MCU that the chip should start operation as NFC TARGET device. When the first command from the INITIATOR is received another IRQ sent with B6 (RX start) set in IRQ register. The MCU must set EN = H (confirm the power-up) in the time between the two IRQs, because the internal power-up ends after the second IRQ. The type and coding of the first initiator (or reader in the case of a tag emulator) command defines the communication protocol type that the target must use. Therefore, the communication protocol type is available in the NFC Target Protocol register immediately after receiving the first command.

Based on the first command from the INITIATOR, the following actions are taken:

- If the first command is SENS_REQ or ALL_REQ the TARGET must enter the SDD protocol for 106-kbps passive communication to begin; afterward, the baud rate can be changed to 212 kbps or 424 kbps, according to the system requirements. If bit B5 in the NFC Target Detection Level register is not set, the MCU handles the SDD and the command received is send to FIFO. If bit B5 is set, the internal SDD state machine is used. The MCU must load the ID (NFCID1) of the device in the 128-byte NFCID Number registers to be used by the SDD state machine. The length of the ID to use in SDD is defined by bits B6 and B7 of the NFC Target Detection Level register. When the SDD is complete and the INITIATOR sends SEL_REQ with full UID on the correct cascade level, the SDD state machine responds with SEL_RES to indicate that the TARGET supports the data exchange protocol. The IRQ (B3 set) is sent to the MCU to signal the successful end of SDD (the device is now selected as TARGET). The SDD state machine is than turned off. If the RF field is turned off (B7 in NFC Target Protocol register is low) at any time, the system sends an IRQ to the MCU with bit B2 (RF field change) in the IRQ register set high. This informs the MCU that the procedure was aborted and the system must be reset. The clock extractor is automatically activated in this mode.
- If the command is SENS_REQ or ALL_REQ and the Tag emulation bit in ISO Control register is set, the system emulates ISO14443A/B or FeliCa tag. The procedure does not differ from the one previously described for the case of a passive target at 106 kbps. The clock extractor is automatically activated in this mode.

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- If the first command is a POLLING request, the system becomes the TARGET in passive communication using 212 kbps or 424 kbps. The SDD is relatively simple and is handled by the MCU directly. The POLLING response is sent in one of the slots automatically calculated by the MCU (first slot starts 2.416 ms after end of command, and slots follow in 1.208 ms).
- If the first command is ATR_REQ, the system operatea as an active TARGET using the same communication speed and bit coding as used by the INITIATOR. Again, all of the replies are handled by MCU. The chip is only requred to time the response collision avoidance, which is done on direct command from MCU. When the RF field is switched on and the minimum wait time is elapsed, the chip sends an IRQ with B1 (RF collision avoidance finished) set high. This signals the MCU that it can send the reply.
- If the first command is coded as ISO14443B and the Tag emulation bit is set in the ISO Control register, the system enters ISO14443B emulation mode. The anticollision must be handled by the MCU, and the chip provides all physical level coding, decoding, and framing for this protocol.

Active Target

If the first command received by the RF interface defines the system as an active target, then the receiver selects the appropriate data decoders (ISO14443A\B reader or FeliCa) and framing option. Only the raw (decoded) data is forwarded to the MCU through the FIFO. SOF, EOF, preamble, sync bytes, CRC, and parity bytes are checked by the framer and discarded.

The transmitting system includes an RF level detector (programmable level) that is used for RF collision avoidance. The RF collision avoidance sequence is started by sending a direct command. If successful, the NFC initiator can send the data that the MCU has loaded in the FIFO register. The coding of this data is done by hardware coders either in ISO14443A format (106-kbps system) or in FeliCa format for (212-kbps and 424-kbps systems). The coders also provide CRC and parity bits (if required) and automatically add preambles, SOF, EOF, and synchronization bytes as defined by selected protocol.

Passive Target

If the first command received by the RF interface defines the system as a passive target, then the receiver selects the appropriate data decoders (ISO14443A\B reader or FeliCa) and framing option. Again, only the raw (decoded) data is forwarded to the MCU through the FIFO; SOF, EOF, preamble, sync bytes, CRC, and parity bytes are checked by the framer and discarded. The receiver works same as in the case of an active target.

For a passive target at 106 kbps, an internal single device detection (SDD) state machine is available and can perform the SDD (same as anticollision in RFID tags) as defined in ISO14443A\B. This relieves the MCU of the demanding task of handling the 'broken bytes'. For synchronization with the Initiator, a 13.56-MHz clock extractor with a glitch-free switch unit between the internal and external clock is integrated. The clock extractor can be disabled by the application.

The transmit system in passive target mode is different and operates similar to the standard tag. There is no RF collision avoidance sequence, and encoders are used to code the data for ISO14443A\B tag (at 106 kbps, to start) or FeliCa (at 212 kbps, to start) format. The coding system adds all of the SOF, EOF, CRC, parity bits, and synchronization bytes required by protocol. On the physical level, the modulation of the initiator's RF field is done by changing the termination impedance of the antenna between 4 Ω and open.

Card Emulation

The chip can enter this mode by setting appropriate option bits. There are two options to emulate a card. For ISO14443A\B, the emulation supports 106-kbps data rate to start. For ISO14443A, the anticollision algorithm can be performed using an internal state machine, which relieves the MCU of any real-time tasks. The unique ID required for anticollision is provided by the MCU after wake-up of the system.

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Table 1-1. Supported Protocols

Device	Supported Protocols						
	ISO-14443A/B				ISO-15693, ISO-18000-3 (Mode 1)	FeliCa	NFC
	106 kbps	212 kbps	424 kbps	848 kbps		212 kbps, 424 kbps	Type 1– Type 4
TRF7970A	√	√	√	√	√	√	√

1.4 Ordering Information

Packaged Devices(1)	Package Type(2)	Transport Media	Quantity
TRF7970ARHBT	RHB-32	Tape and Reel	250
TRF7970ARHBR			3000

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

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1 Introduction **1**
1.1 Features 1
1.2 Applications 1
1.3 Description 1
1.4 Ordering Information 6
2 Physical Characteristics **8**
2.1 Terminal Functions 8
3 Electrical Specifications **11**
3.1 Absolute Maximum Ratings 11
3.2 Recommended Operating Conditions 11
3.3 Dissipation Ratings 11
3.4 Electrical Characteristics 12
4 Application Schematic and Layout Considerations **13**
4.1 TRF7970A Reader System Using Parallel Microcontroller Interface 13
4.2 TRF7970A Reader System Using SPI With SS Mode 14
5 Detailed System Description **15**
5.1 System Block Diagram 15
5.2 Power Supplies 15
5.3 Receiver – Analog Section 19
5.4 Receiver – Digital Section 21
5.5 Oscillator Section 26
5.6 Transmitter – Analog Section 27
5.7 Transmitter – Digital Section 28
5.8 Transmitter – External Power Amplifier and Subcarrier Detector 29
5.9 TRF7970A IC Communication Interface 29
5.10 Special Direct Mode for Improved MIFARE Compatibility 50
5.11 NFC Modes 50
5.12 Direct Commands from MCU to Reader 53
6 Register Description **57**
6.1 Register Preset 57
6.2 Register Overview 57
6.3 Detailed Register Description 59
7 System Design **77**
7.1 Layout Considerations 77
7.2 Impedance Matching TX_Out (Pin 5) to 50 Ω 77
7.3 Reader Antenna Design Guidelines 79
8 Revision History **80**

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2 Physical Characteristics

2.1 Terminal Functions

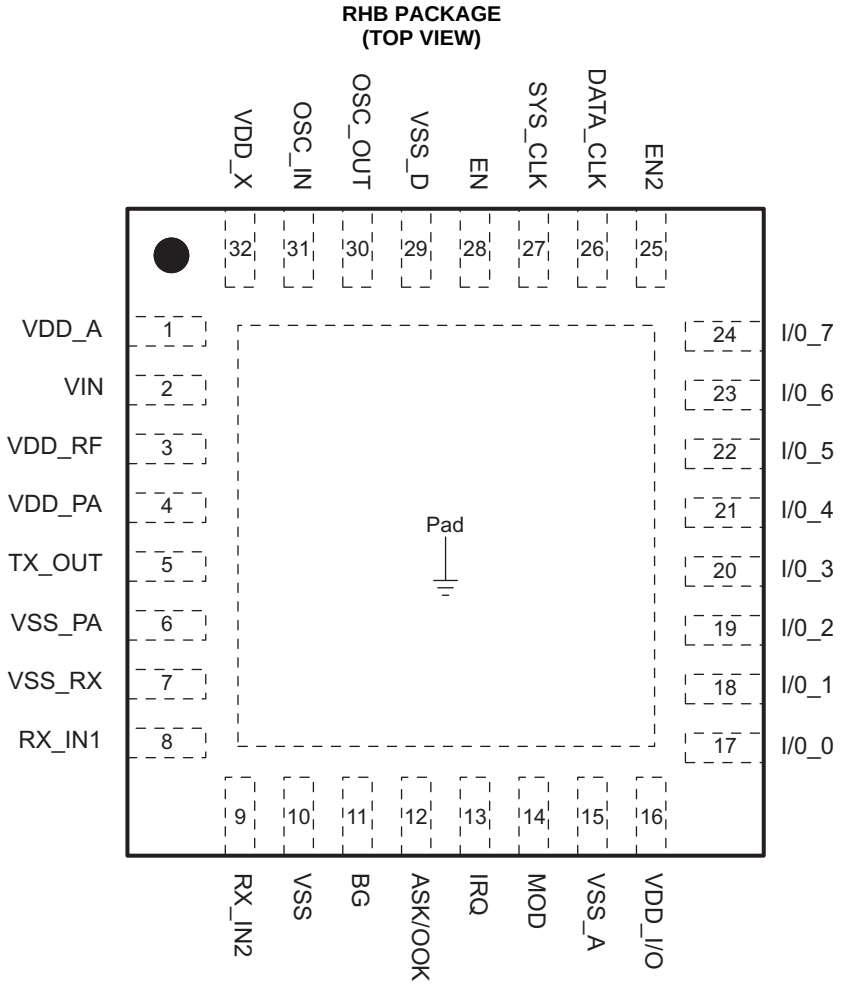


Figure 2-1. Pin Assignments

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Table 2-1. Terminal Functions

TERMINAL		TYPE (1)	DESCRIPTION
NAME	NO.		
V_{DD_A}	1	OUT	Internal regulated supply (2.7 V to 3.4 V) for analog circuitry
V_{IN}	2	SUP	External supply input to chip (2.7 V to 5.5 V)
V_{DD_RF}	3	OUT	Internal regulated supply (2.7 V to 5 V), normally connected to V_{DD_PA} (pin 4)
V_{DD_PA}	4	INP	Supply for PA; normally connected externally to V_{DD_RF} (pin 3)
TX_OUT	5	OUT	RF output (selectable output power, 100 mW or 200 mW, with V_{DD} = 5 V)
V_{SS_PA}	6	SUP	Negative supply for PA; normally connected to circuit ground
V_{SS_RX}	7	SUP	Negative supply for RX inputs; normally connected to circuit ground
RX_IN1	8	INP	Main RX input
RX_IN2	9	INP	Auxiliary RX input
V_{SS}	10	SUP	Chip substrate ground
BAND_GAP	11	OUT	Bandgap voltage (V_{BG} = 1.6 V); internal analog voltage reference
ASK/OOK	12	BID	Selection between ASK and OOK modulation (0 = ASK, 1 = OOK) for Direct Mode 0 or 1. Can be configured as an output to provide the received analog signal output.
IRQ	13	OUT	Interrupt request
MOD	14	INP	External data modulation input for Direct Mode 0 or 1
		OUT	Subcarrier digital data output (see registers 0x1A and 0x1B)
V_{SS_A}	15	SUP	Negative supply for internal analog circuits; connected to GND
$V_{DD_I/O}$	16	INP	Supply for I/O communications (1.8 V to V_{IN}) level shifter. V_{IN} should be never exceeded.
I/O_0	17	BID	I/O pin for parallel communication
I/O_1	18	BID	I/O pin for parallel communication
I/O_2	19	BID	I/O pin for parallel communication TX_Enable (in Special Direct Mode)
I/O_3	20	BID	I/O pin for parallel communication TX_Data (in Special Direct Mode)
I/O_4	21	BID	I/O pin for parallel communication Slave Select signal in SPI mode
I/O_5	22	BID	I/O pin for parallel communication Data clock output in Direct Mode 1 and Special Direct Mode
I/O_6	23	BID	I/O pin for parallel communication MISO for serial communication (SPI) Serial bit data output in Direct Mode 1 or subcarrier signal in Direct Mode 0
I/O_7	24	BID	I/O pin for parallel communication. MOSI for serial communication (SPI)
EN2	25	INP	Selection of power down mode. If EN2 is connected to V_{IN}, then V_{DD_X} is active during power down mode 2 (for example, to supply the MCU).
DATA_CLK	26	INP	Data Clock input for MCU communication (parallel and serial)
SYS_CLK	27	OUT	If EN = 1 (EN2 = don't care) the system clock for MCU is configured. Depending on the crystal that is used, options are as follows (see register 0x09): 13.56-MHz crystal: Off, 3.39 MHz, 6.78 MHz, or 13.56 MHz 27.12-MHz crystal: Off, 6.78 MHz, 13.56 MHz, or 27.12 MHz If EN = 0 and EN2 = 1, then system clock is set to 60 kHz
EN	28	INP	Chip enable input (If EN = 0, then chip is in sleep or power-down mode).
V_{SS_D}	29	SUP	Negative supply for internal digital circuits
OSC_OUT	30	OUT	Crystal or oscillator output
OSC_IN	31	INP	Crystal or oscillator input
		OUT	Crystal oscillator output

(1) SUP = Supply, INP = Input, BID = Bidirectional, OUT = Output

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Table 2-1. Terminal Functions (continued)

TERMINAL		TYPE (1)	DESCRIPTION
NAME	NO.		
V_{DD_X}	32	OUT	Internally regulated supply (2.7 V to 3.4 V) for digital circuit and external devices (for example, MCU)
Thermal Pad	PAD	SUP	Chip substrate ground

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3 Electrical Specifications

3.1 Absolute Maximum Ratings (1) (2)

over operating free-air temperature range (unless otherwise noted)

V_{IN}	Input voltage range		-0.3 V to 6 V
I_{IN}	Maximum current V_{IN}		150 mA
ESD	Electrostatic discharge rating	HBM (Human-Body Model)	2 kV
		CDM (Charged-Device Model)	500 V
		MM (Machine Model)	200 V
T_J	Maximum operating virtual junction temperature	Any condition	140°C
		Continuous operation, long-term reliability (3)	125°C
T_{STG}	Storage temperature range		-55°C to 150°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Operating Conditions are not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to substrate ground terminal V_{SS}.
(3) The maximum junction temperature for continuous operation is limited by package constraints. Operation above this temperature may result in reduced reliability or lifetime of the device.

3.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{IN}	Operating input voltage	2.7	5	5.5	V
T_A	Operating ambient temperature	-40	25	110	°C
T_J	Operating virtual junction temperature	-40	25	125	°C

3.3 Dissipation Ratings

PACKAGE	θ_{JC} (°C/W)	θ_{JC} (1) (°C/W)	POWER RATING (2)	
			$T_A \le 25°C$	$T_A \le 85°C$
RHB (32 pin)	31	36.4	27 W	1.1 W

(1) This data was taken using the JEDEC standard high-K test PCB.
(2) Power rating is determined with a junction temperature of 125°C. This is the point where distortion starts to increase substantially. Thermal management of the final PCB should strive to keep the junction temperature at or below 125°C for best performance and long-term reliability.

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3.4 Electrical Characteristics

Typical operating conditions are TA = 25°C, V_{IN} = 5 V, Full-Power mode (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{PD1}	Supply current in Power Down Mode 1	All building blocks disabled, including supply-voltage regulators; measured after 500-ms settling time (EN = 0, EN2 = 0)		0.5	5	µA
I_{PD2}	Supply current in Power Down Mode 2 (Sleep Mode)	The SYS_CLK generator and V_{DD_X} remain active to support external circuitry; measured after 100-ms settling time (EN = 0, EN2 = 1)		120	200	µA
I_{STBY}	Supply current in stand-by mode	Oscillator running, supply-voltage regulators in low-consumption mode (EN = 1, EN2 = x)		1.9	3.5	mA
I_{ON1}	Supply current without antenna driver current	Oscillator, regulators, RX and AGC active, TX is off		10.5	14	mA
I_{ON2}	Supply current – TX (half power)	Oscillator, regulators, RX and AGC and TX active, P_{OUT} = 100 mW		70	78	mA
I_{ON3}	Supply current – TX (full power)	Oscillator, regulators, RX and AGC and TX active, P_{OUT} = 200 mW		130	150	mA
V_{POR}	Power-on reset voltage	Input voltage at V_{IN}	1.4	2	2.6	V
V_{BG}	Bandgap voltage (pin 11)	Internal analog reference voltage	1.5	1.6	1.7	V
V_{DD_A}	Regulated output voltage for analog circuitry (pin 1)	V_{IN} = 5 V	3.1	3.5	3.8	V
V_{DD_X}	Regulated supply for external circuitry	Output voltage pin 32, V_{IN} = 5 V	3.1	3.4	3.8	V
I_{VDD_Xmax}	Maximum output current of V_{DD_X}	Output current pin 32, V_{IN} = 5 V			20	mA
R_{RFOUT}	Antenna driver output resistance (1)	Half-power mode, V_{IN} = 2.7 V to 5.5 V		8	12	Ω
		Full-power mode, V_{IN} = 2.7 V to 5.5 V		4	6	
R_{RFIN}	RX_IN1 and RX_IN2 input resistance		4	10	20	kΩ
V_{RF_INmax}	Maximum RF input voltage at RX_IN1 and RX_IN2	V_{RF_INmax} should not exceed V_{IN}		3.5		V_{pp}
V_{RF_INmin}	Minimum RF input voltage at RX_IN1 and RX_IN2 (input sensitivity) (2)	$f_{SUBCARRIER}$= 424 kHz		1.4	2.5	mV_{pp}
		$f_{SUBCARRIER}$ = 848 kHz		2.1	3	
f_{SYS_CLK}	SYS_CLK frequency	In power mode 2, EN = 0, EN2 = 1	25	60	120	kHz
f_C	Carrier frequency	Defined by external crystal		13.56		MHz
$t_{CRYSTAL}$	Crystal run-in time	Time until oscillator stable bit is set (register 0x0F) (3)		3		ms
f_{D_CLKmax}	Maximum DATA_CLK frequency (4)	Depends on capacitive load on the I/O lines, recommendation is 2 MHz (4)	2	8	10	MHz
V_{IL}	Input voltage - logic low	I/O lines, IRQ, SYS_CLK, DATA_CLK, EN, EN2			0.2 x $V_{DD_I/O}$	V
V_{IH}	Input voltage threshold, logic high	I/O lines, IRQ, SYS_CLK, DATA_CLK, EN, EN2			0.8 x $V_{DD_I/O}$	V
R_{OUT}	Output resistance I/O_0 to I/O_7			500	800	Ω
R_{SYS_CLK}	Output resistance R_{SYS_CLK}			200	400	Ω
$t_{LO/HI}$	DATA_CLK time high or low, one half of DATA_CLK at 50% duty cycle	Depends on capacitive load on the I/O lines (4)	250	62.5	50	ns
$t_{STE,LEAD}$	Slave select lead time, slave select low to clock			200		ns
$t_{STE,LAG}$	Slave select lag time, last clock to slave Select high			200		ns
$t_{SU,SI}$	MOSI input data setup time		15			ns
$t_{HD,SI}$	MOSI input data hold time		15			ns
$t_{SU,SO}$	MISO input data setup time		15			ns
$t_{HD,SO}$	MISO input data hold time		15			ns
$t_{VALID,SO}$	MISO output data valid time	DATA_CLK edge to MISO valid, C_L ≤ 30 pF	30	50	75	ns

(1) Antenna driver output resistance
(2) Measured with subcarrier signal at RX_IN1 or RX_IN2 and measured the digital output at MOD pin with register 0x1A bit 6 = 1.
(3) Depends on the crystal parameters and components
(4) Recommended DATA_CLK speed is 2 MHz; higher data clock depends on the capacitive load. Maximum SPI clock speed should not exceed 10 MHz. This clock speed is acceptable only when external capacitive load is less than 30 pF. MISO driver has a typical output resistance of 400 Ω (12-ns time constant when 30-pF load used).

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4 Application Schematic and Layout Considerations

4.1 TRF7970A Reader System Using Parallel Microcontroller Interface

4.1.1 General Application Considerations

Figure 4-1 shows the most flexible TRF7970A application schematic. Both ISO15693, ISO14443 and FeliCa systems can be addressed. Due to the low clock frequency on the DATA_CLK line, the parallel interface is the most robust way to connect the TRF7970A with the MCU.

Figure 4-1 shows matching to a 50-Ω port, which allows connecting to a properly matched 50-Ω antenna circuit or RF measurement equipment (for example, a spectrum analyzer or power meter).

4.1.2 Schematic

Figure 4-1 shows a sample application schematic for a parallel MCU interface.

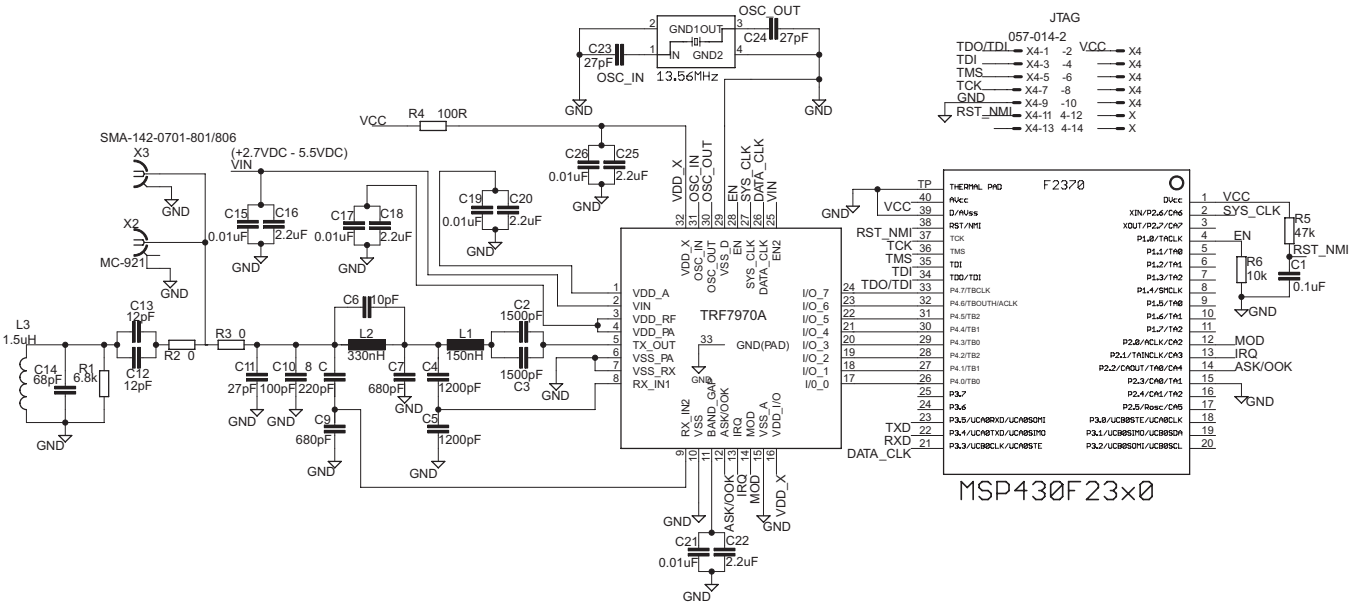


Figure 4-1. Application Schematic – Parallel MCU Interface

An MSP430F2370 (32kB Flash, 2kB RAM) is shown in Figure 4-1. Minimum MCU requirements depend on application requirements and coding style. If only one ISO protocol or a limited command set of a protocol needs to be supported, MCU Flash and RAM requirements can be significantly reduced. Be aware that recursive inventory and anticollision commands require more RAM than single slotted operations. For example, current reference firmware for ISO15693 (with host interface) is approximately 8kB, using 512B RAM; for all supported protocols (also with same host interface) the reference firmware is approximately 12kB and uses a minimum of 1kB RAM. An MCU capable of running its GPIOs at 13.56 MHz is required for Direct Mode 0 operations.

4.2 TRF7970A Reader System Using SPI With SS Mode

4.2.1 General Application Considerations

Figure 4-2 shows the TRF7970A application schematic optimized for both ISO15693 and ISO14443 systems using the Serial Port Interface (SPI). Short SPI lines, proper isolation of radio frequency lines, and a proper ground area are essential to avoid interference. The recommended clock frequency on the DATA_CLK line is 2 MHz.

Figure 4-2 shows matching to a 50-Ω port, which allows connecting to a properly matched 50-Ω antenna circuit or RF measurement equipment (for example, a spectrum analyzer or power meter).

4.2.2 Schematic

Figure 4-2 shows a sample application schematic for SPI with an SS mode MCU interface.

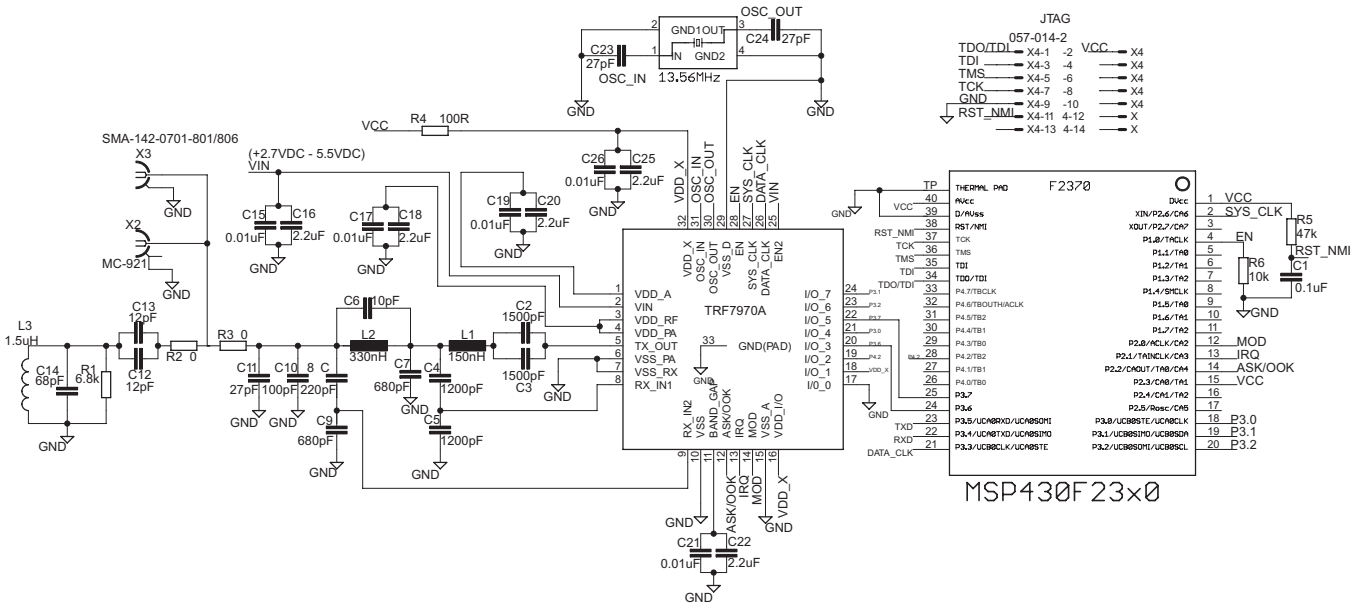


Figure 4-2. Application Schematic – SPI With SS Mode MCU Interface

An MSP430F2370 (32kB Flash, 2kB RAM) is shown in Figure 4-2. Minimum MCU requirements depend on application requirements and coding style. If only one ISO protocol or a limited command set of a protocol needs to be supported, MCU Flash and RAM requirements can be significantly reduced and user should be aware that recursive inventory and anticollision commands require more RAM than single slotted operations. For example, current reference firmware for ISO15693 (with host interface) is approximately 8kB, using 512B RAM and for all supported protocols (also with same host interface) the reference firmware is approximately 12kB and uses a minimum of 1kB RAM. An MCU capable of running its GPIOs at 13.56 MHz is required for Direct Mode 0 operations.

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5 Detailed System Description

5.1 System Block Diagram

Figure 5-1shows a block diagram of the TRF7970A.

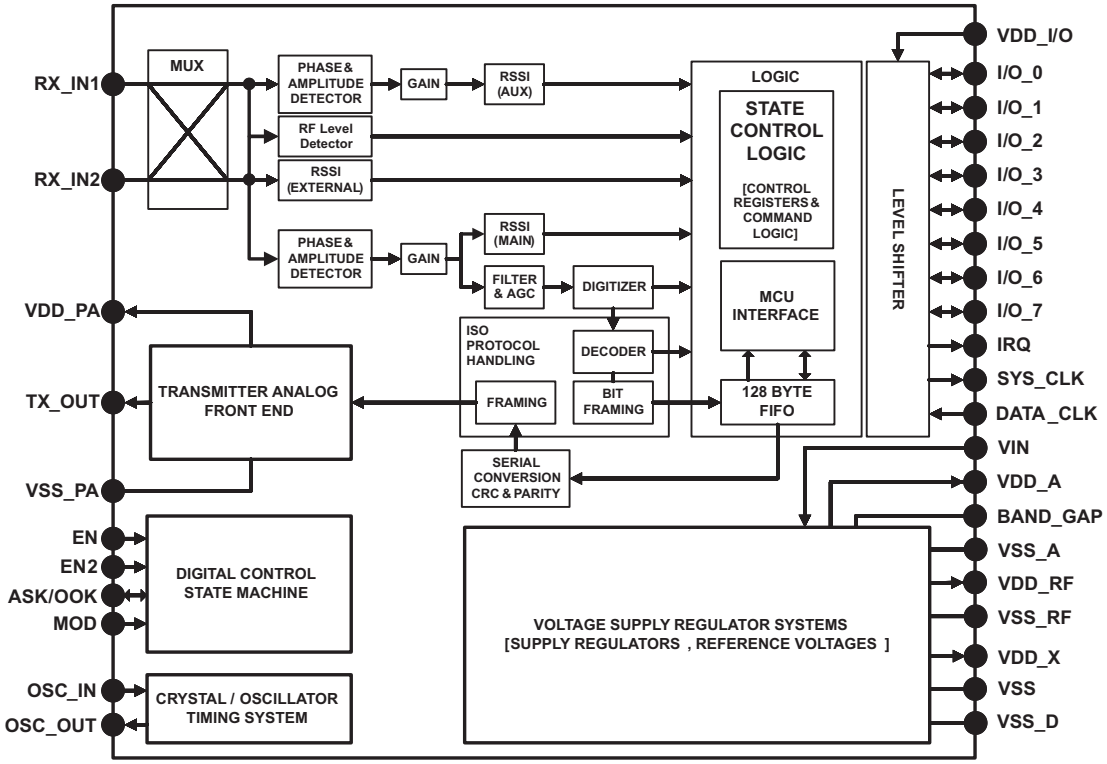


Figure 5-1. System Block Diagram

5.2 Power Supplies

The TRF7970A positive supply input V_{IN} (pin 2) sources three internal regulators with output voltages V_{DD_RF}, V_{DD_A} and V_{DD_X}. All regulators use external bypass capacitors for supply noise filtering and must be connected as indicated in reference schematics. These regulators provide a high power supply reject ratio (PSRR) as required for RFID reader systems. All regulators are supplied by V_{IN} (pin 2).

The regulators are not independent and have common control bits in register 0x0B for output voltage setting. The regulators can be configured to operate in either automatic or manual mode (register 0x0B, bit 7). The automatic regulator setting mode ensures an optimal compromise between PSRR and the highest possible supply voltage for RF output (to ensure maximum RF power output). The manual mode allows the user to manually configure the regulator settings.

5.2.1 Supply Arrangements

Regulator Supply Input: V_{IN}

The positive supply at V_{IN} (pin 2) has an input voltage range of 2.7 V to 5.5 V. V_{IN} provides the supply input sources for three internal regulators with the output voltages V_{DD_RF}, V_{DD_A}, and V_{DD_X}. External bypass capacitors for supply noise filtering must be used (per reference schematics).

NOTE

V_{IN} must be the highest voltage supplied to the TRF7970A.

RF Power Amplifier Regulator: V_{DD_RF}

The V_{DD_RF} (pin 3) regulator is supplying the RF power amplifier. The voltage regulator can be set for either 5-V or 3-V operation. External bypass capacitors for supply noise filtering must be used (per reference schematics). When configured for 5-V manual-operation, the V_{DD_RF} output voltage can be set from 4.3 V to 5 V in 100-mV steps. In 3-V manual-operation, the output can be programmed from 2.7 V to 3.4 V in 100-mV steps. The maximum output current capability for 5-V operation is 150 mA and for 3-V operation is 100 mA.

Analog Supply Regulator: V_{DD_A}

Regulator V_{DD_A} (pin 1) supplies the analog circuits of the device. The output voltage setting depends on the input voltage and can be set for 5-V and 3-V operation. When configured for 5-V manual-operation, the output voltage is fixed at 3.4 V. External bypass capacitors for supply noise filtering must be used (per reference schematics). When configured for 3-V manual-operation, the V_{DD_A} output can be set from 2.7 V to 3.4 V in 100-mV steps (see Table 5-2).

Note: the configuration of V_{DD_A} and V_{DD_X} regulators are not independent from each other. The V_{DD_A} output current should not exceed 20 mA.

Digital Supply Regulator: V_{DD_X}

The digital supply regulator V_{DD_X} (pin 32) provides the power for the internal digital building blocks and can also be used to supply external electronics within the reader system. When configured for 3-V operation, the output voltage can be set from 2.7 to 3.4 V in 100-mV steps. External bypass capacitors for supply noise filtering must be used (per reference schematics).

Note: the configuration of the V_{DD_A} and V_{DD_X} regulators are not independent from each other. The V_{DD_X} output current should not exceed 20 mA.

The RF power amplifier regulator (V_{DD_RF}), analog supply regulator (V_{DD_A}) and digital supply regulator (V_{DD_X}) can be configured to operate in either automatic or manual mode described in Section 5.2.2. The automatic regulator setting mode ensures an optimal compromise between PSRR and the highest possible supply voltage to ensure maximum RF power output.

By default, the regulators are set in automatic regulator setting mode. In this mode, the regulators are automatically set every time the system is activated by setting EN input High or each time the automatic regulator setting bit, B7 in register 0x0B is set to a 1. The action is started on the 0 to 1 transition. This means that, if the user wants to re-run the automatic setting from a state in which the automatic setting bit is already high, the automatic setting bit (B7 in register 0x0B) should be changed: 1-0-1.

By default, the regulator setting algorithm sets the regulator outputs to a "Delta Voltage" of 250 mV below V_{IN}, but not higher than 5 V for V_{DD_RF} and 3.4 V for V_{DD_A} and V_{DD_A}. The "Delta Voltage" in automatic regulator mode can be increased up to 400 mV (for details, see bits B0 to B2 in register 0x0B).

Power Amplifier Supply: V_{DD_PA}

The power amplifier of the TRF7970A is supplied through V_{DD_PA}(pin 4). The positive supply pin for the RF power amplifier is externally connected to the regulator output V_{DD_RF} (pin 3).

I/O Level Shifter Supply: $V_{DD_I/O}$

The TRF7970A has a separate supply input $V_{DD_I/O}$ (pin 16) for the built-in I/O level shifter. The supported input voltage ranges from 1.8 V to V_{IN}, not exceeding 5.5 V. Pin 16 is used to supply the I/O interface pins (I/O_0 to I/O_7), IRQ, SYS_CLK, and DATA_CLK pins of the reader. In typical applications, $V_{DD_I/O}$ is directly connected to V_{DD_X}, while V_{DD_X} also supplies the MCU. This ensures that the I/O signal levels of the MCU match the logic levels of the TRF7970A.

Negative Supply Connections: V_{SS}, V_{SS_TX}, V_{SS_RX}, V_{SS_A}, V_{SS_PA}

The negative supply connections V_{SS_X} of each functional block are all externally connected to GND.

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The substrate connection is V_{SS} (pin 10), the analog negative supply is V_{SS_A} (pin 15), the logic negative supply is V_{SS_D} (pin 29), the RF output stage negative supply is V_{SS_PA} (pin 6), and the negative supply for the RF receiver V_{SS_RX} (pin 7).

5.2.2 Supply Regulator Settings

The input supply voltage mode of the reader needs to be selected. This is done in the Chip Status Control register (0x00). Bit 0 in register 0x00 selects between 5-V or 3-V input supply voltage. The default configuration is 5 V, which reflects an operating supply voltage range of 4.3 V to 5.5 V. If the supply voltage is below 4.3 V, the 3-V configuration should be used.

The various regulators can be configured to operate in automatic or manual mode. This is done in the Regulator and I/O Control register (0x0B) as shown in Table 5-1 and Table 5-2.

Table 5-1. Supply Regulator Setting: 5-V System

Register Address (hex)	Option Bits Setting in Regulator Control Register (1)								Comments
	B7	B6	B5	B4	B3	B2	B1	B0	
Automatic Mode (default)									
0B	1	x	x	x	x	x	1	1	Automatic regulator setting 250-mV difference
0B	1	x	x	x	x	x	1	0	Automatic regulator setting 350-mV difference
0B	1	x	x	x	x	x	0	0	Automatic regulator setting 400-mV difference
Manual Mode									
0B	0	x	x	x	x	1	1	1	V_{DD_RF} = 5 V, V_{DD_A} = 3.4 V, V_{DD_X} = 3.4 V
0B	0	x	x	x	x	1	1	0	V_{DD_RF} = 4.9 V, V_{DD_A} = 3.4 V, V_{DD_X} = 3.4 V
0B	0	x	x	x	x	1	0	1	V_{DD_RF} = 4.8 V, V_{DD_A} = 3.4 V, V_{DD_X} = 3.4 V
0B	0	x	x	x	x	1	0	0	V_{DD_RF} = 4.7 V, V_{DD_A} = 3.4 V, V_{DD_X} = 3.4 V
0B	0	x	x	x	x	0	1	1	V_{DD_RF} = 4.6 V, V_{DD_A} = 3.4 V, V_{DD_X} = 3.4 V
0B	0	x	x	x	x	0	1	0	V_{DD_RF} = 4.5 V, V_{DD_A} = 3.4 V, V_{DD_X} = 3.4 V
0B	0	x	x	x	x	0	0	1	V_{DD_RF} = 4.4 V, V_{DD_A} = 3.4 V, V_{DD_X} = 3.4 V
0B	0	x	x	x	x	0	0	0	V_{DD_RF} = 4.3 V, V_{DD_A} = 3.4 V, V_{DD_X} = 3.4 V

(1) x = Don't care

Table 5-2. Supply Regulator Setting: 3-V System

Register Address (hex)	Option Bits Setting in Regulator Control Register (1)								Comments
	B7	B6	B5	B4	B3	B2	B1	B0	
Automatic Mode (default)									
0B	1	x	x	x	x	x	1	1	Automatic regulator setting 250-mV difference
0B	1	x	x	x	x	x	1	0	Automatic regulator setting 350-mV difference
0B	1	x	x	x	x	x	0	0	Automatic regulator setting 400-mV difference
Manual Mode									
0B	0	x	x	x	x	1	1	1	V_{DD_RF} = 3.4 V, V_{DD_A} = 3.4 V, V_{DD_X} = 3.4 V
0B	0	x	x	x	x	1	1	0	V_{DD_RF} = 3.3 V, V_{DD_A} = 3.3 V, V_{DD_X} = 3.3 V
0B	0	x	x	x	x	1	0	1	V_{DD_RF} = 3.2 V, V_{DD_A} = 3.2 V, V_{DD_X} = 3.2 V
0B	0	x	x	x	x	1	0	0	V_{DD_RF} = 3.1 V, V_{DD_A} = 3.1 V, V_{DD_X} = 3.1 V
0B	0	x	x	x	x	0	1	1	V_{DD_RF} = 3.0 V, V_{DD_A} = 3.0 V, V_{DD_X} = 3.0 V
0B	0	x	x	x	x	0	1	0	V_{DD_RF} = 2.9 V, V_{DD_A} = 2.9 V, V_{DD_X} = 2.9 V
0B	0	x	x	x	x	0	0	1	V_{DD_RF} = 2.8 V, V_{DD_A} = 2.8 V, V_{DD_X} = 2.8 V
0B	0	x	x	x	x	0	0	0	V_{DD_RF} = 2.7 V, V_{DD_A} = 2.7 V, V_{DD_X} = 2.7 V

(1) x = Don't care

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The regulator configuration function adjusts the regulator outputs by default to 250 mV below V_{IN} level, but not higher than 5 V for V_{DD_RF} , 3.4 V for V_{DD_A} and V_{DD_X}. This ensures the highest possible supply voltage for the RF output stage while maintaining an adequate PSRR (power supply rejection ratio).

To further improve the PSRR, it is possible to increase the target voltage difference across V_{DD_X} and V_{DD_A} from its default to 350 mV or even 400 mV (for details see Regulator and I/O Control register (0x0B) definition in Table 5-1 and Table 5-2.)

5.2.3 Power Modes

The chip has several power states, which are controlled by two input pins (EN and EN2) and several bits in the chip status control register (0x00) (see Table 5-3).

Table 5-3. Power Modes (1)

Mode	EN2	EN	Chip Status Control Register (0x00)	Regulator Control Register (0x0B)	Trans-mitter	Receiver	SYS_CLK (13.56 MHz)	SYS_CLK (60 kHz)	V_{DD_X}	Typical Current (mA)	Typical Power Out (dBm)	Time (From Previous State)
Mode 4 (Full Power) at 5 VDC	X	1	21	07	ON	ON	ON	X	ON	105	23	approx. 20-25 µs
Mode 4 (Full Power) at 3.3 VDC	X	1	20	07	ON	ON	ON	X	ON	68	17	
Mode 3 (Half Power) at 5 VDC	X	1	31	07	ON	ON	ON	X	ON	82	20	approx. 20-25 µs
Mode 3 (Half Power) at 3.3 VDC	X	1	30	07	ON	ON	ON	X	ON	53	14	
Mode 2 at 5 VDC	X	1	03	07	OFF	ON	ON	X	ON	13	—	approx. 20-25 µs
Mode 2 at 3.3 VDC	X	1	02	00	OFF	ON	ON	X	ON	10	—	
Mode 1 at 5 VDC	X	1	01	07	OFF	OFF	ON	X	ON	5	—	approx. 20-25 µs
Mode 1 at 3.3 VDC	X	1	00	00	OFF	OFF	ON	X	ON	3		
Standby Mode at 5 VDC	X	1	81	07	OFF	OFF	ON	X	ON	3	—	4.8 ms
Standby Mode at 3.3 VDC	X	1	80	00	OFF	OFF	ON	X	ON	2	—	
Power Down Mode 2 (Sleep)	1	0	X	X	OFF	OFF	OFF	ON	ON	0.120	—	1.5 ms
Power Down Mode 1 (Total PD)	0	0	X	X	OFF	OFF	OFF	OFF	OFF	<0.001	—	Start

(1) X = Don't care

Table 5-3 shows the configuration for the different power modes when using a 5-V or 3-V system supply. The main reader enable signal is pin EN. When EN is set high, all of the reader regulators are enabled, the 13.56-MHz oscillator is running and the SYS_CLK (output clock for external micro controller) is also available.

The input pin EN2 has two functions:

- A direct connection from EN2 to V_{IN} to ensure the availability of the regulated supply V_{DD_X} and an auxiliary clock signal (60 kHz, SYS_CLK) for an external MCU. This mode (EN = 0, EN2 = 1) is intended for systems in which the MCU is also being supplied by the reader supply regulator (V_{DD_X}) and the MCU clock is supplied by the SYS_CLK output of the reader. This allows the MCU supply and clock to be available during sleep mode.
- EN2 enables the start-up of the reader system from complete power down (EN = 0, EN2 = 0). In this case the EN input is being controlled by the MCU (or other system device) that is without supply voltage during complete power down (thus unable to control the EN input). A rising edge applied to the EN2 input (which has an approximately 1-V threshold level) starts the reader supply system and 13.56-MHz oscillator (identical to condition EN = 1).

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When user MCU is controlling EN and EN2, a delay of 5 ms between EN and EN2 must be used. If the MCU controls only EN, EN2 is recommended to be connected to either V_{IN} or GND, depending on the application MCU requirements for V_{DD_X} and SYS_CLK.

NOTE

Using EN = 1 and EN2 = 1 in parallel at start up should not be done as it can cause incorrect operation.

This start-up mode lasts until all of the regulators have settled and the 13.56-MHz oscillator has stabilized. If the EN input is set high (EN = 1) by the MCU (or other system device), the reader stays active. If the EN input is not set high (EN = 0) within 100 µs after the SYS_CLK output is switched from auxiliary clock (60 kHz) to high-frequency clock (derived from the crystal oscillator), the reader system returns to complete Power-Down Mode1. This option can be used to wake-up the reader system from complete Power Down (PD Mode 1) by using a pushbutton switch or by sending a single pulse.

After the reader EN line is high, the other power modes are selected by control bits within the chip status control register (0x00). The power mode options and states are listed in Table 5-3.

When EN is set high (or on rising edge of EN2 and then confirmed by EN = 1) the supply regulators are activated and the 13.56-MHz oscillator started. When the supplies are settled and the oscillator frequency is stable, the SYS_CLK output is switched from the auxiliary frequency of 60 kHz to the 13.56-MHz frequency derived from the crystal oscillator. At this point, the reader is ready to communicate and perform the required tasks. The MCU can then program the chip status control register 0x00 and select the operation mode by programming the additional registers.

- Stand-by Mode (bit 7 = 1 of register 0x00), the reader is capable of recovering to full operation in 100 µs.
- Mode 1 (active mode with RF output disabled, bit 5 = 0 and bit 1 = 0 of register 0x00) is a low power mode which allows the reader to recover to full operation within 25 µs.
- Mode 2 (active mode with only the RF receiver active, bit 1 = 1 of register 0x00) can be used to measure the external RF field (as described in RSSI measurements paragraph) if reader-to-reader anticollision is implemented.
- Modes 3 and 4 (active modes with the entire RF section active, bit 5 = 1 of register 0x00) are the normal modes used for normal transmit and receive operations.

5.3 Receiver – Analog Section

5.3.1 Main and Auxiliary Receivers

The TRF7970A has two receiver inputs: RX_IN1 (pin 8) and RX_IN2 (pin 9). Each of the input is connected to an external capacitive voltage divider to ensure that the modulated signal from the tag is available on at least one of the two inputs. This architecture eliminates any possible communication holes that may occur from the tag to the reader.

The two RX inputs (RX_IN1 and RX_IN2) are multiplexed into two receivers - the main receiver and the auxiliary receiver. Only the main receiver is used for reception, the auxiliary receiver is used for signal quality monitoring. Receiver input multiplexing is controlled by bit B3 in the Chip Status Control register (address 0x00).

After startup, RX_IN1 is multiplexed to the main receiver which is composed of an RF envelope detection, first gain and band-pass filtering stage, second gain and filtering stage with AGC. Only the main receiver is connected to the digitizing stage which output is connected to the digital processing block. The main receiver also has an RSSI measuring stage, which measures the strength of the demodulated signal (subcarrier signal).

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The primary function of the auxiliary receiver is to monitor the RX signal quality by measuring the RSSI of the demodulated subcarrier signal (internal RSSI). After startup, RX_IN2 is multiplexed to the auxiliary receiver. The auxiliary receiver has an RF envelope detection stage, first gain and filtering with AGC stage and finally the auxiliary RSSI block.

The default MUX setting is RX_IN1 connected to the main receiver and RX_IN2 connected to the auxiliary receiver. To determine the signal quality, the response from the tag is detected by the "main" (pin RX_IN1) and "auxiliary" (pin RX_IN2) RSSI. Both values measured and stored in the RSSI level register (address 0x0F). The MCU can read the RSSI values from the TRF7970A RSSI register and make the decision if swapping the input- signals is preferable or not. Setting B3 in Chip Status Control register (address 0x00) to 1 connects RX_IN1 (pin 8) to the auxiliary received and RX_IN2 (pin 9) to the main receiver. This mechanism needs to be used to avoid reading holes.

The main and auxiliary receiver input stages are RF envelope detectors. The RF amplitude at RX_IN1 and RX_IN2 should be approximately 3 VPP for a V_{IN}supply level greater than 3.3 V. If the V_{IN} level is lower, the RF input peak-to-peak voltage level should not exceed the V_{IN}level.

5.3.2 Receiver Gain and Filter Stages

The first gain and filtering stage has a nominal gain of 15 dB with an adjustable band-pass filter. The band-pass filter has programmable 3d-B corner frequencies between 110 kHz to 450 kHz for the high-pass filter and 570 kHz to 1500 kHz for the low-pass filter. After the band-pass filter, there is another gain-and-filtering stage with a nominal gain of 8 dB and with frequency characteristics identical to the first band-pass stage.

The internal filters are configured automatically depending on the selected ISO communication standard in the ISO Control register (address 0x01). If required, additional fine tuning can be done by writing directly to the RX special setting registers (address 0x0A).

The main receiver also has a second receiver gain and digitizer stage which is included in the AGC loop. The AGC loop is activated by setting the bit B2 = 1 in the Chip Status Control register (0x00). When activated, the AGC continuously monitors the input signal level. If the signal level is significantly higher than an internal threshold level, gain reduction is activated.

By default, the AGC is frozen after the first 4 pulses of the subcarrier signal. This prevents the AGC from interfering with the reception of the remaining data packet. In certain situations, this AGC freeze is not optimal, so it can be removed by setting B0 = 1 in the RX special setting register (address 0x0A).

Table 5-4. RX Special Setting Register (0x0A)

Bit	Function	Comments
B7	Bandpass from 110 kHz to 570 kHz	Appropriate for any 212-kHz subcarrier systems (for example, FeliCa)
B6	Bandpass from 200 kHz to 900 kHz	Appropriate for 424-kHz subcarrier systems (for example, used in ISO15693)
B5	Bandpass from 450 kHz to 1.5 MHz	Appropriate for Manchester-coded 106-kbps 848-kHz subcarrier systems (for example, used in ISO14443A)
B4	Bandpass from 100 kHz to 1.5 MHz	Appropriate for highest bit rate (848 kbps) used in high-bit-rate ISO14443B. Gain is reduced by 7 dB.
B3 B2	00 = no gain reduction 01 = gain reduction for 5 dB 10 = gain reduction for 10 dB 11 = gain reduction for 15 dB	Sets the RX digital gain reduction (changing the window of the digitizing comparator)
B1	0 = 5 times minimum digitizing level 1 = 3 times minimum digitizing level	AGC activation level change. From 5 times the minimum RX digitizing level to 3 times the minimum digitizing level. The minimum RX digitizing level can be adjusted by B2 and B3 (gain reduction)
B0	0 = AGC freeze after 16 subcarrier edges 1 = AGC always on during receive	AGC action is not limited in time or to the start of receive. AGC action can be done any time during receive process. The AGC can only increase and, therefore, clips on the peak RX level during the enable period. AGC level is reset automatically at the beginning of each receive start frame.

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Table 5-4 shows the various settings for the receiver analog section. It is important to note that setting B4, B5, B6, and B7 to 0 results to a band-pass characteristic of 240 kHz to 1.4 MHz, which is appropriate for ISO14443B 106 kbps, ISO14443A/B data-rates of 212 kbps and 424 kbps and FeliCa 424 kbps.

5.4 Receiver – Digital Section

The output of the TRF7970A analog receiver block is a digitized subcarrier signal and is the input to the digital receiver block. This block includes a Protocol Bit Decoder section and the Framing Logic section.

The protocol bit decoders convert the subcarrier coded signal into a serial bit stream and a data clock. The decoder logic is designed for maximum error tolerance. This enables the decoder section to successfully decode even partly corrupted subcarrier signals that otherwise would be lost due to noise or interference.

In the framing logic section, the serial bit stream data is formatted in bytes. Special signals such as the start of frame (SOF), end of frame (EOF), start of communication, and end of communication are automatically removed. The parity bits and CRC bytes are also checked and removed. This "clean" data is then sent to the 128 byte FIFO register where it can be read by the external microcontroller system. Providing the data this way, in conjunction with the timing register settings of the TRF7970A means the firmware developer has to know about much less of the finer details of the ISO protocols to create a very robust application, especially in low cost platforms where code space is at a premium and high performance is still required.

The start of the receive operation (successfully received SOF) sets the IRQ-flags in the IRQ and Status Register (0x0C). The end of the receive operation is signaled to the external system MCU by setting pin 13 (IRQ) to high. When data is received in the FIFO, an interrupt is sent to the MCU to signal that there is data to be read from the FIFO. The FIFO status register (0x1C) should be used to provide the number of bytes that should be clocked out during the actual FIFO read.

Any error in the data format, parity, or CRC is detected and notified to the external system by an interrupt-request pulse. The source condition of the interrupt request pulse is available in the IRQ status register (0x0C). The main register controlling the digital part of the receiver is the ISO Control register (0x01). By writing to this register, the user selects the protocol to be used. With each new write in this register, the default presets are reloaded in all related registers, so no further adjustments in other registers are needed for proper operation.

NOTE

If register setting changes are needed for fine tuning the system, they must be done after setting the ISO Control register (0x01).

The framing section also supports the bit-collision detection as specified in ISO14443A. When a bit collision is detected, an interrupt request is sent and a flag is set in the IRQ and Status Register (0x0C). The position of the bit collision is written in two registers: Collision Position Register (0x0E) and partly in Collision Position and Interrupt Mask Register (0x0D) (bits B6 and B7).

The collision position is presented as sequential bit number, where the count starts immediately after the start bit. This means a collision in the first bit of a UID would give the value 00 0001 0000 in these registers when their contents are combined after being read. (the count starts with 0 and the first 16 bits are the command code and the Number of Valid Bits (NVB) byte)

The receive section also contains two timers. The RX wait time timer is controlled by the value in the RX Wait Time Register (0x08). This timer defines the time interval after the end of the transmit operation in which the receive decoders are not active (held in reset state). This prevents false detections resulting from transients following the transmit operation. The value of the RX Wait Time Register (0x08) defines the time in increments of 9.44 µs. This register is preset at every write to ISO Control Register (0x01) according to the minimum tag response time defined by each standard.

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The RX no response timer is controlled by the RX No Response Wait Time Register (0x07). This timer measures the time from the start of slot in the anticollision sequence until the start of tag response. If there is no tag response in the defined time, an interrupt request is sent and a flag is set in the IRQ Status Register (0x0C). This enables the external controller to be relieved of the task of detecting empty slots. The wait time is stored in the register in increments of 37.76 µs. This register is also preset, automatically for every new protocol selection.

The digitized output of the analog receiver is at the input of the digital portion of the receiver. This input signal is the subcarrier coded signal, which is a digital representation of modulation signal on the RF envelope.

The digital part of the receiver consists of two sections which partly overlap. The first section contains the bit decoders for the various protocols. The bit decoders convert the subcarrier coded signal to a bit stream and also the data clock. Thus the subcarrier coded signal is transformed to serial data and the data clock is extracted. The decoder logic is designed for maximum error tolerance. This enables the decoders to successfully decode even partly corrupted (due to noise or interference) subcarrier signals.

The second section contains the framing logic for the protocols supported by the bit decoder section. In the framing section, the serial bit stream data is formatted in bytes. In this process, special signals like the SOF (start of frame), EOF (end of frame), start of communication, end of communication are automatically removed. The parity bits and CRC bytes are checked and also removed. The end result is "clean or raw" data which is sent to the 128-byte FIFO register where it can be read out by the external microcontroller system.

The start of the receive operation (successfully received SOF) sets the flags in the IRQ and Status register. The end of the receive operation is signaled to the external system (MCU) by sending an interrupt request (pin 13 IRQ). If the receive data packet is longer than 96 bytes, an interrupt is sent to the MCU when the received data occupies 75% of the FIFO capacity to signal that the data should be removed from the FIFO.

Any error in data format, parity or CRC is detected and the external system is made aware of the error by an interrupt request pulse. The nature of the interrupt request pulse is available in the IRQ and Status register (address 0x0C). The bit coding description of this register is shown in Section 6.3.3.1. The information in IRQ and Status register differs if the chip is configured as RFID reader or as NFC device (including tag emulation). The case of NFC operation is presented in Section 5.11.

The main register controlling the digital part of the receiver is the ISO Control register (address 0x01). By writing to this register, the user selects the protocol to be used. At the same time (with each new write in this register) the default preset in all related registers is done, so no further adjustments in other registers are needed for proper operation. Table 5-5 shows the coding of the ISO Control register (0x01).

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Table 5-5. Coding of the ISO Control Register

Bit	Signal Name	Function	Comments
B7	rx_crc_n	Receiving without CRC	1 = No RX CRC 0 = RX CRC
B6	dir_mode	Direct mode type	0 = output is subcarrier data 1 = output is bit stream and clock from decoder selected by ISO bits
B5	rfid	RFID mode	0 = RFID reader mode 1 = NFC or Card Emulator mode
B4	iso_4	RFID protocol, NFC target	RFID: Mode selection NFC: 0 = NFC target 1 = NFC initiator
B3	iso_3	RFID protocol, NFC mode	RFID: Mode selection (see Table 5-6) NFC: 0 = passive mode 1 = active mode
B2	iso_2	RFID protocol, Card Emulation	RFID: Mode selection NFC: 0 = NFC normal modes 1 = Card Emulation mode
B1	iso_1	RFID protocol, NFC bit rate	RFID: Mode selection NFC: Bit rate selection or Card Emulation selection (see Table 5-7)
B0	iso_0	RFID protocol, NFC bit rate	RFID: Mode selection NFC: Bit rate selection or Card Emulation selection (see Table 5-7)

Table 5-6. Coding of the ISO Control Register For RFID Mode (B5 = 0)

Iso_4	Iso_3	Iso_2	Iso_1	Iso_0	Protocol	Remarks
0	0	0	0	0	ISO15693 low bit rate, one subcarrier, 1 out of 4	
0	0	0	0	1	ISO15693 low bit rate, one subcarrier, 1 out of 256	
0	0	0	1	0	ISO15693 high bit rate, one subcarrier, 1 out of 4	Default for RFID IC
0	0	0	1	1	ISO15693 high bit rate, one subcarrier, 1 out of 256	
0	0	1	0	0	ISO15693 low bit rate, double subcarrier, 1 out of 4	
0	0	1	0	1	ISO15693 low bit rate, double subcarrier, 1 out of 256	
0	0	1	1	0	ISO15693 high bit rate, double subcarrier, 1 out of 4	
0	0	1	1	1	ISO15693 high bit rate, double subcarrier, 1 out of 256	
0	1	0	0	0	ISO14443A, bit rate 106 kbps	
0	1	0	0	1	ISO14443 A high bit rate 212 kbps	RX bit rate when TX rate different than RX rate (see register 0x03)
0	1	0	1	0	ISO14443 A high bit rate 424 kbps	
0	1	0	1	1	ISO14443 A high bit rate 848 kbps	
0	1	1	0	0	ISO14443B, bit rate 106 kbps	
0	1	1	0	1	ISO14443 B high bit rate 212 kbps	RX bit rate when TX rate different than RX rate (see register 0x03)
0	1	1	1	0	ISO14443 B high bit rate 424 kbps	
0	1	1	1	1	ISO14443 B high bit rate 848 kbps	
1	0	0	1	1	Reserved	
1	0	1	0	0	Reserved	
1	1	0	1	0	FeliCa 212 kbps	
1	1	0	1	1	FeliCa 424 kbps	

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Table 5-7. Coding of the ISO Control Register For NFC Mode (B5 = 1, B2 = 0) or Card Emulation (B5 = 1, B2 = 1)

Iso_1	Iso_0	NFC (B5 = 1, B2 = 0)	Card Emulation (B5 = 1, B2 = 1)
0	0	N/A	ISO14443A
0	1	106 kbps	ISO14443B
1	0	212 kbps	N/A
1	1	424 kbps	N/A

The framing section also supports the bit collision detection as specified in ISO14443A. In the event of a detected bit collision, an interrupt request is sent and flag set in the IRQ and Status registers. The position of the bit collision is written in two registers: the Collision Position register (0x0E) and partly in the Collision Position and Interrupt Mask register (0x0D), in which only the bits B7 and B6 are used for collision position. The collision position is presented as sequential bit number, where the counting starts immediately after the start bit. This means, the collision in the first bit of the UID would give value 00 0001 0000 in the collision position registers (the counting starts with 0 and the first 16 bits are the command code and the NVB byte).

The receive part also contains two timers. The RX wait time timer setting is controlled by the value in the RX Wait Time register (0x08). This timer defines the time after the end of transmit operation in which the receive decoders are not active (held in reset state). This prevents any incorrect detections from occurring as a result of transients following the transmit operation. The value of the RX Wait Time register defines this time with increments of 9.44 µs. This register is preset at every write to the ISO Control register (0x01) according to the minimum tag response time defined by each standard.

The RX no response timer setting is controlled by the RX No Response Wait Time register (0x07). This timer measures the time from the start of slot in the anticollision sequence until the start of tag response. If there is no tag response in the defined time, an interrupt request is sent and a flag is set in IRQ Status Control register. This enables the external controller to be relieved of the task of detecting empty slots. The wait time is stored in the register with increments of 37.76 µs. This register is also preset, automatically, for every new protocol selection.

5.4.1 Received Signal Strength Indicator (RSSI)

The TRF7970A incorporates in total three independent RSSI building blocks: Internal Main RSSI, Internal Auxiliary RSSI, and External RSSI. The internal RSSI blocks are measuring the amplitude of the subcarrier signal; the External RSSI block measures the amplitude of the RF carrier signal at the receiver input.

5.4.1.1 Internal RSSI – Main and Auxiliary Receivers

Each receiver path has its own RSSI block to measure the envelope of the demodulated RF signal (subcarrier). Internal Main RSSI and Internal Auxiliary RSSI are identical however connected to different RF input pins. The Internal RSSI is intended for diagnostic purposes to set the correct RX path conditions.

The Internal RSSI values can be used to adjust the RX gain settings or decide which RX path (Main or Auxiliary) provides the greater amplitude and hence to decide if the MUX may need to be reprogrammed to swap the RX input signal. The measuring system latches the peak value, so the RSSI level can be read after the end of each receive packet. The RSSI register values are reset with every transmission (TX) by the reader. This guarantees an updated RSSI measurement for each new tag response.

The Internal RSSI has 7 steps (3 bit) with a typical increment of approximately 4 dB. The operating range is between 600 mV_{PP} and 4.2 V_{PP} with a typical step size of approximately 600 mV. Both Internal Main and Internal Auxiliary RSSI values are stored in the RSSI Levels and Oscillator Status register (0x0F). The nominal relationship between the input RF peak level and the RSSI value is shown in Figure 5-2.

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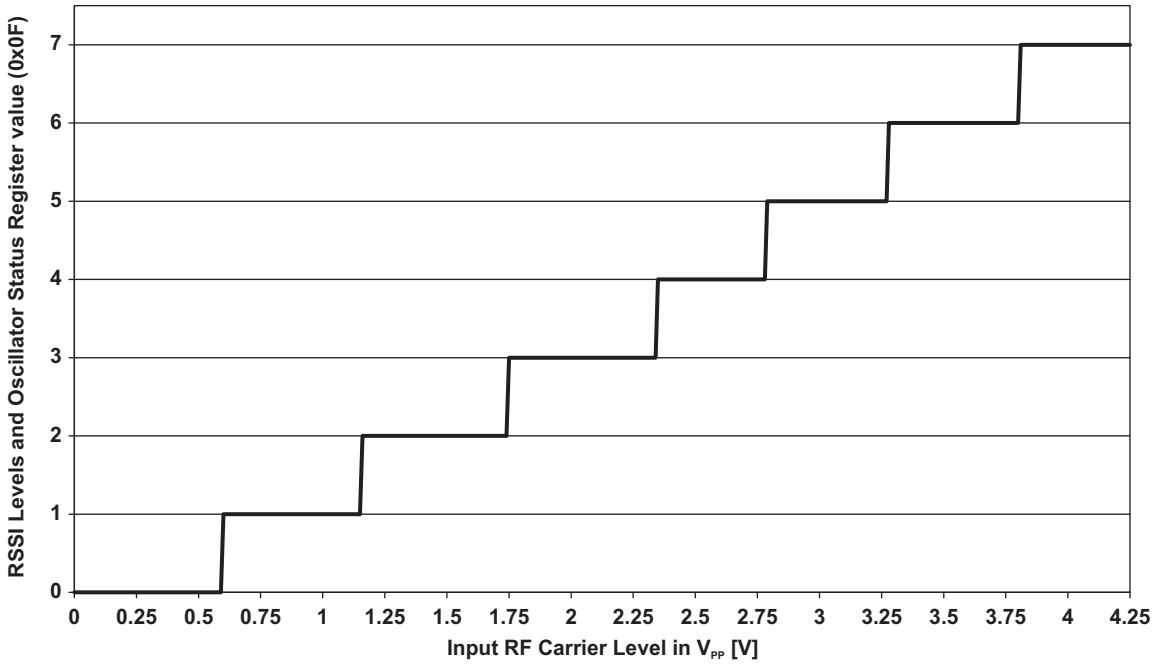


Figure 5-2. Digital Internal RSSI (Main and Auxiliary) Value vs RF Input Level in V_{PP} (V)

This RSSI measurement is done during the communication to the Tag; this means the TX must be on. Bit1 in the Chip Status Control Register (0x00) defines if Internal RSSI or the External RSSI value is stored in the RSSI Levels and Oscillator Status Register 0x0F. Direct command 0x18 is used to trigger an Internal RSSI measurement.

5.4.1.2 External RSSI

The External RSSI is mainly used for test and diagnostic to sense the amplitude of any 13.56-MHz signal at the receivers RX_IN1 input. The External RSSI measurement is typically done in active mode when the receiver is on but transmitter output is off. The level of the RF signal received at the antenna is measured and stored in the RSSI Levels and Oscillator Status register 0x0F. The relationship between the voltage at the RX_IN1 input and the 3-bit code is shown in Figure 5-3.

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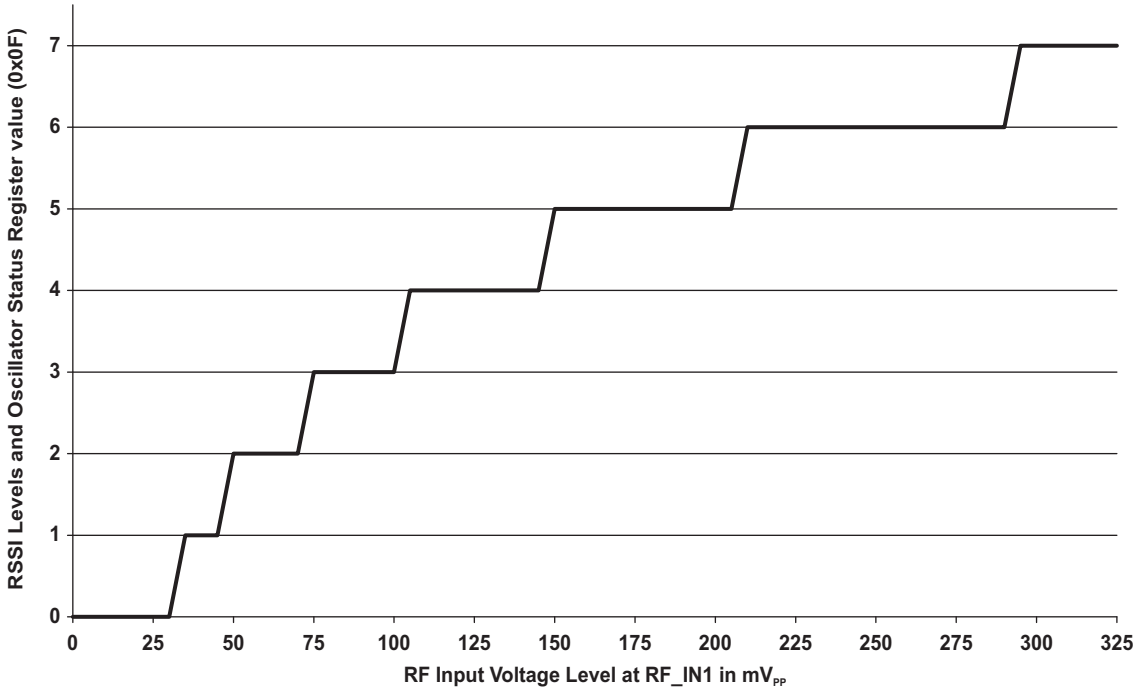


Figure 5-3. Digital External RSSI Value vs RF Input Level in V_{PP} (mV)

The relation between the 3-bit code and the external RF field strength (A/m) sensed by the antenna must be determined by calculation or by experiments for each antenna design. The antenna Q-factor and connection to the RF input influence the result. Direct command 0x19 is used to trigger an Internal RSSI measurement.

For clarity, to check the internal or external RSSI value independent of any other operation, the user must:

- Set transmitter to desired state (on or off) using Bit 5 of Chip Status Control Register (0x00)
- Set the receiver using direct command 0x17.
- Check internal or external RSSI using direct commands 0x18 or 0x19, respectively. This action places the RSSI value in the RSSI register
- Read the RSSI register using direct command 0x0F; values range from 0x40 to 0x7F.
- Repeat steps 1-4 as desired, as register is reset after it is read.

5.5 Oscillator Section

The 13.56-MHz or 27.12-MHz crystal (or oscillator) is controlled by the Chip Status Control Register (0x00) and the EN and EN2 terminals. The oscillator generates the RF frequency for the RF output stage as well as the clock source for the digital section. The buffered clock signal is available at pin 27 (SYS_CLK) for any other external circuits. B4 and B5 inside the Modulation and SYS_CLK Register (0x09) can be used to divide the external SYS_CLK signal at pin 27 by 1, 2 or 4.

Typical start-up time from complete power down is in the range of 3.5 ms.

During Power Down Mode 2 (EN = 0, EN2 = 1) the frequency of SYS_CLK is switched to 60 kHz (typical).

The crystal needs to be connected between pin 31 and pin 32. The external shunt capacitors values for C_1 and C_2 must be calculated based on the specified load capacitance of the crystal being used. The external shunt capacitors are calculated as two identical capacitors in series plus the stray capacitance of the TRF7970A and parasitic PCB capacitance in parallel to the crystal.

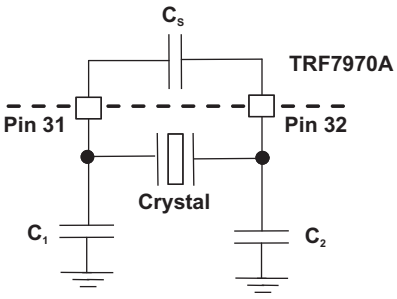
The parasitic capacitance (C_S, stray and parasitic PCB capacitance) can be estimated at 4 to 5 pF (typical).

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As an example, using a crystal with a required load capacitance (C_L) of 18 pF, the calculation is shown in Equation 1.

$$C_1 = C_2 = 2 \times (C_L - C_S) = 2 \times (18\ pF - 4.5\ pF) = 27\ pF \quad (1)$$

A 27-pF capacitor must be placed on pins 30 and 31 to ensure proper crystal oscillator operation.



$C_1 = C_2 = 2 \times (C_L - C_S) = 2 \times (18\ pF - 4.5\ pF) = 27\ pF$

A 27-pF capacitor needs to be placed on pins 30 and 31 to ensure proper crystal oscillator operation.

Figure 5-4. Crystal Block Diagram

Any crystal used with TRF7970A should have minimum characteristics shown in Table 5-8.

Table 5-8. Minimum Crystal Requirements

Parameter	Specification
Frequency	13.56 MHz or 27.12 MHz
Mode of Operation	Fundamental
Type of Resonance	Parallel
Frequency Tolerance	±20 ppm
Aging	< 5 ppm/year
Operation Temperature Range	-40°C to 85°C
Equivalent Series Resistance	50 Ω

As an alternative, an external clock oscillator source can be connected to Pin 31 to provide the system clock; pin 32 can be left open.

5.6 Transmitter – Analog Section

The 13.56-MHz oscillator generates the RF signal for the PA stage. The power amplifier consists of a driver with selectable output resistance of nominal 4 Ω or 8 Ω. The transmit power level is set by bit B4 in the Chip Status Control Register (0x00). The transmit power levels are selectable between 100 mW (half power) or 200 mW (full power) when configured for 5-V automatic operation. The transmit power levels are selectable between 33 mW (half power) or 70 mW (full power) when configured for 3-V automatic operation.

The ASK modulation depth is controlled by bits B0, B1, and B2 in the Modulator and SYS_CLK Control Register (0x09). The ASK modulation depth range can be adjusted between 7% to 30% or 100% (OOK).

External control of the transmit modulation depth is possible by setting the ISO Control Register (0x01) to direct mode. While operating the TRF7970A in direct mode, the transmit modulation is made possible by selecting the modulation type ASK or OOK at pin 12. External control of the modulation type is made possible only if enabled by setting B6 in the Modulator and SYS_CLK Control Register (0x09) to 1.

In normal operation mode, the length of the modulation pulse is defined by the protocol selected in the ISO Control Register (0x01). With a high-Q antenna, the modulation pulse is typically prolonged, and the tag detects a longer pulse than intended. For such cases, the modulation pulse length needs to be corrected by using the TX Pulse Length Register (0x05).

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If the register contains all zeros, then the pulse length is governed by the protocol selection. If the register contains a value other than 0x00, the pulse length is equal to the value of the register multiplied by 73.7 ns; therefore, the pulse length can be adjusted between 73.7 ns and 18.8 s in 73.7-ns increments.

5.7 Transmitter – Digital Section

The digital part of the transmitter is a mirror of the receiver. The settings controlled the ISO Control Register (0x01) are applied to the transmitter just like the receiver. In the TRF7970A default mode the TRF7970A automatically adds these special signals: start of communication, end of communication, SOF, EOF, parity bits, and CRC bytes.

The data is then coded to modulation pulse levels and sent to the RF output stage modulation control unit. Similar to working with the receiver, this means that the external system MCU only has to load the FIFO with data and all the microcoding is done automatically, again saving the firmware developer code space and time. Additionally, all of the registers used for transmit parameter control are automatically preset to optimum values when a new selection is entered into the ISO Control register (0x01).

Note: FIFO must be reset before starting any transmission with Direct Command 0x0F.

There are two ways to start the transmit operation:

- Load the number of bytes to be sent into registers 0x1D and 0x1E and load the data to be sent into the FIFO (address 0x1F), followed by sending a transmit command (see Direct Commands section). The transmission then starts when the transmit command is received.
- Send the transmit command and the number of bytes to be transmitted first, and then start to send the data to the FIFO. The transmission starts when first data byte is written into the FIFO.

NOTE

If the data length is longer than the FIFO, the TRF7970A notifies the external system MCU when most of the data from the FIFO has been transmitted by sending an interrupt request with a flag in the IRQ register to indicate a FIFO low or high status. The external system should respond by loading the next data packet into the FIFO.

At the end of a transmit operation, the external system MCU is notified by interrupt request (IRQ) with a flag in IRQ Register (0x0C) indicating TX is complete (example value = 0x80).

The TX Length registers also support incomplete byte transmission. The high two nibbles in register 0x1D and the nibble composed of bits B4 through B7 in register 0x1E store the number of complete bytes to be transmitted. Bit B0 in register 0x1E is a flag indicating that there are also additional bits to be transmitted that do not form a complete byte. The number of bits is stored in bits B1 through B3 of the same register (0x1E).

Some protocols have options, and there are two sublevel configuration registers to select the TX protocol options.

- ISO14443B TX Options register (0x02). This register controls the SOF and EOF selection and EGT selection for the ISO14443B protocol.
- ISO14443A High Bit Rate Options and Parity register (0x03). This register enables the use of different bit rates for RX and TX operations in the ISO14443 high bit rate protocol and also selects the parity method in the ISO14443A high bit rate protocol.

The digital section also has a timer. The timer can be used to start the transmit operation at a specified time in accordance with a selected event.

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5.8 Transmitter – External Power Amplifier and Subcarrier Detector

The TRF7970A can be used in conjunction with an external TX power amplifier or external subcarrier detector for the receiver path. In this case, certain registers must be programmed as shown here:

- Bit B6 of the Regulator and I/O Control Register (0x0B) must be set to 1. This setting has two functions: first, to provide a modulated signal for the transmitter if needed, and second, to configure the TRF7970A receiver inputs for an external demodulated subcarrier input.
- Bit B3 of the Modulation and SYS_CLK Control Register (0x09) must be set to 1 (see Section 6.3.2.8). This function configures the ASK/OOK pin for either a digital or analog output (B3 = 0 enables a digital output, B3 = 1 enables an analog output). The design of an external power amplifier requires detailed RF knowledge. There are also readily designed and certified high-power HF reader modules on the market.

5.9 TRF7970A IC Communication Interface

5.9.1 General Introduction

The communication interface to the reader can be configured in two ways: with a eight line parallel interface (D0:D7) plus DATA_CLK, or with a three or four wire Serial Peripheral Interface (SPI). The SPI interface uses traditional Master Out/Slave In (MOSI), Master In/Slave Out (MISO), IRQ, and DATA_CLK lines. The SPI can be operated with or without using the Slave Select line.

These communication modes are mutually exclusive; that is, only one mode can be used at a time in the application.

When the SPI interface is selected, the unused I/O_2, I/O_1, and I/O_0 pins must be hard-wired as shown in Table 5-9. At power up, the TRF7970A samples the status of these three pins and then enters one of the possible SPI modes.

The TRF7970A always behaves as the slave device, and the microcontroller (MCU) behaves as the master device. The MCU initiates all communications with the TRF7970A, and the TRF7970A makes use of the Interrupt Request (IRQ) pin in both parallel and SPI modes to prompt the MCU for servicing attention.

Table 5-9. Pin Assignment in Parallel and Serial Interface Connection or Direct Mode

Pin	Parallel	Parallel (Direct Mode)	SPI With SS	SPI Without SS
DATA_ CLK	DATA_CLK	DATA_CLK	DATA_CLK from master	DATA_CLK from master
I/O_7	A/D[7]	(not used)	MOSI(1) = data in (reader in)	MOSI(1) = data in (reader in)
I/O_6	A/D[6]	Direct mode, data out (subcarrier or bit stream)	MISO(2) = data out (MCU out)	MISO(2) = data out (MCU out)
I/O_5(3)	A/D[5]	Direct mode, strobe – bit clock out	See (3)	See (3)
I/O_4	A/D[4]	(not used)	SS – slave select(4)	(not used)
I/O_3	A/D[3]	(not used)	(not used)	(not used)
I/O_2	A/D[2]	(not used)	At VDD	At VDD
I/O_1	A/D[1]	(not used)	At VDD	At V_{SS}
I/O_0	A/D[0]	(not used)	At V_{SS}	At V_{SS}
IRQ	IRQ interrupt	IRQ interrupt	IRQ interrupt	IRQ interrupt

(1) MOSI = Master Out, Slave In
(2) MISO = Master In, Slave Out
(3) I/O_5 pin is used only for information when data is put out of the chip (for example, reading 1 byte from the chip). It is necessary first to write in the address of the register (8 clocks) and then to generate another 8 clocks for reading out the data. The I/O_5 pin goes high during the second 8 clocks. But for normal SPI operations, I/O_5 pin is not used.
(4) Slave_Select pin is active low

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Communication is initialized by a start condition, which is expected to be followed by an Address/Command word (Adr/Cmd). The Adr/Cmd word is 8 bits long, and its format is shown in Table 5-10.

Table 5-10. Address/Command Word Bit Distribution

Bit	Description	Bit Function	Address	Command
B7	Command control bit	0 = address 1 = command	0	1
B6	Read/Write	0 = write 1 = read	R/W	0
B5	Continuous address mode	1 = Continuous mode	R/W	0
B4	Address/Command bit 4		Adr 4	Cmd 4
B3	Address/Command bit 3		Adr 3	Cmd 3
B2	Address/Command bit 2		Adr 2	Cmd 2
B1	Address/Command bit 1		Adr 1	Cmd 1
B0	Address/Command bit 0		Adr 0	Cmd 0

The MSB (bit 7) determines if the word is to be used as a command or as an address. The last two columns of Table 5-10 show the function of the separate bits if either address or command is written. Data is expected once the address word is sent. In continuous-address mode (Cont. mode = 1), the first data that follows the address is written (or read) to (from) the given address. For each additional data, the address is incremented by one. Continuous mode can be used to write to a block of control registers in a single stream without changing the address; for example, setup of the predefined standard control registers from the MCU non-volatile memory to the reader. In non-continuous address mode (simple addressed mode), only one data word is expected after the address.

Address Mode is used to write or read the configuration registers or the FIFO. When writing more than 12 bytes to the FIFO, the Continuous Address Mode should be set to 1.

The Command Mode is used to enter a command resulting in reader action (for example, initialize transmission, enable reader, and turn reader on or off).

Examples of expected communications between an MCU and the TRF7970A are shown in the following sections.

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5.9.1.1 Continuous Address Mode

Table 5-11. Continuous Address Mode

Start	Adr x	Data(x)	Data(x+1)	Data(x+2)	Data(x+3)	Data(x+4)	...	Data(x+n)	StopCont

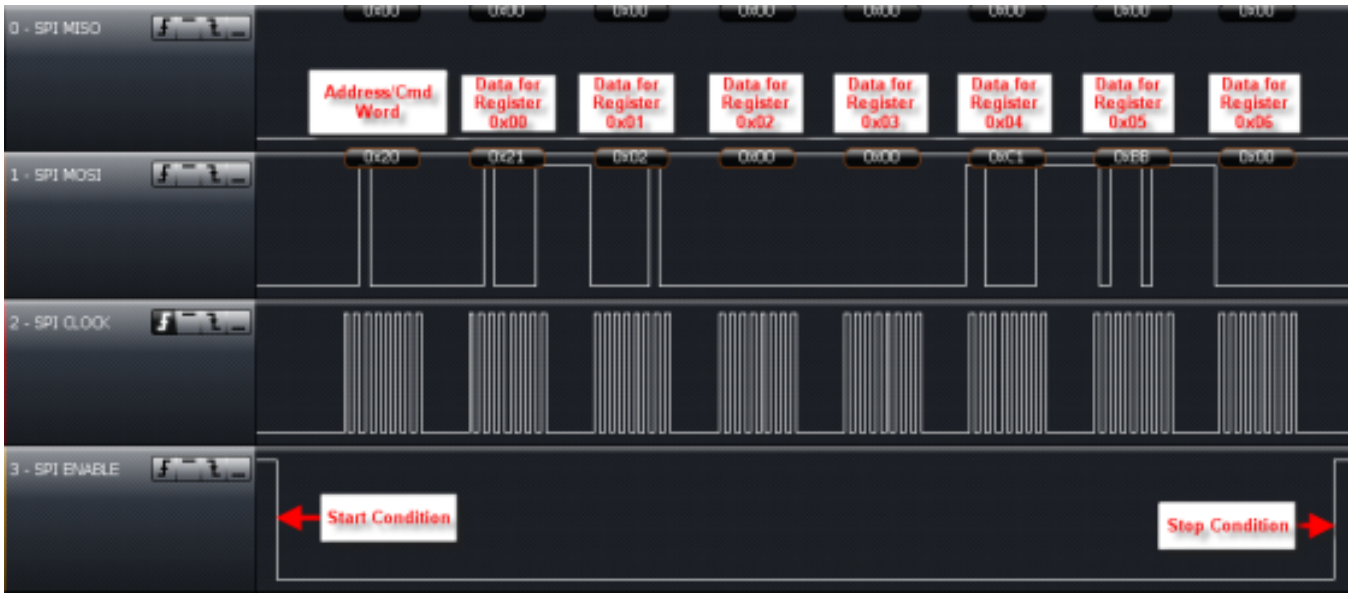


Figure 5-5. Continuous Address Register Write Example Starting with Register 0x00 Using SPI With SS

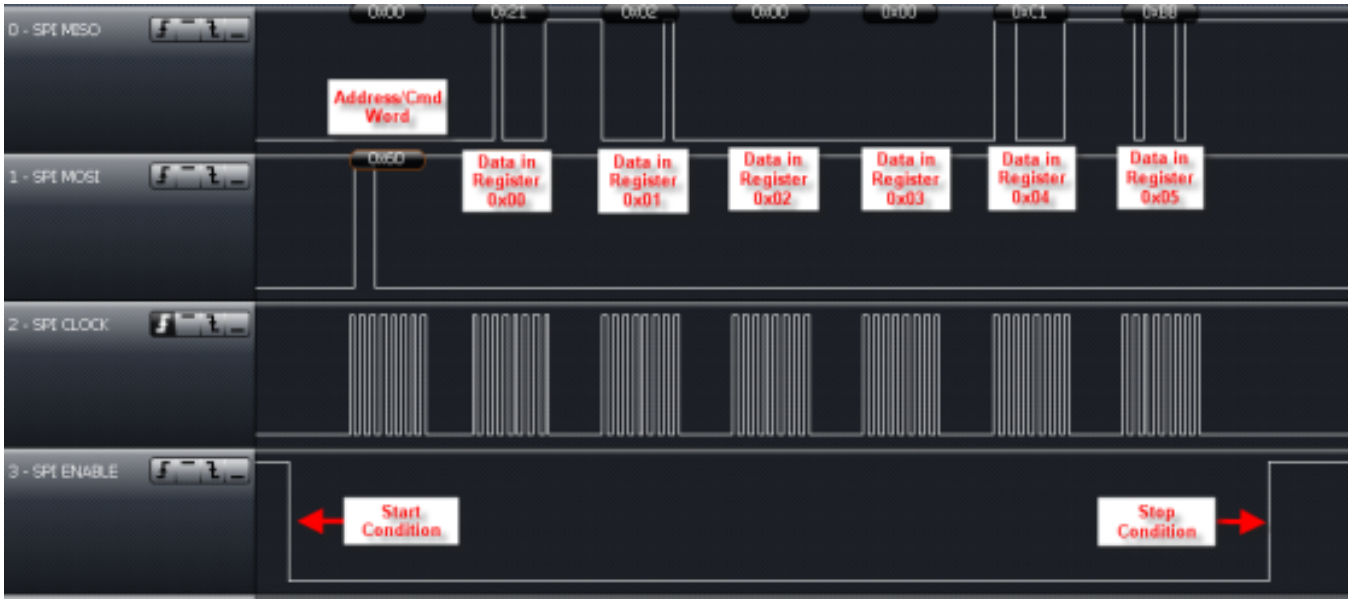


Figure 5-6. Continuous Address Register Read Example Starting with Register 0x00 Using SPI With SS

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5.9.1.2 Noncontinuous Address Mode (Single Address Mode)

Table 5-12. Noncontinuous Address Mode (Single Address Mode)

Start	Adr x	Data(x)	Adr y	Data(y)	...	Adr z	Data(z)	StopSgl

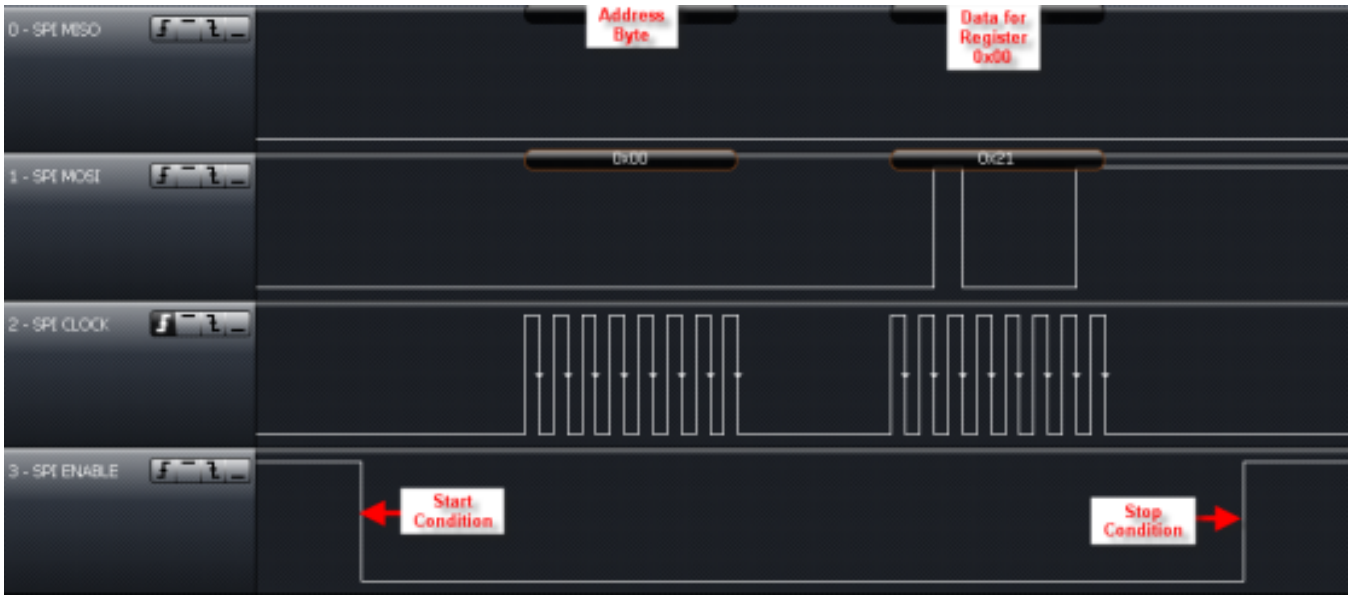


Figure 5-7. Single Address Register Write Example of Register 0x00 Using SPI With SS

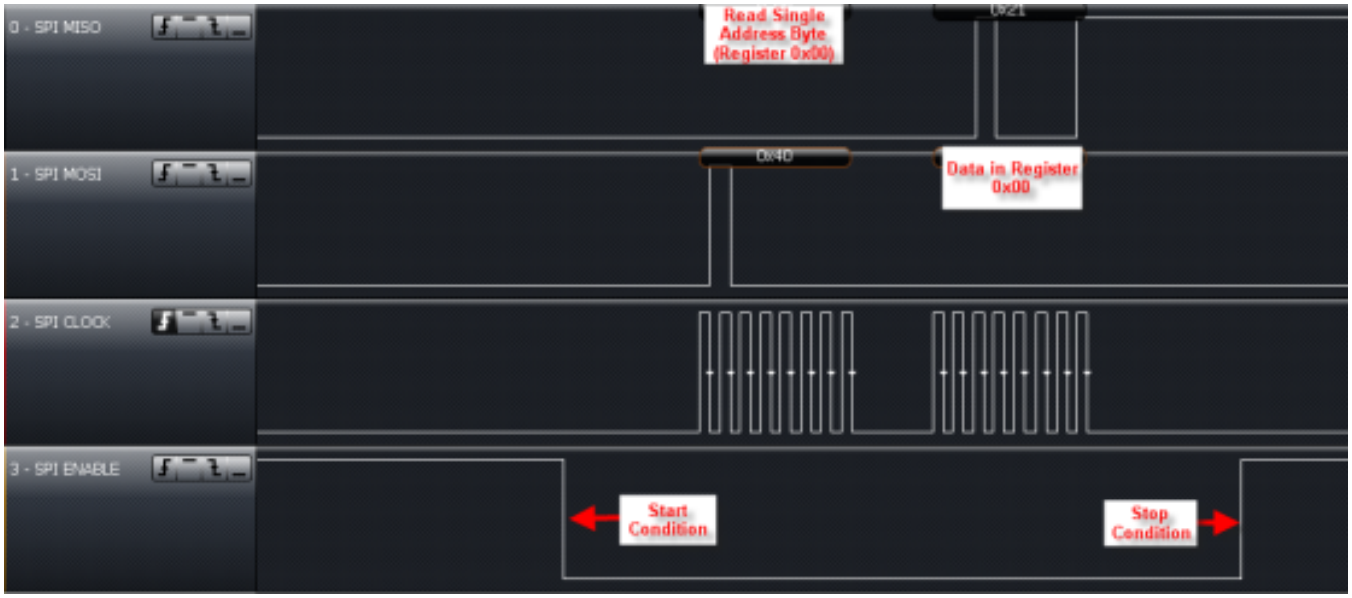


Figure 5-8. Single Address Register Read Example of Register 0x00 Using SPI With SS

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5.9.1.3 Direct Command Mode

Table 5-13. Direct Command Mode

Start	Cmd x	(Optional data or command)	Stop

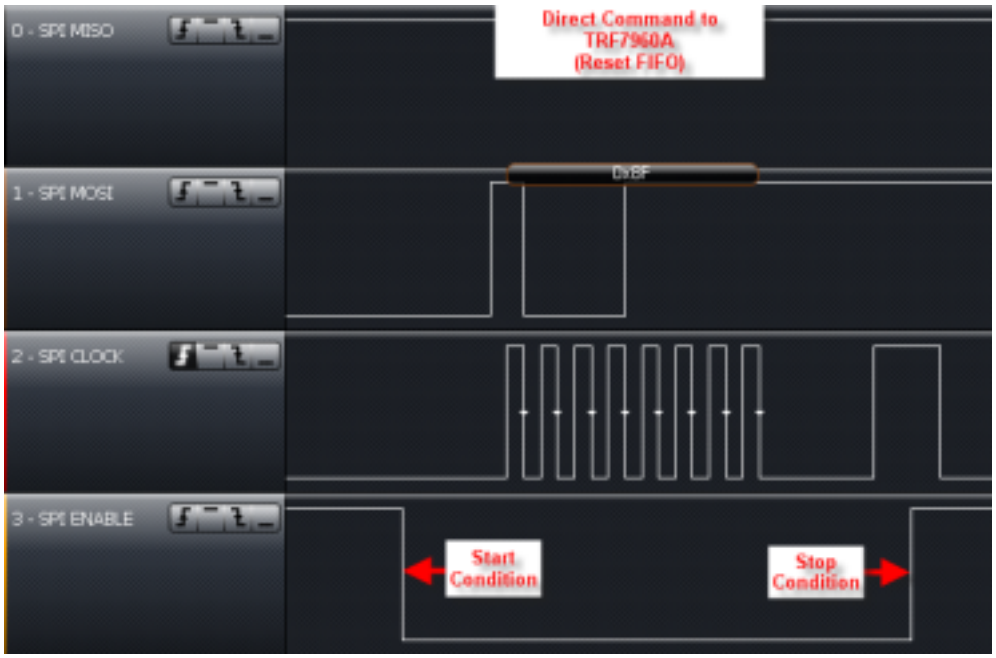


Figure 5-9. Direct Command Example of Sending 0x0F (Reset) Using SPI With SS

The other Direct Command Codes from MCU to TRF7970A IC are described in Section 5.12.

5.9.1.4 FIFO Operation

The FIFO is a 128-byte register at address 0x1F with byte storage locations 0 to 127. FIFO data is loaded in a cyclical manner and can be cleared by a reset command (0x0F) (see Figure 5-9 showing this Direct Command).

Associated with the FIFO are two counters and three FIFO status flags. The first counter is a 7-bit FIFO byte counter (bits B0 to B6 in register 0x1C) that tracks the number of bytes loaded into the FIFO. If the number of bytes in the FIFO is n, the register value is n (number of bytes in FIFO register). For example, if 8 bytes are in the FIFO, the FIFO counter (Register 0x1C) has the hexadecimal value of 0x08 (binary value of 00001000).

A second counter (12 bits wide) indicates the number of bytes being transmitted (registers 0x1D and 0x1E) in a data frame. An extension to the transmission-byte counter is a 4-bit broken-byte counter also provided in register 0x1E (bits B0 to B3). Together these counters make up the TX length value that determines when the reader generates the EOF byte.

FIFO status flags are as follows:

- **FIFO overflow** (bit B7 of register 0x1C) – indicates that the FIFO has more than 128 bytes loaded

During transmission, the FIFO is checked for an almost-empty condition, and during reception for an almost-full condition. The maximum number of bytes that can be loaded into the FIFO in a single sequence is 128 bytes.

NOTE

The number of bytes in a frame, transmitted or received, can be greater than 128 bytes.

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During transmission, the MCU loads the TRF7970A IC's FIFO (or during reception the MCU removes data from the FIFO), and the FIFO counter counts the number of bytes being loaded into the FIFO. Meanwhile, the byte counter keeps track of the number of bytes being transmitted. An interrupt request is generated if the number of bytes in the FIFO is less than 32 or greater than 96, so that MCU can send new data or remove the data as necessary. The MCU also checks the number of data bytes to be sent, so as to not surpass the value defined in *TX length bytes*. The MCU also signals the transmit logic when the last byte of data is sent or was removed from the FIFO during reception. Transmission starts automatically after the first byte is written into FIFO.

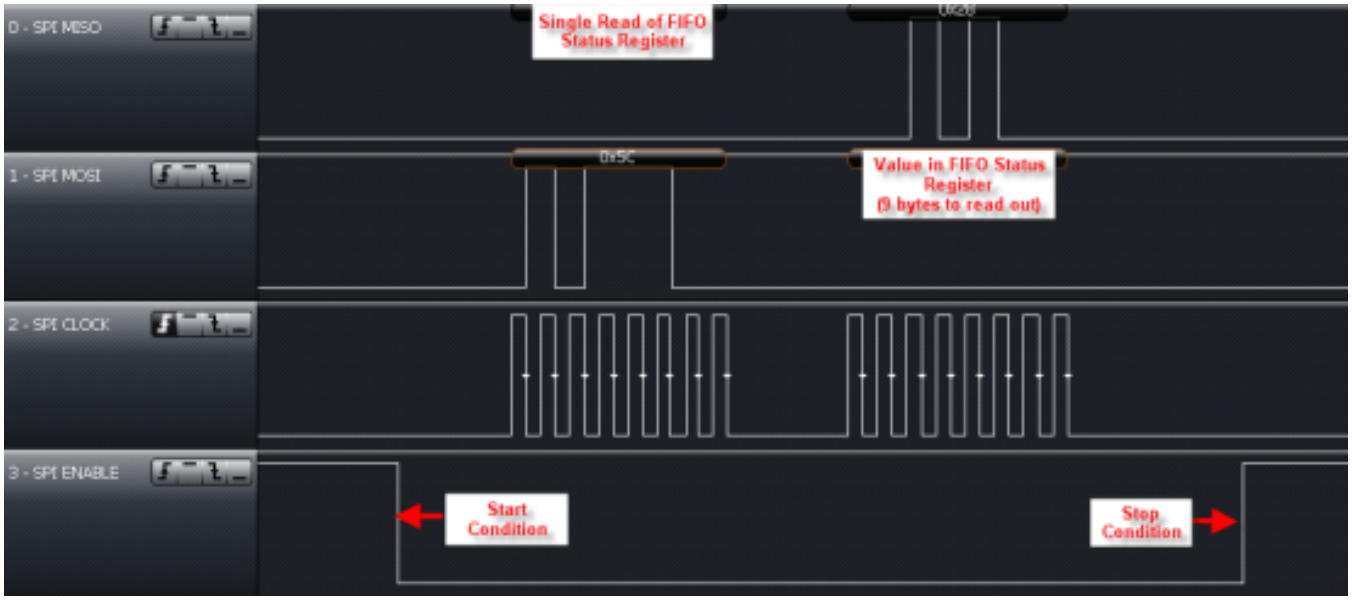


Figure 5-10. Example of Checking the FIFO Status Register Using SPI With SS

5.9.2 Parallel Interface Mode

In parallel mode, the start condition is generated on the rising edge of the I/O_7 pin while the CLK is high.

This is used to reset the interface logic. Figure 5-11 shows the sequence of the data, with an 8-bit address word first, followed by data.

Communication is ended by:

- The StopSmpl condition, where a falling edge on the I/O_7 pin is expected while CLK is high.
- The StopCont condition, where the I/O_7 pin must have a successive rising and falling edge while CLK is low to reset the parallel interface and be ready for the new communication sequence.
- The *StopSmpl* condition is also used to terminate the direct mode.

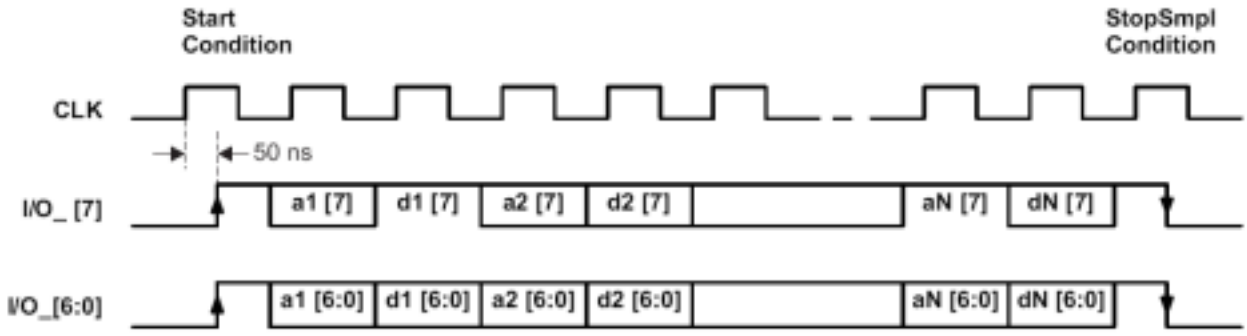


Figure 5-11. Parallel Interface Communication With Simple Stop Condition (StopSmpl)

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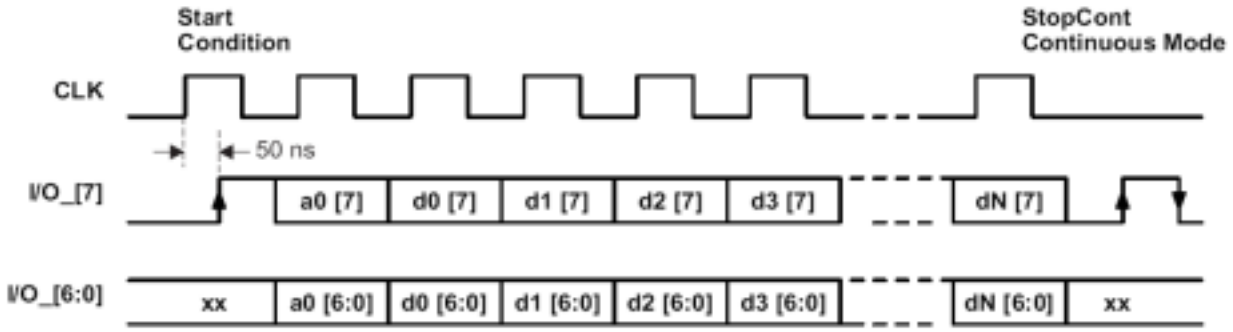


Figure 5-12. Parallel Interface Communication with Continuous Stop Condition (StopCont)

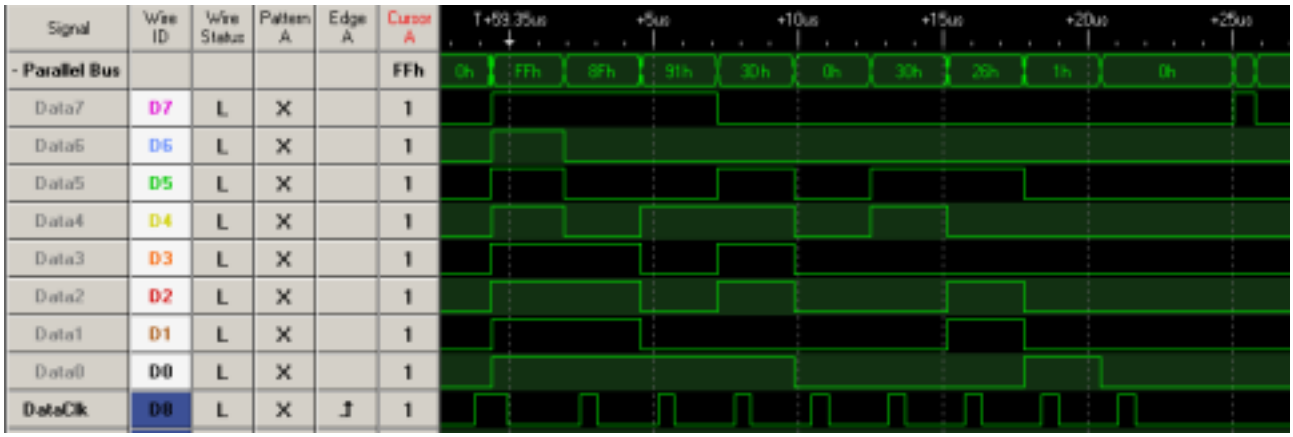


Figure 5-13. Example of Parallel Interface Communication with Continuous Stop Condition

5.9.3 Reception of Air Interface Data

At the start of a receive operation (when SOF is successfully detected), B6 is set in the IRQ Status register. An interrupt request is sent to the MCU at the end of the receive operation if the receive data string was shorter than or equal to 8 bytes. The MCU receives the interrupt request, then checks to determine the reason for the interrupt by reading the IRQ Status register (0x0C), after which the MCU reads the data from the FIFO.

If the received packet is longer than 96 bytes, the interrupt is sent before the end of the receive operation when the 96th byte is loaded into the FIFO (75% full). The MCU should again read the content of the IRQ Status register to determine the cause of the interrupt request. If the FIFO is 75% full (as marked with flag B5 in IRQ Status register and by reading the FIFO Status register), the MCU should respond by reading the data from FIFO to make room for new incoming receive data. When the receive operation is finished, the interrupt is sent and the MCU must check how many words are still present in the FIFO before it finishes reading.

If the reader detects a receive error, the corresponding error flag is set (framing error, CRC error) in the IRQ Status register, indicating to the MCU that reception was not completed correctly.

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5.9.4 Data Transmission to MCU

Before beginning data transmission, the FIFO should always be cleared with a reset command (0x0F). Data transmission is initiated with a selected command (see Section 5.12). The MCU then commands the reader to do a continuous write command (0x3D) starting from register 0x1D. Data written into register 0x1D is the TX Length Byte1 (upper and middle nibbles), while the following byte in register 0x1E is the TX Length Byte2 (lower nibble and broken byte length) (see Table 6-34 and Table 6-35) . Note that the TX byte length determines when the reader sends the end of frame (EOF) byte. After the TX length bytes are written, FIFO data is loaded in register 0x1F with byte storage locations 0 to 127. Data transmission begins automatically after the first byte is written into the FIFO. The loading of TX length bytes and the FIFO can be done with a continuous-write command, as the addresses are sequential.

At the start of transmission, the flag B7 (IRQ_TX) is set in the IRQ Status register, and at the end of the transmit operation, an interrupt is sent to inform the MCU that the task is complete.

5.9.5 Serial Interface Communication (SPI)

When an SPI interface is used, I/O pins I/O_2, I/O_1, and I/O_0 must be hard wired according to Table 5-9. On power up, the TRF7970A looks for the status of these pins and then enters into one of two possible SPI modes:

- SPI with Slave Select
- SPI without Slave Select

The choice of one of these modes over another should be predicated by the available GPIOs and the desired control of the system.

The serial communications work in the same manner as the parallel communications with respect to the FIFO, except for the following condition. On receiving an IRQ from the reader, the MCU reads the TRF7970A IRQ Status register to determine how to service the reader. After this, the MCU must to do a dummy read to clear the reader's IRQ status register. The dummy read is required in SPI mode because the reader's IRQ status register needs an additional clock cycle to clear the register. This is not required in parallel mode because the additional clock cycle is included in the Stop condition. When first establishing communications with the TRF7970A, the SOFT_INIT (0x03) command should be sent first from the MCU (see Table 5-18).

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The procedure for a dummy read is as follows:

1. Start the dummy read:
   (a) When using slave select (SS): set SS bit low.
   (b) When not using SS: start condition is when Data Clock is high (see Table 5-9).
2. Send address word to IRQ status register (0x0C) with read and continuous address mode bits set to 1 (see Table 5-9).
3. Read 1 byte (8 bits) from IRQ status register (0x0C).
4. Dummy-read 1 byte from register 0x0D (collision position and interrupt mask).
5. Stop the dummy read:
   (a) When using slave select (SS): set SS bit high.
   (b) When not using SS: stop condition when Data Clock is high.

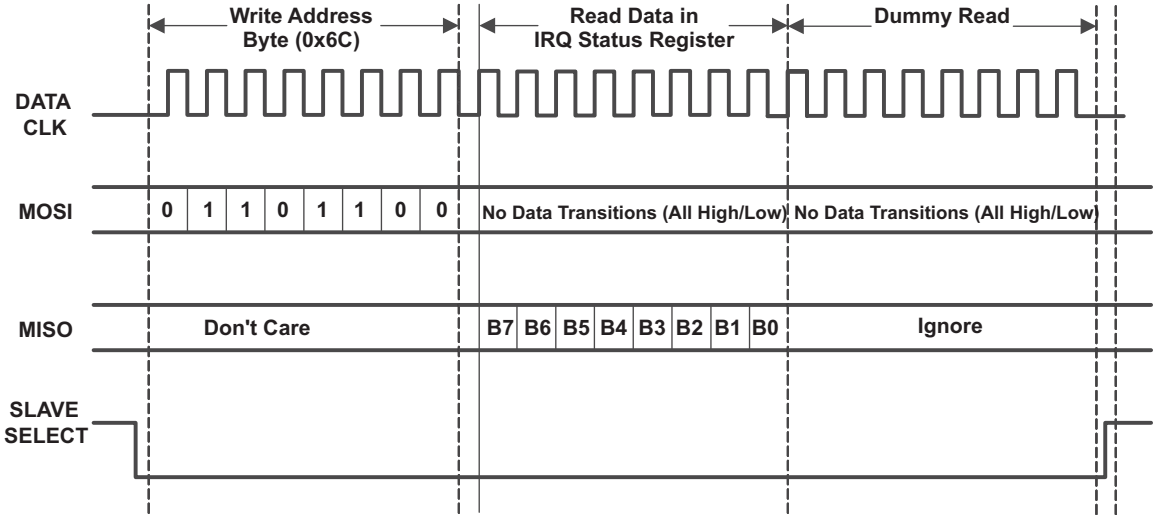


Figure 5-14. Procedure for Dummy Read

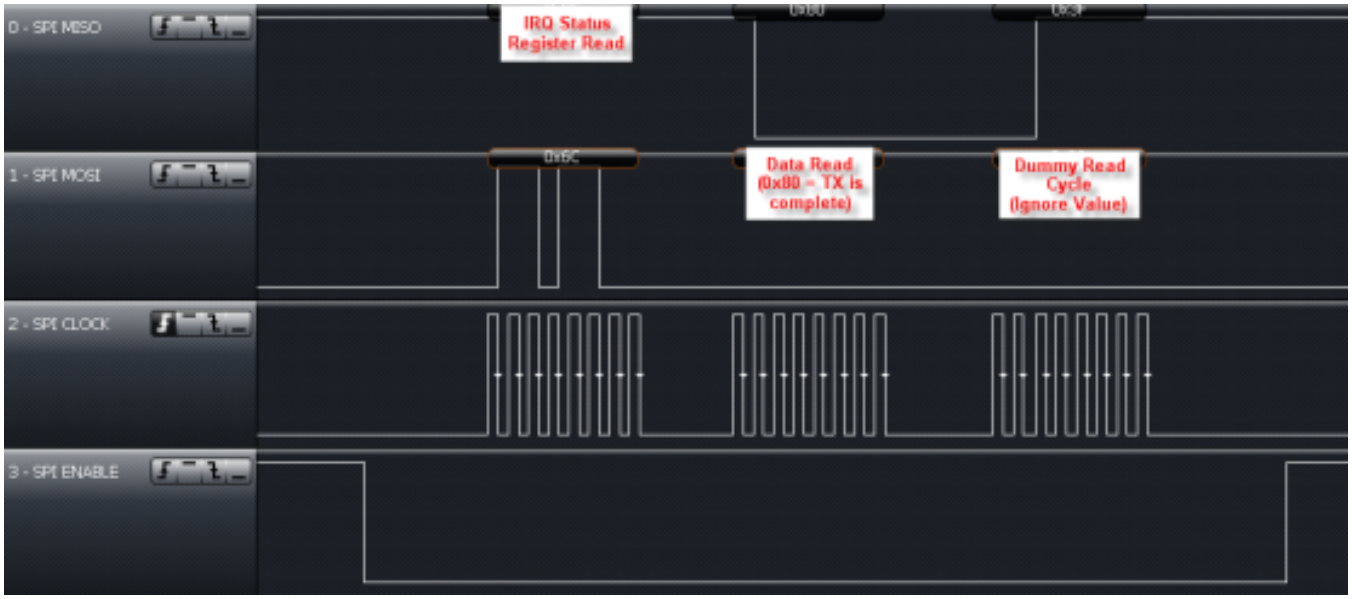


Figure 5-15. Example of Dummy Read Using SPI With SS

5.9.5.1 Serial Interface Mode Without Slave Select (SS)

The serial interface without the slave select pin must use delimiters for the start and stop conditions. Between these delimiters, the address, data, and command words can be transferred. All words must be 8 bits long with MSB transmitted first.

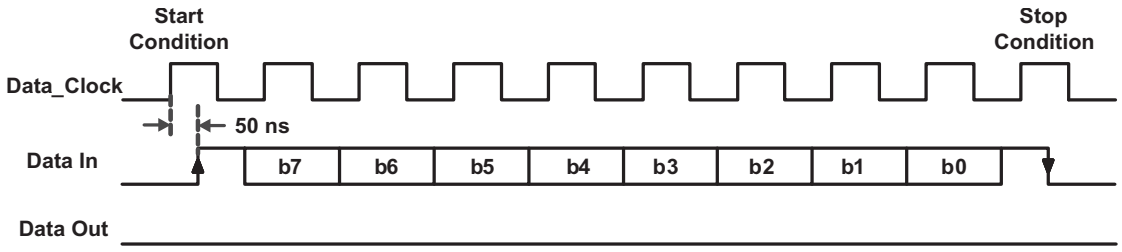


Figure 5-16. SPI Without Slave Select Timing Diagram

In this mode, a rising edge on data-in (I/O_7, pin 24) while SCLK is high resets the serial interface and prepares it to receive data. Data-in can change only when SCLK is low and is taken by the reader on the SCLK rising edge. Communication is terminated by the stop condition when the data-in falling edge occurs during a high SCLK period.

5.9.5.2 Serial Interface Mode With Slave Select (SS)

The serial interface is in reset while the Slave Select signal is high. Serial data in (MOSI) changes on the falling edge, and is validated in the reader on the rising edge, as shown in Figure 5-17. Communication is terminated when the Slave Select signal goes high.

All words must be 8 bits long with the MSB transmitted first.

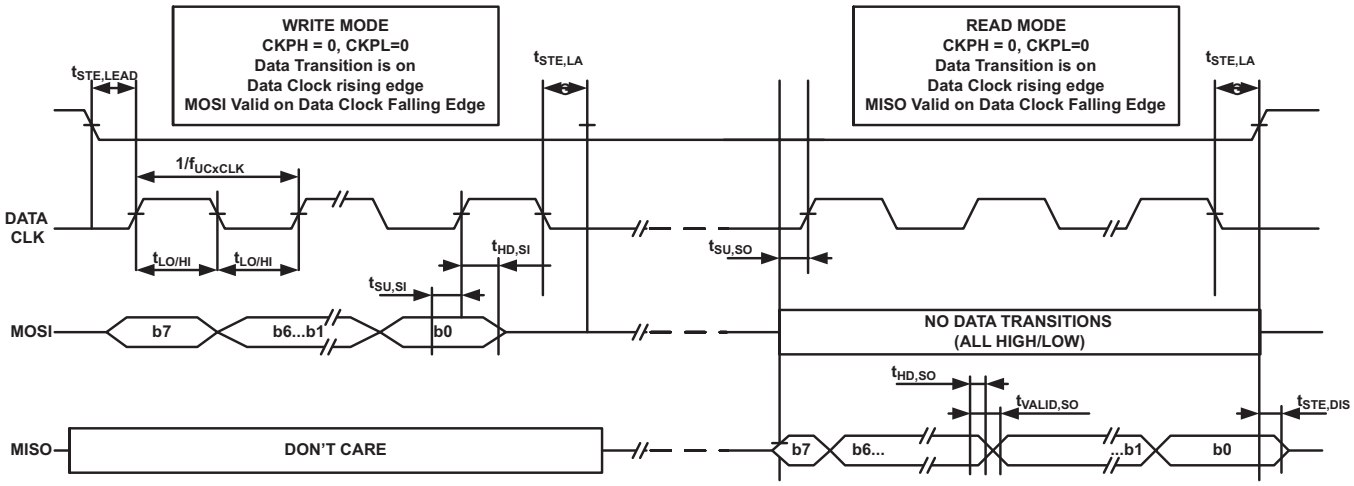


Figure 5-17. SPI With Slave Select Timing Diagram

The read command is sent out on the MOSI pin, MSB first, in the first eight clock cycles. MOSI data changes on the falling edge, and is validated in the reader on the rising edge, as shown in Figure 5-17. During the write cycle, the serial data out (MISO) is not valid. After the last read command bit (B0) is validated at the eighth rising edge of SCLK, after half a clock cycle, valid data can be read on the MISO pin at the falling edge of SCLK. It takes eight clock edges to read out the full byte (MSB first). See Section 3.4 for electrical specifications related to Figure 5-17.

The continuous read operation is shown in Figure 5-18.

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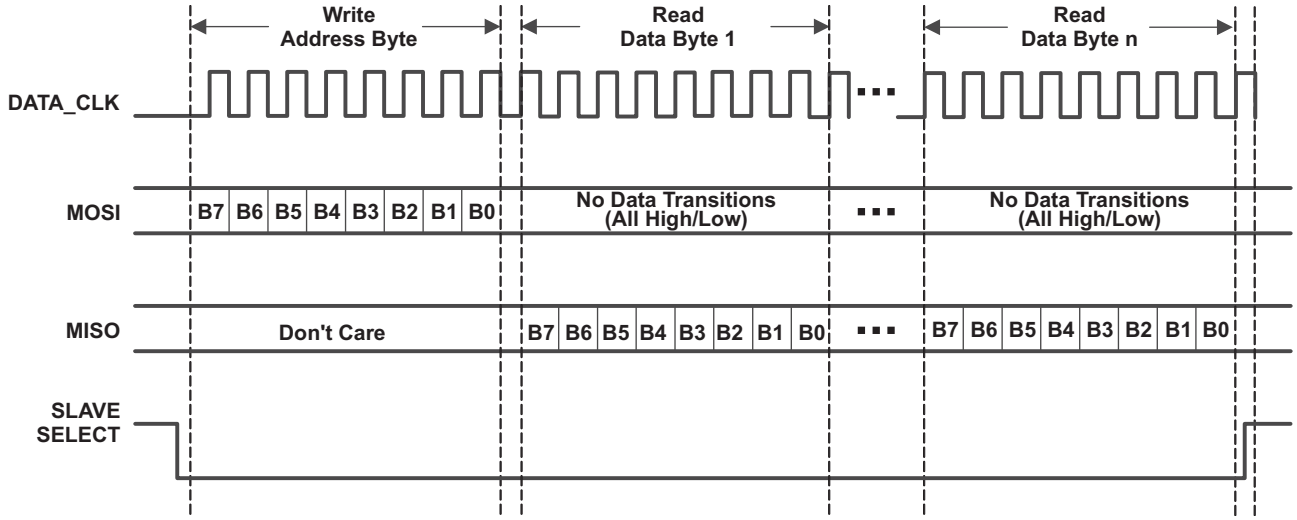


Figure 5-18. Continuous Read Operation Using SPI With Slave Select

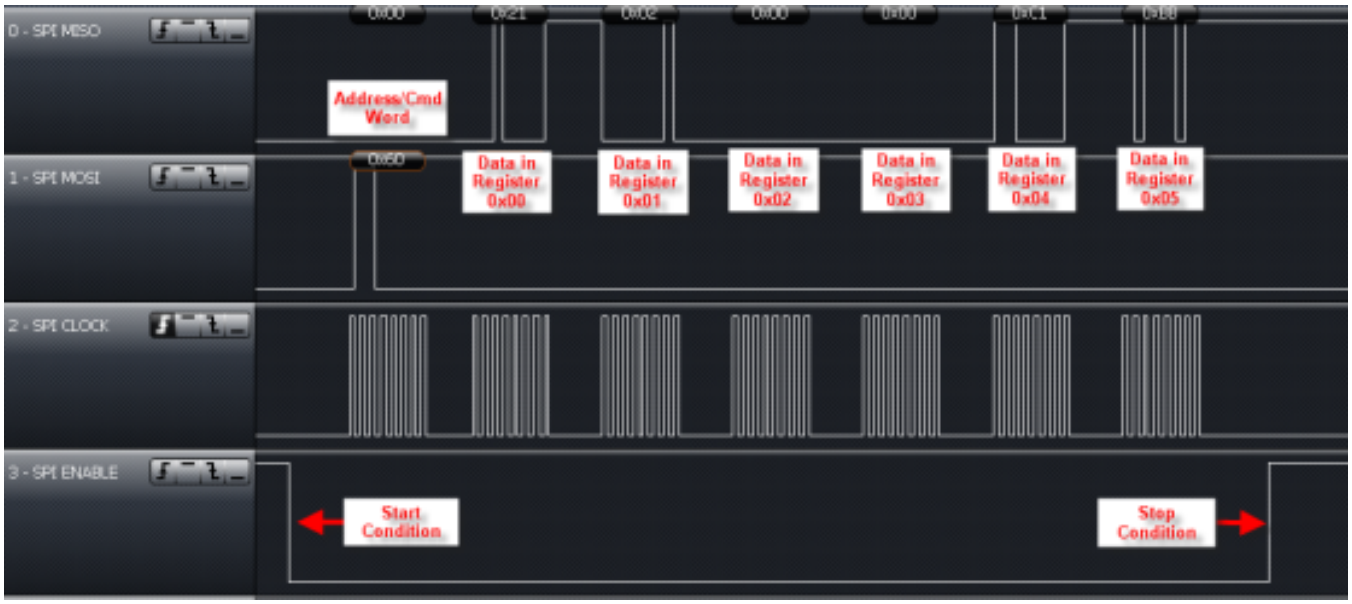


Figure 5-19. Continuous Read of Registers 0x00 Through 0x05 Using SPI With SS

Performing Single Slot Inventory Command as an example is shown in Figure 5-20. Reader registers (in this example) are configured for 5 VDC in and default operation. For full sequences for other settings and protocols can be found here: http://www.ti.com/lit/zip/sloc240

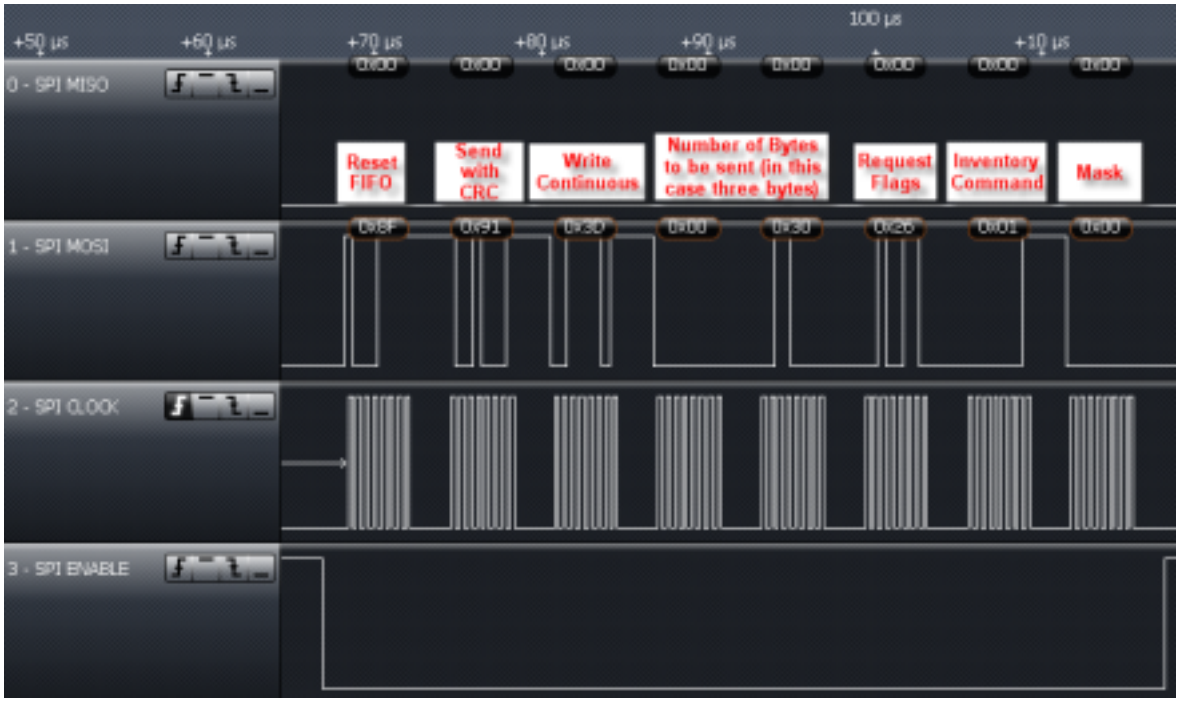


Figure 5-20. Inventory Command Sent From MCU to TRF7970A

The TRF7970A takes these bytes from the MCU and then send out Request Flags, Inventory Command ,and Mask over the air to the ISO15693 transponder. After these three bytes have been transmitted, an interrupt occurs to indicate back to the reader that the transmission has been completed. In the example in Figure 5-21, this IRQ occurs approximately 1.6 ms after the SS line goes high after the Inventory command is sent out.

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Figure 5-21. IRQ After Inventory Command

The IRQ status register read (0x6C) yields 0x80, which indicates that TX is indeed complete. This is followed by dummy clock and reset of FIFO with dummy clock. Then, if a tag is in the field and no error is detected by the reader, a second interrupt is expected and occurs (in this example) approximately 4 ms after first IRQ is read and cleared.

In the continuation of the example (see Figure 5-22), the IRQ Status Register is read using method previously recommended, followed by a single read of the FIFO status register, which indicates that there are at least 9 bytes to be read out.

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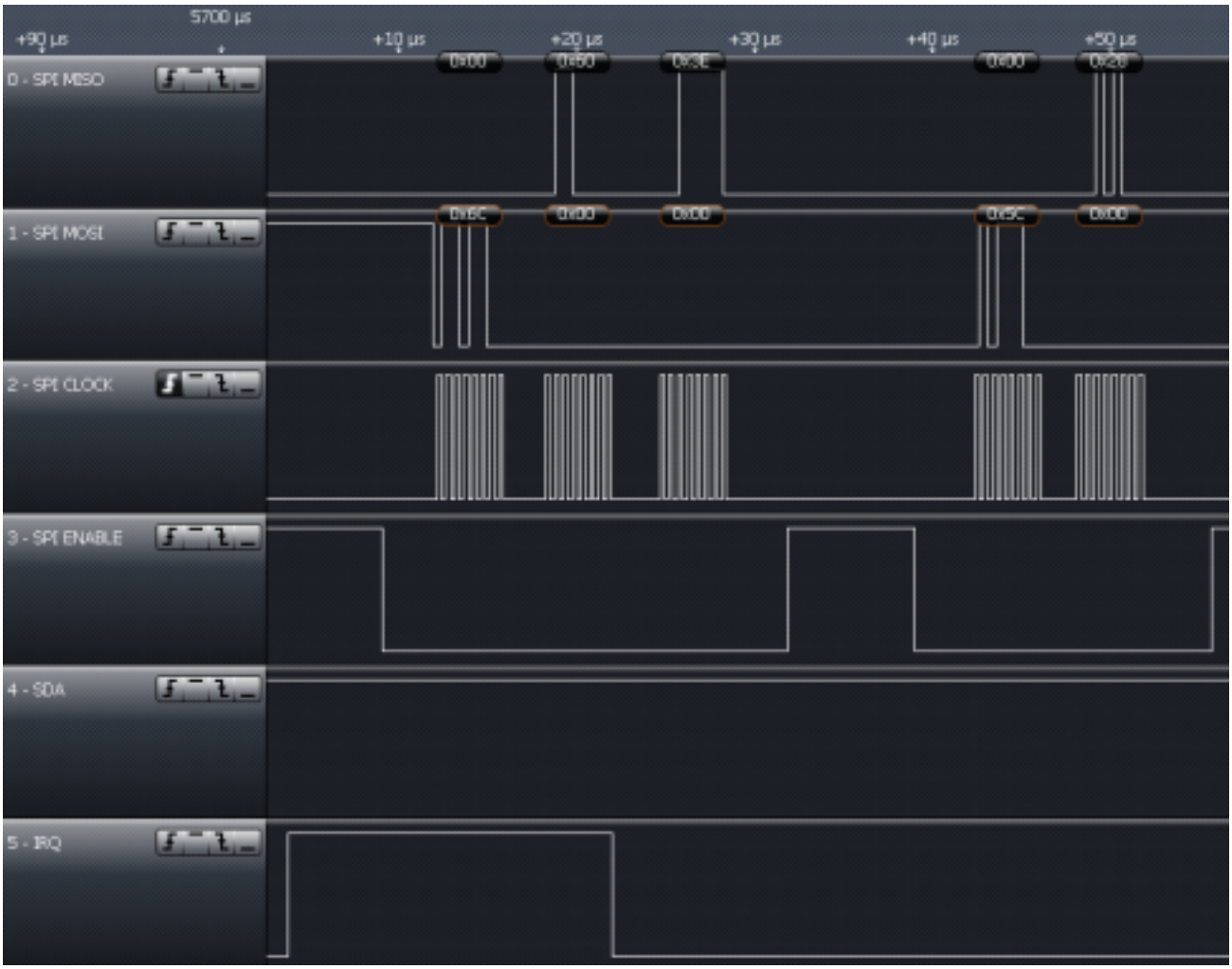


Figure 5-22. Read IRQ Status Register After Inventory Command

This is then followed by a continuous read of the FIFO. The first byte is (and should be) 0x00 for no error. The next byte is the DSFID (usually shipped by manufacturer as 0x00), then the UID, shown here up to the next most significant byte, the MFG code (shown as 0x07 (TI silicon)).

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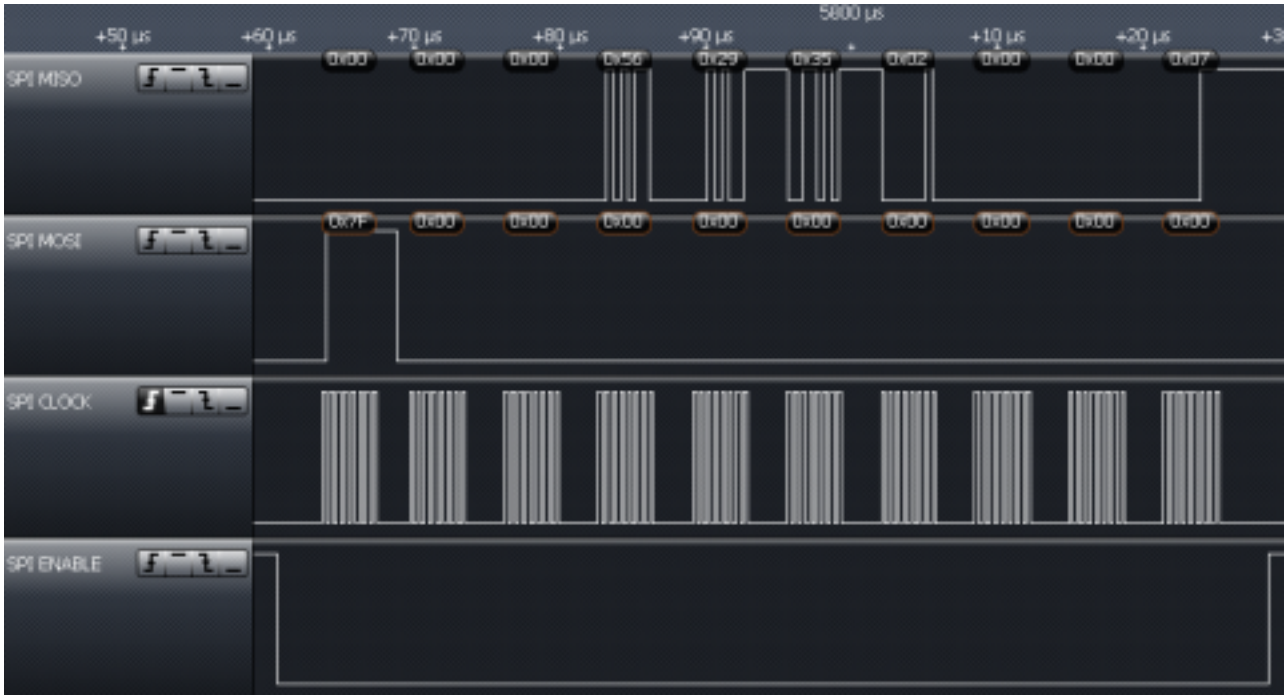


Figure 5-23. Continuous Read of FIFO After Inventory Command

This is followed by another IRQ approximately 160 µs later, as there is still one byte in FIFO, the MSB of the UID, which must be retrieved. IRQ register read shows RX is complete and FIFO register status shows one byte available, as expected and it is the E0, indicating ISO15693 transponder.

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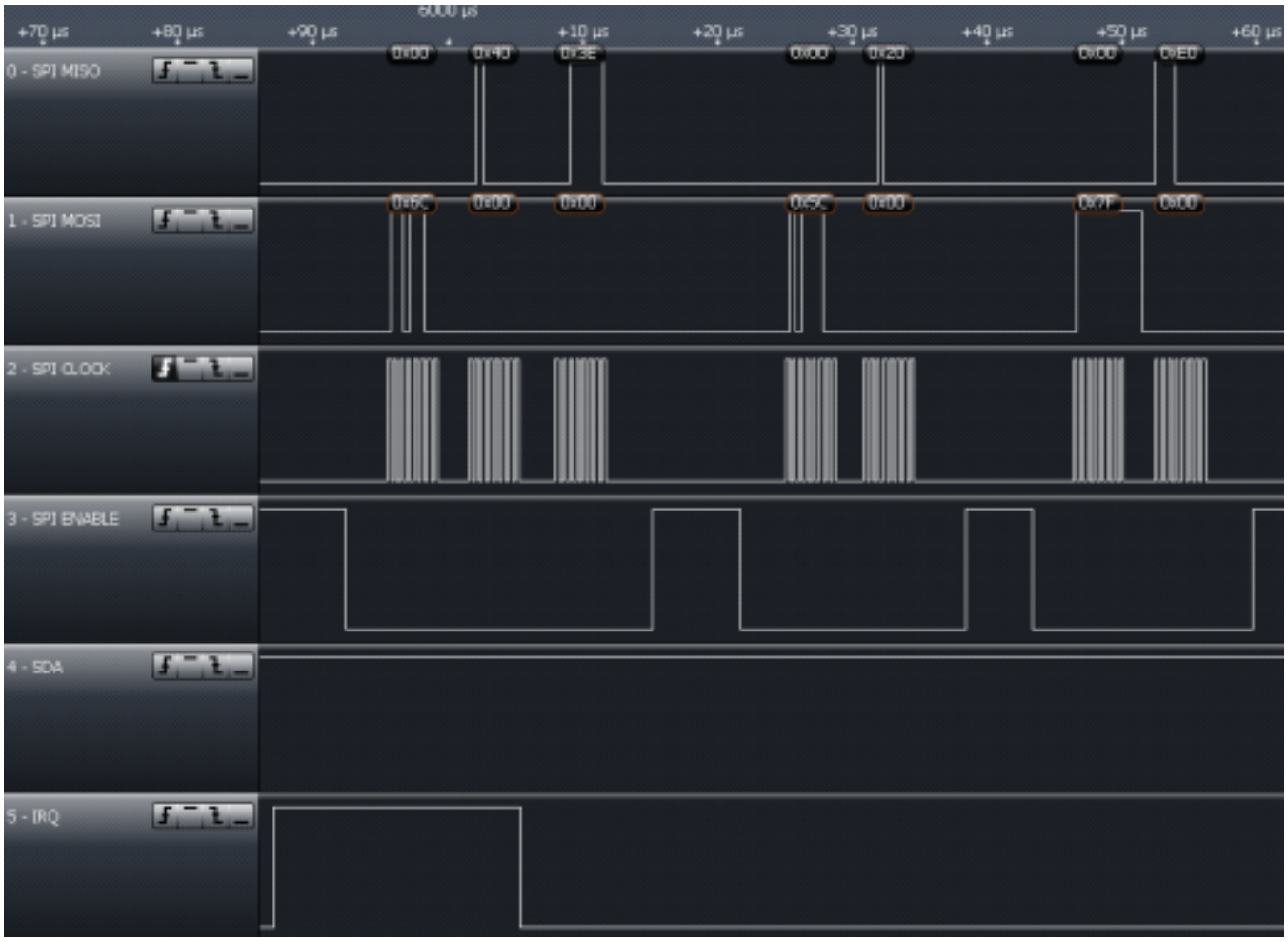


Figure 5-24. Second IRQ After Inventory Command

At this point it is good form to reset the FIFO and then read out the RSSI value of the tag. In this case the transponder is very close to the antenna, so value of 0x7E is recovered.

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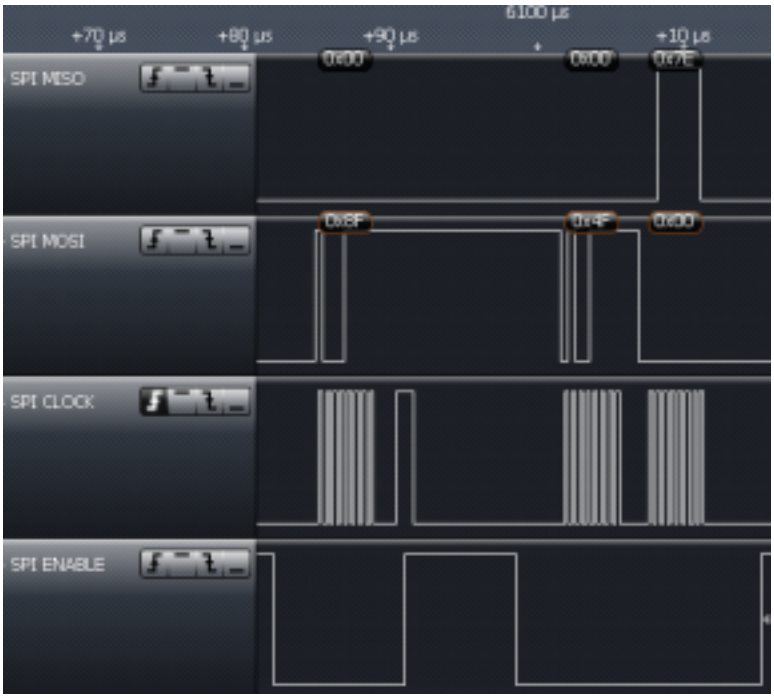


Figure 5-25. Reset FIFO and Read RSSI

5.9.6 Direct Mode

Direct mode allows the user to configure the reader in one of two ways. Direct Mode 0 (bit 6 = 0, as defined in ISO Control register) allows the user to use only the front-end functions of the reader, bypassing the protocol implementation in the reader. For transmit functions, the user has direct access to the transmit modulator through the MOD pin (pin 14). On the receive side, the user has direct access to the subcarrier signal (digitized RF envelope signal) on I/O_6 (pin 23).

Direct Mode 1 (bit 6 = 1, as defined in ISO Control register) uses the subcarrier signal decoder of the selected protocol (as defined in ISO Control register). This means that the receive output is not the subcarrier signal but the decoded serial bit stream and bit clock signals. The serial data is available on I/O_6 (pin 23) and the bit clock is available on I/O_5 (pin 22). The transmit side is identical; the user has direct control over the RF modulation through the MOD input. This mode is provided so that the user can implement a protocol that has the same bit coding as one of the protocols implemented in the reader, but needs a different framing format.

To select direct mode, the user must first choose which direct mode to enter by writing B6 in the ISO Control register. This bit determines if the receive output is the direct subcarrier signal (B6 = 0) or the serial data of the selected decoder. If B6 = 1, then the user must also define which protocol should be used for bit decoding by writing the appropriate setting in the ISO Control register.

The reader actually enters the direct mode when B6 (direct) is set to 1 in the chip status control register. Direct mode starts immediately. The write command should not be terminated with a stop condition (see communication protocol), because the stop condition terminates the direct mode and clears B6. This is necessary as the direct mode uses one or two I/O pins (I/O_6, I/O_5). Normal parallel communication is not possible in direct mode. Sending a stop condition terminates direct mode.

Figure 5-26 shows the different configurations available in direct mode.

- In mode 0, the reader is used as an AFE only, and protocol handling is bypassed.
- In mode 1, framing is not done, but SOF and EOF are present. This allows for a user-selectable framing level based on an existing ISO standard.

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- In mode 2, data is ISO-standard formatted. SOF, EOF, and error checking are removed, so the microprocessor receives only bytes of raw data through a 128-byte FIFO.

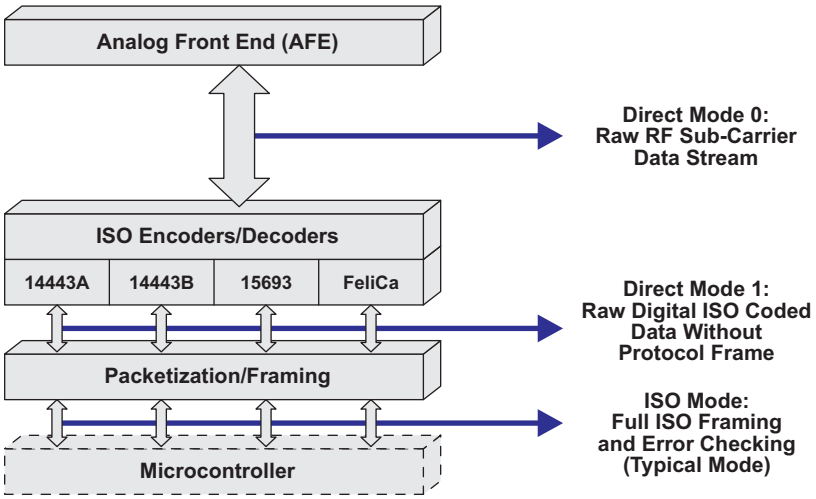


Figure 5-26. User-Configurable Modes

The steps to enter Direct Mode are listed below, using SPI with SS communication method only as one example, as Direct Modes are also possible with parallel and SPI without SS. The must enter Direct Mode 0 to accommodate non-ISO standard compliant card type communications. Direct Mode can be entered at any time, so in the event a card type started with ISO standard communications, then deviated from the standard after being identified and selected, the ability to go into Direct Mode 0 becomes very useful.

Step 1: Configure Pins I/O_0 to I/O_2 for SPI with SS

Step 2: Set Pin 12 of the TRF7970A (ASK/OOK pin) to 0 for ASK or 1 for OOK

Step 3: Program the TRF7970A registers

The following registers need to be explicitly set before going into the Direct Mode.

1. ISO Control register (0x01) to the appropriate standard
   - 0x02 for ISO 15693 High Data Rate (26.48 kbps)
   - 0x08 for ISO14443A (106 kbps)
   - 0x1A for FeliCa 212 kbps
   - 0x1B for FeliCa 424 kbps
2. Modulator and SYS_CLK Register (0x09) to the appropriate clock speed and modulation
   - 0x21 for 6.78 MHz Clock and OOK (100%) modulation
   - 0x20 for 6.78 MHz Clock and ASK 10% modulation
   - 0x22 for 6.78 MHz Clock and ASK 7% modulation
   - 0x23 for 6.78 MHz Clock and ASK 8.5% modulation
   - 0x24 for 6.78 MHz Clock and ASK 13% modulation
   - 0x25 for 6.78 MHz Clock and ASK 16% modulation
     (See register 0x09 definition for all other possible values)

Example register setting for ISO14443A at 106 kbps:

- ISO Control register (0x01) to 0x08
- RX No Response Wait Time register (0x07) to 0x0E
- RX Wait Time register (0x08) to 0x07
- Modulator control register (0x09) to 0x21 (or any custom modulation)
- RX Special Settings register (0x0A) to 0x20

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Step 4: Entering Direct Mode 0

The following registers need to be programmed to enter Direct Mode 0

1. Set bit B6 of the Modulator and SYS_CLK Control register (0x09) to 1.
2. Set bit B6 of the ISO Control (Register 01) to 0 for Direct Mode 0 (default its 0)
3. Set bit B6 of the Chip Status Control register (0x00) to 1 to enter Direct Mode
4. Send extra eight clock cycles (see Figure 5-27, this step is TRF7970A specific)

NOTE

– It is important that the last write is not terminated with a stop condition. For SPI, this means that Slave Select (I/O_4) stays low.
– Sending a Stop condition terminates the Direct Mode and clears bit B6 in the Chip Status Control register (0x00).

NOTE

Access to Registers, FIFO, and IRQ is not available during Direct Mode 0.

The reader enters the Direct Mode 0 when bit 6 of the Chip Status Control register (0x00) is set to a 1 and stays in Direct Mode 0 until a stop condition is sent from the microcontroller.

NOTE

The write command should not be terminated with a stop condition (for example, in SPI mode this is done by bringing the Slave Select line high after the register write), because the stop condition terminates the direct mode and clears bit 6 of the Chip Status Control Register (0x00), making it a 0.

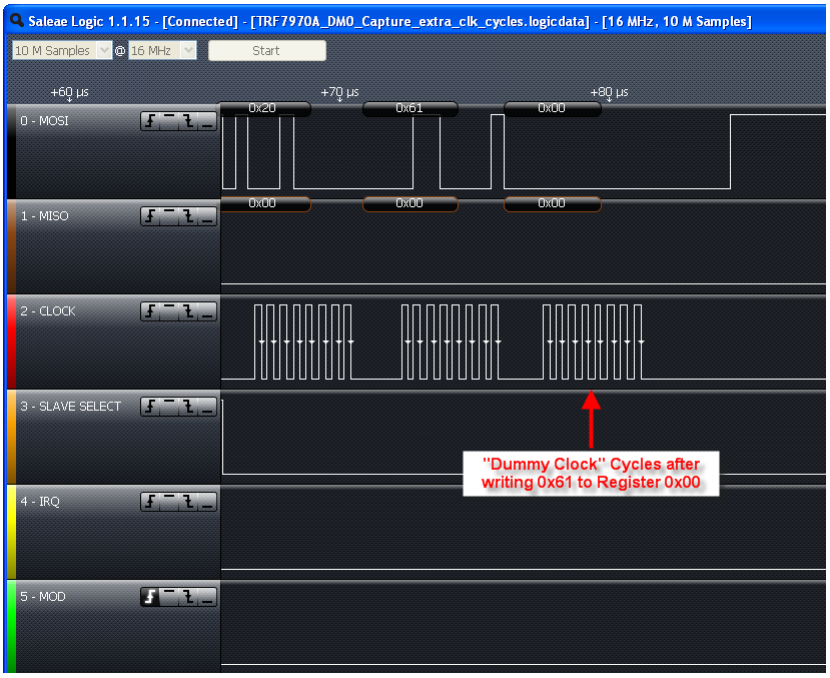


Figure 5-27. Entering Direct Mode 0

Step 5: Transmit Data Using Direct Mode

The application now has direct control over the RF modulation through the MOD input (see Figure 5-28).

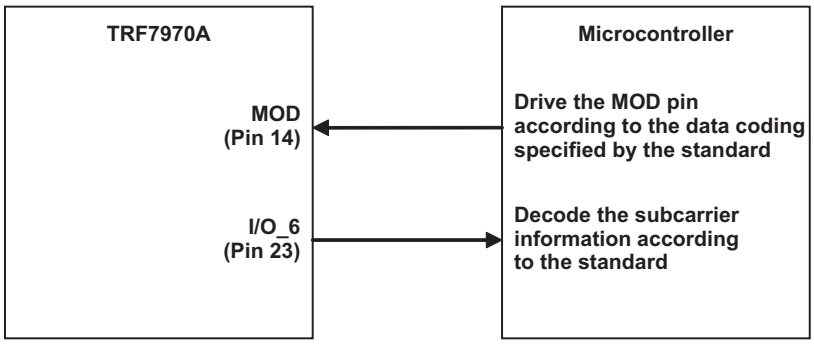


Figure 5-28. Direct Control Signals

The microcontroller is responsible for generating data according to the coding specified by the particular standard. The microcontroller must generate SOF, EOF, Data, and CRC. In direct mode, the FIFO is not used and no IRQs are generated. See the applicable ISO standard to understand bit and frame definitions. As an example of what the developer sees when using DM0 in an actual application, Figure 5-29 is presented to clearly show the relationship between the MOD pin being controlled by the MCU and the resulting modulated 13.56-MHz carrier signal.

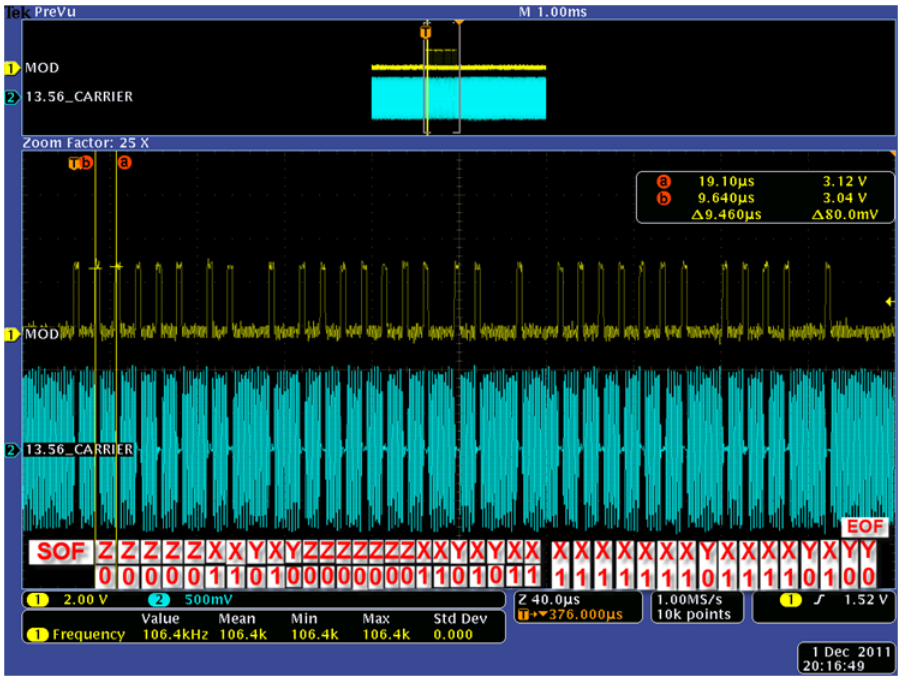


Figure 5-29. TX Sequence Out in DM0

Step 6: Receive Data Using Direct Mode

After the TX operation is complete, the tag responds to the request and the subcarrier data is available on pin I/O_6. The microcontroller needs to decode the subcarrier signal according to the standard. This includes decoding the SOF, data bits, CRC, and EOF. The CRC then needs to be checked to verify data integrity. The receive data bytes must be buffered locally.

As an example of the receive data bits and framing level according to the ISO14443A standard is shown in Figure 5-30 (taken from ISO14443 specification and TRF7970A air interface).

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- 128/fc = 9.435 µs = t_b (106-kbps data rate)
- 64/fc = 4.719 µs = t_x time
- 32/fc = 2.359 µs = t_1 time

Table 7 — Parameters for sequences

Parameter	Bit rate			
	fc/128	fc/64	fc/32	fc/16
t_b	128/fc	64/fc	32/fc	16/fc
t_x	64/fc	32/fc	16/fc	8/fc
t_1	see t_1 of Table 3	see t_1 of Table 5		

Figure 10 together with the timing parameters in Table 7 illustrate sequences X, Y and Z.

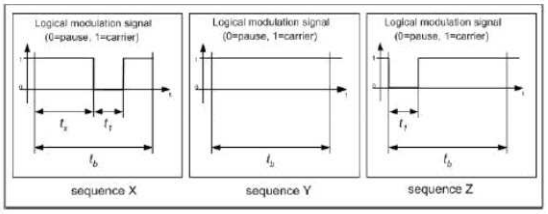


Figure 10 — Sequences for Type A communication PCD to PICC

The above sequences shall be used to code the following information:

— logic "1": sequence X,

— logic "0": sequence Y with the following two exceptions:

i) If there are two or more contiguous "0"s, sequence Z shall be used from the second "0" on,

ii) If the first bit after a "start of frame" is "0", sequence Z shall be used to represent this and any "0"s which follow directly thereafter.

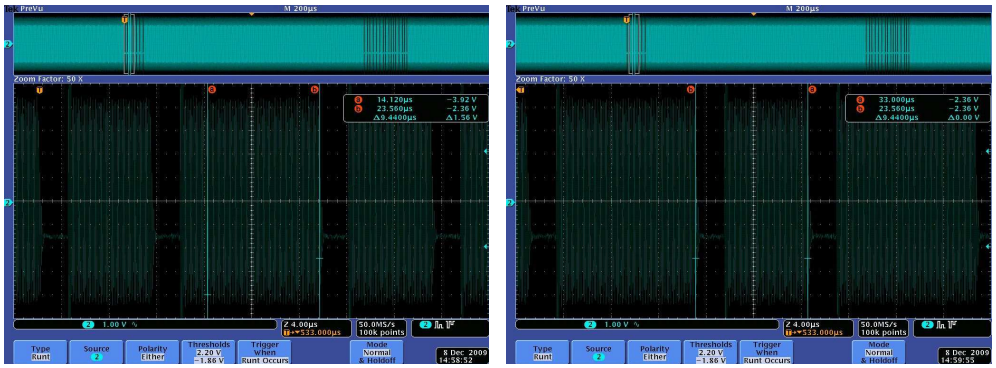
— start of communication: sequence Z,

— end of communication: logic "0" followed by sequence Y,

— no information: at least two sequences Y.



t_b = 9.44 µs t_x = 4.72 µs t_1 = 2.48 µs



Sequence Y = Carrier for 9.44 µs

Sequence Z = Pause for 2 to 3 µs, Carrier for Remainder of 9.44 µs

Figure 5-30. Receive Data Bits and Framing Level

Figure 5-31 is presented to clearly show an example of what the developer should expect on the I/O_6 line during the RX process while in Direct Mode 0.

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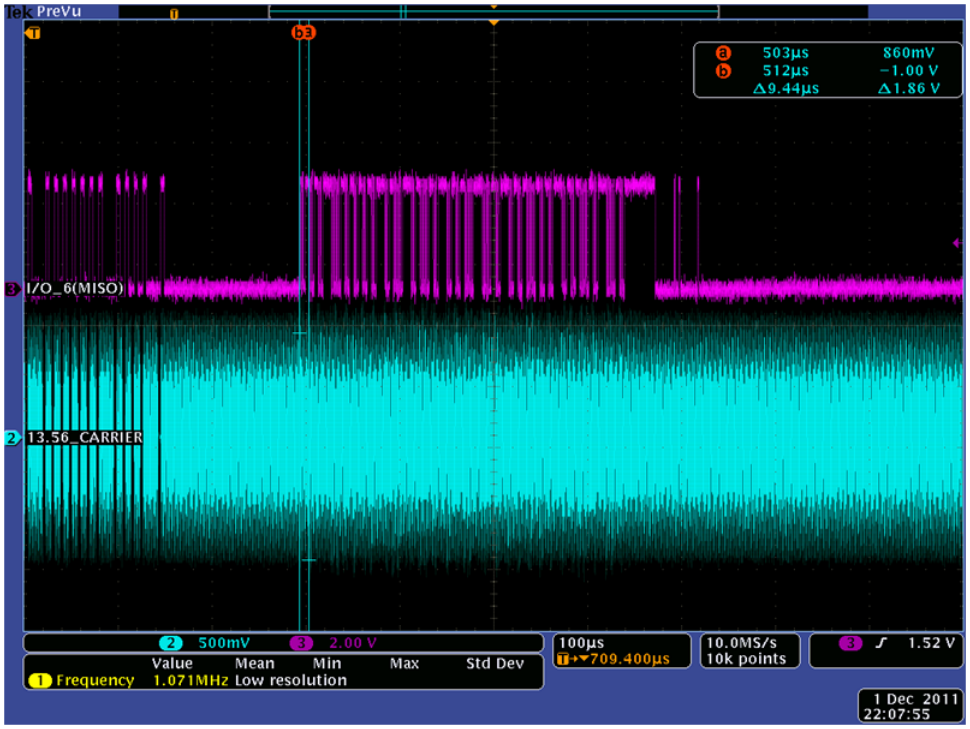


Figure 5-31. RX Sequence on I/O_6 in DM0 (Analog Capture)

Step 7: Terminating Direct Mode 0

After the EOF is received, data transmission is over, and Direct Mode 0 can be terminated by sending a Stop Condition (in the case of SPI, make the Slave Select go high). The TRF7970A is returned to default state.

5.10 Special Direct Mode for Improved MIFARE Compatibility

See the application report *TRF7970A Firmware Design Hints* (SLOA159).

5.11 NFC Modes

5.11.1 Target

When used as the NFC target, the chip is typically in a power down or standby mode. If EN2 = H, the chip keeps the supply system on. If EN2 = L and EN = L the chip is in complete power down. To operate as NFC target or Tag emulator the MCU must load a value different than zero (0) in Target Detection Level register (b0-b2) which enables the RF measurement system (supplied by VEXT, so it can operate also during complete power down and consumes only 3.5 µA). The RF measurement constantly monitors the RF signal on the antenna input. When the RF level on the antenna input exceeds the level defined in the in Target Detection Level register, the chip is automatically activated (EN is internal forced high). The typical RF value that causes power-up for each value of B0 to B2 and the function of Target Detection Level register is listed in Table 5-14.

NFC Target Detection Level Register (0x18) – defines level for RF level for wake-up, enables automatic SDD and gives information of NFCID size. This register is directly supplied by VEXT to ensure data retention during complete power down.

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Table 5-14. NFC Target Detection Level Register

Bit	Signal Name	Function	Comments
B7	Id_s1	NFCID1 size used in 106 kbps passive target SDD	
B6	Id_s0		
B5	Sdd_en	1 = Enables internal SDD protocol	Automatic SDD using internal state machine and ID stored in NFCID Number register
B4		N/A	
B3	Hi_rf	Extended range for RF measurements	
B2	Rfdet_h2	RF field level required for system wake-up. If all bits are 0, the RF level detection is switched off.	Comparator output is displayed in NFC Target Protocol register B7 (rf_h)
B1	Rfdet_h1		
B0	Rfdet_h0		

Default: reset to 00 at POR on VEXT (not on POR based on V_{DD_X}), not reset at EN = 0

Table 5-15. Bits B0 to B3 of the NFC Target Detection Level Register

	b0 B1 B2	000	001	010	011	100	101	110	111
B3 = 0	RF Vpp	Not active	480 mV	350 mV	250 mV	220 mV	190 mV	180 mV	170 mV
B3 = 1	RF Vpp	Not active	1500 mV	700 mV	500 mV	450 mV	400 mV	320 mV	280 mV

When the voltage supply system and the oscillator are started and is stable, the osc_ok goes high (B6 of RSSI Level and Oscillator Status register) and IRQ is sent with bit B2 = 1 of IRQ register (field change). Bit B7 NFC Target Protocol in register directly displays the status of RF level detection (running constantly also during normal operation). This informs the MCU that the chip should start operation as an NFC TARGET device.

When the first command from the INITIATOR is received another IRQ sent with B6 (RX start) set in IRQ register. The MCU must set EN = H (confirm the power-up) in the time between the two IRQs as the internal power-up ends after the second IRQ. The type and coding of the first initiator (or reader in the case of a tag emulator) command define the communication protocol type which the target must use. So the communication protocol type is available in the NFC Target Protocol register immediately after receiving the first command. The coding of the NFC Target Protocol register is described next.

NFC Target Protocol Register (0x19) – displays the bit rate and protocol type (active or passive) transmitted by initiator in the first command. It also displays the comparator outputs of both RF level detectors.

Table 5-16. NFC Target Protocol Register

Bit	Signal Name	Function	Comments
B7	Rf_h	1 = RF level is above the set wake-up level	The wake-up level is defined by bits b0-b3 of NFC Target Detection Level register
B6	Rf_l	1 = RF level is above the RF collision avoidance level.	The collision avoidance level is defined by bits b0-b2 of NFC Low Field Detection Level register
B5		N/A	
B4	FeliCa	1 = FeliCa type 0 = ISO14443A type	The first initiator command had physical level coding like FeliCa or like ISO14443A
B3	Pas106	Passive target 106 kbps or tag emulation	The first initiator/reader command was SENS_REQ or ALL_REQ
B2	Pas14443B	Tag emulation ISO14443B	The first reader command was of ISO14443B type
B1	Nfcbr1	Bit rate of first received command	00 = N/A 01 = 106 kbps 10 = 212 kbps 11 = 424 kbps
B0	Nfcbr0		

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Default: reset to 00 at POR and EN = L. B0 to B4 are automatically reset after MCU read operation. B6 and B7 continuously display the RF level comparator outputs.

Based on the first command from INITIATOR following actions are taken:

- If the first command is SENS_REQ or ALL_REQ, the TARGET must enter the SDD protocol for 106 kbps passive communication. If bit B5 in NFC Target Detection Level register is not set, the MCU handles the SDD and the command received is send to FIFO. If bit B5 is set, the internal SDD state machine is used. The MCU must load the ID (NFCID1) of the device in the 128 bytes deep NFCID Number registers to be used by the SDD state machine. The length of the ID which should be used in SDD is defined by bits B6 and B7 of the NFC Target Detection Level register. When the SDD is complete and the INITIATOR sends SEL_REQ with full UID on the correct cascade level the SDD state machine responds with SEL_RES indicating the TARGET supports the data exchange protocol. The IRQ (B3 set) is send to MCU to signal successful end of SDD (the device is now selected as TARGET). The SDD state machine is than turned off. If the RF field is turned off (B7 in the NFC Target Protocol register goes low) at any time, the system sends an IRQ to the MCU with bit B2 (RF field change) in the IRQ register set high. This informs the MCU that the procedure was aborted and the system must be reset. The clock extractor is automatically activated in this mode.
- If the command is SENS_REQ or ALL_REQ and the Tag emulation bit in ISO Control register is set, the system emulates an ISO14443A tag. The procedure does not differ from the one previously described for a passive target at 106 kbps. The clock extractor is automatically activated in this mode.
- If the first command is a POLLING request, the system becomes a TARGET in passive communication using 212 kbps or 424 kbps. The SDD is relatively simple and is handled by the MCU directly. The POLLING response is sent in one of the slots automatically calculated by the MCU (first slot starts 2.416 ms after the end of the command and slots follow in 1.208 ms).
- If the first command is ATR_REQ, the system operates as an active TARGET using the same communication speed and bit coding as used by the INITIATOR. Again, all of the replies are handled by MCU. The chip is only required to time the response collision avoidance, which is done on direct command from MCU. When the RF field is switched on and the minimum wait time is elapsed, the chip sends an IRQ with B1 (RF collision avoidance finished) set high. This signals the MCU that it can send the reply.
- If the first command is coded as ISO14443B and the Tag emulation bit is set in the ISO Control register, the system enters ISO14443B emulator mode. The anticollision must be handled by the MCU, and the chip provides all physical level coding, decoding, and framing for this protocol.

Table 5-17 shows the function of the IRQ and Status register in NFC and Tag emulation. This register is preset to 0 at POR = H or EN = L and at each write to ISO Control. It is also automatically reset at the end of read phase. The reset also removes the IRQ flag.

Table 5-17. IRQ and Status Register (0x0C) for NFC and Card Emulation Operation (1)

Bit	Signal Name	Function	Comments
B7	Irq_tx	IRQ set due to end of TX	Signals the TX is in progress. The flag is set at the start of TX but the interrupt request is sent when TX is finished.
B6	Irg_srx	IRQ set due to RX start	Signals that RX SOF was received and RX is in progress. The flag is set at the start of RX but the interrupt request is sent when RX is finished
B5	Irq_fifo	Signals the FIFO is 1/3 > FIFO > 2/3	Signals FIFO high or low
B4	Irq_err1	Protocol error	Any protocol error
B3	Irq_sdd	SDD finished	SDD (passive target at 106 kbps) successfully finished
B2	Irq_rf	RF field change	Sufficient RF signal level for operation was reached or lost
B1	Irq_col	RF collision avoidance finished	The system has finished collision avoidance and the minimum wait time is elapsed.
B0	Irq_col_err	RF collision avoidance not finished successfully	The external RF field was present so the collision avoidance could not be carried out.

(1) Displays the cause of IRQ and TX/RX status

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5.11.2 Initiator

The chip is fully controlled by the MCU as in RFID reader operation. The MCU activates the chip and writes the mode selection in the ISO Control register. The MCU uses RF collision avoidance commands, so it is relieved of any real-time task. The normal transmit and receive procedure (through the FIFO) are used to communicate with the TARGET device as described in Section 5.9.

5.12 Direct Commands from MCU to Reader

5.12.1 Command Codes

Table 5-18. Address/Command Word Bit Distribution

Command Code	Command	Comments
0x00	Idle	
0x03	Software Initialization	Same as Power on Reset
0x04	Perform RF Collision Avoidance	
0x05	Perform response RF Collision Avoidance	
0x06	Perform response RF Collision Avoidance (n = 0)	
0x0F	Reset	
0x10	Transmission without CRC	
0x11	Transmission with CRC	
0x12	Delayed Transmission without CRC	
0x13	Delayed Transmission with CRC	
0x14	End of Frame/Transmit Next Time Slot	ISO15693
0x15	Close Slot Sequence	
0x16	Block Receiver	
0x17	Enable Receiver	
0x18	Test external RF (RSSI at RX input with TX on)	
0x19	Test internal RF (RSSI at RX input with TX off)	
0x1A	Receiver Gain Adjust	

The command code values from Table 5-18 are substituted in Table 5-19, Bits 0 through 4. Also, the most-significant bit (MSB) in Table 5-19 must be set to 1. (Table 5-19 is same as Table 5-10, shown here again for user clarity).

Table 5-19. Address/Command Word Bit Distribution

Bit	Description	Bit Function	Address	Command
B7	Command control bit	0 = address 1 = command	0	1
B6	Read/Write	0 = write 1 = read	R/W	0
B5	Continuous address mode	1 = Continuous mode	R/W	0
B4	Address/Command bit 4		Adr 4	Cmd 4
B3	Address/Command bit 3		Adr 3	Cmd 3
B2	Address/Command bit 2		Adr 2	Cmd 2
B1	Address/Command bit 1		Adr 1	Cmd 1
B0	Address/Command bit 0		Adr 0	Cmd 0

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The MSB determines if the word is to be used as a command or address. The last two columns of Table 5-19 show the function of each bit, depending on whether address or command is written. Command mode is used to enter a command resulting in reader action (initialize transmission, enable reader, and turn reader on or off).

5.12.1.1 Software Initialization (0x03)

This command starts a Power on Reset.

5.12.1.2 Initial RF Collision Avoidance (0x04)

This command executes the initial collision avoidance and sends out IRQ after 5 ms from establishing RF field (so the MCU can start sending commands/data). If the external RF field is present (higher than the level set in NFC Low Field Detection Level register (0x16)) then the RF field can not be switched on and hence a different IRQ is returned.

5.12.1.3 Response RF Collision Avoidance (0x05)

This command executes the response collision avoidance and sends out IRQ after 75 µs from establishing

RF field (so the MCU can start sending commands/data). If the external RF field is present (higher than the level set in NFC Low Field Detection Level register (0x16)) then the RF field can not be switched on and hence a different IRQ is returned.

5.12.1.4 Response RF Collision Avoidance (0x06, n = 0)

This command executes the response collision avoidance without random delay. It sends out IRQ after 75 µs from establishing RF field (so the MCU can start sending commands/data). If the external RF field is present (higher than the level set in NFC Low Field Detection Level register (0x16)) then the RF field can not be switched on and hence a different IRQ is returned.

5.12.1.5 Reset (0x0F)

The reset command clears the FIFO contents and FIFO status register (0x1C). It also clears the register storing the collision error location (0x0E).

5.12.1.6 Transmission With CRC (0x11)

The transmission command must be sent first, followed by transmission length bytes, and FIFO data. The reader starts transmitting after the first byte is loaded into the FIFO. The CRC byte is included in the transmitted sequence.

5.12.1.7 Transmission Without CRC (0x10)

Same as Section 5.12.1.6 with CRC excluded.

5.12.1.8 Delayed Transmission With CRC (0x13)

The transmission command must be sent first, followed by the transmission length bytes, and FIFO data.

The reader transmission is triggered by the TX timer.

5.12.1.9 Delayed Transmission Without CRC (0x12)

Same as Section 5.12.1.8 with CRC excluded.

5.12.1.10 Transmit Next Time Slot (0x14)

When this command is received, the reader transmits the next slot command. The next slot sign is defined by the protocol selection.

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5.12.1.11 Block Receiver (0x16)

The block receiver command puts the digital part of receiver (bit decoder and framer) in reset mode. This is useful in an extremely noisy environment, where the noise level could otherwise cause a constant switching of the subcarrier input of the digital part of the receiver. The receiver (if not in reset) would try to catch a SOF signal, and if the noise pattern matched the SOF pattern, an interrupt would be generated, falsely signaling the start of an RX operation. A constant flow of interrupt requests can be a problem for the external system (MCU), so the external system can stop this by putting the receive decoders in reset mode. The reset mode can be terminated in two ways. The external system can send the enable receiver command. The reset mode is also automatically terminated at the end of a TX operation. The receiver can stay in reset after end of TX if the RX wait time register (0x08) is set. In this case, the receiver is enabled at the end of the wait time following the transmit operation.

5.12.1.12 Enable Receiver (0x17)

This command clears the reset mode in the digital part of the receiver if the reset mode was entered by the block receiver command.

5.12.1.13 Test Internal RF (RSSI at RX Input With TX ON) (0x18)

The level of the RF carrier at RF_IN1 and RF_IN2 inputs is measured. Operating range between 300 mV_P and 2.1 V_P (step size is 300 mV). The two values are displayed in the RSSI levels register (0x0F). The command is intended for diagnostic purposes to set correct RF_IN levels. Optimum RFIN input level is approximately 1.6 V_P or code 5 to 6. The nominal relationship between the RF peak level and RSSI code is shown in Table 5-20 and in Section 5.4.1.1.

NOTE

If the command is executed immediately after power-up and before any communication with a tag is performed, the command must be preceded by Enable RX command. The Check RF commands require full operation, so the receiver must be activated by Enable RX or by a normal Tag communication for the Check RF command to work properly.

Table 5-20. Test Internal RF Peak Level to RSSI Codes

RF_IN1 [mV_{PP}]	300	600	900	1200	1500	1800	2100
Decimal Code	1	2	3	4	5	6	7
Binary Code	001	010	011	001	101	011	111

5.12.1.14 Test External RF (RSSI at RX Input with TX OFF) (0x19)

This command can be used in active mode when the RF receiver is switched on but RF output is switched off. This means bit B1 = 1 in Chip Status Control Register. The level of RF signal received on the antenna is measured and displayed in the RSSI Levels register (0x0F). The relation between the 3 bit code and the external RF field strength [A/m] must be determinate by calculation or by experiments for each antenna type as the antenna Q and connection to the RF input influence the result. The nominal relation between the RF peak to peak voltage in the RF_IN1 input and RSSI code is shown in Table 5-21 and in Section 5.4.1.2.

NOTE

If the command is executed immediately after power-up and before any communication with a tag is performed, the command must be preceded by an Enable RX command. The Check RF commands require full operation, so the receiver must be activated by Enable RX or by a normal Tag communication for the Check RF command to work properly.

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Table 5-21. Test External RF Peak Level to RSSI Codes

RF_IN1 [mV_{PP}]	40	60	80	100	140	180	300
Decimal Code	1	2	3	4	5	6	7
Binary Code	001	010	011	001	101	011	111

5.12.1.15 Receiver Gain Adjust (0x1A)

This command should be executed when the MCU determines that no TAG response is coming and when the RF and receivers are switched ON. When this command is received, the reader observes the digitized receiver output. If more than two edges are observed in 100 ms, the window comparator voltage is increased. The procedure is repeated until the number of edges (changes of logical state) of the digitized reception signal is less than 2 (in 100 ms). The command can reduce the input sensitivity in 5-dB increments up to 15 dB. This command ensures better operation in a noisy environment. The gain setting is reset to maximum gain at EN = 0 and POR = 1.

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6 Register Description

6.1 Register Preset

After power-up and the EN pin low-to-high transition, the reader is in the default mode. The default configuration is ISO15693, single subcarrier, high data rate, 1-out-of-4 operation. The low-level option registers (0x02 to 0x0B) are automatically set to adapt the circuitry optimally to the appropriate protocol parameters. When entering another protocol (by writing to the ISO Control register 0x01), the low-level option registers (0x02 to 0x0B) are automatically configured to the new protocol parameters. After selecting the protocol, it is possible to change some low-level register contents if needed. However, changing to another protocol and then back, reloads the default settings, and so then the custom settings must be reloaded.

The Clo0 and Clo1 register (0x09) bits, which define the microcontroller frequency available on the SYS_CLK pin, are the only two bits in the configuration registers that are not cleared during protocol selection.

6.2 Register Overview

Table 6-1. Register Definitions

Address	Register	Read/Write
Main Control Registers		
0x00	Chip Status Control	R/W
0x01	ISO Control	R/W
Protocol Sub-Setting Registers		
0x02	ISO14443B TX options	R/W
0x03	ISO14443A high bit rate options	R/W
0x04	TX timer setting, H-byte	R/W
0x05	TX timer setting, L-byte	R/W
0x06	TX pulse-length control	R/W
0x07	RX no response wait	R/W
0x08	RX wait time	R/W
0x09	Modulator and SYS_CLK control	R/W
0x0A	RX Special Setting	R/W
0x0B	Regulator and I/O control	R/W
0x10	Special Function Register, Preset 0x00	R/W
0x11	Special Function Register, Preset 0x00	R/W
0x14	Adjustable FIFO IRQ Levels Register	R/W
0x15	Reserved	R/W
0x16	NFC Low Field Detection Level	R/W
0x17	NFCID1 Number (up to 10 bytes wide)	W
0x18	NFC Target Detection Level	R/W
0x19	NFC Target Protocol	R/W
Status Registers		
0x0C	IRQ status	R
0x0D	Collision position and interrupt mask register	R/W
0x0E	Collision position	R
0x0F	RSSI levels and oscillator status	R
RAM		
0x12	RAM	R/W
0x13	RAM	R/W

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Table 6-1. Register Definitions (continued)

Address	Register	Read/Write
Test Registers		
0x1A	Test Register. Preset 0x00	R/W
0x1B	Test Register. Preset 0x00	R/W
FIFO Registers		
0x1C	FIFO status	R
0x1D	TX length byte1	R/W
0x1E	TX length byte2	R/W
0x1F	FIFO I/O register	R/W

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6.3 Detailed Register Description

6.3.1 Main Configuration Registers

6.3.1.1 Chip Status Control Register (0x00)

Table 6-2. Chip Status Control Register (0x00)

Function: Control of Power mode, RF on/off, AGC, AM/PM, Direct Mode			
Default: 0x01, preset at EN = L or POR = H			
Bit	**Name**	**Function**	**Description**
B7	stby	1 = Standby Mode	Standby mode keeps all supply regulators, 13.56-MHz SYS_CLK oscillator running. (typical start-up time to full operation 100 µs)
		0 = Active Mode	Active Mode (default)
B6	direct	1 = Direct Mode 0 or 1	Provides user direct access to AFE (Direct Mode 0) or allows user to add their own framing (Direct Mode 1). Bit 6 of ISO Control register must be set by user before entering Direct Mode 0 or 1.
		0 = Direct Mode 2 (default)	Uses SPI or parallel communication with automatic framing and ISO decoders
B5	rf_on	1 = RF output active	Transmitter on, receivers on
		0 = RF output not active	Transmitter off
B4	rf_pwr	1 = half output power	TX_OUT (pin 5) = 8-Ω output impedance P = 100 mW (20 dBm) at 5 V, P = 33 mW (+15 dBm) at 3.3 V
		0 = full output power	TX_OUT (pin 5) = 4-Ω output impedance P = 200 mW (+23 dBm) at 5 V, P = 70 mW(+18 dBm) at 3.3 V
B3	pm_on	1 = selects Aux RX input	RX_IN2 input is used
		0 = selects Main RX input	RX_IN1 input is used
B2	agc_on	1 = AGC on	Enables AGC (AGC gain can be set in register 0x0A)
		0 = AGC off	AGC block is disabled
B1	rec_on	1 = Receiver activated for external field measurement	Forced enabling of receiver and TX oscillator. Used for external field measurement.
		0 = Automatic Enable	Allows enable of the receiver by Bit 5 of this register (0x00)
B0	vrs5_3	1 = 5 V operation 0 = 3 V operation	Selects the V_{IN} voltage range

6.3.1.2 ISO Control Register (0x01)

Table 6-3. ISO Control Register (0x01)

Function: Controls the selection of ISO Standard protocol, Direct Mode and Receive CRC			
Default: 0x02 (ISO15693 high bit rate, one subcarrier, 1 out of 4); it is preset at EN = L or POR = H			
Bit	**Name**	**Function**	**Description**
B7	rx_crc_n	CRC Receive selection	0 = RX CRC (CRC is present in the response) 1 = no RX CRC (CRC is not present in the response)
B6	dir_mode	Direct mode type selection	0 = Direct Mode 0 1 = Direct Mode 1
B5	rfid	RFID / Reserved	0 = RFID Mode 1 = NFC or Card Emulation Mode
B4	iso_4	RFID / NFC Target	RFID: See Table 6-4 for B0:B4 settings based on ISO protocol desired by application NFC: 0 = target, 1 = initiator
B3	iso_3	RFID / NFC Mode	NFC : 0 = passive mode, 1 = active mode
B2	iso_2	RFID / Card Emulation	NFC : 0 = NFC Normal Modes, 1 = Card Emulation Mode
B1	iso_1	RFID / NFC bit rate	NFC: 0 = bit rate selection or card emulation selection, see Table 6-5
B0	iso_0	RFID / NFC bit rate	NFC: 0 = bit rate selection or card emulation selection, see Table 6-5

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Table 6-4. ISO Control Register ISO_x Settings, RFID Mode

ISO_4	ISO_3	ISO_2	ISO_1	ISO_0	Protocol	Remarks
0	0	0	0	0	ISO15693 low bit rate, 6.62 kbps, one subcarrier, 1 out of 4	
0	0	0	0	1	ISO15693 low bit rate, 6.62 kbps, one subcarrier, 1 out of 256	
0	0	0	1	0	ISO15693 high bit rate, 26.48 kbps, one subcarrier, 1 out of 4	Default for reader
0	0	0	1	1	ISO15693 high bit rate, 26.48 kbps, one subcarrier, 1 out of 256	
0	0	1	0	0	ISO15693 low bit rate, 6.67 kbps, double subcarrier, 1 out of 4	
0	0	1	0	1	ISO15693 low bit rate, 6.67 kbps, double subcarrier, 1 out of 256	
0	0	1	1	0	ISO15693 high bit rate, 26.69 kbps, double subcarrier, 1 out of 4	
0	0	1	1	1	ISO15693 high bit rate, 26.69 kbps, double subcarrier, 1 out of 256	
0	1	0	0	0	ISO14443A RX bit rate, 106 kbps	RX bit rate (1)
0	1	0	0	1	ISO14443A RX high bit rate, 212 kbps	
0	1	0	1	0	ISO14443A RX high bit rate, 424 kbps	
0	1	0	1	1	ISO14443A RX high bit rate, 848 kbps	
0	1	1	0	0	ISO14443B RX bit rate, 106 kbps	RX bit rate (1)
0	1	1	0	1	ISO14443B RX high bit rate, 212 kbps	
0	1	1	1	0	ISO14443B RX high bit rate, 424 kbps	
0	1	1	1	1	ISO14443B RX high bit rate, 848 kbps	
1	0	0	1	1	Reserved	
1	0	1	0	0	Reserved	
1	1	0	1	0	FeliCa 212 kbps	
1	1	0	1	1	FeliCa 424 kbps	

(1) For ISO14443A/B, when bit rate of TX is different than RX, settings can be done in register 0x02 or 0x03.

Table 6-5. ISO Control Register ISO_x Settings, NFC Mode (B5 = 1, B2 = 0) or Card Emulation (B5 = 1, B2 = 1)

ISO_1	ISO_0	NFC (B5 = 1, B2 = 0)	Card Emulation (B5 = 1, B2 = 1)
0	0	N/A	ISO14443A
0	1	106 kbps	ISO14443B
1	0	212 kbps	N/A
1	1	424 kbps	N/A

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6.3.2 Control Registers – Sub Level Configuration Registers

6.3.2.1 ISO14443B TX Options Register (0x02)

Table 6-6. ISO14443B TX Options Register (0x02)

Function: Selects the ISO subsets for ISO14443B – TX			
Default: 0x00 at POR = H or EN = L			
Bit	**Name**	**Function**	**Description**
B7	egt2	TX EGT time select MSB	Three bit code defines the number of etu (0-7) which separate two characters. ISO14443B TX only
B6	egt1	TX EGT time select	
B5	egt0	TX EGT time select LSB	
B4	eof_l0	1 = EOF→ 0 length 11 etu 0 = EOF→ 0 length 10 etu	ISO14443B TX only
B3	sof_l1	1 = SOF→ 1 length 03 etu 0 = SOF→ 1 length 02 etu	
B2	sof _l0	1 = SOF→ 0 length 11 etu 0 = SOF→ 0 length 10 etu	
B1	l_egt	1 = EGT after each byte 0 = EGT after last byte is omitted	
B0	Auto SDD_SAK	1 = ISO14443A Layer 4 compliant (in SAK response) 0 = not Layer 4 compliant (in SAK response)	for use with Auto SDD configuration, makes B6 in ISO14443A response 1 or 0, indicating Layer 4 compliance (or not), for all other cases, this bit is unused

6.3.2.2 ISO14443A High-Bit-Rate and Parity Options Register (0x03)

Table 6-7. ISO14443A High-Bit-Rate and Parity Options Register (0x03)

Function: Selects the ISO subsets for ISO14443A – TX			
Default: 0x00 at POR = H or EN = L, and at each write to ISO Control register			
Bit	**Name**	**Function**	**Description**
B7	dif_tx_br	TX bit rate different than RX bit rate enable	Valid for ISO14443A/B high bit rate
B6	tx_br1	TX bit rate	tx_br1 = 0, tx_br = 0 → 106 kbps tx_br1 = 0, tx_br = 1 → 212 kbps tx_br1 = 1, tx_br = 0 → 424 kbps tx_br1 = 1, tx_br = 1 → 848 kbps
B5	tx_br0		
B4	parity-2tx	1 = parity odd except last byte which is even for TX	For 14443A high bit rate, coding and decoding
B3	parity-2rx	1 = parity odd except last byte which is even for RX	
B2			Unused
B1			Unused
B0			Unused

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6.3.2.3 TX Timer High Byte Control Register (0x04)

Table 6-8. TX Timer High Byte Control Register (0x04)

Function: For Timings			
Default: 0xC2 at POR = H or EN = L, and at each write to ISO Control register			
Bit	**Name**	**Function**	**Description**
B7	tm_st1	Timer Start Condition	tm_st1 = 0, tm_st0 = 0 → beginning of TX SOF tm_st1 = 0, tm_st0 = 1 → end of TX SOF tm_st1 = 1, tm_st0 = 0 → beginning of RX SOF tm_st1 = 1, tm_st0 = 1 → end of RX SOF
B6	tm_st0	Timer Start Condition	
B5	tm_lengthD	Timer Length MSB	
B4	tm_lengthC	Timer Length	
B3	tm_lengthB	Timer Length	
B2	tm_lengthA	Timer Length	
B1	tm_length9	Timer Length	
B0	tm_length8	Timer Length LSB	

6.3.2.4 TX Timer Low Byte Control Register (0x05)

Table 6-9. TX Timer Low Byte Control Register (0x05)

Function: For Timings			
Default: 0x00 at POR = H or EN = L, and at each write to ISO Control register			
Bit	**Name**	**Function**	**Description**
B7	tm_length7	Timer Length MSB	Defines the time when delayed transmission is started. RX wait range is 590 ns to 9.76 ms (1 to 16383) Step size is 590 ns All bits low = timer disabled (0x00) Preset 0x00 for all other protocols
B6	tm_length6	Timer Length	
B5	tm_length5	Timer Length	
B4	tm_length4	Timer Length	
B3	tm_length3	Timer Length	
B2	tm_length2	Timer Length	
B1	tm_length1	Timer Length	
B0	tm_length0	Timer Length LSB	

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6.3.2.5 TX Pulse Length Control Register (0x06)

The length of the modulation pulse is defined by the protocol selected in the ISO Control register 0x01. With a high Q antenna, the modulation pulse is typically prolonged, and the tag detects a longer pulse than intended. For such cases, the modulation pulse length can be corrected by using the TX pulse length register 0x06. If the register contains all zeros, then the pulse length is governed by the protocol selection. If the register contains a value other than 0x00, the pulse length is equal to the value of the register in 73.7-ns increments. This means the range of adjustment can be 73.7 ns to 18.8 µs.

Table 6-10. TX Pulse Length Control Register (0x06)

Function: Controls the length of TX pulse			
Default: 0x00 at POR = H or EN = L and at each write to ISO Control register.			
Bit	**Name**	**Function**	**Description**
B7	Pul_p2	Pulse length MSB	The pulse range is 73.7 ns to 18.8 µs (1….255), step size 73.7 ns. All bits low (00): pulse length control is disabled. The following default timings are preset by the ISO Control register (0x01): 9.44 µs → ISO15693 (TI Tag-It HF-I) 11 µs → Reserved 2.36 µs → ISO14443A at 106 kbps 1.4 µs → ISO14443A at 212 kbps 737 ns → ISO14443A at 424 kbps 442 ns → ISO14443A at 848 kbps; pulse length control disabled
B6	Pul_p1		
B5	Pul_p0		
B4	Pul_c4		
B3	Pul_c3		
B2	Pul_c2		
B1	Pul_c1		
B0	Pul_c0	Pulse length LSB	

6.3.2.6 RX No Response Wait Time Register (0x07)

The RX No Response timer is controlled by the RX NO Response Wait Time Register 0x07. This timer measures the time from the start of slot in the anticollision sequence until the start of tag response. If there is no tag response in the defined time, an interrupt request is sent and a flag is set in IRQ status control register 0x0C. This enables the external controller to be relieved of the task of detecting empty slots. The wait time is stored in the register in increments of 37.76 µs. This register is also preset, automatically, for every new protocol selection.

Table 6-11. RX No Response Wait Time Register (0x07)

Function: Defines the time when "no response" interrupt is sent; only for ISO15693			
Default: 0x0E at POR = H or EN = L and at each write to ISO Control register			
Bit	**Name**	**Function**	**Description**
B7	NoResp7	No response MSB	Defines the time when "no response" interrupt is sent. It starts from the end of TX EOF. RX no response wait range is 37.76 µs to 9628 µs (1 to 255), step size is: 37.76 µs. The following default timings are preset by the ISO Control register (0x01): 390 µs → Reserved 529 µs → for all protocols supported, but not listed here 604 µs → Reserved 755 µs → ISO15693 high data rate (TI Tag-It HF-I) 1812 µs → ISO15693 low data rate (TI Tag-It HF-I)
B6	NoResp6		
B5	NoResp5		
B4	NoResp4		
B3	NoResp3		
B2	NoResp2		
B1	NoResp1		
B0	NoResp0	No response LSB	

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6.3.2.7 RX Wait Time Register (0x08)

The RX-wait-time timer is controlled by the value in the RX wait time register 0x08. This timer defines the time after the end of the transmit operation in which the receive decoders are not active (held in reset state). This prevents incorrect detections resulting from transients following the transmit operation. The value of the RX wait time register defines this time in increments of 9.44 µs. This register is preset at every write to ISO Control register 0x01 according to the minimum tag response time defined by each standard.

Table 6-12. RX Wait Time Register (0x08)

Function: Defines the time after TX EOF when the RX input is disregarded for example, to block out electromagnetic disturbance generated by the responding card.			
Default: 0x1F at POR = H or EN = L and at each write to*ISO control* register.			
Bit	**Name**	**Function**	**Description**
B7	Rxw7	RX wait time	Defines the time after the TX EOF during which the RX input is ignored. Time starts from the end of TX EOF. RX wait range is 9.44 µs to 2407 µs (1 to 255), Step size 9.44 µs. The following default timings are preset by the ISO Control register (0x01): 9.44 µs → FeliCa 66 µs → ISO14443A and B 180 µs → Reserved 293 µs → ISO15693 (TI Tag-It HF-I)
B6	Rxw6		
B5	Rxw5		
B4	Rxw4		
B3	Rxw3		
B2	Rxw2		
B1	Rxw1		
B1	Rxw0		

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6.3.2.8 Modulator and SYS_CLK Control Register (0x09)

The frequency of SYS_CLK (pin 27) is programmable by the bits B4 and B5 of this register. The frequency of the TRF7970A system clock oscillator is divided by 1, 2 or 4 resulting in available SYS_CLK frequencies of 13.56 MHz or 6.78 MHz or 3.39 MHz.

The ASK modulation depth is controlled by bits B0, B1 and B2. The range of ASK modulation is 7% to 30% or 100% (OOK). The selection between ASK and OOK (100%) modulation can also be done using direct input OOK (pin 12). The direct control of OOK/ASK using OOK pin is only possible if the function is enabled by setting B6 = 1 (en_ook_p) in this register (0x09) and the ISO Control Register (0x01, B6 = 1). When configured this way, the MOD (pin 14) is used as input for the modulation signal.

Table 6-13. Modulator and SYS_CLK Control Register (0x09)

Function: Controls the modulation input and depth, ASK / OOK control and clock output to external system (MCU)						
Default: 0x91 at POR = H or EN = L, and at each write to ISO control register, except Clo1 and Clo0.						
Bit	**Name**	**Function**	**Description**			
B7	27MHz	Enables 27.12-MHz crystal	Default = 1 (enabled)			
B6	en_ook_p	1 = Enables external selection of ASK or OOK modulation 0 = Default operation as defined in B0 to B2 (0x09)	Enable ASK/OOK pin (pin 12) for "on the fly change" between any preselected ASK modulation as defined by B0 to B2 and OOK modulation: If B6 is 1, pin 12 is configured as follows: 1 = OOK modulation 0 = Modulation as defined in B0 to B2 (0x09)			
B5	Clo1	SYS_CLK output frequency MSB	**Clo1**	**Clo0**	**SYS_CLK Output** (if 13.56-MHz crystal is used)	**SYS_CLK Output** (if 27.12-MHz crystal is used)
			0	0	Disabled	Disabled
			0	1	3.39 MHz	6.78 MHz
B4	Clo0	SYS_CLK output frequency LSB	1	0	6.78 MHz	13.56 MHz
			1	1	13.56 MHz	27.12 MHz
B3	en_ana	1 = Sets pin 12 (ASK/OOK) as an analog output 0 = Default	For test and measurement purpose. ASK/OOK pin 12 can be used to monitor the analog subcarrier signal before the digitizing with DC level equal to AGND.			
B2	Pm2	Modulation depth MSB	**Pm2**	**Pm1**	**Pm0**	**Mod Type and %**
			0	0	0	ASK 10%
			0	0	1	OOK (100%)
B1	Pm1	Modulation depth	0	1	0	ASK 7%
			0	1	1	ASK 8.5%
			1	0	0	ASK 13%
B0	Pm0	Modulation depth LSB	1	0	1	ASK 16%
			1	1	0	ASK 22%
			1	1	1	ASK 30%

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6.3.2.9 RX Special Setting Register (Address 0x0A)

Table 6-14. RX Special Setting Register (Address 0x0A)

Function: Sets the gains and filters directly			
Default: 0x40 at POR = H or EN = L, and at each write to the ISO Control register 0x01. When bits B7, B6, B5 and B4 are all zero, the filters are set for ISO14443B (240 kHz to 1.4 MHz).			
Bit	**Name**	**Function**	**Description**
B7	C212	Bandpass 110 kHz to 570 kHz	Appropriate for 212-kHz subcarrier system (FeliCa)
B6	C424	Bandpass 200 kHz to 900 kHz	Appropriate for 424-kHz subcarrier used in ISO15693
B5	M848	Bandpass 450 kHz to 1.5 MHz	Appropriate for Manchester-coded 848-kHz subcarrier used in ISO14443A and B
B4	hbt	Bandpass 100 kHz to 1.5 MHz Gain reduced for 18 dB	Appropriate for highest bit rate (848 kbps) used in high-bit-rate ISO14443
B3	gd1	00 = Gain reduction 0 dB 01 = Gain reduction for 5 dB 10 = Gain reduction for 10 dB 11 = Gain reduction for 15 dB	Sets the RX gain reduction, and reduces sensitivity
B2	gd2		
B1	agcr	AGC activation level change	AGC activation level changed from five times the digitizing level to three times the digitizing level. 1 = 3x 0 = 5x
B0	no-lim	AGC action is not limited in time	AGC action can be done any time during receive process. It is not limited to the start of receive ("max hold"). 1 = continuously – no time limit 0 = 8 subcarrier pulses

The first four steps of the AGC control are comparator adjustment. The second three steps are real gain reduction done automatically by AGC control. The AGC is turned on after TX.

The first gain and filtering stage following the RF envelope detector has a nominal gain of 15 and the 3-dB band-pass frequencies are adjustable in the range from 100 kHz to 400 kHz for high pass and 600 kHz to 1.5 MHz for low pass. The next gain and filtering stage has a nominal gain of 8 and the frequency characteristic identical to first stage. The filter setting is done automatically with internal preset for each new selection of communication standard in ISO Control register (0x01). Additional corrections can be done by directly writing into the RX Special Setting register 0x0A.

The second receiver gain stage and digitizer stage are included in the AGC loop. The AGC loop can be activated by setting the bit B2 = 1 (agc-on) in Chip Status Control register 0x00. If activated the AGC monitors the signal level at the input of digitizing stage. If the signal level is significantly higher than the digitizing threshold level, the gain reduction is activated. The signal level, at which the action is started, is by default five times the digitizing threshold level. It can be reduced to three times the digitizing level by setting bit B1 = 1 (agcr) in RX Special Setting register (0x0A).

The AGC action is fast and it typically finishes after four subcarrier pulses. By default the AGC action is blocked after first few pulses of subcarrier signal so AGC cannot interfere with signal reception during rest of data packet. In certain cases, this is not optimal, so this blocking can be removed by setting B0 = 1 (no_lim) in RX Special Setting register (0x0A).

NOTE

The setting of bits B4, B5, B6 and B7 to zero selects bandpass characteristic of 240 kHz to 1.4 MHz. This is appropriate for ISO14443B, FeliCa protocol, and ISO14443A higher bit rates 212 kbps and 424 kbps.

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6.3.2.10 Regulator and I/O Control Register (0x0B)

Table 6-15. Regulator and I/O Control Register (0x0B)

Function: Control the three voltage regulators			
Default: 0x87 at POR = H or EN = L			
Bit	**Name**	**Function**	**Description**
B7	auto_reg	0 = Manual settings; see B0 to B2 in Table 6-16 and Table 6-17 1 = Automatic setting; see Table 6-18 and Table 6-19	Auto system sets $V_{DD_RF} = V_{IN} – 250$ mV and $V_{DD_A} = V_{IN} – 250$ mV and $V_{DD_X} = V_{IN} – 250$ mV, but not higher than 3.4 V.
B6	en_ext_pa	Support for external power amplifier	Internal peak detectors are disabled, receiver inputs (RX_IN1 and RX_IN2) accept externally demodulated subcarrier. At the same time ASK/OOK pin 12 becomes modulation output for external TX amplifier.
B5	io_low	1 = enable low peripheral communication voltage	When B5 = 1, maintains the output driving capabilities of the I/O pins connected to the level shifter under low voltage operation. Should be set 1 when $V_{DD_I/O}$ voltage is between 1.8 V to 2.7 V.
B4	Unused	No function	Default is 0.
B3	Unused	No function	Default is 0.
B2	vrs2	Voltage set MSB voltage set LSB	Vrs3_5 = L: V_{DD_RF}, V_{DD_A}, V_{DD_X} range 2.7 V to 3.4 V; see Table 6-16 through Table 6-19
B1	vrs1		
B0	vrs0		

Table 6-16. Supply-Regulator Setting – Manual 5-V System

Register	**Option Bits Setting in Control Register**								**Action**
	B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**	
00								1	5-V system
0B	0								Manual regulator setting
0B	0					1	1	1	V_{DD_RF} = 5 V, V_{DD_A} = 3.5 V, V_{DD_X} = 3.4 V
0B	0					1	1	0	V_{DD_RF} = 4.9 V, V_{DD_A} = 3.5 V, V_{DD_X} = 3.4 V
0B	0					1	0	1	V_{DD_RF} = 4.8 V, V_{DD_A} = 3.5 V, V_{DD_X} = 3.4 V
0B	0					1	0	0	V_{DD_RF} = 4.7 V, V_{DD_A} = 3.5 V, V_{DD_X} = 3.4 V
0B	0					0	1	1	V_{DD_RF} = 4.6 V, V_{DD_A} = 3.5 V, V_{DD_X} = 3.4 V
0B	0					0	1	0	V_{DD_RF} = 4.5 V, V_{DD_A} = 3.5 V, V_{DD_X} = 3.4 V
0B	0					0	0	1	V_{DD_RF} = 4.4 V, V_{DD_A} = 3.5 V, V_{DD_X} = 3.4 V
0B	0					0	0	0	V_{DD_RF} = 4.3 V, V_{DD_A} = 3.5 V, V_{DD_X} = 3.4 V

Table 6-17. Supply-Regulator Setting – Manual 3-V System

Register	**Option Bits Setting in Control Register**								**Action**
	B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**	
00								0	3-V system
0B	0								Manual regulator setting
0B	0					1	1	1	V_{DD_RF} = 3.4 V, V_{DD_A} and V_{DD_X} = 3.4 V
0B	0					1	1	0	V_{DD_RF} = 3.3 V, V_{DD_A} and V_{DD_X} = 3.3 V
0B	0					1	0	1	V_{DD_RF} = 3.2 V, V_{DD_A} and V_{DD_X} = 3.2 V
0B	0					1	0	0	V_{DD_RF} = 3.1 V, V_{DD_A} and V_{DD_X} = 3.1 V
0B	0					0	1	1	V_{DD_RF} = 3.0 V, V_{DD_A} and V_{DD_X} = 3.0 V
0B	0					0	1	0	V_{DD_RF} = 2.9 V, V_{DD_A} and V_{DD_X} = 2.9 V
0B	0					0	0	1	V_{DD_RF} = 2.8 V, V_{DD_A} and V_{DD_X} = 2.8 V
0B	0					0	0	0	V_{DD_RF} = 2.7 V, V_{DD_A} and V_{DD_X} = 2.7 V

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Table 6-18. Supply-Regulator Setting – Automatic 5-V System

Register	Option Bits Setting in Control Register								Action
	B7	B6	B5	B4	B3	B2	B1	B0	
00								1	5-V system
0B	1					x (1)	1	1	Automatic regulator setting 250-mV difference
0B	1					x	1	0	Automatic regulator setting 350-mV difference
0B	1					x	0	0	Automatic regulator setting 400-mV difference

(1) x = don't care

Table 6-19. Supply-Regulator Setting – Automatic 3-V System

Register	Option Bits Setting in Control Register								Action
	B7	B6	B5	B4	B3	B2	B1	B0	
00								0	3-V system
0B	1					x (1)	1	1	Automatic regulator setting 250-mV difference
0B	1					x	1	0	Automatic regulator setting 350-mV difference
0B	1					x	0	0	Automatic regulator setting 400-mV difference

(1) x = don't care

6.3.3 Status Registers

6.3.3.1 IRQ Status Register (0x0C)

Table 6-20. IRQ Status Register (0x0C)

Function: Information available about TRF7970A IRQ and TX/RX status			
Default: 0x00 at POR = H or EN = L, and at each write to the ISO Control Register 0x01. It is also automatically reset at the end of a read phase. The reset also removes the IRQ flag.			
Bit	**Name**	**Function**	**Description**
B7	Irq_tx	IRQ set due to end of TX	Signals that TX is in progress. The flag is set at the start of TX but the interrupt request (IRQ = 1) is sent when TX is finished.
B6	Irg_srx	IRQ set due to RX start	Signals that RX SOF was received and RX is in progress. The flag is set at the start of RX but the interrupt request (IRQ = 1) is sent when RX is finished.
B5	Irq_fifo	Signals the FIFO is 1/3 > FIFO > 2/3	Signals FIFO high or low
B4	Irq_err1	CRC error	Indicates receive CRC error only if B7 (no RX CRC) of ISO Control register is set to 0.
B3	Irq_err2	Parity error	Indicates parity error for ISO14443A
B2	Irq_err3	Byte framing or EOF error	Indicates framing error
B1	Irq_col	Collision error	Collision error for ISO14443A and ISO15693 single subcarrier. Bit is set if more then 6 or 7 (as defined in register 0x01) are detected inside one bit period of ISO14443A 106 kbps. Collision error bit can also be triggered by external noise.
B0	Irq_noresp	No-response timeinterrupt	No response within the "No-response time" defined in RX No-response Wait Time register (0x07). Signals the MCU that next slot command can be sent. Only for ISO15693.

To reset (clear) the register 0x0C and the IRQ line, the register must be read. During Transmit the decoder is disabled, only bits B5 and B7 can be changed. During Receive only bit B6 can be changed, but does not trigger the IRQ line immediately. The IRQ signal is set at the end of Transmit and Receive phase.

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Table 6-21. IRQ Status Register (0x0C) for NFC and Card Emulation Operation

Function: Information available about TRF7970A IRQ and TX/RX status			
Default: 0x00 at POR = H or EN = L, and at each write to the ISO Control Register 0x01. It is also automatically reset at the end of a read phase. The reset also removes the IRQ flag.			
Bit	**Name**	**Function**	**Description**
B7	Irq_tx	IRQ set due to end of TX	Signals that TX is in progress. The flag is set at the start of TX but the interrupt request (IRQ = 1) is sent when TX is finished.
B6	Irg_srx	IRQ set due to RX start	Signals that RX SOF was received and RX is in progress. The flag is set at the start of RX but the interrupt request (IRQ = 1) is sent when RX is finished.
B5	Irq_fifo	Signals the FIFO is 1/3 > FIFO > 2/3	Signals FIFO high or low
B4	Irq_err1	Protocol error	Any protocol error
B3	Irq_sdd	SDD completed	SDD (passive target at 106 kbps) successfully finished
B2	Irq_rf	RF field change	Sufficient RF signal level for operation was reached or lost
B1	Irq_col	RF collision avoidance finished	The system has finished collision avoidance and the minimum wait time is elapsed.
B0	Irq_col_err	RF collision avoidance not finished successfully	The external RF field was present so the collision avoidance could not be carried out.

6.3.3.2 Collision Position Register (0x0D) and Interrupt Mask Register (0x0E)

Table 6-22. Collision Position Register (0x0D) and Interrupt Mask Register (0x0E)

Default: 0x3E at POR = H and EN = L. Collision bits reset automatically after read operation.			
Bit	**Name**	**Function**	**Description**
B7	Col9	Bit position of collision MSB	Supports ISO14443A
B6	Col8	Bit position of collision	
B5	En_irq_fifo	Interrupt enable for FIFO	Default = 1
B4	En_irq_err1	Interrupt enable for CRC	Default = 1
B3	En_irq_err2	Interrupt enable for Parity	Default = 1
B2	En_irq_err3	Interrupt enable for Framing error or EOF	Default = 1
B1	En_irq_col	Interrupt enable for collision error	Default = 1
B0	En_irq_noresp	Enables no-response interrupt	Default = 0

Table 6-23. Collision Position Register (0x0E)

Function: Displays the bit position of collision or error			
Default: 0x00 at POR = H and EN = L. Automatically reset after read operation.			
Bit	**Name**	**Function**	**Description**
B7	Col7	Bit position of collision MSB	ISO14443A mainly supported, in the other protocols this register shows the bit position of error. Either frame, SOF/EOF, parity or CRC error.
B6	Col6		
B5	Col5		
B4	Col4		
B3	Col3		
B2	Col2		
B1	Col1		
B0	Col0	Bit position of collision LSB	

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6.3.3.3 RSSI Levels and Oscillator Status Register (0x0F)

Table 6-24. RSSI Levels and Oscillator Status Register (0x0F)

Function: Displays the signal strength on both reception channels and RF amplitude during RF-off state. The RSSI values are valid from reception start till start of next transmission.			
Bit	**Name**	**Function**	**Description**
B7	Unused		
B6	osc_ok	Crystal oscillator stable indicator	13.56-MHz frequency stable (≈200 µs)
B5	rssi_x2	MSB RSSI value of auxiliary RX (RX_IN2)	Auxiliary channel is by default RX_IN2. The input can be swapped by B3 = 1 (Chip State Control register 0x00). If "swapped", the Auxiliary channel is connected to RX_IN1 and, hence, the Auxiliary RSSI represents the signal level at RX_IN2.
B4	rssi_x1	Auxiliary channel RSSI	
B3	rssi_x0	MSB RSSI value of auxiliary RX (RX_IN2)	
B2	rssi_2	MSB RSSI value of main RX (RX_IN1)	Active channel is default and can be set with option bit B3 = 0 of chip state control register 0x00.
B1	rssi_1	Main channel RSSI	
B0	rssi_0	LSB RSSI value of main RX (RX_IN1)	

RSSI measurement block is measuring the demodulated envelope signal (except in case of direct command for RF amplitude measurement described later in direct commands section). The measuring system is latching the peak value, so the RSSI level can be read after the end of receive packet. The RSSI value is reset during next transmit action of the reader, so the new tag response level can be measured. The RSSI levels calculated to the RF_IN1 and RF_IN2 are presented in Section 5.4.1.1 and Section 5.4.1.2. The RSSI has 7 steps (3 bits) with 4-dB increment. The input level is the peak to peak modulation level of RF signal measured on one side envelope (positive or negative).

6.3.3.4 Special Functions Register (0x10)

Table 6-25. Special Functions Register (0x10)

Function: User configurable options for ISO14443A specific operations			
Bit	**Name**	**Function**	**Description**
B7		Reserved	Reserved
B6		Reserved	Reserved
B5	par43	Disables parity checking for ISO14443A	
B4	next_slot_37us	0 = 18.88 µs 1 = 37.77 µs	Sets the time grid for next slot command in ISO15693
B3	Sp_dir_mode	Bit stream transmit for MIFARE at 106 kbps	Enables direct mode for transmitting ISO14443A data, bypassing the FIFO and feeding the data bit stream directly onto the encoder.
B2	4_bit_RX	0 = normal receive 1 = 4-bit receive	Enable 4-bit replay for example, ACK, NACK used by some cards; for example, MIFARE Ultralight
B1	14_anticoll	0 = anticollision framing (0x93, 0x95, 0x97) 1 = normal framing (no broken bytes)	Disable anticollision frames for 14443A (this bit should be set to 1 after anticollision is finished)
B0	col_7_6	0 = 7 subcarrier pulses 1 = 6 subcarrier pulses	Selects the number of subcarrier pulses that trigger collision error in the 14443A - 106 kbps

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6.3.3.5 Special Functions Register (0x11)

Table 6-26. Special Functions Register (0x11)

Function: Indicate IRQ status for RX operations.			
Bit	**Name**	**Function**	**Description**
B7	Reserved		Reserved
B6	Reserved		Reserved
B5	Reserved		Reserved
B4	Reserved		Reserved
B3	Reserved		Reserved
B2	Reserved		Reserved
B1	Reserved		Reserved
B0	irg_srx	Copy of the RX start signal (Bit 6) of the IRQ Status Register (0x0C)	Signals the RX SOF was received and the RX is in progress. IRQ when RX is completed.

6.3.3.6 Adjustable FIFO IRQ Levels Register (0x14)

Table 6-27. Adjustable FIFO IRQ Levels Register (0x14)

Function: Adjusts level at which FIFO indicates status by IRQ					
Default: 0x00 at POR = H and EN = L					
Bit	**Name**	**Function**	**Description**		
B7	Reserved		Reserved		
B6	Reserved		Reserved		
B5	Reserved		Reserved		
B4	Reserved		Reserved		
B3	Wlh_1	FIFO high IRQ level (during RX)	**Wlh_1**	**Wlh_0**	**IRQ Level**
B2	Wlh_0		0	0	124
			0	1	120
			1	0	112
			1	1	96
B1	Wll_1	FIFO low IRQ level (during TX)	**Wll_1**	**Wll_0**	**IRQ Level**
B0	Wll_0		0	0	4
			0	1	8
			1	0	16
			1	1	32

6.3.3.7 NFC Low Field Level Register (0x16)

Table 6-28. NFC Low Field Level Register (0x16)

Function: Defines level for RF collision avoidance			
Default: 0x00 at POR = H and EN = L.			
Bit	**Name**	**Function**	**Description**
B7	Clex_dis	Disable clock extractor	NFC passive 106-kbps and ISO14443A card emulation
B6	Hash6	N/A	
B5	Hash5	N/A	
B4	Hash4	N/A	
B3	Hash3	N/A	
B2	Rfdet_I2	RF field level for RF collision avoidance	Comparator output is displayed in B6 of the NFC Target Protocol register (0x19)
B1	Rfdet_I1		
B0	Rfdet_I0		

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6.3.3.8 NFCID1 Number Register (0x17)

This register is used to hold the ID of the TRF7970A for use during card emulation and NFC peer-to-peer target operations.

The procedure for writing the ID into register 0x17 is the following:

1. Write bits 5, 6, and 7 in register 0x18 to enable SDD anticollision (bit 5), and set bit 6 and 7 to select the ID length of 4, 7, or 10 bytes.
2. Write the ID into register 0x17. This should be done using write continuous mode with 4, 7, or 10 bytes (according to what was set in register 0x18 bits 6 and 7).

6.3.3.9 NFC Target Detection Level Register (0x18)

Table 6-29. NFC Target Detection Level Register (0x18)

<table>
<tr><td colspan="5">Function: Defines level for RF wake up, enables automatic SDD and gives NFCID size. This register is supplied by Vin to ensure data retention during complete power down.</td></tr>
<tr><td colspan="5">Default: 0x00 at POR on Vin (not POR based on V_{DD_X}) and not reset at EN = 0</td></tr>
<tr><th>Bit</th><th>Name</th><th>Function</th><th colspan="2">Description</th></tr>
<tr><td rowspan="5">B7

B6</td><td rowspan="5">Id_s1

Id_s0</td><td rowspan="5">NFCID1 size used in 106-kbps passive target SDD</td><td>Id_s1</td><td>Id_s0</td><td>NFCID1 Size (bytes)</td></tr>
<tr><td>0</td><td>0</td><td>4</td></tr>
<tr><td>0</td><td>1</td><td>7</td></tr>
<tr><td>1</td><td>0</td><td>10</td></tr>
<tr><td>1</td><td>1</td><td>Not allowed</td></tr>
<tr><td>B5</td><td>Sdd_en</td><td></td><td colspan="3">Automatic SDD using internal state machine and ID stored in the NFCID1 Number register (0x17)</td></tr>
<tr><td>B4</td><td></td><td>N/A</td><td colspan="3"></td></tr>
<tr><td>B3</td><td>Hi_rf</td><td>Extended range for RF measurements</td><td colspan="3"></td></tr>
<tr><td>B2</td><td>Rfdet_h2</td><td rowspan="3">RF field level required for system wakeup. If all bits are 0, then the RF level detection is off.</td><td colspan="3" rowspan="3">Comparator output is displayed in B7 of the NFC Target Protocol register (0x19)</td></tr>
<tr><td>B1</td><td>Rfdet_h1</td></tr>
<tr><td>B0</td><td>Rfdet_h0</td></tr>
</table>

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6.3.3.10 NFC Target Protocol Register (0x19)

This register is used (when read) to display the bit rate and protocol type when an NFC/RFID Initiator/Reader is presented. An example use of this scenario would be when the TRF7970A is placed into card emulation (Type A or Type B) and another TRF7970A or NFC device (polling for other NFC devices) is presented to the TRF7970A in card emulation mode. The IRQ indicates that a field was detected (IRQ Status = 0x04) or that Auto SDD has completed (IRQ Status = 0x08, if configured for AutoSDD).

If Auto SDD is set and 0x04 is returned in IRQ status, then this register can be read out to see which commands are coming in for gaining knowledge of the polling cycle sequence. Then, when the correct first matching command (that is, REQA or REQB) is issued from Reader or Initiator, if AutoSDD is set, the IRQ fires and the IRQ Status is 0x08, indicating completion of the SDD. The next IRQ should return 0x40 as status, the Register 0x19 can be checked to make sure it is correct value (that is, 0xC9 for Type A at 106 kpbs or 0xC5 for Type B at 106 kbps) indicating there are bytes in the FIFO and a read of the FIFO status indicates how many bytes to read out. For example, after AutoSDD is completed, there are four bytes in the FIFO, and these should be the RATS command coming in from the reader, which the MCU controlling the TRF7970A in Card Emulation mode must respond to. If AutoSDD is not set, as another example with the TRF7970A in ISO14443B Card Emulation mode, then the field detect happens as previously described and IRQs also fire to indicate RX is complete (0x40). This register must be checked and compared against case statement structure that is set up for the value of this register to be 0xC5, indicating that an ISO14443B command at 106 kbps was issued. When this register (0x19) is 0xC5, then the FIFO Status can be read and should hold a value of 0x03, and when read, be the REQB command (0x05, 0x00, 0x00); the controlling MCU must respond with the ATQB response. The next steps for either of these examples follow the revelent portions of the ISO14443-3 or -4 standards, then the NFC Forum specifications, depending on the system use case or application.

Table 6-30. NFC Target Protocol Register (0x19)

Function: Displays the bit rate and protocol type (active or passive) transmitted by initiator in first command. It also displays the comparator outputs of both RF level detectors.			
Default: 0x00 at POR = H and EN = L. B0 – B4 are automatically reset after MCU read operation. B6 and B7 continuously display the RF level comparator outputs.			
Bit	**Name**	**Function**	**Description**
B7	Rf_h	RF level is above the wake-up level setting	The wakeup level is defined by bits B0 to B2 in the NFC Target Detection Level register (0x18)
B6	Rf_l	RF level is above the RF collision avoidance level setting	The collision avoidance level is defined by bits B0 – B2 in the register 0x16 (NFC Low Field Detection Level)
B5	Reserved	Reserved	Reserved
B4	FeliCa	1 = FeliCa 0 = ISO14443A	The first initiator command had physical level coding of FeliCa or ISO14443A
B3	Pas_106	Passive target at 106 kbps or transponder emulation	The first initiator/reader command was SENS_REQ or ALL_REQ
B2	Pas_14443B	ISO14443B transponder emulation	The first reader command was ISO14443B
B1	NFCBR1	Bit rate of first received command	00 = Reserved 01 = 106 kbps 10 = 212 kbps 11 = 424 kbps
B0	NFCBR0		

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6.3.4 Test Registers

6.3.4.1 Test Register (0x1A)

Table 6-31. Test Register (0x1A) (for Test or Direct Use)

Default: 0x00 at POR = H and EN = L.			
Bit	**Name**	**Function**	**Description**
B7	OOK_Subc_In	Subcarrier Input	OOK Pin becomes decoder digital input
B6	MOD_Subc_Out	Subcarrier Output	MOD Pin becomes receiver subcarrier output
B5	MOD_Direct	Direct TX modulation and RX reset	MOD Pin becomes receiver subcarrier output
B4	o_sel	First stage output selection	o_sel = L: Second Stage output used for analog out and digitizing o_sel = H: Second Stage output used for analog out and digitizing
B3	low2	Second stage gain -6 dB, HP corner frequency/2	
B2	low1	First stage gain -6 dB, HP corner frequency/2	
B1	zun	Input followers test	
B0	Test_AGC	AGC test, AGC level is seen on rssi_210 bits	

6.3.4.2 Test Register 0x1B

Table 6-32. Test Register (0x1B) (for Test or Direct Use)

Default: 0x00 at POR = H and EN = L. When a test_dec or test_io is set IC is switched to test mode. Test Mode persists until a stop condition arrives. At stop condition the test_dec and test_io bits are cleared.			
Bit	**Name**	**Function**	**Description**
B7	test_rf_level	RF level test	
B6			
B5			
B4			
B3	test_io1	I/O test	Not implemented
B2	test_io0		
B1	test_dec	Decoder test mode	
B0	clock_su	Coder clock 13.56 MHz	For faster test of coders

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6.3.5 FIFO Control Registers

6.3.5.1 FIFO Status Register (0x1C)

Table 6-33. FIFO Status Register (0x1C)

Function: Number of bytes available to be read from FIFO (= N number of bytes, in hexadecimal)			
Bit	**Name**	**Function**	**Description**
B7	Foverflow	FIFO overflow error	Bit is set when FIFO has more than 128 bytes presented to it
B6	Fb6	FIFO bytes fb[6]	
B5	Fb5	FIFO bytes fb[5]	
B4	Fb4	FIFO bytes fb[4]	
B3	Fb3	FIFO bytes fb[3]	Bits B0:B6 indicate how many bytes that are in the FIFO to be read out (= N number of bytes, in hex)
B2	Fb2	FIFO bytes fb[2]	
B1	Fb1	FIFO bytes fb[1]	
B0	Fb0	FIFO bytes fb[0]	

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6.3.5.2 TX Length Byte1 Register (0x1D), TX Length Byte2 Register (0x1E)

Table 6-34. TX Length Byte1 Register (0x1D)

Function: High 2 nibbles of complete, intended bytes to be transferred through FIFO			
Register default is set to 0x00 at POR and EN = 0. It is also automatically reset at TX EOF			
Bit	**Name**	**Function**	**Description**
B7	Txl11	Number of complete byte bn[11]	High nibble of complete, intended bytes to be transmitted
B6	Txl10	Number of complete byte bn[10]	
B5	Txl9	Number of complete byte bn[9]	
B4	Txl8	Number of complete byte bn[8]	
B3	Txl7	Number of complete byte bn[7]	Middle nibble of complete, intended bytes to be transmitted
B2	Txl6	Number of complete byte bn[6]	
B1	Txl5	Number of complete byte bn[5]	
B0	Txl4	Number of complete byte bn[4]	

Table 6-35. TX Length Byte2 Register (0x1E)

Function: Low nibbles of complete bytes to be transferred through FIFO; Information about a broken byte and number of bits to be transferred from it			
Default: 0x00 at POR and EN = 0. It is also automatically reset at TX EOF			
Bit	**Name**	**Function**	**Description**
B7	Txl3	Number of complete byte bn[3]	Low nibble of complete, intended bytes to be transmitted
B6	Txl2	Number of complete byte bn[2]	
B5	Txl1	Number of complete byte bn[1]	
B4	Txl0	Number of complete byte bn[0]	
B3	Bb2	Broken byte number of bits bb[2]	Number of bits in the last broken byte to be transmitted. It is taken into account only when broken byte flag is set.
B2	Bb1	Broken byte number of bits bb[1]	
B1	Bb0	Broken byte number of bits bb[0]	
B0	Bbf	Broken byte flag	B0 = 1, indicates that last byte is not complete 8 bits wide.

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7 System Design

7.1 Layout Considerations

Keep all decoupling capacitors as close to the IC as possible, with the high-frequency decoupling capacitors (10 nF) closer than the low-frequency decoupling capacitors (2.2 µF).

Place ground vias as close as possible to the ground side of the capacitors and reader IC pins to minimize possible ground loops.

It is not recommend to use any inductor sizes below 0603, as the output power can be compromised. If smaller inductors are necessary, output performance must be confirmed in the final application.

Pay close attention to the required load capacitance of the crystal, and adjust the two external shunt capacitors accordingly. Follow the recommendations of the crystal manufacturer for those values.

There should be a common ground plane for the digital and analog sections. The multiple ground sections or islands should have vias that tie the different sections of the planes together.

Ensure that the exposed thermal pad at the center of the reader IC is properly laid out. It should be tied to ground to help dissipate any heat from the package.

All trace line lengths should be made as short as possible, particularly the RF output path, crystal connections, and control lines from the reader to the microprocessor. Proper placement of the TRF7970A, microprocessor, crystal, and RF connection/connector help facilitate this.

Avoid crossing of digital lines under RF signal lines. Also, avoid crossing of digital lines with other digital lines when possible. If the crossings are unavoidable, 90° crossings should be used to minimize coupling of the lines.

Depending on the production test plan, consider possible implementations of test pads or test vias for use during testing. The necessary pads or vias should be placed in accordance with the proposed test plan to enable easy access to those test points.

If the system implementation is complex (for example, if the RFID reader module is a subsystem of a greater system with other modules (Bluetooth, WiFi, microprocessors, and clocks), special considerations should be taken to ensure that there is no noise coupling into the supply lines. If needed, special filtering or regulator considerations should be used to minimize or eliminate noise in these systems.

For more information/details on layout considerations, see the *TRF796x HF-RFID Reader Layout Design Guide* (SLOA139).

7.2 Impedance Matching TX_Out (Pin 5) to 50 Ω

The output impedance of the TRF7970A when operated at full power out setting is nominally 4 + j0 (4 Ω real). This impedance must be matched to a resonant circuit and TI recommends matching circuit from 4 Ω to 50 Ω, as commercially available test equipment (for example, spectrum analyzers, power meters, and network analyzers) are 50-Ω systems. An impedance-matching reference circuit can be seen in Figure 7-1 and Figure 7-2. This section explains how the values were calculated.

Starting with the 4-Ω source, the process of going from 4 Ω to 50 Ω can be represented on a Smith Chart simulator (available from http://www.fritz.dellsperger.net/). The elements are combined where appropriate (see Figure 7-1).

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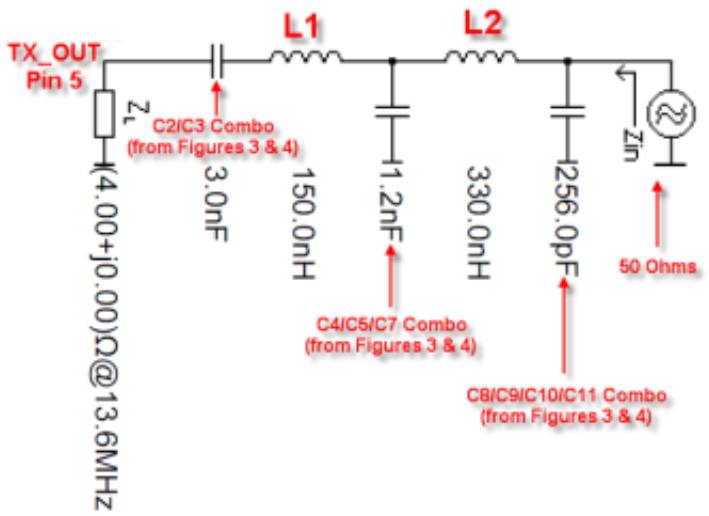


Figure 7-1. Impedance Matching Circuit

This yields the Smith Chart Simulation shown in Figure 7-2.

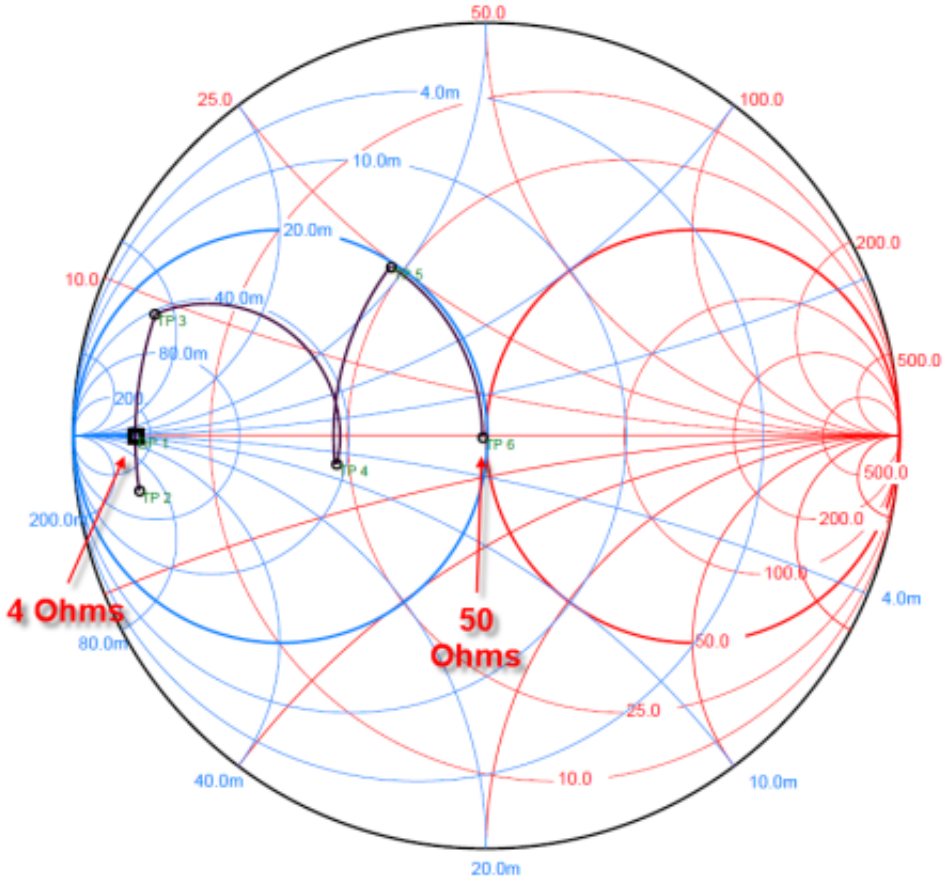


Figure 7-2. Smith Chart Simulation

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Resulting power out can be measured with a power meter or spectrum analyzer with power meter function or other equipment capable of making a "hot" measurement. Observe maximum power input levels on test equipment and use attenuators whenever available to avoid damage to equipment. Expected output power levels under various operating conditions are shown in Table 6-2.

7.3 Reader Antenna Design Guidelines

For HF antenna design considerations using the TRF7970A, see these documents:

- *Antenna Matching for the TRF7960 RFID Reader* (SLOA135)
- *TRF7960TB HF RFID Reader Module User's Guide* (SLOU297)

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8 Revision History

Revision	Comments
SLOS743	Initial release
SLOS743A	Changed Figure 4-1, Figure 4-2, and Figure 5-17. Changed Section 5.9.6, Step 5 and Step 6, including adding figures. Changed Table 6-6, Table 6-13, and Table 6-33. Added paragraph for NFC Target Protocol Register (0x19) to cover use with two examples.
SLOS743B	Section 5.9.1.4, Fixed typo. Section 6.3.3.1, Changed bit B5. Section 6.3.1.1, Changed bit B3. Section 6.3.5.2, Changed high, middle, low nibble descriptions.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TRF7970ARHBR	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TRF7970ARHBT	ACTIVE	QFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TRF7970ATB	ACTIVE			0	1	TBD	Call TI	Call TI	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

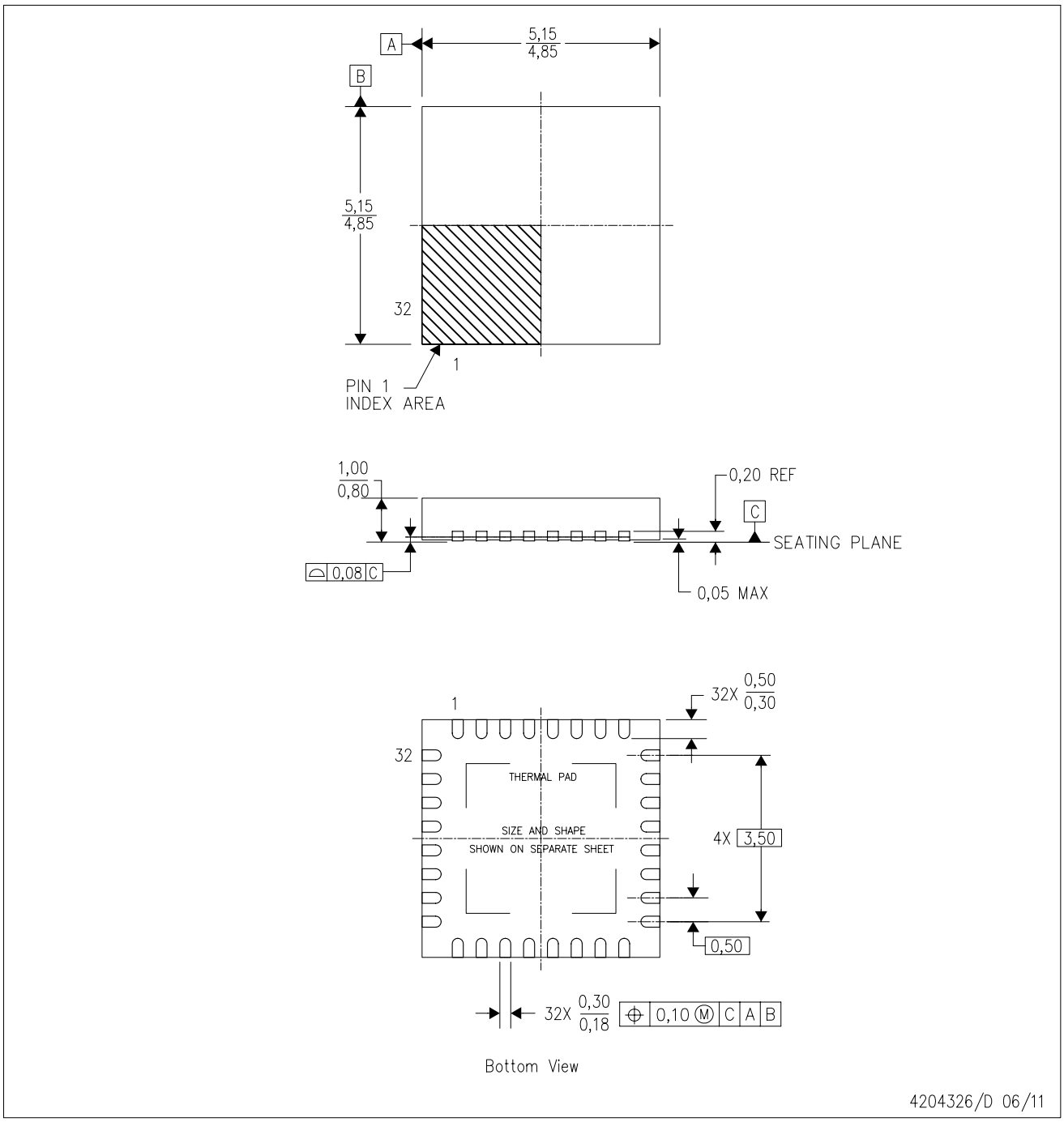
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

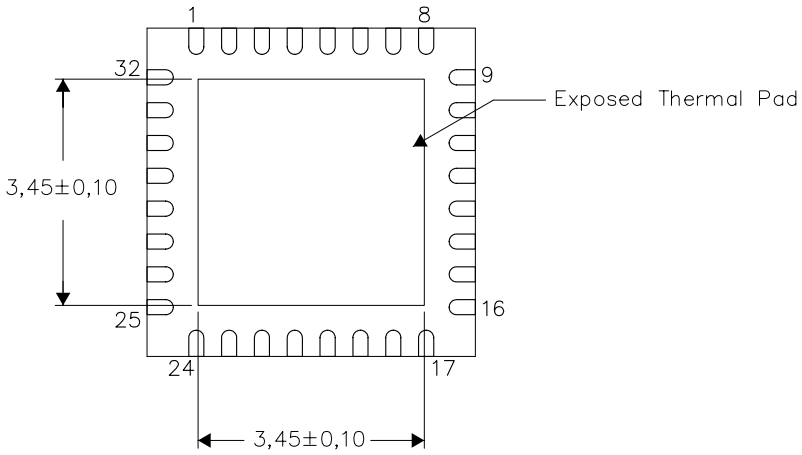
RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



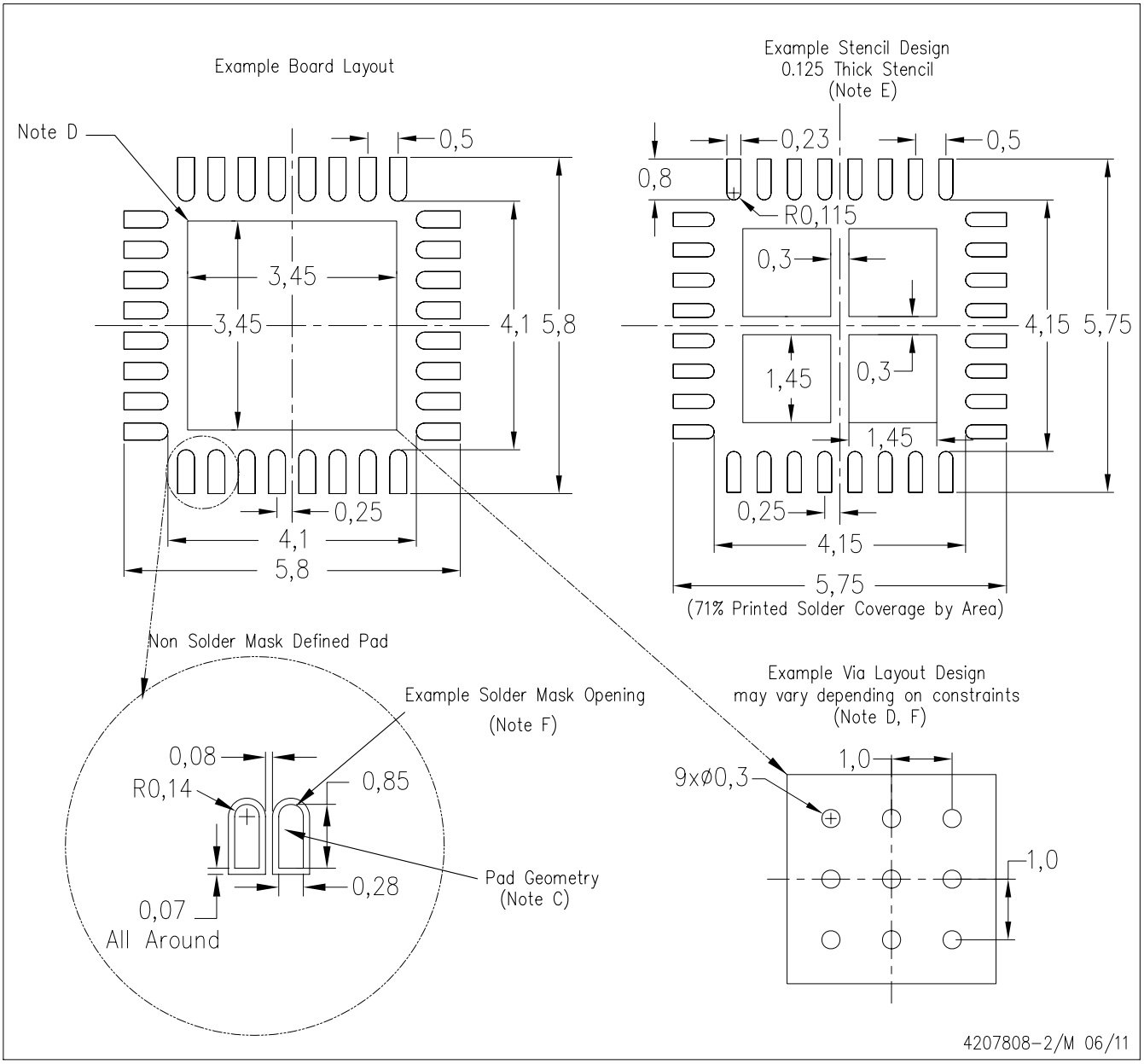
Bottom View

Exposed Thermal Pad Dimensions

4206356–2/U 06/11

NOTE: A. All linear dimensions are in millimeters

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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