# MASW-008902-000DIE

Bumped GaAs SP3T Switch for WLAN
2.4 - 2.5 GHz

Rev. V4

## Features

- 802.11b/g and Bluetooth Applications
- Insertion Loss: 0.60 dB typical
- Isolation:
  31 dB typical ($R_X$ Path)
  22 dB typical ($T_X$ / BT paths)
- Flip-chip configuration
- RoHS* Compliant

## Description

The MASW-008902-000DIE is a bumped single band GaAs pHEMT MMIC SP3T switch. Typical applications are for single band 2.4 GHz WLAN (802.11 b/g) and Bluetooth applications.

The MASW-008902-000DIE delivers high isolation, low insertion loss, and high linearity at 2.4 - 2.5 GHz.

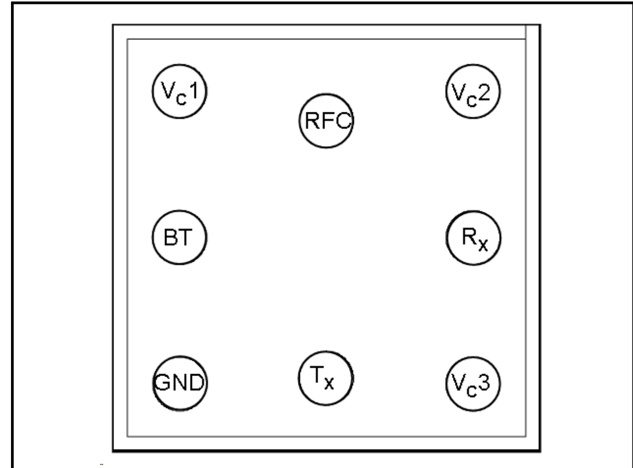
The MASW-008902-000DIE is fabricated using a 0.5 micron gate length GaAs pHEMT process. The process features full passivation for performance and reliability. This die features SnAg (2.5%) solder bumps for WLCSP applications.

## Ordering Information [1,2]

| Part Number | Package |
|---|---|
| MASW-008902-000DIE | Separated Die on Grip Ring |
| MASW-008902-000D3K | Die in 3000 piece reel |
| MASW-008902-001SMB | Sample Board SP3T |

1. Die quantity varies.
2. Die on Grip Ring not available with orientation mark.

## Die Bump Pad Layout (bump side up)




## Die Bump Pad Configuration

| Name | Description |
|---|---|
| $V_C1$ | Voltage Control 1 |
| BT | Blue Tooth $T_X/R_X$ Port |
| GND | Ground |
| $T_X$ | 2.5 GHz $T_X$ Port |
| $V_C3$ | Voltage Control 3 |
| $R_X$ | 2.5 GHz $R_X$ Port |
| $V_C2$ | Voltage Control 2 |
| RFC | Antenna Port |

## Absolute Maximum Ratings [3,4]

| Parameter | Absolute Maximum |
|---|---|
| Input Power @ 3 V Control | +32 dBm |
| Input Power @ 5 V Control | +35 dBm |
| Operating Voltage | +8 volts |
| Operating Temperature | -40°C to +85°C |
| Storage Temperature | -65°C to +150°C |

3. Exceeding any one or combination of these limits may cause permanent damage to this device.
4. M/A-COM Technology does not recommend sustained operation near these survivability limits.

* Restrictions on Hazardous Substances, European Union Directive 2002/95/EC.



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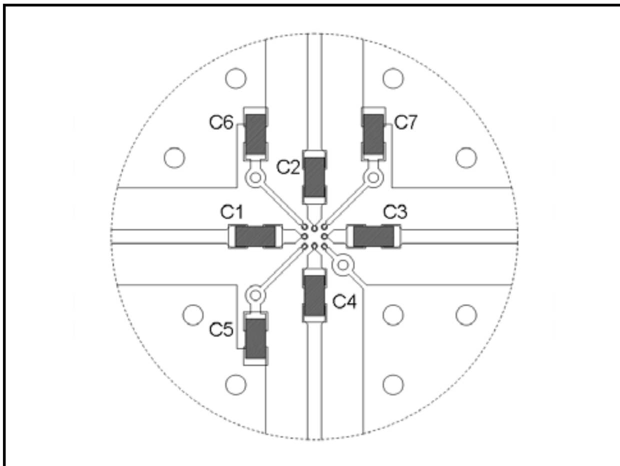
## Electrical Specifications[5]: $T_A$ = 25°C, $Z_0$ = 50 Ω, $V_C$ = 0/3V, $P_{IN}$ = 0 dBm

| Parameter | Test Conditions | Units | Min. | Typ. | Max. |
|---|---|---|---|---|---|
| Insertion Loss | RFC to $T_X$/$R_X$/BT, 2.4 GHz | dB | — | 0.60 | 0.75 |
| Isolation | RFC to $T_X$, 2.4 GHz<br>RFC to $R_X$, 2.4 GHz<br>RFC to BT, 2.4 GHz | dB | 20<br>30<br>20 | 23.5<br>31.0<br>21.0 | —<br>—<br>— |
| Return Loss | 2.4 - 2.5 GHz | dB | — | 15 | — |
| IP3 | RF to $T_X$/$R_X$/BT, 2.4 GHz, 20 dBm Total Power, 1 MHz Spacing | dBm | — | 55 | — |
| Input P1dB | RF to $T_X$, 2.4 - 2.5 GHz<br>RF to $R_X$, 2.4 - 2.5 GHz<br>RF to BT, 2.4 - 2.5 GHz | dBm | —<br>—<br>— | 32<br>28<br>32 | —<br>—<br>— |
| Harmonics | RF to $T_X$, 2.4 - 2.5 GHz, 20 dBm | dBm | — | -75 | — |
| Switching Speed | 50% control to 90% RF<br>50% control to 10% RF | ns | —<br>— | 165<br>25 | —<br>— |
| Control Current | $\|V_C\|$ = 3 V | µA | — | <1 | 10 |

5. External blocking capacitors on all RF ports.

## Recommended PCB Configuration




## Parts List

| Part | Value | Case Style |
|---|---|---|
| C1 - C4 | 39 pF | 0402 |
| C5 - C7 | 1000 pF | 0402 |

## Truth Table [6,7,8]

| $V_C1$ | $V_C2$ | $V_C3$ | RFC–BT | RFC-$T_X$ | RFC-$R_X$ |
|---|---|---|---|---|---|
| 1 | 0 | 0 | On | Off | Off |
| 0 | 1 | 0 | Off | On | Off |
| 0 | 0 | 1 | Off | Off | On |

6. For positive voltage control, external DC blocking capacitors are required on all RF ports.
7. Differential voltage, V(state 1) - V(state 0), must be +2.7 V minimum and must not exceed +5 V.
8. 0 = 0 ± 0.3 V, 1 = +2.7 V to +5 V.

## Handling Procedures

Please observe the following precautions to avoid damage:

### Static Sensitivity

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.



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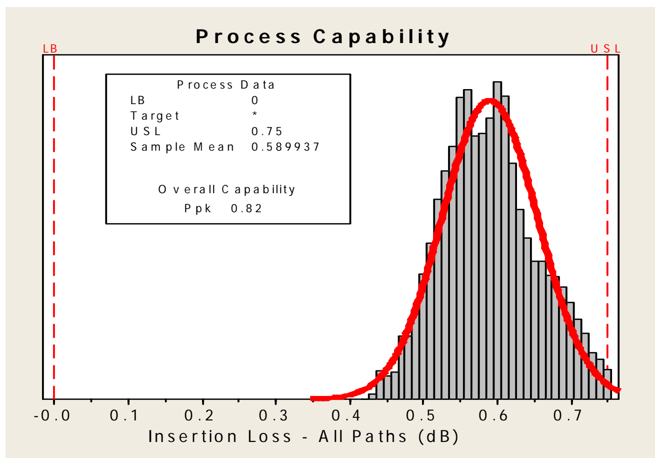
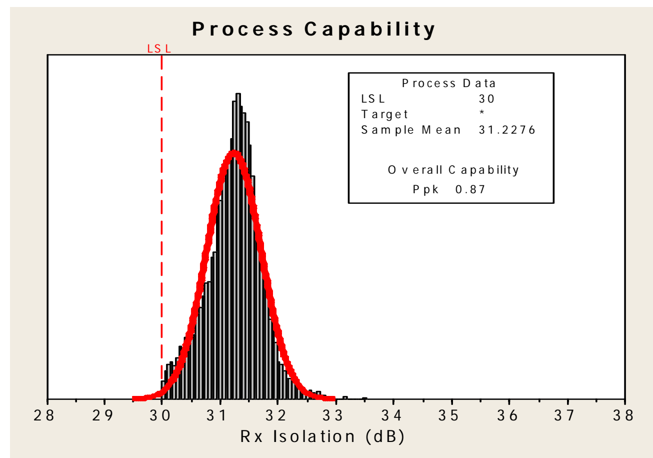
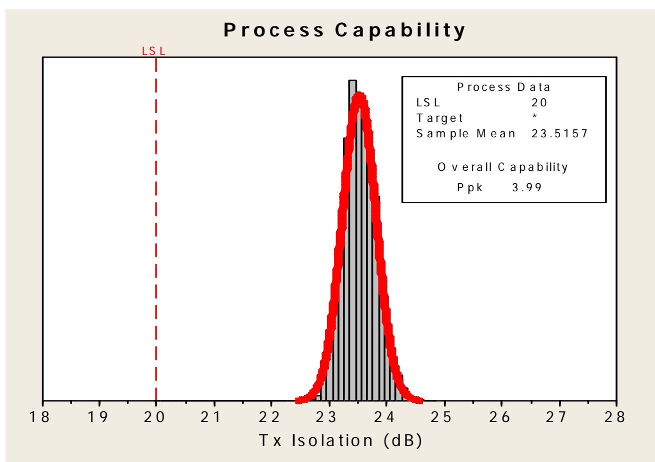
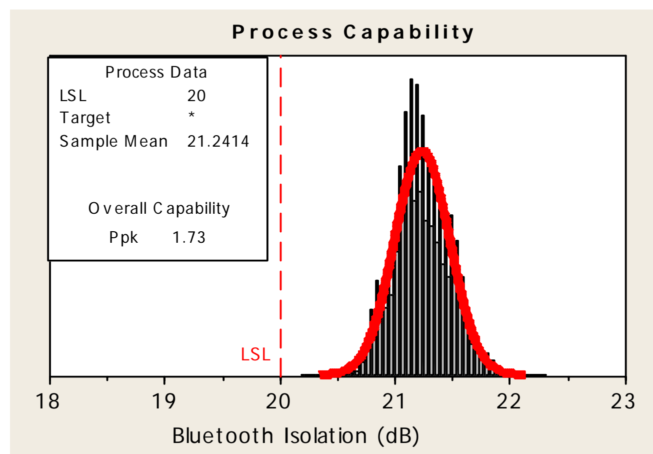
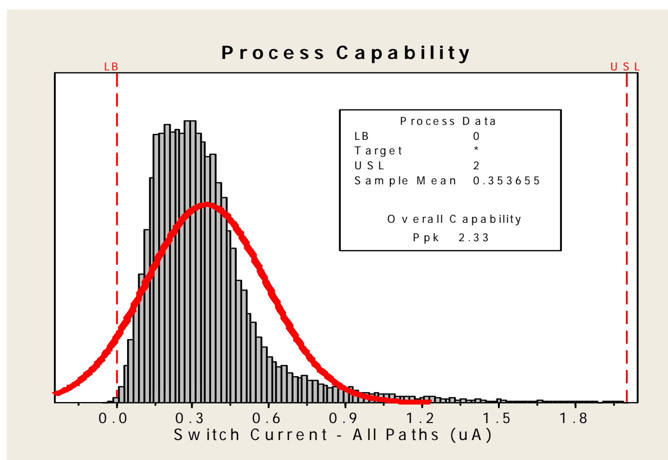
## Product Consistency Distribution Charts[9] (on wafer RF test)




9. Represents >50 wafers, tested per electrical specifications: Freq. = 2.4 GHz, $T_A$ = 25°C, $Z_0$ = 50 Ω, $V_C$ = 0/3V, $P_{IN}$ = 0 dBm



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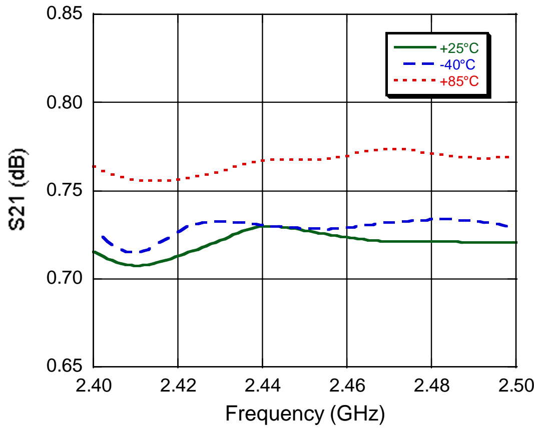
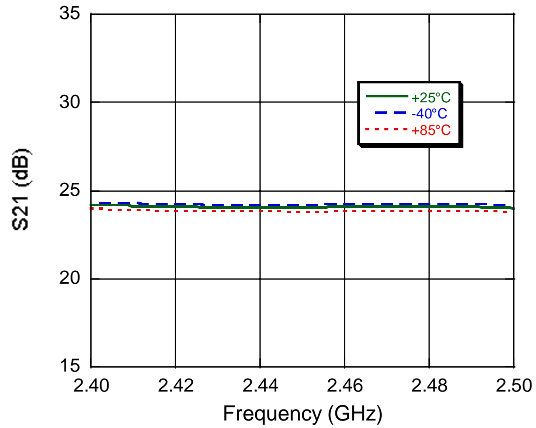
## Typical Performance Curves (plots = chip on board assembly)

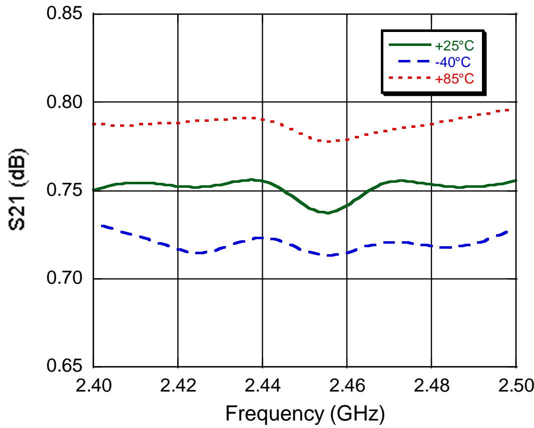
### $T_X$ Insertion Loss



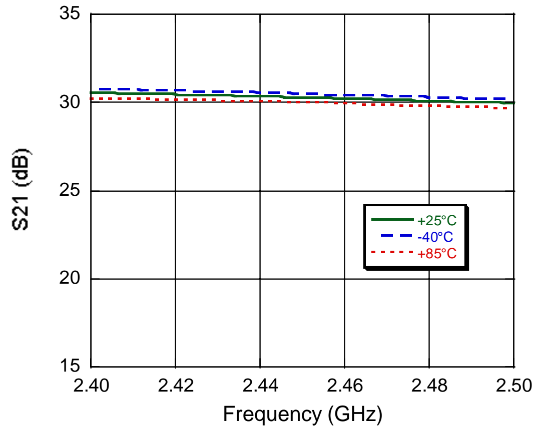

### $T_X$ Isolation



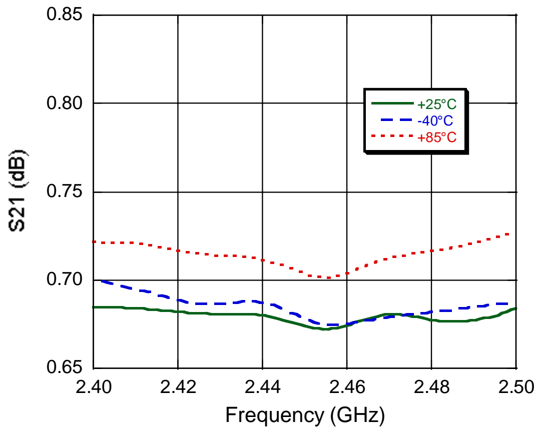

### $R_X$ Insertion Loss



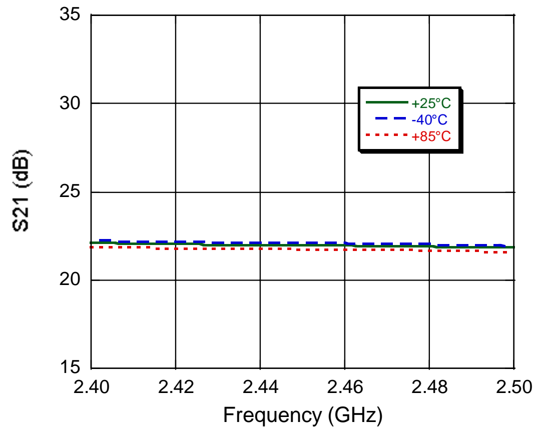

### $R_X$ Isolation




### BT Insertion Loss




### BT Isolation



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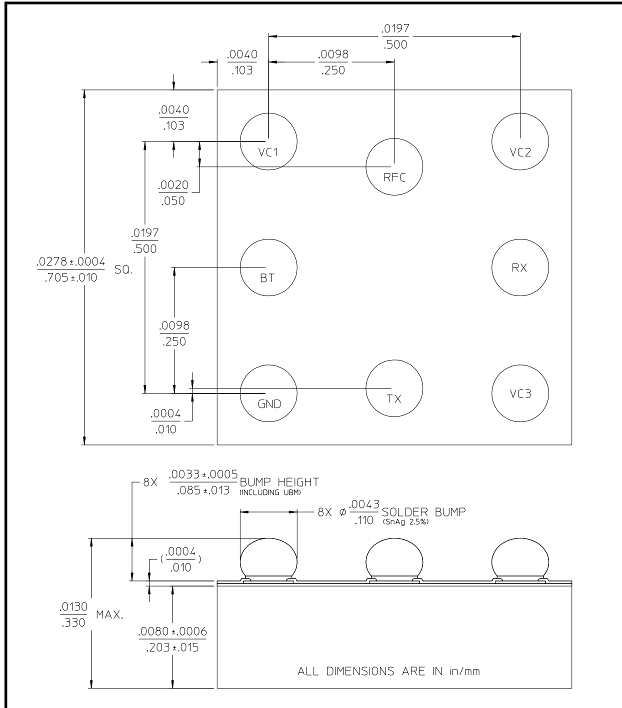
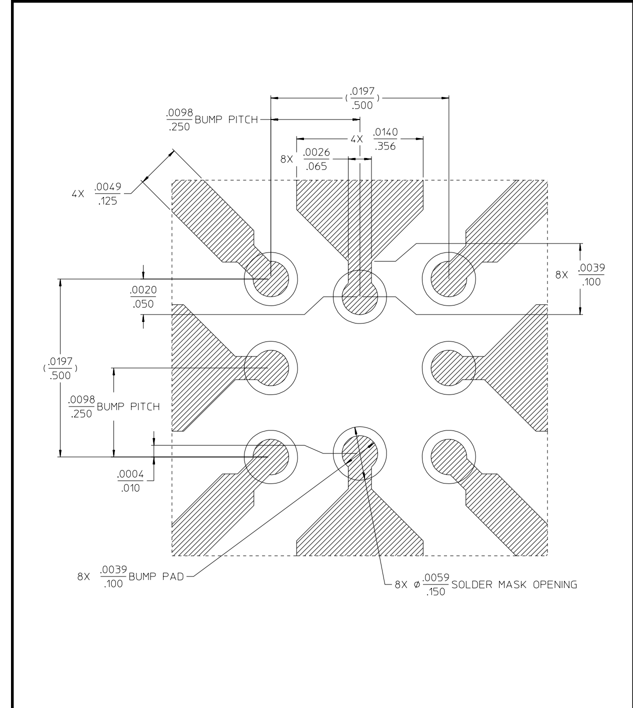
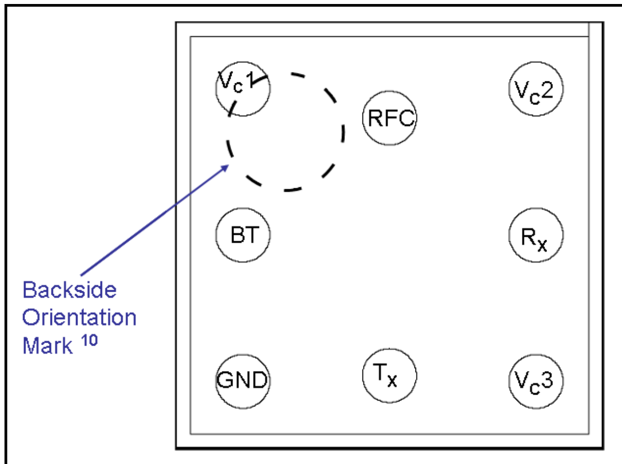
## Die Dimensions (Top and Side Views)



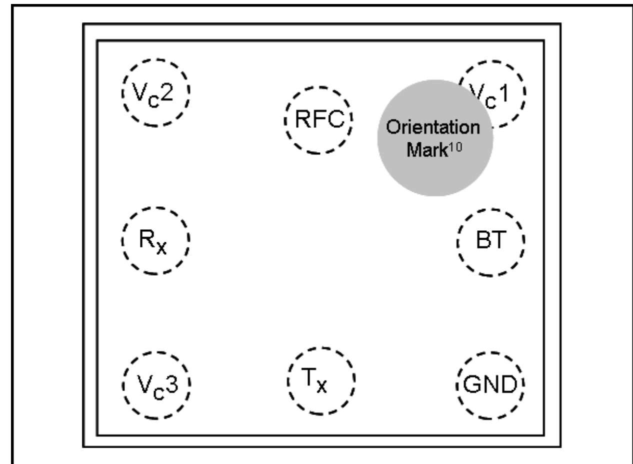

## PCB Top Metal / Solder Mask




## Die Bump Pad Layout - Top View (bump side up)




## Die Bump Pad Layout - Bottom View (bump side down - as installed on board)




10. Orientation mark is only on material that is shipped in tape and reel. The mark is not available on die shipped on grip ring.

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