

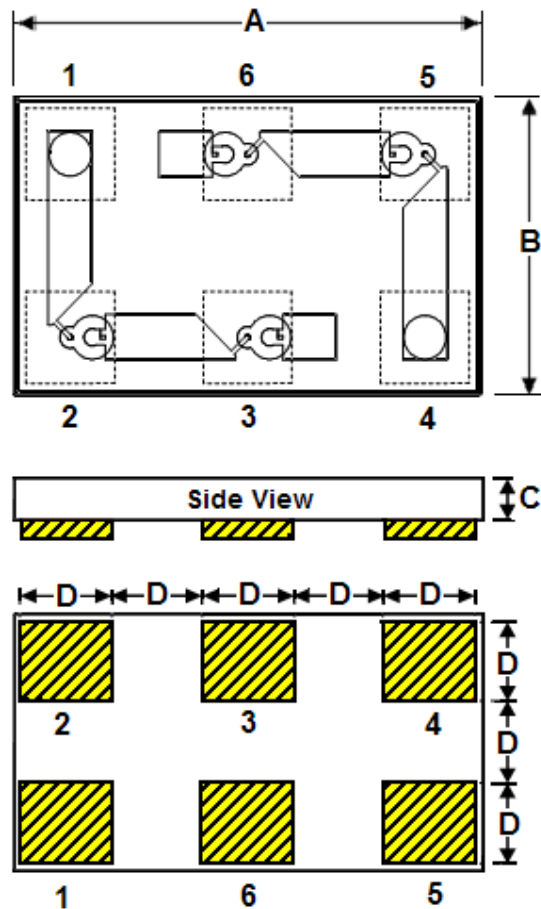
Features

- ◆ No Wire Bonds Required
- ◆ Rugged Silicon-Glass Construction
- ◆ Silicon Nitride Passivation
- ◆ Polymer Scratch Protection
- ◆ Ultra-Low Parasitic Capacitance and Inductance
- ◆ Higher RF C.W. Power Handling
- ◆ Better Performance than Packaged Devices

Description and Applications

This device is a silicon glass PIN diode chip fabricated with M/A-COM Tech Solutions patented HMIC process. This 80µm I-region length device features six silicon pedestals embedded in a low loss, low dispersion glass. The diodes are formed on the top of a pedestal and connections to the backside of the device are facilitated by making the pedestal sidewalls electrically conductive. Selective backside metallization is applied producing a surface mount device. The topside is fully encapsulated with silicon nitride and has an additional polymer layer for scratch protection. These protective coatings prevent damage to the junction and the anode air-bridge during handling and assembly. The vertical silicon diode topology provides for a highly efficient heat transfer medium. These surface mount devices are suitable for usage in higher (3W avg.) incident power switches. Small parasitic inductance and excellent RC constant make these devices ideal for absorptive SPST, reflective SP2T switches, and attenuator circuits, where higher P1db and power handling values are required.

Case Style - ODS-1310



Absolute Maximum Ratings¹

@ T_{AMB} = +25°C (unless otherwise specified)

| Parameter | Absolute Maximum |
|-----------------------|-----------------------|
| Forward Current | 250mA |
| Reverse Voltage | -100V |
| Operating Temperature | -55°C to +125°C |
| Storage Temperature | -55°C to +150°C |
| Junction Temperature | +175°C |
| C.W. Incident Power | +35dBm |
| Mounting Temperature | +300°C for 10 seconds |

| Dim | Inches | | Millimeters | |
|-----|--------|-------|-------------|-------|
| | Min. | Max. | Min. | Max. |
| A | 0.060 | 0.062 | 1.524 | 1.575 |
| B | 0.036 | 0.038 | 0.914 | 0.965 |
| C | 0.004 | 0.008 | 0.102 | 0.203 |
| D | 0.011 | 0.012 | 0.279 | 0.305 |

1. Operation of this device above any one of these parameters may cause permanent damage.

1. Backside Metal: 0.1microns thick.
2. Shaded Areas Indicate Backside Ohmic Gold Contacts.

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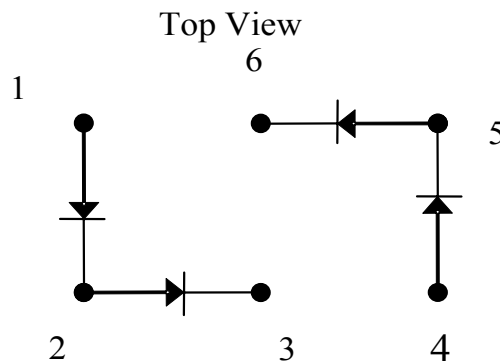
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Electrical Specifications @ +25 °C, per Diode Junction

| Symbol | Conditions | Units | Min. | Typ. | Max. |
|---------------|---------------------------|----------------|------|------|------|
| C_T | -40V, 1MHz ¹ | pF | | 0.05 | 0.07 |
| C_T | -40V, 1GHz ^{1,3} | pF | | 0.04 | 0.06 |
| R_S | 10mA, 1GHz ^{2,3} | Ω | | 5.0 | |
| V_F | 10mA | V | | 0.83 | 1.00 |
| V_R | -10 μ A | V | -70 | -100 | |
| I_R | -70V | μ A | | -0.1 | -10 |
| T_L | +10mA /-6mA | ns | | 200 | |
| θ_{TH} | 1A /10mA | $^{\circ}$ C/W | | 150 | |

1. Total capacitance, C_T , is equivalent to the sum of Junction Capacitance, C_j , and Parasitic Capacitance, C_{par} .
2. Series resistance R_S is equivalent to the total diode resistance : $R_s = R_j$ (Junction Resistance) + R_c (Ohmic Resistance)
3. R_s , C_T , T_L , θ_{TH} are measured on an HP4291A Impedance Analyzer with die mounted in a ceramic package with Sn 60/Pb 40 solder

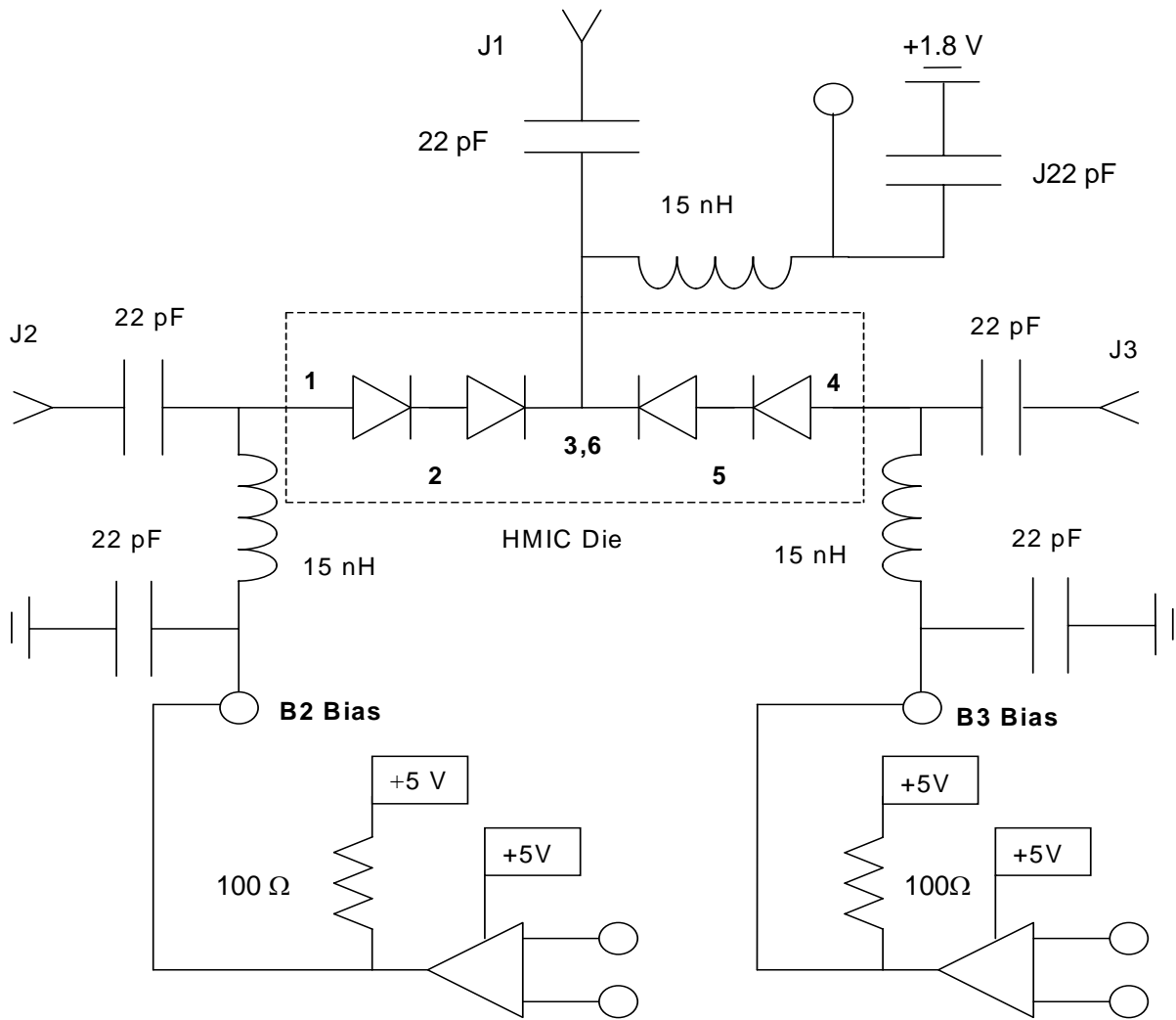
Equivalent Double Tee Equivalent Circuit



Notes:

1. Ports 2 and 5 have a Connected Cathode-Anode Node.
2. Ports 1,3,4, and 6 Have a Singular, Un-Connected Node.

SP2T All Series Reflective Switch with +5V and TTL Logic Control (2-18 GHz)



SN7406, SN7416 TTL Open Collector Gate Driver (X2)

RF Truth Table for Reflective SP2T using Singular Power Supply: +5V, + I Only

| RF State | B2 Diode Bias | B3 Diode Bias |
|-------------------------------------|---------------|-----------------|
| J1 – J2 Low Loss & J1– J3 Isolation | +3.6V @ +14mA | +0.5V @ 0mA |
| J1 – J3 Low Loss & J1–J2 Isolation | +0.5V @ 0mA | + 3.6V @ + 14mA |

Notes:

1. Diode Forward Voltage Differential (ΔV_f) @ 15mA = 0.9V
2. Insertion Loss Diode Bias = $(+ 5V - (2) * 0.9V - 1.8V) / (100\Omega) = 14mA$
3. Off Isolation Diode Back Bias Voltage = $| - (+1.8V - 0.5V) | = | - 1.3V |$.

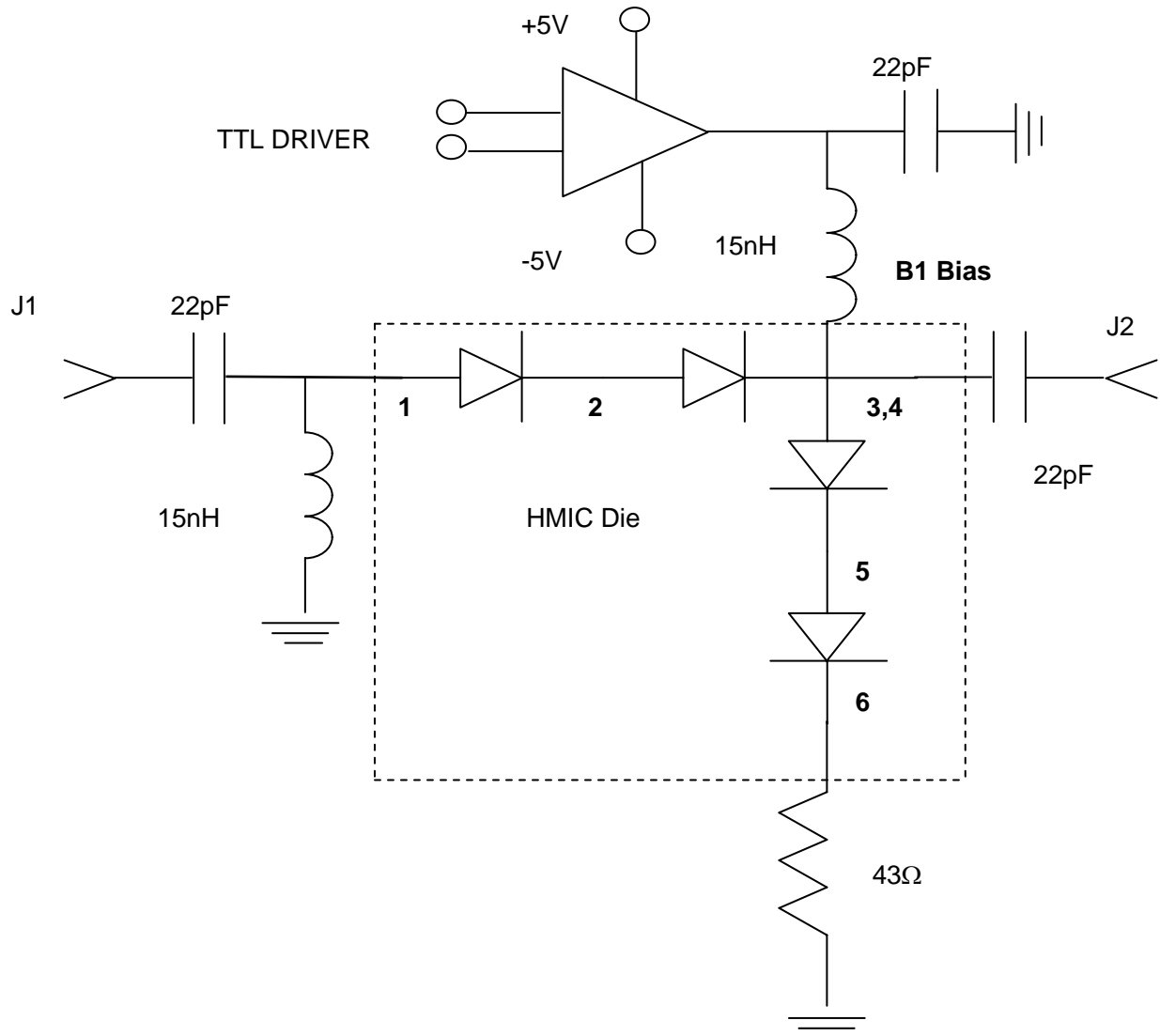
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SPST All Series Absorptive Switch with +5V and TTL Logic Control (2-18 GHz)



RF Truth Table for Absorptive SPST using +5V, -5V Power Supplies

| RF State | TTL Value | B1 Diode Bias |
|-------------------|-----------|----------------|
| J1 – J2 Low Loss | 0 | - 1.8V @ -20mA |
| J1 – J2 Isolation | 1 | +2.7V @ + 20mA |

Notes:

1. Diode Forward Voltage Differential (ΔV_f) @ 20mA = 0.9 V
2. Diode R_s @ 20mA = 3.5 Ω
3. Insertion Loss Diode Bias = - 1.8 V @ -20mA from a Constant Current Source
4. Off Isolation Diode Back Bias Voltage through (2) Diodes = $| - (+2.7 V - 0 V) | = | - 2.7 V |$.

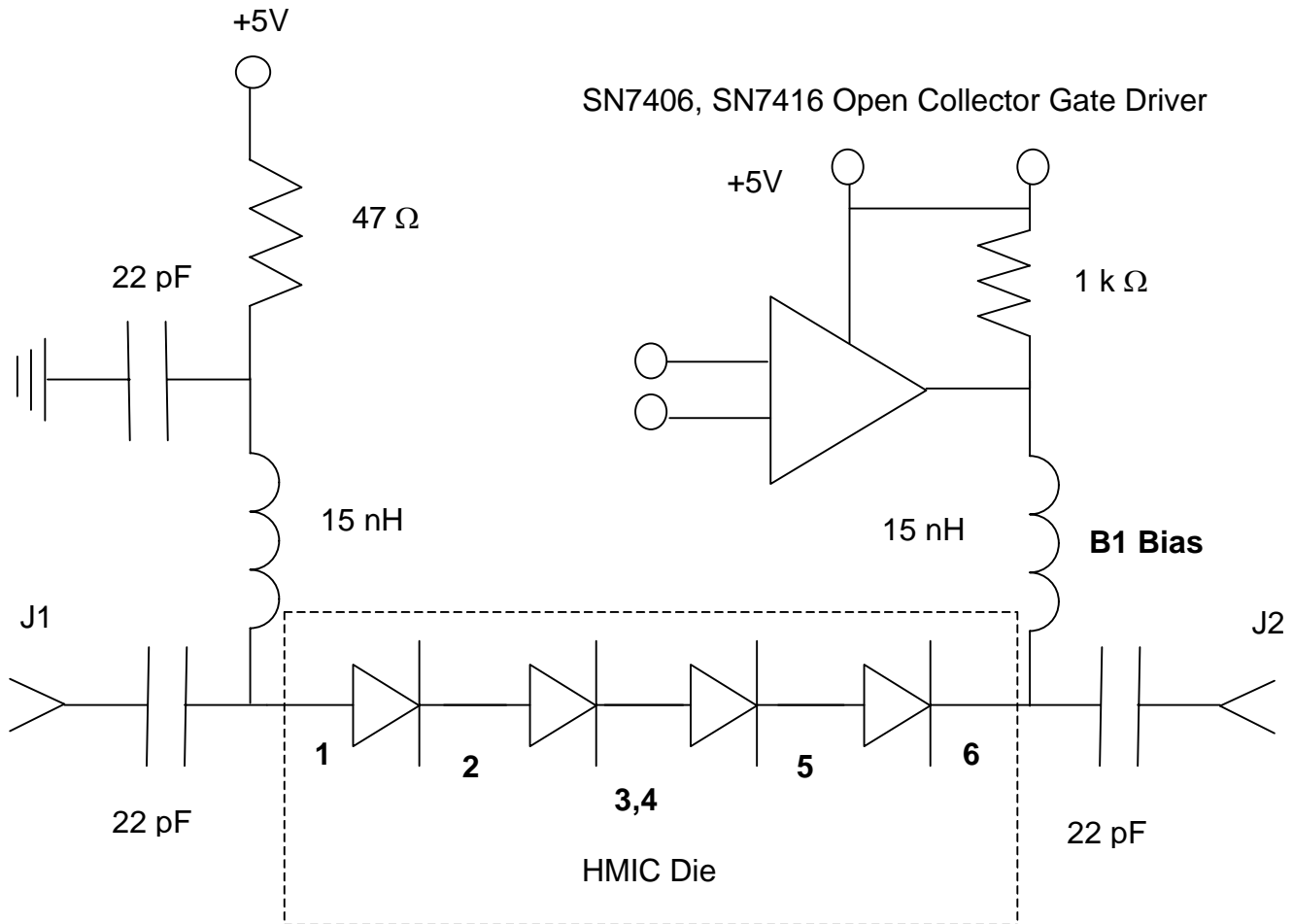
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SPST All Series Reflective Switch with +5V and TTL Logic Control (2–18 GHz)



RF Truth Table for Reflective SPST using Singular Power Supply: +5V, + I Only

| RF State | TTL Value | B1 Diode Bias |
|------------------|-----------|----------------|
| J1 – J2 Low Loss | 0 | + 0.5V @ +20mA |
| J1–J2 Isolation | 1 | +5.0V @ 0mA |

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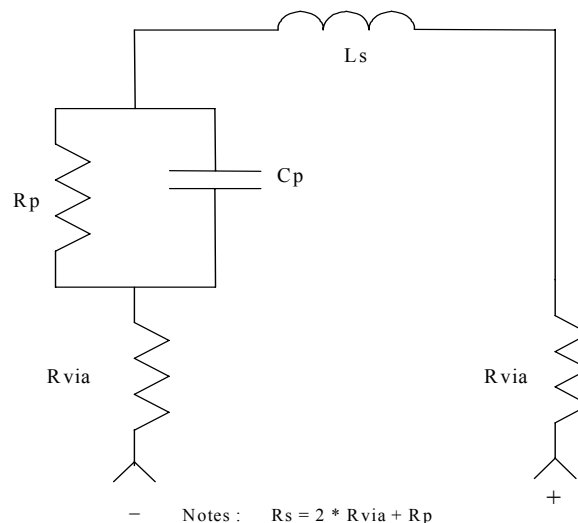
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MADP-064908 SPICE Model

PinDiodeModel wBv=80 V
NLPINM1 wPmax=3.0 W
Is=1.0E-14 A Ffe=1.0
Vi=0.0 V
Un=900 cm²/V-sec
Wi=7.5 um
Rr=20 K Ohm
Cmin=0.05 pF
Tau=0.20 usec
Rs=0.1 Ohm
Cj0=0.06 pF
Vj=0.7 V
M=0.5
Fc=0.5
Imax=1.0E+6 A/m²
Kf=0.0
Af=1.0

Equivalent per Diode Schematic



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Assembly Guidelines

Handling

All semiconductor chips should be handled with care to avoid damage or contamination from perspiration and skin oils. The use of plastic tipped tweezers or vacuum pickups is strongly recommended for individual components. Bulk handling should insure that abrasion and mechanical shock are minimized.

Bonding

Attachment to a circuit board is made simple through the use of surface mount technology. Mounting pads are conveniently located on the bottom surface of these devices and are removed from the active junction locations. These devices are well suited for solder attachment onto hard and soft substrates. Conductive silver epoxy may also be used for lower Incident power applications (<1W Average Power). The epoxy should be approximately 1-2mils thick and cured at approximately 90°C to 150°C per the manufacturer's schedule.

When soldering these devices on to a hard substrate, hot gas die bonding is preferred. We recommend utilizing a vacuum tip and force of 60 to 100 grams be applied to the top surface of the device. Position the die so that its mounting pads are aligned with the circuit board mounting pads and reflow the solder by heating the circuit trace near the mounting pad while applying 60 to 100 grams of force perpendicular to the top surface of the die. The solder connections to the pads must **not** be made one at a time. Doing so would create un-equal heat flow and thermal stress to the chip. Solder reflow should not be performed by causing heat to flow through the top surface of the die. Since the HMIC glass is transparent, the edges of the mounting pads can be visually inspected through the die to ensure proper solder flow after attachment is complete.

Typical solder re-flow profiles are provided in [Application Note 538](#) "Surface Mounting Instructions" located on the MA-COM website at www.macomtech.com

Ordering Information

| Part Number | Packaging |
|--------------------|-----------------|
| MADP-064908-131000 | Die in Gel Pack |

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